Formal Specification & Analysis of Autonomous Systems in PrCCSL/Simulink Design Verifier

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ABSTRACT

Modeling and analysis of timing constraints is crucial in automotive systems. EAST-ADL is a domain specific architectural language dedicated to safety-critical automotive embedded system design. In most cases, a bounded number of violations of timing constraints in systems would not lead to system failures when the results of the violations are negligible, called Weakly-Hard (WH). We have previously specified EAST-ADL timing constraints in Clock Constraint Specification Language (CCSL) and transformed timed behaviors in CCSL into formal models amenable to model checking. Previous work is extended in this paper by including support for probabilistic analysis of timing constraints in the context of WH: Probabilistic extension of CCSL, called PrCCSL, is defined and the EAST-ADL timing constraints with stochastic properties are specified in PrCCSL. The semantics of the extended constraints in PrCCSL is translated into Proof Objective Models that can be verified using SIMULINK DESIGN VERIFIER. Furthermore, a set of mapping rules is proposed to facilitate guarantee of translation. Our approach is demonstrated on an autonomous traffic sign recognition vehicle case study.

Keywords: CPS, EAST-ADL, UPPAAL-smc, SIMULINK DESIGN VERIFIER, Verification & Validation
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Chapter 1

Introduction

Software development for Cyber-Physical Systems (CPS) requires both functional and non-functional quality assurance to guarantee that CPS operate in a safety-critical context under timing constraints. Automotive electric/electronic systems are ideal examples of CPS in which the software controllers interact with physical environments. The continuous time behaviors of those systems often rely on complex dynamics as well as on stochastic behaviors. Formal verification and validation (V&V) technologies are indispensable and highly recommended for development of safe and reliable automotive systems [3,4].

Conventional formal analysis of timing models addresses worst case designs, typically used for hard deadlines in safety critical systems, however, there is great incentive to include “less-than-worst-case” designs with a view to improving efficiency without affecting the quality of timing analysis in the systems. The challenge is the definition of suitable model semantics providing reliable predictions of system timing, given the timing of individual components and their compositions. While the standard worst case models are well understood in this respect, the behavior and the expressiveness of “less-than-worst-case’ models is far less investigated. In most cases, a bounded number of violations of timing constraints in systems would not lead to system failures when the results of the violations are negligible, called Weakly-Hard (WH) [8,26]. In this paper, we propose a formal probabilistic modeling and analysis technique by extending the known concept of WH constraints to what is called “typical” worst case model and analysis.

EAST-ADL (Electronics Architecture and Software Technology- Architecture Description Language) [5,11], aligned with AUTOSAR (Automotive Open System Architecture) standard [1], is the model-based development approach for the architectural modeling of safety-critical automotive embedded systems. A system in EAST-ADL is described by Functional Architectures (FA) at different abstraction levels. The FA are composed of a number of interconnected functionprototypes ($f_p$), and the $f_p$s have ports and connectors for communication. EAST-ADL relies on external tools for the analysis of specifications related to requirements. For example, behavioral description in EAST-ADL is captured in external tools, i.e., SIMULINK/STATEFLOW [30]. The latest release of EAST-ADL has adopted the time
model proposed in the Timing Augmented Description Language (TADL) [9]. TADL expresses and composes the basic timing constraints, i.e., repetition rates, end-to-end delays, and synchronization constraints. The time model of TADL specializes the time model of MARTE, the UML profile for Modeling and Analysis of Real-Time and Embedded systems [27]. MARTE provides CCSL, a time model and a Clock Constraint Specification Language, that supports specification of both logical and dense timing constraints for MARTE models, as well as functional causality constraints [23].

We have previously specified non-functional properties (timing and energy constraints) of automotive systems specified in EAST-ADL and MARTE/CCLSL, and proved the correctness of specification by mapping the semantics of the constraints into UPPAAL models for model checking [21]. Previous work is extended in this paper by including support for probabilistic analysis of timing constraints of automotive systems in the context WH: 1. Probabilistic extension of CCSL, called PrCCSL, is defined and the EAST-ADL/TADL timing constraints with stochastic properties are specified in PrCCSL; 2. The semantics of the extended constraints in PrCCSL is translated into verifiable Proof Objective Models (POMs) for formal verification using SIMULINK DESIGN VERIFIER (SDV) [2]; 3. A set of mapping rules is proposed to facilitate guarantee of translation. Our approach is demonstrated on an autonomous traffic sign recognition vehicle (AV) case study.

The paper is organized as follows: Sec. 2 presents an overview of CCSL, SIMULINK/STATEFLOW and SDV. The AV is introduced as a running example in Sec. 3. Sec. 4 presents the formal definition of PrCCSL and Sec. 5 demonstrates the specification of EAST-ADL timing constraints in CCSL/PrCCSL. Sec. 6 describes a set of translation patterns from CCSL/PrCCSL to POMs and how our approaches provide support for formal analysis at the design level. The modeling of AV system and its environments in S/S are illustrated in Sec. 7. The applicability of our method is demonstrated by performing verification on the AV case study in Sec. 8. Sec. 9 and Sec. 10 present related work and the conclusion.
Chapter 2

Preliminary

In our framework, we consider a subset of C
CSL and its extension with stochastic properties that is sufficient to specify EAST-ADL timing constraints in the context of WH automotive systems. SIMULINK and EMBEDDED MATLAB (EML) are utilized for modeling purposes, and V&V are performed by the SIMULINK built-in verification tool, SIMULINK DESIGN VERIFIER (SDV).

2.1 Clock Constraint Specification Language (C
CSL)

C
CSL [7,23] clocks describe events in a system and measure occurrences of the events. The physical time is represented by a dense clock (with a base) and discretized into a logical clock. idealClock is a predefined dense clock whose unit is second. We define a universal clock ms based on idealClock: ms = idealClock discretizedBy 0.001, where ms is a periodic clock that ticks every 1 millisecond. A step is a tick of the universal clock. Hence the length of one step is 1 millisecond in this paper.

C
CSL provides two types of clock constraints, relation and expression: A relation limits the occurrences among different events/clocks. Let C be a set of clocks, c1,c2 ∈ C, Coincidence relation (c1 ≡ c2) specifies that two clocks must tick simultaneously. Precedence relation (c1 ≺ c2) limits that c1 runs faster than c2, i.e., ∀k ∈ N+, where N+ is the set of positive natural numbers, the kth tick of c1 must occur prior to the kth tick of c2. Causality relation (c1 ≲ c2) represents a relaxed version of Precedence, allowing the two clocks to tick at the same time. Subclock (c1 ⊆ c2) indicates the relation between two clocks, superclock (c1) and subclock (c2), s.t. each tick of the subclock must correspond to a tick of its superclock at the same step. Exclusion (c1 # c2) prevents the instants of two clocks from being coincident. An expression derives new clocks from the already defined clocks: PeriodicOn builds a new clock found on a base clock and a period parameter, s.t., the instants of the new clocks are separated by a number of instants of the base clock. The number is given as period. DelayFor results in a clock by delaying the base clock for a given number of ticks of a reference clock. Infimum, denoted Inf, is
defined as the slowest clock that is faster than both \( c_1 \) and \( c_2 \). **Supremum**, denoted \( \text{Sup} \), is defined as the fastest clock that is slower than \( c_1 \) and \( c_2 \).

### 2.2 Simulink and SDV

**Simulink** [30] is a synchronous data flow language, which provides different types of **blocks** for modeling and simulation of dynamic systems and code generation. **Simulink** supports the definition of custom blocks via **Stateflow** diagrams or **user-defined function** blocks written in EML, C, and C++. **SDV** is a formal verification tool that performs reachability analysis on **Simulink/Stateflow (S/S)** model with **Prover** plugin. The satisfiability of each reachable state is determined by a SAT solver. A proof objective model is specified in **Simulink/SDV** and illustrated in Fig.2.1. A set of data (predicates) on the input flows of **System** is constrained via \( \langle \text{Proof Assumption} \rangle \) blocks during proof construction. A set of proof objectives are constructed via a function \( F \) block and the output of \( F \) is specified as input to a property \( P \) block. \( P \) passes its output signal to an \( \langle \text{Assertion} \rangle \) block and returns \emph{true} when the predicates set on the input data flows of the outline model are satisfied. Whenever \( \langle \text{Assertion} \rangle \) is utilized, **SDV** verifies whether the specified input data flow is always \emph{true}. Any failed proof attempt ends in the generation of a counterexample representing an execution path to an invalid state. A harness model is generated to analyze the counterexample and refine the model.

![Figure 2.1: General verification models in SDV](image)

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[30] Reference to be added.
Chapter 3

Running Example: Traffic Sign Recognition Vehicle

An autonomous vehicle (AV) \([19, 20]\) application using Traffic Sign Recognition is adopted to illustrate our approach. The AV reads the road signs, e.g., “speed limit” or “right/left turn”, and adjusts speed and movement accordingly. The functionality of AV, augmented with timing constraints and viewed as Functional Design Architecture (FDA) (designFunctionTypes), consists of the following \(f_p\)s in Fig[3.1]: System function type contains four \(f_p\)s, i.e., the Camera captures sign images and relays the images to SignRecognition periodically. Sign Recognition analyzes each frame of the detected images and computes the desired images (sign types). Controller determines how the speed of the vehicle is adjusted based on the sign types and the current speed of the vehicle. VehicleDynamic specifies the kinematics behaviors of the vehicle. Environment function type consists of three \(f_p\)s, i.e., the information of traffic signs, random obstacles, and speed changes caused by environmental influences described in TrafficSign, Obstacle, and Speed \(f_p\)s respectively.

We consider the Periodic, Execution, End-to-End, Synchronization, Sporadic, and Comparison timing constraints on top of the AV EAST-ADL model, which are sufficient to capture the constraints described in Fig[3.1]. Furthermore, we extend EAST-ADL/TADL with an Exclusion timing constraint that integrates relevant concepts from the CCSL constraint, i.e., two events cannot occur simultaneously (R27 – R31).

R1. The camera must capture an image every 50ms. In other words, a Periodic acquisition of Camera must be carried out every 50ms.
R2. The captured image must be recognized by an AV every 200ms, i.e., a Periodic constraint on SignRecognition \(f_p\).
R3. The obstacle must be detected by an AV every 40ms, i.e., the Periodic timing constraint is applied on the input port of Controller.
R4. The speed of AV is updated periodically with the period of 30ms.
R5. The detected image must be computed within [100, 150]ms in order to generate the desired sign type, SignRecognition must complete its execution within [100,
Figure 3.1: AV in EAST-ADL augmented with TADL timing constraints (R.ID), specified in PrCSSL (Spec.R.ID)
should not revert back to “turn left” mode within a specific time period. It is inter-
preted as a Sporadic constraint, i.e., the mode of AV is changed to Stop because of
the encounter with an obstacle, it should not revert back to turn left mode within
500ms.

R12. If the mode of AV switches to “emergency stop” due to the certain obstacle,
it should not revert back to “turn right” mode within a specific time period. It is in-
terpreted as a Sporadic constraint, i.e., the mode of AV is changed to Stop because
of the encounter with an obstacle, it should not revert back to turn right mode
within 500ms.

R13. The necessary information from environment must be arrived to Controller
within 40ms, e.g., all the input signals arriving on the speed, signType, direct,
gear and torque ports of Controller must be within a given time window, i.e.,
the tolerated maximum constraint is 40ms. It is called Input Synchronization
constraint.

R14. Once the execution of Controller is completed, it sends out the computed
signals/values to VehicleDynamic within 30ms, e.g., all the output signals leaving
via reqTorq, reqDirect, reqGear, reqBrake ports of Controller must be within
a given time window, i.e., the tolerated maximum constraint is 30ms. It is called
Output Synchronization constraint.

R15. The necessary information from Controller must be arrived to VehicleDyna-
metric within 30ms. The Input Synchronization constraint applied on the input
ports of VehicleDynamic (reqTorq, reqDirect, reqGear, reqBrake) should be
30ms.

R16. Once VehicleDynamic completes its execution, the information of AV must
be updated within 40ms. The Output Synchronization constraint applied on the
output ports of VehicleDynamic (speed, direct, gear, torque) should be 40ms.

R17. When a traffic sign is recognized, the speed of AV should be updated within
[150, 250]ms. An End-to-End constraint on Controller and VehicleDynamic,
i.e., the time interval from the input of Controller to the output of VehicleDynamic
must be within a certain time.

R18. When Camera is triggered, the computation of image processing based on
the traffic signs captured by Camera must be finished within [120, 180]ms, i.e., the
End-to-End timing constraint applied on Camera and SignRecognition should be
between 120ms and 180ms.

R19. The time interval between Camera capturing an image of traffic sign and the
status of AV (i.e., speed, direction etc.) being updated according to the recognized
sign type should be within [270, 430]ms, End-to-End timing constraint measured
from the input of Camera to the output of VehicleDynamic should be between 270
and 430ms.

R20. When a “left turn” sign is recognized, AV must turn left within 500ms, i.e., a
End-to-End timing constraint applied on the events DetectLeftSign and StartTurn-
Left is 500ms.

R21. When a “right turn” sign is recognized, AV must turn right within 500ms, i.e., a End-to-End timing constraint applied on the events DetectRightSign and StartTurnRight is 500ms.

R22. When a “stop” sign is recognized, AV must start to brake within 200ms, i.e., a End-to-End timing constraint applied on the events DetectStopSign and StartBrake is 20ms.

R23. When a “stop” sign is recognized, AV must be stop completely within 3000ms, i.e., a End-to-End timing constraint applied on the events DetectStopSign and Stop is 3000ms.

R24. The execution time interval between Controller and VehicleDynamic is less than or equal to the sum of the worst case execution time interval of each $f_p$.

R25. The execution time interval between Camera and SignRecognition is less than or equal to the sum of the worst case execution time interval of each $f_p$.

R26. The execution time interval between Camera and VehicleDynamic is less than or equal to the sum of the worst case execution time interval of each $f_p$.

R27. While AV turns left, the “turning right” mode should not be activated. The events of turning left and right considered as exclusive and specified as an Exclusion constraint.

R28. While AV is braking, the “accelerate” mode should not be activated. The events of braking and accelerating are considered as exclusive and specified as an Exclusion constraint.

R29. When AV is in the “emergency” mode because of encountering an obstacle, “turning left” mode must not be activated, i.e., the events of handling “emergency” and “turning left” are exclusive. It is specified as an Exclusion constraint.

R30. When AV is in the “emergency” mode because of encountering an obstacle, “turning right” mode must not be activated, i.e., the events of handling “emergency” and “turning right” are exclusive. It is specified as an Exclusion constraint.

R31. When AV is in the “emergency” mode because of encountering an obstacle, “accelerating” mode must not be activated, i.e., the events of handling “emergency” and “accelerating” are exclusive. It is specified as an Exclusion constraint.

Delay constraint gives duration bounds (minimum and maximum) between two events source and target. This is specified using lower, upper values given as either Execution constraints (R5 – R8) or End-to-End constraints (R17 – R23).

Synchronization constraint describes how tightly the occurrences of a group of events follow each other. All events must occur within a sliding window, specified by the tolerance attribute, i.e., the maximum time interval allowed between events (R13 – R16). Periodic constraint states that the period of successive occurrences of a single event must have a time interval (R1 – R4). Sporadic constraint states that events can arrive at arbitrary points in time, but with defined minimum inter-arrival times between two consecutive occurrences (R9 – R12). Comparison constraint
delimits that two consecutive occurrences of an event should have a minimum inter-arrival time (R24 – R26). Exclusion constraint states that two events must not occur at the same time (R27 – R31). Those timing constraints are formally specified (seen as Spec. R. IDs in Fig.2) using clock relation and expression in the context of WH then verified utilizing probabilistic analysis techniques that are described further in the following sections.
Chapter 4

Probabilistic Extension of Relations in CCSL

To perform the formal specification and probabilistic verification of EAST-ADL timing constraints (R1 – R31 in Sec 3.), CCSL relations are augmented with probabilistic properties, called PrCCSL, based on WH [8]. To describe the bound on the number of allowed constraint violations in WH, we extend CCSL relations with a probabilistic parameter $p$, where $p$ is the probability threshold. PrCCSL is satisfied if and only if the probability of relation constraint being satisfied is greater than or equal to $p$.

**Definition 1 (PrCCSL)** Let $c_1$ and $c_2$ be two logical clocks and a system model. The probabilistic extension of relation constraints, denoted $c_1 \sim_p c_2$, is satisfied if the following condition holds:

$$M \models c_1 \sim_p c_2 \iff \Pr(c_1 \sim c_2) \geq p$$

where $\sim \in \{\subseteq, \equiv, <, \preceq, \#\}$, $\Pr(c_1 \sim c_2)$ is the probability of the relation $c_1 \sim c_2$ being satisfied, and $p \in [0, 1]$ is the probability threshold.

$Pr(c_1 \sim c_2)$ is calculated based on clock ticks: $Pr(c_1 \sim c_2) = \frac{m}{k}$, where $k$ is the total number of ticks and $m$ is a number of ticks satisfying the clock relation $c_1 \sim c_2$.

**Definition 2 (Tick and History)** For $c \in C$, the tick of $c$ is indicated by a function $t_c: \mathbb{N} \rightarrow \{0, 1\}$. For $i \in \mathbb{N}$, $t_c(i)$ is a boolean variable that indicates whether $c$ ticks at the $i^{th}$ step, which is defined as: if $c$ ticks at step $i$, $t_c(i) = 1$; otherwise $t_c(i) = 0$. The history of $c$ is a function $h_c: \mathbb{N} \rightarrow \mathbb{N}$. $h_c(i)$ that represents the number of ticks of $c$ that have been fired prior to the $i^{th}$ step, which can be defined as: (1) $h_c(0) = 0$; (2) $\forall i \in \mathbb{N}^+, t_c(i) = 0 \implies h_c(i + 1) = h_c(i)$; (3) $\forall i \in \mathbb{N}^+, t_c(i) = 1 \implies h_c(i + 1) = h_c(i) + 1$.

The five CCSL relations, Subclock, Coincidence, Exclusion, Causality and Precedence, are considered and the related probabilistic extensions are defined.

**Definition 3 (Probabilistic Subclock)** The probability of subclock relation between $c_1$ and $c_2$, denoted $c_1 \subseteq_p c_2$, is satisfied if the following conditions hold:
$\mathcal{M} \models c_1 \subseteq_p c_2 \iff Pr(c_1 \subseteq c_2) \geq p$

where $Pr(c_1 \subseteq c_2) = \frac{m}{k}$, $k = \sum_{i=0}^{n} t_{c_1}(i)$, $m = \sum_{i=0}^{n} \{ t_{c_1}(i) \land (t_{c_1}(i) \implies t_{c_2}(i)) \}$

$n$ refers to the simulation bound (number of steps of an execution). $k$ is the total number of ticks of the subclock $c_1$ during the execution. $m$ is the number of ticks of $c_1$ satisfying the subclock relation. A tick of the subclock $c_1$ satisfies the relation if at the step it occurs, its superclock $c_2$ ticks. An example is shown in Fig. 4.1: among the 30 steps, $c_1$ ticks seven times, and six of them (denoted by the arrows) satisfy subclock relation. In this case, $n=30$, $k=7$ and $m=6$.

Coincidence relation states that two clocks should tick at the same step. i.e., they are subclocks of each other.

Definition 4 (Probabilistic Coincidence) The probability of coincidence relation between $c_1$ and $c_2$, denoted $c_1 \equiv_p c_2$, is satisfied if the following conditions hold:

$\mathcal{M} \models c_1 \equiv_p c_2 \iff Pr(c_1 \equiv c_2) \geq p$

where $Pr(c_1 \equiv c_2) = \frac{m}{k}$, $k = \sum_{i=0}^{n} \{ t_{c_1}(i) \lor t_{c_2}(i) \}$, $m = \sum_{i=0}^{n} \{ t_{c_1}(i) \land t_{c_2}(i) \}$

$Pr(c_1 \equiv c_2)$ represents the probability of the instants $c_1$ that are coincident with the instants of $c_2$. Coincidence relation is bidirectional, which means that $c_1$ and $c_2$ are equivalent in the relation. In this case, $k$ is the total number of steps at which either $c_1$ or $c_2$ ticks. $m$ is the number of ticks of steps at which coincidence relation is satisfied, i.e., the steps at which both $c_1$ and $c_2$ tick.

The inverse of coincidence relation, called exclusion, hinders two clocks from ticking simultaneously.

Definition 5 (Probabilistic Exclusion) The probability of exclusion relation between $c_1$ and $c_2$, denoted $c_1\#_p c_2$, is satisfied if the following conditions hold:

$\mathcal{M} \models c_1 \#_p c_2 \iff Pr(c_1 \# c_2) \geq p$, where $Pr(c_1 \# c_2) = \frac{m}{k}$,

$$k = \sum_{i=0}^{n} \{ t_{c_1}(i) \lor t_{c_2}(i) \},$$

$$m = \sum_{i=0}^{n} \{ (t_{c_1}(i) \land \neg t_{c_2}(i)) \lor (\neg t_{c_1}(i) \land t_{c_2}(i)) \}$$
k is the total number of steps at which either c1 or c2 ticks. m indicates the number of steps at which exclusion relation is satisfied, i.e., the steps at which only one of the two clocks ticks.

The probabilistic extension of causality and precedence relations are defined based on the history of the clocks. Recall that $h_{c1}(i)$ ($h_{c2}(i)$) indicates how many times $c1$ ($c2$) has ticked before the step $i$. If the history of $c1$ is greater than the one of $c2$ at the same step, we say that $c1$ runs faster than $c2$ at that step. Causality relation specifies that an event causes another one, i.e., the effect cannot occur if the cause has not.

**Definition 6 (Probabilistic Causality)** The probabilistic causality relation between $c1$ and $c2$ ($c1$ is the cause and $c2$ is the effect), denoted, $c1 \preceq_p c2$, is satisfied if the following conditions hold:

\[
\mathcal{M} \models c1 \preceq_p c2 \iff Pr(c_1 \preceq c_2) \geq p
\]

where $Pr(c_1 \preceq c_2) = \frac{m}{k}$, $k = \sum_{i=0}^{n} t_{c1}(i)$, $m = \sum_{i=0}^{n} \{ t_{c1}(i) \land h_{c1}(i) \geq h_{c2}(i) \}$

$k$ is the total number of ticks of $c1$. $m$ is the number of ticks of $c1$ satisfying causality relation. A tick of $c1$ satisfies causality relation if $c2$ does not occur prior to $c1$, i.e., the history of $c2$ is less than or equal to the history of $c1$ at the current step.

The strict causality, called precedence, constrains that one clock must always run faster than the other.

**Definition 7 (Probabilistic Precedence)** The probabilistic precedence relation between $c1$ and $c2$, denoted, $c1 \prec_p c2$, is satisfied if the following conditions hold:

\[
\mathcal{M} \models c1 \prec_p c2 \iff Pr(c_1 \prec c_2) \geq p,
\]

where

\[
Pr(c_1 \prec c_2) = \frac{m}{k}, \quad k = \sum_{i=0}^{n} t_{c1}(i),
\]

\[
m = \sum_{i=0}^{n} t_{c1}(i) \land h_{c1}(i) \geq h_{c2}(i) \land (h_{c1}(i) = h_{c2}(i) \implies \neg t_{c2}(i))
\]

$k$ indicates the total number of ticks of $c1$. $m$ is the number of ticks of $c1$ satisfying precedence and holding the two conditions: (1) the history of $c1$ is greater than or equal to the history of $c2$ at the same step; (2) $c1$ and $c2$ must not be coincident, i.e., when the history of $c1$ and $c2$ are equal, $c2$ must not tick.
Chapter 5

Specification of Timing Constraints in PrCCSL

To describe the property that a timing constraint is satisfied with the probability greater than or equal to a given threshold, CCSL and its extension PrCCSL are employed to capture the semantics of probabilistic timing constraints in the context of WH. Below, we show how EAST-ADL timing constraints, including Execution, Periodic, End-to-End, Sporadic, Synchronization, Exclusion and Comparison timing constraints, can be specified in CCSL/PrCCSL. In the system, events are represented as clocks. The ticks of clocks correspond to the occurrences of the events.

Periodic timing constraints (R1 – R4) can be specified using PeriodicOn expression and probabilistic coincident relation. For example, R1 states that the camera must be triggered periodically with a period 50ms. We first construct a periodic clock \( \text{prd}_{-50} \) which ticks every 50 ticks of \( ms \) (the universal clock). Then the property that the periodic timing constraint is satisfied with probability no less than the threshold \( p \) can be interpreted as the probabilistic coincidence relation between \( \text{cmrTrig} \) (the event that Camera \( f_p \) being triggered) and \( \text{prd}_{-50} \). The corresponding specification is given below, where \( \triangleq \) means “is defined as”:

\[
\text{prd}_{-50} \triangleq \text{PeriodicOn } ms \text{ period } 50 \quad (5.1)
\]

\[
\text{cmrTrig} \equiv_p \text{prd}_{-50} \quad (5.2)
\]

By combining (1) and (2), we can obtain the the specification of R1:

\[
\text{cmrTrig} \equiv_p \{\text{PeriodicOn } ms \text{ period } 50\} \quad (5.3)
\]

In similar, the CCSL/PrCCSL specification of R3 – R4 can be derived:

\[
\text{R3} : \ \text{obsDetect} \equiv_p \{\text{PeriodicOn } ms \text{ period } 40\} \quad (5.4)
\]

\[
\text{R4} : \ \text{spUpdate} \equiv_p \{\text{PeriodicOn } ms \text{ period } 30\} \quad (5.5)
\]
where $\text{signTrig}$ is the event/clock that $\text{SignRecognition}_f$ will be triggered, $\text{obsDetect}$ represents the event that the object detection is activated by the vehicle and $\text{spU pdate}$ denotes the event that the speed is updated (i.e., recieved by $\text{Controller}$) from the environment.

Since the $\text{period}$ attribute of the periodic timing constraint $R2$ is 200ms, which is a integral multiple of the $\text{period}$ of $R1$, $R2$ can be interpreted as a subclock relation, i.e., the event $\text{signTrig}$ should be a subclock of $\text{cmrTrig}$. The specification is given below:

$$\text{signTrig} \subseteq_p \text{cmrTrig} \quad (5.6)$$

**Execution** timing constraints (R5 – R8) can be specified using DelayFor expression and probabilistic causality relation. To specify R5, which states that the $\text{SignRecognition}_f$ must finish execution within [100, 150]ms, i.e., the interval measured from the input event of the $f_p$ (i.e., the event that the image is received by the $f_p$, denoted $\text{imIn}$) to the output event of the $f_p$ (denoted $\text{signOut}$) must have a minimum value 100 and a maximum value 150. We divide this property into two sub-properties: R5(1). The time duration between $\text{imIn}$ and $\text{signOut}$ should be greater than 100ms. R5(2). The time duration between $\text{imIn}$ and $\text{signOut}$ should be less than 150ms. To specify property R5(1), we first construct a new clock $\text{imIn}_{dly100}$ by delaying $\text{imIn}$ (the input event of $\text{SignRecognition}$) for 100ms. To check whether R5(1) is satisfied within a probability threshold is to verify whether the probabilistic causality relation between $\text{imIn}_{dly100}$ and $\text{signOut}$ is valid. The specification of R5(1) is given below:

$$\text{imIn}_{dly100} \triangleq \text{imIn} \text{ DelayFor } 100 \text{ on } ms \quad (5.7)$$

$$\text{imIn}_{dly100} \preceq_p \text{signOut} \quad (5.8)$$

By combining (7) and (8), we can obtain the the specification of R5(1):

$$\{\text{imIn} \text{ DelayFor } 100 \text{ on } ms\} \preceq_p \text{signOut} \quad (5.9)$$

Similarly, to specify property R5(2), a new clock $\text{imIn}_{dly150}$ is generated by delaying $\text{imIn}$ for 150 ticks on $ms$. Afterwards, the property that R5(2) is satisfied with a probability greater than or equal to $p$ relies on whether the probabilistic causality relation between $\text{imIn}_{dly150}$ and $\text{signOut}$ is satisfied. The specification is illustrated as follows:

$$\text{imIn}_{dly150} \triangleq \text{imIn} \text{ DelayFor } 150 \text{ on } ms \quad (5.10)$$

$$\text{signOut} \preceq_p \text{mIn}_{dly150} \quad (5.11)$$

By combining (10) and (11), we can obtain the the specification of R5(2):

$$\text{signOut} \preceq_p \{\text{imIn} \text{ DelayFor } 150 \text{ on } ms\} \quad (5.12)$$
Analogously, the CCSL/PrCCSL specification of R6 – R8 can be derived:

**R6** : \(\{\text{cmrTrig} \text{ DelayFor 20 on ms}\} \preceq_p \text{cmrOut} \quad \text{cmrOut} \preceq_p \{\text{cmrTrig} \text{ DelayFor 30 on ms}\} \) \tag{5.13}

**R7** : \(\{\text{ctrlIn} \text{ DelayFor 100 on ms}\} \preceq_p \text{ctrlOut} \quad \text{ctrlOut} \preceq_p \{\text{ctrlIn} \text{ DelayFor 150 on ms}\} \) \tag{5.14}

**R8** : \(\{\text{vdIn} \text{ DelayFor 50 on ms}\} \preceq_p \text{vdOut} \quad \text{vdOut} \preceq_p \{\text{vdIn} \text{ DelayFor 100 on ms}\} \) \tag{5.15}

where \text{cmrTrig} is the event that the Camera \(f_p\) is triggered, \text{cmrOut} represents the event that the captured image is sent out. \text{ctrlIn} (\text{ctrlOut}) represents the input (resp. output) of Controller \(f_p\). \text{vdIn} (\text{vdOut}) represents the input (resp. output) of VehicleDynamic \(f_p\).

Sporadic timing constraints (R9 – R12) can be specified using DelayFor expression and probabilistic precedence relation. For instance, R9 states that there should be a minimum delay between the event \text{veRun} (the event that the vehicle is in the Run mode) and the event \text{obstc} (the event that the vehicle detects an obstacle), which is specified as 500ms. To specify R9, we first build a new clock \text{obstc} \text{dly500} by delaying \text{obstc} for 500 ticks of \text{ms}. We then check whether the probabilistic precedence relation between \text{obstc} \text{dly500} and \text{veRun}:

\(\text{obstc_dly500} \triangleq \text{obstc} \text{ DelayFor 500 on ms} \) \tag{5.16}

\(\text{obstc_dly500} \prec_p \text{veRun} \) \tag{5.17}

By combining (16) and (17), we can obtain the the specification of R9:

\(\{\text{obstc} \text{ DelayFor 500 on ms}\} \prec_p \text{veRun} \) \tag{5.18}

Analogously, the CCSL/PrCCSL specification of R10 – R12 can be derived:

**R10** : \(\{\text{obstc} \text{ DelayFor 500 on ms}\} \prec_p \text{veAcc} \) \tag{5.19}

**R11** : \(\{\text{obstc} \text{ DelayFor 500 on ms}\} \prec_p \text{tLeft} \) \tag{5.20}

**R12** : \(\{\text{obstc} \text{ DelayFor 500 on ms}\} \prec_p \text{tRight} \) \tag{5.21}

where \text{veAcc} is the event/clock that the vehicle is accelerating. \text{tLeft} and \text{tRight} represent the event that the vehicle transits from the emergency stop mode to turn left and turn right mode respectively.
Synchronization timing constraints (R13 – R16) can be specified using Infimum and Supremum expression, together with probabilistic precedence relation. R13 states that the five input events must be detected by Controller within the maximum tolerated time, given as 40ms. The synchronization timing constraint can be interpreted as: the time interval between the earliest/fastest and the latest/slowest event among the five input events, i.e., speed, signType, direct, gear and torque, must not exceed 40ms. To specify the constraints, Infimum is utilized to express the fastest event (denoted in f ctrlIn) while Supremum is utilized to specify the slowest event sup ctrlIn. sup ctrlIn and in f ctrlIn are defined as:

\[ sup_{ctrl} \triangleq \text{Sup}(\text{Sup}(\text{speed, signType}), \text{Sup}(\text{direct, gear}, \text{torque})) \] (5.22)

\[ in_{f ctrl} \triangleq \text{Inf}(\text{Inf}(\text{speed, signType}), \text{Inf}(\text{Inf}(\text{direct, gear}, \text{torque})) \] (5.23)

where Inf(c1, c2) (resp. Sup(c1, c2)) is the Infimum (resp. Supremum) operator returns the slowest (resp. fastest) clock faster (resp. slower) than c1 and c2. Afterwards, we construct a new clock in f ctrlIn.dly40 that is the in f ctrlIn delayed for 40 ticks of ms, which is defined as:

\[ in_{f ctrlIn.dly40} \triangleq in_{f ctrlIn} \text{DelayFor 40 on ms} \] (5.24)

Therefore, the synchronization constraint R13 can be represented as the probabilistic causality relation between sup ctrlIn and in f ctrlIn.dly40, given as the CCSL/PrCCSL expression below:

\[ sup_{ctrlIn} \preceq_p in_{f ctrlIn.dly40} \] (5.25)

By combining (24) and (25), we can obtain the the specification of R13:

\[ sup_{ctrlIn} \preceq_p \{in_{f ctrlIn} \text{DelayFor 40 on ms}\} \] (5.26)

In similar, the CCSL/PrCCSL specification of R14 – R16 can be derived. For R14, we first construct the clocks that represent the fastest and slowest output event/clock among the four output events of Controller fp, i.e., reqTorq, reqDirec, reqGear and reqBrake. Then the property that the synchronization constraint is satisfied with a probability greater than or equal to p can be interpreted as a probabilistic causality relation:

\[ \text{R14: } sup_{ctrlOut} \triangleq \text{Sup}(\text{Sup}(\text{reqTorq, reqDirec}), \text{Sup}(\text{reqGear, reqBrake})) \]

\[ inf_{ctrlOut} \triangleq \text{Inf}(\text{Inf}(\text{reqTorq, reqDirec}), \text{Inf}(\text{reqGear, reqBrake})) \]

\[ sup_{ctrlOut} \preceq_p \{inf_{ctrlOut} \text{DelayFor 30 on ms}\} \] (5.27)

For R15, we first construct the fastest and slowest input event/clock among the four input events of VehicleDynamic, i.e., reqTorq, reqDirec, reqGear and reqBrake.
Then the property that the synchronization constraint is satisfied with a probability greater than or equal to \( p \) can be interpreted as a probabilistic causality relation:

\[
R_{15}: \sup_{vdIn} \triangleq \text{Sup}(\text{Sup}(\text{reqTorq}, \text{reqDirec}), \text{Sup}(\text{reqGear}, \text{reqBrake})) \\
\inf_{vdIn} \triangleq \text{Inf}(\text{Inf}(\text{reqTorq}, \text{reqDirec}), \text{Inf}(\text{reqGear}, \text{reqBrake})) \tag{5.28}
\]

\[
\sup_{vdIn} \preceq_p \{\inf_{vdIn} \text{DelayFor 40 on ms}\}
\]

For \( R_{16} \), we first construct the fastest and slowest output event/clock among the four output events of \text{VehicleDynamic}, i.e., \text{speed}, \text{direct}, \text{torque} and \text{gear}. Then the property that the synchronization constraint is satisfied with a probability greater than or equal to \( p \) can be interpreted as a probabilistic causality relation:

\[
R_{16}: \sup_{vdOut} \triangleq \text{Sup}(\text{Sup}(\text{speed}, \text{direct}), \text{Sup}(\text{gear}, \text{torq})) \\
\inf_{vdOut} \triangleq \text{Inf}(\text{Inf}(\text{speed}, \text{direct}), \text{Inf}(\text{gear}, \text{torque})) \tag{5.29}
\]

\[
\sup_{vdOut} \preceq_p \{\inf_{vdOut} \text{DelayFor 40 on ms}\}
\]

**End-to-End** timing constraints (\( R_{17} – R_{23} \)) can be specified using \text{DelayFor} expression and probabilistic precedence relation. To specify \( R_{17} \), which limits that the time duration measured from the instant of the occurrence of the event that Controller \( f_p \) receive the traffic sign type information (denoted as \text{signIn} ), to the occurrence of event that the speed is sent out from \text{VehicleDynamic} \( f_p \) (denoted as \text{spOut} ) should be between 150 and 250ms. We divide this property into two subproperties: \( R_{17}(1) \). The time duration between \text{signIn} and \text{spOut} should be larger than 150ms. \( R_{17}(2) \). The time duration between \text{signIn} and \text{spOut} should be less than 250ms. To specify property \( R_{17}(1) \), we first construct a new clock \text{signIn\_dly150} by delaying \text{signIn} for 150ms. To check whether \( R_{17}(1) \) is satisfied within a probability threshold \( p \) is to verify whether the probabilistic precedence between \text{signIn\_dly150} and \text{spOut} is valid. The specification of \( R_{17}(1) \) is given below:

\[
\text{signIn\_dly150} \triangleq \text{signIn \text{DelayFor 150 on ms}} \tag{5.30}
\]

\[
\text{signIn\_dly150} \prec_p \text{spOut} \tag{5.31}
\]

By combining (30) and (31), we can obtain the the specification of \( R_{17}(1) \):

\[
\{\text{signIn \text{DelayFor 150 on ms}}\} \prec_p \text{spOut} \tag{5.32}
\]

Similarly, to specify property \( R_{17}(2) \), a new clock \text{signIn\_dly250} is generated by delaying \text{signIn} for 250 ticks of ms. Afterwards, the property that \( R_{17}(2) \) is satisfied with a probability greater than or equal to \( p \) relies on whether the probabilistic precedence relation is satisfied. The specification is illustrated as follows:

\[
\text{signIn\_dly250} \triangleq \text{signIn \text{DelayFor 250 on ms}} \tag{5.33}
\]
\[ spOut \prec_p signIn_{dly250} \]  

By combining (33) and (34), we can obtain the specification of R17(2):

\[ spOut \prec_p \{signIn \text{ DelayFor 250 on ms} \} \]  

In similar, the CCSL/PrCCSL specification of R18 – R23 can be derived:

\[ R18 : \{cmrTrig \text{ DelayFor 120 on ms} \} \prec_p signOut \]
\[ signOut \prec_p \{cmrTrig \text{ DelayFor 180 on ms} \} \]  

\[ R19 : \{cmrTrig \text{ DelayFor 270 on ms} \} \prec_p spOut \]
\[ spOut \prec_p \{cmrTrig \text{ DelayFor 430 on ms} \} \]  

\[ R20 : \{startTurnLeft \prec_p DetectLeftSign \text{ DelayFor 500 on ms} \} \]  

\[ R21 : \{startTurnRight \prec_p DetectRightSign \text{ DelayFor 500 on ms} \} \]  

\[ R22 : \{startBrake \prec_p DetectStopSign \text{ DelayFor 500 on ms} \} \]  

\[ R23 : \{Stop \prec_p DetectStopSign \text{ DelayFor 3000 on ms} \} \]  

Comparison timing constraints (R24 – R26) can be specified using DelayFor expression and probabilistic causality relation. R24 states that the execution time interval from Controller to VehicleDynamic should be less than or equal to the sum of the worst case execution time of Controller and VehicleDynamic, denoted as \( W_{ctrl} \) and \( W_{vd} \) respectively. To specify comparison constraint, we first construct a new clock \( signIn_{dly250} \) by delaying \( signIn \) for 250 ticks of ms. Afterwards, we generate another new clock \( signIn_{dlysw} \) that is the \( signIn \) clock delayed for sum of the worst case execution time of the two \( f_p \)s. The specification is illustrated as follows:

\[ signIn_{dly250} \triangleq signIn \text{ DelayFor 250 on ms} \]  

\[ signIn_{dlysw} \triangleq signIn \text{ DelayFor } (W_{ctrl} + W_{vd}) \text{ on ms} \]  

Therefore, the property that the probability of comparison constraint is satisfied should be greater than or equal to the threshold \( p \) can be interpreted as a probabilistic causality relation between \( signIn_{dly250} \) and \( signIn_{dlysw} \):

\[ signIn_{dly250} \preceq_p signIn_{dlysw} \]
By combining (42), (43) and (44), we can obtain the specification of R24:
\[
\{\text{signIn} \ \text{DelayFor} \ 250 \ \text{on} \ \text{ms}\} \preceq_p \ \{\text{signIn} \ \text{DelayFor} (W_{ctrl} + W_{vd}) \ \text{on} \ \text{ms}\} \quad (5.45)
\]
Analogously, the CCSL/PrCCSL specification of R25 and R26 can be derived:

**R25**: \[
\{\text{cmrTrig} \ \text{DelayFor} \ 180 \ \text{on} \ \text{ms}\} \preceq_p \ \{\text{cmrTrig} \ \text{DelayFor} (W_{cmr} + W_{sr}) \ \text{on} \ \text{ms}\} \quad (5.46)
\]

**R26**: \[
\{\text{cmrTrig} \ \text{DelayFor} \ 430 \ \text{on} \ \text{ms}\} \preceq_p \ \{\text{cmrTrig} \ \text{DelayFor} (W_{cmr} + W_{sr} + W_{ctrl} + W_{vd}) \ \text{on} \ \text{ms}\} \quad (5.47)
\]

where \(W_{cmr}\) and \(W_{vd}\) represent the worst case execution time of Camera and SignRecognition respectively.

**Exclusion** timing constraints (R27 – R31) can be specified using exclusion relation directly. R27 states that the two events *turnLeft* (the event that the vehicle is turning left) and *rightOn* (the event that the turn right mode is activated) should be exclusive, which can be expressed as:

\[
\text{turnLeft} \ #_p \ \text{rightOn} \quad (5.48)
\]

Analogously, the exclusion timing constraints R28 – R31 can be specified using exclusion relation:

**R27**: \[
\text{turnLeft} \ #_p \ \text{rightOn} \quad (5.49)
\]

**R28**: \[
\text{veAcc} \ #_p \ \text{veBrake} \quad (5.50)
\]

**R29**: \[
\text{emgcy} \ #_p \ \text{turnLeft} \quad (5.51)
\]

**R30**: \[
\text{emgcy} \ #_p \ \text{rightOn} \quad (5.52)
\]

**R31**: \[
\text{emgcy} \ #_p \ \text{veAcc} \quad (5.53)
\]

where *emgcy* is the event that the vehicle is in the emergency mode, *veBrake* and *veAcc* represent the event that the vehicle is braking or accelerating, respectively.
Chapter 6

Translation of CCSL & PrCCSL into SDV

In order to formally prove the EAST-ADL timing constraints (given in Sec. 3) using Simulink Design Verifier (SDV), we investigate how those constraints, specified in CCSL expressions and PrCCSL relations (Spec. R.ID in Fig. 3.1), can be translated into Proof Objective Models (POM). CCSL expressions constructs new clocks and the relations between the new clocks are specified using PrCCSL. We first provide strategies that represent CCSL expressions in Simulink/Stateflow (S/S). We then present how the EAST-ADL timing constraints defined in PrCCSL can be translated into the corresponding POMs, which are integrated with the S/S models of CCSL expressions, based on the strategies.

6.1 Mapping CCSL Expressions into S/S

We first describe how tick and history of CCSL can be mapped to corresponding S/S models. Using the mapping, we show CCSL expressions can be modeled in S/S. A “step” (defined in Sec. 2) is represented as a sample time in Simulink and set to 0.001 second. The clock ticks are expressed as boolean variables (1 “ticking” or 0 “non-ticking”) during simulation. The history of clock (expressed as integer) is increased as the clock ticks and interpreted as a function $\text{His}(c)$ in Fig. 6.1. Since $h_c$, the history of clock $c$, is determined by the value of $c$ at the immediate precedent step, a $<\text{Delay}>$ block is employed to delay $c$ by one step. Whenever $c$ ticks at the prior step, $<\text{ES}>$ is executed and increases $h_c$ by 1.

Based on the mapping patterns of tick and history, we present how PeriodicOn, DelayFor, Infimum and Supremum expressions can be represented as S/S models.

PeriodicOn: $res \triangleq \text{PeriodicOn base period } p$, where $\triangleq$ means “is defined as”,

Figure 6.1: $h_c = \text{His}(c)$
builds a new clock res based on base clock and a period parameter p, i.e., res ticks at every $p^{th}$ tick of base. The SIMULINK model of PeriodicOn is illustrated in Fig 6.2. When base ticks, the «Matlab Function» (code is shown in the box), embedded in the «ES» subsystem, is triggered and checks if the history of the base, His(base), is an integral multiple of p. When base ticks and its history equals to the integral multiple of p, res ticks. The PeriodicOn S/S model is employed for the translation of EAST-ADL Periodic timing constraint (R1 – R4 in Fig 3.1) into its POM in SDV.

**Infimum (resp. Supremum):** res ≜ Inf(c1, c2) (resp. Sup(c1, c2)), creates a new clock res, which is the slowest (resp. fastest) clock faster (resp. slower) than the two clocks, c1 and c2. In other words, res ticks at the step whereby the faster (slower) clock between c1 and c2 ticks. The SIMULINK model of Infimum (resp. Supremum) is depicted in Fig 6.3. When c1 or c2 ticks, the inf (resp. sup) function embedded in «ES» is executed and decides which clock is faster (resp. slower) than the other by comparing the history of c1 and c2 (h1 and h2). If the clock (either c1 or c2) ticking at the current step is the faster (resp. slower) clock, res ticks. The Infimum and Supremum S/S models are utilized for the translation of EAST-ADL Synchronization timing constraint (R13 – R16 in Sec. 3) into POM. DelayFor:

**Figure 6.2:** res ≜ PeriodicOn base period p

**Infimum (resp. Supremum):** res ≜ Inf(c1, c2) (resp. Sup(c1, c2))

res ≜ base DelayFor d on ref, constructs a new clock res based on base clock and reference clock (ref), i.e., each time base ticks, res ticks at the $d^{th}$ tick of ref. The SIMULINK model of DelayFor is shown in Fig. 6.4; A STATEFLOW chart is utilized to observe the ticks of base and ref. A queue, Q, whose enqueue/dequeue operation is implemented in the function queue. y indicates whether ref has ticked $d$ times since base ticked. When base ticks (base == 1), an element with value $d$ is enqueued, and each time ref ticks, the value of the element is decreased by 1. After $d$ ticks of ref, the element becomes 0 and y becomes true. An «And» block

**Figure 6.3:** res ≜ Inf(c1, c2) (resp. Sup(c1, c2))
is applied to delimit that the tick of \( \text{res} \) must coincide with the tick of \( \text{ref} \) (i.e., \( \text{res} \) is a subclock of \( \text{ref} \)). The DelayFor S/S model is adapted to construct the POM models of EAST-ADL timing requirements R5 – R26 in Sec.[3]

![Figure 6.4: res ≜ base DelayFor d on ref](image)

### 6.2 Representation of PrCCSL in SDV

We present how the translation of EAST-ADL timing constraints (specified in PrCCSL relations and CCSL expressions) can be interpreted as POMs in the view point of analysis engine SDV. Recall the definitions of PrCCSL in Sec. 4. A PrCCSL relation is valid if the probability of a relation \( \phi \) being satisfied is greater than or equal to the given probability threshold \( p \). It can be interpreted as a Hypothesis Testing [29]: Decide whether \( \mathcal{M} \models \Pr(\phi) \geq p \) (hypothesis \( H_0 \)) against \( \mathcal{M} \models \Pr(\phi) < p \) (alternative hypothesis \( H_1 \)).

**Probabilistic Subclock** is employed to specify EAST-ADL Periodic timing constraint, given as \( \text{signRecTrig} \subseteq_p \text{cTrig} \) (Spec. R2 in Fig.3.1). The corresponding POM is shown in Fig.6.5. The STATEFLOW chart \( \text{Obs} \) in Fig.6.5(b) is utilized for Hypothesis Testing, where \( k \) is the total number of ticks of \( \text{signRecTrig} \) (subclock) and \( m \) is the number of ticks satisfying the subclock relation. Whenever

![Figure 6.5: POM of Probabilistic Subclock](image)

\( \text{signRecTrig} \) ticks, \( k \) is increased by 1, and if the subclock relation holds on that tick (i.e., the condition “\( \text{signRecTrig} \implies \text{cTrig} \)” is true), \( m \) is increased by 1. When \( k \) is increased to the sample size \( N \), the STATEFLOW chart then judges whether the number of “success” ticks of \( \text{signRecTrig} \) is greater than or equal to “\( p \times k \)” (i.e., whether
\[
m/k \geq p \text{ is valid, and it activates either valid ("H_0" is accepted) or fail state ("H_1" is accepted). A } \text{Proof Objective} \text{ block with false value is employed to check whether the probabilistic subclock relation is satisfied, i.e., the fail is never reached. In similar, using the Obs chart, other PrCCSL relations can be represented as POMs. Further details are given below. Probabilistic Coincidence is adapted to specify EAST-ADL Periodic timing constraint, given as } c_{Trig} \equiv_p \{\text{PeriodicOn ms period 50}\} \text{ (Spec. R1 in Fig.3.1). The representative POM is shown in Fig.6.6(a): A PeriodicOn subsystem (whose internal blocks are shown in Fig.6.2) is utilized to generates a periodic clock res that ticks every 50ms. According to Definition 4 in Sec. 4, if either } c_{Trig} \text{ or res ticks ("c_{Trig} OR res" is true), } c \text{ becomes true and } k \text{ is increased by 1. Meanwhile, if } c_{Trig} \text{ and res tick simultaneously ("c_{Trig} AND res" is true), } r \text{ becomes true and } m \text{ is increased by 1. Based on the value of } m \text{ and } k, \text{ Obs checks whether the probability of coincidence relation being satisfied is greater than or equal to } p \text{ and activates either valid or fail state. } \text{Proof Objective} \text{ block checks whether fail state is always inactive, i.e., H_0 is accepted.}
\]

![Diagram of POM for Probabilistic Coincidence](image)

**Probabilistic Exclusion** is utilized to specify EAST-ADL Exclusion timing constraint, given as \(\text{turnLeft} \#_p \text{ rightOn}\) (Spec. R27 in Fig.3.1). The corresponding POM is shown in Fig.6.6(b): \(k\) is increased by 1 when either \(\text{turnLeft}\) or \(\text{rightOn}\) ticks. If only one of the two clocks ticks at the current step, i.e., \(r\) (the input of \(\text{Obs}\)) is true, \(m\) is increased by 1. \(\text{Proof Objective}\) block with false value checks whether \(\text{fail}\) state is never reached, i.e., \(H_0\) is accepted.

**Probabilistic Causality** is employed to specify EAST-ADL Synchronization timing constraint, \(\sup \preceq_p \{\inf \text{ DelayFor 40 on ms}\}\) (Spec. R13 in Fig.3.1), where \(\sup\) (\(\inf\)) is the fastest (slowest) event slower (faster) than the five input events, \(\text{speed}, \text{signType}, \text{direct}, \text{gear}\) and \(\text{torque}\). \(\sup\) and \(\inf\) are defined as:

\[
\sup \triangleq \text{Sup}(\text{Sup}(\text{speed}, \text{signType}), \text{Sup}(\text{Sup}(\text{direct}, \text{gear}), \text{torque}))
\]

\[
\inf \triangleq \text{Inf}(\text{Inf}(\text{speed}, \text{signType}), \text{Inf}(\text{Inf}(\text{direct}, \text{gear}), \text{torque}))
\]
The representative POM is illustrated in Fig.6.7. The S/S models of Inf and Sup (shown in Fig.6.3) are utilized in order to construct inf (54) and sup (55), modeled as INF and SUP subsystems, respectively. A new clock dinf is generated by delaying inf for 40 ticks of ms, i.e., dinf ≜ {inf DelayFor 40 on ms}, and it is represented by using the S/S model of DelayFor (shown in Fig.6.4). Then Probabilistic Causality relation between sup and dinf is checked. According to Definition 6, when sup ticks, k is increased by 1. At the same step, if the causality relation between sup and dinf is satisfied, i.e., the history of sup is greater than or equal to the history of dinf, m is increased by 1. «Proof Objective» block analyzes if the Probabilistic Causality relation is satisfied, i.e., the fail state is never activated.

Figure 6.7: sup ≲ p {inf DelayFor 40 on ms} 

In Similar, EAST-ADL Execution (R5) can be specified in Probabilistic Causality using DelayFor and translated into corresponding POMs. The execution timing constraint R5 can be divided into two sub-properties, given as R5(1) and R5(2) in Sec.5. The POM models of R5(1) and R5(2) are illustrated in Fig.6.8(a) and Fig.6.8(b) respectively. Two intermediate clocks are generated by delaying imIn for 100 ticks and 150 ticks of ms (the output of the DelayFor subsystem). Then the execution timing constraints, interpreted as the probabilistic causality relation, can be modeled with Obs chart.

Figure 6.8: POM of Probabilistic Coincidence and Exclusion 

Comparison (R24) timing constraint, specified in Probabilistic Causality and DelayFor (see Sec.5), can be translated into the POMs presented in Fig.6.9. Two intermediate clocks are generated by using the S/S model of DelayFor, i.e., d1 is the signIn clock delayed for 250 and d2 is the clock generated by delaying signIn for (Wctrl + Wvd) ticks of ms. Afterwards, the Obs is applied to check whether the
Probabilistic Causality relation between \( d_1 \) and \( d_2 \) is satisfied, i.e., whether the history of \( d_1 \) is always greater than or equal to the history of \( d_2 \).

**Figure 6.9:** \( \{ \text{signIn DelayFor 250 on ms} \} \preceq_p \{ \text{signIn DelayFor (Wctrl + Wvd) on ms} \} \)

**Probabilistic Precedence** is used to specify EAST-ADL Sporadic timing constraint, given as \( \{ \text{obstc DelayFor 500 on ms} \} \prec_p \text{veRun} \) (Spec. R9 in Fig 3.1). The constraint delimits that two events \( \text{obstc} \) and \( \text{veRun} \) must have a minimum delay 500ms, and its corresponding POM is illustrated in Fig 6.10. A new clock \( \text{res} \) is generated by delaying \( \text{obstc} \) by 500 ticks of \( \text{ms} \), i.e., \( \text{res} \triangleq \{ \text{obstc DelayFor 500 on ms} \} \), and it is modeled by using the S/S model of DelayFor. Then R9 can be checked by verifying \( \text{res} \prec_p \text{veRun} \). As presented in Fig 6.10 whenever \( \text{res} \) ticks, \( c \) becomes true and \( k \) is increased by 1. If the tick of \( \text{obstc} \) satisfies the precedence relation, i.e., the history of \( \text{res} \) is greater than or equal to the history of \( \text{veRun} \) (excludes \( \text{res} \) and \( \text{veRun} \) are coincident), \( r \) becomes true and \( m \) is be increased by 1. <Proof Objective> block checks whether Probabilistic Precedence is satisfied, i.e., the fail state is never activated.

**Figure 6.10:** \( \{ \text{obstc DelayFor 500 on ms} \} \prec_p \text{veRun} \)

Similarly, End-to-End timing constraint (R17) specified in Probabilistic Precedence (see Sec 5) can be translated into its corresponding POM. The constraint R17 can be divided into two sub-properties, R17(1) and R17(2) (see Sec 5). The corresponding POM of R17(1) and R17(2) are presented in Fig 6.11. For R17(1), a new clock \( v \) (the output of DelayFor subsystem) is generated by using the S/S model of DelayFor such that the ticks of \( v \) is the ticks of \( \text{signIn} \) delayed for 150 ticks of \( \text{ms} \). To check whether R17(1) is satisfied is to verify whether \( v \) always precedes \( \text{signOut} \). For R17(2), a new clock \( u \) is constructed by delaying \( \text{signIn} \) for 250 ticks on \( \text{ms} \). The \( \text{Obs} \) chart is then utilized to check whether the Probabilistic Precedence between \( \text{signOut} \) and \( u \) is satisfied.
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(a) \{\text{signIn $\text{DelayFor}$ 150 on ms}\} \prec_p \text{tqOut}

(b) \text{tqOut} \prec_p \{\text{signIn $\text{DelayFor}$ 250 on ms}\}

Figure 6.11: POM of End-to-End timing constraint
Chapter 7

Modeling of AV System and its Environment in S/S

We have presented how the EAST-ADL timing constraints, specified in PrC/CSL relations and CCSL expressions are converted to POMs. To enable verification of the timed and stochastic behaviors of AV using SDV, the behaviors of each $f_p$ is described in S/S. The $FA_{SYS}$, consisting of a set of S/S is considered the entire behavior model of AV. The top-view architecture of $FA_{SYS}$ in S/S is shown in Fig.7.1.

![Figure 7.1: Top-view of AV in S/S](image)

Each $f_p$ in EAST-ADL model is modeled in a «Subsystem» with input and output ports for communication with other $f_p$s. To describe the stochastic environments of AV (modeled in the Environment subsystem in Fig.7.1), a pseudo random number generator, Mersenne Twister [25] implemented in MATLAB script is employed: 1. The traffic signs (6 types) are randomly recognized by AV and the probability of each sign type occurred is equally set as 16.7%; 2. The probability of AV being obstructed by any obstacles is set to maximum 5%; 3. Since AV runs under different road conditions, speed variation influenced by the conditions ranges within [0, 2] m/s.
Figure 7.2: Simulink model of Camera and SignRecognition

Figure 7.3: Stateflow chart of Controller
The S/S model of Camera and SignRecognition are illustrated in Fig.7.2(a) and Fig.7.2(b) respectively. Since Camera and SignRecognition are triggered to execute periodically, \textit{ExeTime} subsystem is utilized to generate a boolean signal that becomes true periodically that can be the trigger signal of the Camera and SignRecognition subsystem. In SignRecognition, the computation of traffic sign type of the detected image is implemented in a «Matlab Function» block.

As shown in Fig.7.3, a Stateflow chart is employed to model the control logic of Controller. Fig.7.3(a) presents the top-view of the Controller, which consists of two parallel states (in “AND” decomposition), \textit{Control} and \textit{Sporadic}. If the vehicle is in the emergency mode because of encounter of obstacles, \textit{emg} state will be activated. Otherwise the \textit{Normal} state will be activated. There are five substates inside \textit{Normal} states (see Fig.7.3(b)), i.e., \textit{turnLeft} (the vehicle is turning left), \textit{turnRight} (the vehicle is turning right), \textit{Stop} (the vehicle is braking to stop), \textit{dec} (the vehicle is decelerating) and \textit{acc} (the vehicle is accelerating).

The inner behaviors of VehicleDynamic in S/S is illustrated in Fig.7.4, VehicleDynamic updates the speed and running direction of the vehicle according to the requests/commands of torque, gear and direction from Controller.
Chapter 8

Experiments: Verification & Validation

We have formally specified and analyzed over 30 properties (associated with timing constraints) of the AV system. The properties (given in Sec. 3) are verified using SDV and the results are listed in Table 8.1. The simulation bound and the probability threshold are set to 60000 steps and 95% respectively. Maximum 4 properties per each EAST-ADL timing constraint are verified and all properties are established as valid. For further details regarding the full POMs and S/S models used in the experiment, refer to [6].
| Category       | R.ID | Expression                                                                 | Result | Time (Min) | Mem (Mb) | CPU (%) |
|----------------|------|----------------------------------------------------------------------------|--------|------------|----------|---------|
| Periodic       | R1   | cTrig $\lll_{0.95}$ (PeriodicOn ms period 50)                            | valid  | 6.28       | 2491     | 24.7    |
|                | R2   | signTrig $\lll_{0.95}$ (PeriodicOn ms period 200)                        | valid  | 6.36       | 3920     | 24.13   |
|                | R3   | obsDetect $\lll_{0.95}$ (PeriodicOn ms period 40)                        | valid  | 6.35       | 2357     | 24.7    |
|                | R4   | spL plate $\lll_{0.95}$ (PeriodicOn ms period 30)                        | valid  | 7          | 2218     | 24.01   |
| Execution      | R5   | $\{\text{inln DelayFor 100 on ms} \} \lll_{0.95} \text{signOut} \lll_{0.95} \{\text{inln DelayFor 150 on ms} \}$ | valid  | 38.20      | 4086     | 24.73   |
|                | R6   | $\{\text{cmrTrig DelayFor 20 on ms} \} \lll_{0.95} \text{cmrOut} \lll_{0.95} \{\text{cmrTrig DelayFor 30 on ms} \}$ | valid  | 44.26      | 14379    | 18.39   |
|                | R7   | $\{\text{ctrlIn DelayFor 100 on ms} \} \lll_{0.95} \text{ctrlOut} \lll_{0.95} \{\text{ctrlIn DelayFor 150 on ms} \}$ | valid  | 62.83      | 18306    | 6.09    |
|                | R8   | $\{\text{vdIn DelayFor 50 on ms} \} \lll_{0.95} \text{vdOut} \lll_{0.95} \{\text{vdIn DelayFor 100 on ms} \}$ | valid  | 49.13      | 17705    | 6.40    |
| Sporadic       | R9   | $\{\text{obst DelayFor 500 on ms} \} \lll_{0.95} \text{veRun} \lll_{0.95} \{\text{inln DelayFor 40 on ms} \}$ | valid  | 100.5      | 13961    | 18.05   |
|                | R10  | $\{\text{obst DelayFor 500 on ms} \} \lll_{0.95} \text{veAcc} \lll_{0.95} \{\text{inln DelayFor 30 on ms} \}$ | valid  | 120.45     | 13873    | 17.99   |
|                | R11  | $\{\text{obst DelayFor 500 on ms} \} \lll_{0.95} \text{tLeft} \lll_{0.95} \{\text{inln DelayFor 40 on ms} \}$ | valid  | 106.89     | 13775    | 16.94   |
|                | R12  | $\{\text{obst DelayFor 500 on ms} \} \lll_{0.95} \text{tRight} \lll_{0.95} \{\text{inln DelayFor 40 on ms} \}$ | valid  | 143.62     | 13775    | 16.07   |
| Synchronization| R13  | $\text{spInOut} \lll_{0.95} \{\text{inlnSpOut DelayFor 40 on ms} \}$       | valid  | 38.95      | 14135    | 16.85   |
|                | R14  | $\text{spOut} \lll_{0.95} \{\text{inlnOut DelayFor 30 on ms} \}$         | valid  | 42.66      | 20616    | 18.32   |
|                | R15  | $\text{spOut} \lll_{0.95} \{\text{inlnOut DelayFor 40 on ms} \}$         | valid  | 66.78      | 2196     | 23.36   |
|                | R16  | $\text{spOut} \lll_{0.95} \{\text{inlnOut DelayFor 40 on ms} \}$         | valid  | 34.66      | 3164     | 24.07   |
| End-to-End     | R17  | $\{\text{inln DelayFor 150 on ms} \} \lll_{0.95} \text{tqOut} \lll_{0.95} \{\text{inln DelayFor 250 on ms} \}$ | valid  | 35.95      | 6307     | 24.31   |
|                | R18  | $\{\text{cmrTrig DelayFor 120 on ms} \} \lll_{0.95} \text{signOut} \lll_{0.95} \{\text{cmrTrig DelayFor 180 on ms} \}$ | valid  | 33.96      | 6309     | 24.49   |
|                | R19  | $\{\text{cmrTrig DelayFor 270 on ms} \} \lll_{0.95} \text{spOut} \lll_{0.95} \{\text{cmrTrig DelayFor 430 on ms} \}$ | valid  | 132.45     | 16287    | 9.53    |
|                | R20  | $\text{startTurnLeft} \lll_{0.95} \{\text{DetectLeftSign DelayFor 500 on ms} \}$ | valid  | 63.23      | 130529   | 12.74   |
|                | R21  | $\text{startTurnRight} \lll_{0.95} \{\text{DetectRightSign DelayFor 500 on ms} \}$ | valid  | 76.5       | 15132    | 10.46   |
|                | R22  | $\text{startBrake} \lll_{0.95} \{\text{DetectStopSign DelayFor 500 on ms} \}$ | valid  | 69         | 15293    | 9.38    |
|                | R23  | $\text{Stop} \lll_{0.95} \{\text{DetectStopSign DelayFor 3000 on ms} \}$  | valid  | 95.7       | 15396    | 9.38    |
| Comparison     | R24  | $\{\text{inln DelayFor 250 on ms} \} \lll_{0.95} \{\text{inln DelayFor 500 on ms} \}$ | valid  | 17.88      | 6309     | 24.61   |
|                | R25  | $\{\text{cmrTrig DelayFor 180 on ms} \} \lll_{0.95} \{\text{cmrTrig DelayFor 250 on ms} \}$ | valid  | 60.15      | 6410     | 24.43   |
|                | R26  | $\{\text{cmrTrig DelayFor 430 on ms} \} \lll_{0.95} \{\text{cmrTrig DelayFor 500 on ms} \}$ | valid  | 43.33      | 17370    | 14.15   |
| Exclusion      | R27  | $\text{turnLeft} \lll_{0.95} \text{rightOn} \lll_{0.95} \text{veAcc}$       | valid  | 387.76     | 20987    | 8.25    |
|                | R28  | $\text{veAcc} \lll_{0.95} \text{veBrake} \lll_{0.95} \text{turnLeft}$       | valid  | 360.15     | 21168    | 18.15   |
|                | R29  | $\text{emgcy} \lll_{0.95} \text{turnLeft} \lll_{0.95} \text{turnRight}$    | valid  | 233.6      | 22861    | 11.98   |
|                | R30  | $\text{emgcy} \lll_{0.95} \text{turnRight} \lll_{0.95} \text{veAcc}$       | valid  | 498.51     | 23245    | 9.97    |
|                | R31  | $\text{emgcy} \lll_{0.95} \text{veAcc}$                                  | valid  | 260.96     | 22257    | 8.85    |
Chapter 9

Related work

Considerable research efforts have been devoted to formal analysis of CPS by applying SDV [12][14], which are however, limited to the functional properties without consideration of non-functional properties, i.e., timing constraints. In the context of EAST-ADL, efforts on the integration of EAST-ADL and formal techniques based on timing constraints were investigated in several works [13][16][22][28], which are however, restricted to the executional aspects of system functions without addressing stochastic behaviors. Kang [21] and Suryadevara [31][32] defined the execution semantics of both the controller and the environment of industrial systems in CCSL which are given as mapping to UPPAAL models amenable to model checking. In contrast to our current work, those approaches lack precise probabilistic annotations specifying stochastic properties. Zhang [33] transformed CCSL into first order logics that are verifiable using SMT solver. However, this work is limited to functional properties, and no timing constraints are addressed. Though, Kang et al. [15][18] and Marinescu et al. [24] presented both simulation and model checking approaches of SIMULINK and UPPAAL-SMC on EAST-ADL models, neither formal specification nor verification of extended EAST-ADL timing constraints with probability were conducted. Our approach is a first application on the integration of EAST-ADL and formal V&V techniques based on probabilistic extension of EAST-ADL/TADL constraints using SDV. An earlier study [17][19][20] defined a probabilistic extension of EAST-ADL timing constraints and presented model checking approaches on EAST-ADL models, which inspires our current work. Specifically, the techniques provided in this paper define new operators of CCSL with stochastic extensions (PrCCSL) and formally verify the extended EAST-ADL timing constraints of CPS. Du. et al. [10] proposed the use of CCSL with probabilistic logical clocks to enable stochastic analysis of hybrid systems by limiting the possible solutions of clock ticks. Whereas, our work is based on the probabilistic extension of EAST-ADL timing constraints with the focus on probabilistic verification of the extended constraints, particularly, in the context of WH.
Chapter 10

Conclusion

We present an approach to perform probabilistic analysis of EAST-ADL timing constraints in automotive systems at the early design phase: 1. Probabilistic extension of CCSL, called PrCCSL, is defined and the EAST-ADL/TADL timing constraints with stochastic properties are specified in PrCCSL; 2. The semantics of the extended constraints in PrCCSL, captured in SIMULINK/STATEFLOW, is translated into verifiable POMs for formal verification; 3. A set of mapping rules is proposed to facilitate guarantee of translation. Our approach is demonstrated on an autonomous traffic sign recognition vehicle (AV) case study. Although, we have shown that defining and translating a subset of CCSL with probabilistic extension into POMs is sufficient to verify EAST-ADL timing constraints, as ongoing work, advanced techniques covering a full set of CCSL constraints are further studied. Despite the fact that SDV supports probabilistic analysis of the timing constraints of AV, the computational cost of verification in terms of time is rather expensive. Thus, we continuously investigate complexity-reducing design/mapping patterns for CPS to improve effectiveness and scalability of system design and verification.
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