A process flow for the heterogeneous integration of III-V epitaxial material onto a silicon host wafer using CMOS-compatible materials and methods toward the goal of forming electronic-photonic circuitry is presented. Epitaxial structures for compound-semiconductor-based transistors are assembled on a silicon carrier wafer using a commercially-available polymer and then formed into distinct patterns for scalable processing. A CMOS-compatible metallization process is performed on the back side collector terminal of the aligned epitaxial structures, followed by a metal-eutectic bonding process that transfers the wafer-scale array of III-V material onto a separate silicon host wafer allowing the fabrication of both electronic and photonic devices on a single wafer. Characterization of the epitaxial bonding and transfer is performed to ensure material alignment is maintained without additional tooling and that the interconnect layer established between III-V collector and silicon host wafer performs as an ohmic contact, thermal path, and mechanical bond compatible with back-end-of-line (BEOL) integrated circuit processing. These processes are shown for GaAs-based light-emitting transistor (LET) epitaxial material to demonstrate that subsequent photonic devices and systems may be patterned into the integrated material allowing a direct electrical interconnect to embedded CMOS-based electronic systems for new functionalities as electronic-photonic integrated circuitry.

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photic system with suitable performance rests on the capability for reliable thermal and electrical management of its devices,\textsuperscript{15} so the need to establish a bonding process that addresses these is imperative for scaling novel integrated circuitry. A bonding technique that can pattern a metal interface in a CMOS-compatible manner for integrating the photonic devices is ideal.

This paper describes the methods and fabrication techniques that allow for wide-area selective and patterned distribution of III-V materials onto a silicon host, such that a bond may be formed that addresses drawbacks faced by other methods and acts as an interconnect between III-V bulk material and the carrier wafer (Figure\textsuperscript{2}). The bonding polymer (AI Technology) consists of a blend of copolymers that together act similarly to a polyimide, allowing for the polymer to create a high integrity bond between wafers that is soluble and dry-etchable in an ashless manner such that it allows for temporary adhesion.\textsuperscript{22} Thermal tests have been performed to characterize the bonding polymer, assuring that the polymer will not outgas in an N\textsubscript{2}-purged chamber up to 450 °C and as a consequence will be removable following subsequent bonding and anneal steps. The polymer is commercially-available and is in current use for handling in back side wafer processing (3D-TSV) and for other backend wafer-level processing (WLP), as well as it spins on in a void-free planar manner and is durable across a wide thermal range once it is cured. This is in line with past analyses on how to verify compatibility of temporary bonding polymers for CMOS.\textsuperscript{25} Here, this polymer's use is extended to the handling of III-V material atop a carrier wafer. In the first step of the process, the bonding polymer is spun onto the carrier wafer at a thickness of roughly 2–4 μm and a set of diced III-V epitaxial wafers are assembled epi-side down directly on the polymer in a manner similar to high-speed (low accuracy) “pick-and-place” tooling. Crystalline axes of the cleaved wafer pieces can be oriented and maintained by this tooling as well, ensuring that no misalignment occurs between pieces that may affect later etching or coupling of photonic devices.

Following the initial contact, a purged vacuum anneal is performed at 250 °C for 2 hours, applying a constant force of 5 N to the III-V bulk substrate pieces to ensure good planarization of the temporary bond during its vacuum lamination. The remaining polymer exposed between each of the bulk III-V wafer pieces is then removed in a high-power ICP-RIE O\textsubscript{2} plasma (100 sccm O\textsubscript{2}, 10 mT, 200 W RIE, 600 W ICP), as shown in Figure\textsuperscript{2}b. The final assembly is shown in Figure\textsuperscript{3}, where the III-V epitaxial pieces are seen in distribution after curing (Figure\textsuperscript{3}a) and again after the excess polymer is removed by plasma etching (Figure\textsuperscript{3}b). Critical is the fact that the III-V epitaxial layers are face-down into the bonding polymer, as shown in the scanning electron microscope (SEM) micrograph in Figure\textsuperscript{3}c, leaving the collector terminal most upward facing underneath the bulk substrate.

The assembly of the III-V wafers on the silicon carrier wafer is then prepared for removal of the GaAs-based bulk substrate on which the epitaxial layers were grown. A combination of diamond-based lapping and chemo-mechanical polishing (CMP) removes the bulk substrate of the III-V wafers (Figure\textsuperscript{2}c). The bonding polymer

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**Experimental**

**Epitaxial bonding.**—The integration of III-V material onto a silicon host begins by establishing an epitaxial bonding process. In this, III-V epitaxial wafers can be prepared on a separate silicon carrier wafer and converted into an array of fine-aligned III-V materials, ready for integration with a separate CMOS-based electronic device layer. The epitaxial bonding process is shown in Figure 2. Smaller 50 mm (2") silicon wafers are utilized here due to tooling constraints, but the process is shown to be fundamentally scalable.

A temporary bonding polymer is first used to establish a bond between III-V bulk material and the carrier wafer (Figure 2a). The temporary bonding polymer (AI Technology) consists of a blend of copolymers that together act similarly to a polyimide, allowing for the polymer to create a high integrity bond between wafers that is soluble and dry-etchable in an ashless manner such that it allows for temporary adhesion\textsuperscript{22}. Thermal tests have been performed to characterize the bonding polymer, assuring that the polymer will not outgas in an N\textsubscript{2}-purged chamber up to 450 °C and as a consequence will be removable following subsequent bonding and anneal steps. The polymer is commercially-available and is in current use for handling in back side wafer processing (3D-TSV) and for other backend wafer-level processing (WLP), as well as it spins on in a void-free planar manner and is durable across a wide thermal range once it is cured. This is in line with past analyses on how to verify compatibility of temporary bonding polymers for CMOS.\textsuperscript{25} Here, this polymer’s use is extended to the handling of III-V material atop a carrier wafer. In the first step of the process, the bonding polymer is spun onto the carrier wafer at a thickness of roughly 2–4 μm and a set of diced III-V epitaxial wafers are assembled epi-side down directly on the polymer in a manner similar to high-speed (low accuracy) “pick-and-place” tooling. Crystalline axes of the cleaved wafer pieces can be oriented and maintained by this tooling as well, ensuring that no misalignment occurs between pieces that may affect later etching or coupling of photonic devices.

Following the initial contact, a purged vacuum anneal is performed at 250 °C for 2 hours, applying a constant force of 5 N to the III-V bulk substrate pieces to ensure good planarization of the temporary bond during its vacuum lamination. The remaining polymer exposed between each of the bulk III-V wafer pieces is then removed in a high-power ICP-RIE O\textsubscript{2} plasma (100 sccm O\textsubscript{2}, 10 mT, 200 W RIE, 600 W ICP), as shown in Figure 2b. The final assembly is shown in Figure 3, where the III-V epitaxial pieces are seen in distribution after curing (Figure 3a) and again after the excess polymer is removed by plasma etching (Figure 3b). Critical is the fact that the III-V epitaxial layers are face-down into the bonding polymer, as shown in the scanning electron microscope (SEM) micrograph in Figure 3c, leaving the collector terminal most upward facing underneath the bulk substrate.

The assembly of the III-V wafers on the silicon carrier wafer is then prepared for removal of the GaAs-based bulk substrate on which the epitaxial layers were grown. A combination of diamond-based lapping and chemo-mechanical polishing (CMP) removes the bulk substrate of the III-V wafers (Figure 2c). The bonding polymer
Figure 2. Process flow of epitaxial bonding and epitaxial transfer processes. The bonding proceeds by: a) placing the III-V epitaxial wafers onto the bonding polymer, b) removing excess bonding polymer, c) performing substrate thinning on the III-V wafers, d) photolithographically defining and etching III-V islands in an array, e) removing excess bonding polymer between islands, and f) establishing an ohmic collector contact on the III-V islands. The transfer process then proceeds by: g) bringing the III-V islands in contact with a metallized host wafer, h) eutectically alloying the interface, i) removing the carrier wafer and bonding polymer, and finally j) planarizing the epitaxial material.

maintains mechanical stability of the III-V material atop the silicon during mechanical lapping and allows for scalable removal of the excess substrate. An additional wet-etch consisting of dilute ammonium hydroxide and hydrogen peroxide (NH$_4$OH:H$_2$O$_2$:H$_2$O, 4:1:8) at room temperature can also be used to remove the bulk GaAs material while maintaining its polished surface and maintaining the polymer underneath. The epitaxial structures are protected from the thinning processes throughout by means of being face-down toward the polymer. Additional findings show that the inclusion of a grown nitride dielectric on the carrier wafer beneath the bonding polymer helps alleviate stress in the polymer during substrate thinning and provides higher yield. This is notable as the yield from epitaxial bonding carries toward the final integration without further degradation. By this, substrate thinning stands as the largest factor in the overall process yield, as improvements in wet-etching chemistries and lapping techniques atop dielectric have shown pronounced increases in the area of suitable epitaxial layers, and it is expected that more automated industry-scale thinning processes can completely alleviate this factor. A wide-area distribution of III-V epitaxial material is thus formed on the carrier wafer, removed of its substrate yet held rigidly in place by the bonding polymer.

The temporarily bonded materials proceed through photolithography in order to define a geometric array of material (hereafter known as III-V islands). The III-V islands are patterned in a manner such that they take the thinned III-V wafer pieces and convert them into photolithographically-aligned blocks with high accuracy (Figure 2d). Each III-V island is defined so as to be suitable for photonic device formation, sized on the order of photonic devices (i.e. 10$^2$ μm$^2$s) and distributed as functional blocks capable of containing multiple interconnected photonic devices. A dry etch process using chlorine-based chemistry (7 sccm BCl$_3$, 20 sccm Cl$_2$, 5 mT, 100 W RIE, 800 W ICP) is calibrated so as to remove excess III-V material and establish isolated III-V islands, with the etch proceeding from the collector material and stopping at the bonding polymer. A secondary dry etch in a high-power O$_2$ plasma then removes the newly exposed bonding polymer between each III-V island (Figure 2e). Optical microscope photomicrographs of these etch processes are shown in Figure 4. The striations shown in the floor in Figure 4a are a result of the thermal stress in the bonding polymer during plasma etching, but the resulting III-V island grid in Figure 4b shows a wide-area arrangement of suitable material that maintains good adhesion to the carrier wafer. Noting the epitaxial layers are a modified HBT structure for light emission, the most upward-facing epitaxial layer after III-V island formation is the collector (n-GaAs) across the aligned grid of material.

Figure 3. Wafer-scale placement of III-V epitaxial wafers on carrier wafer during epitaxial bonding. The silicon carrier wafer is shown with a) III-V wafers placed on top of the bonding polymer after curing, b) the same assembly after removal of excess polymer, and c) a close-up SEM micrograph of the temporary bonding polymer interface, where the composition of the epitaxial layers is shown (via selective A-B etch) face-down into the polymer and the n-type collector is upwards.
This collector layer of each of the III-V islands is then utilized to establish a novel form of interconnect to enable integration. Common metallization strategies for GaAs-based photonic devices employ gold-bearing alloys, yet gold is not compatible with CMOS fabrication due to its status as a deep trap in silicon, so new contacts must be pursued. A non-gold contact is analyzed and formed by the use of a solid-phase regrowth process between palladium and germanium, where germanium migrates across the palladium during annealing and works to both alloy and degenerately dope the n-GaAs surface on the host wafer remains an aluminum layer. This still compatible with the approach outlined here so long as the terminatin on titanium-based gate contacts or using other refractory metals—is to be bonded. This metallization allows for further optimization of the III-V on Si system given titanium’s role in silicide formation and its use in self-aligning processes. Future work that might look to other metallizations used in CMOS fabrication—such as variations on titanium-based gate contacts or using other refractory metals—is still compatible with the approach outlined here so long as the terminating surface on the host wafer remains an aluminum layer. This allows for this process to accommodate a range of FEOL metallization schemes and interconnects.

A metal-eutectic bond is then pursued between the two surfaces, as shown in Figure 6. As shown, the annealed collector contact on the III-V islands ends with a terminating germanium surface, while the host wafer separately presents an aluminum floor to patterned electronics, providing an ideal platform for wide-spread interconnects of III-V islands. The Al-Ge system exhibits a straightforward binary phase alloy that has only minimal mutual solid solubility, allowing for a reliable regular-alloy to form that has seen success in silicon-based bonding processes. The interface of Al-Ge contains an intrinsic eutectic point at 420 °C that is within the range of acceptable III-V processing temperatures, far below the melting point of aluminum (660.3°C) and germanium (938.3°C). By raising the...
Figure 6. Interconnect formation between III-V and silicon material. a) The collector electrical contact is patterned on the n-GaAs while b) a separate ohmic layer is patterned on the carrier (CMOS) wafer. c) The collector contact is annealed and creates an ohmic contact to the III-V island terminating in germanium and similarly d) the carrier wafer contact is annealed and terminates in aluminum. Finally, e) a bond at the Al-Ge interface is formed by ramping the thermal profile to above the eutectic point.

After bonding, a stack of material is formed that sandwiches III-V epitaxial material between a carrier and a host wafer, held in place by temporary bonding polymer and a permanent metal-eutectic alloy, respectively. The stack of material is then submerged in a solvent stripping bath, which works to dissolve the remaining bonding polymer and allow for the liftoff of the entire silicon carrier wafer (Figure 2i) while not affecting the metal-eutectic bond. The bonding polymer comes off readily in the solvent bath, requiring only minimal heating and agitation to release the entire carrier wafer. Once the carrier wafer is clearly removed, the host wafer is inspected for the permanent bonding of III-V epitaxial material in an array. This is shown in the SEM micrograph in Figure 7, where a clear distribution of integrated III-V epitaxial material is found that maintains its fine alignment and is now electrically interconnected to a host by its collector terminal. Small amounts of the bonding polymer may remain on the integrated III-V on Si after bonding, but this is removed by conducting a final high-power ICP-RIE O₂ plasma etch to eliminate any residual organics from the surface of the host wafer in a CMOS-compatible manner. A pattern of III-V epitaxial material is now permanently integrated onto silicon, with the emitter contact facing upward and an interconnect layer below that unites collector contact to the silicon host. This arrangement has the advantage of...
allowing for thermal and electrical flow to pass vertically through the material and into the silicon substrate while any light emission from the quantum wells (QW) in the base travels parallel to the host wafer, and into the silicon substrate while any light emission from the quantum wells (QW) in the base travels parallel to the host wafer, allowing for thermal and electrical flow to pass vertically through the material and into the silicon substrate while any light emission from the quantum wells (QW) in the base travels parallel to the host wafer, distinguishing optical and electrical reference planes uniquely.

**Device preparation.**—The epitaxial layers are shown after O₂ cleaning in Figure 8. The emitter face is upward in the SEM image (Figure 8a) and what is clear is that the III-V islands stay in good form throughout the bonding process, with no signs of breakage or misaligned material that might disrupt the eventual layout of integrated photonic devices. The dimensions of the final bonded III-V islands also show strong consistency to the intended feature sizes, implying a good anisotropic dry-etch is attainable with the III-V islands also show strong consistency to the intended feature sizes, im-

![Image](image_url)
material on Si is assembled by the preceding processes and a focused ion beam (FIB) mill is performed on the surface to inspect the underlying layers and the bond, in particular. The interface at the end of one III-V island is chosen and a wide-area ion-mill (gallium ion-based) is used to etch deep into the host substrate. The results of this are shown in a series of FIB-SEM micrographs in Figure 10. In these, it is clearly seen that the bonding and transfer processes have reduced the III-V substrate to just its epitaxial layers and, by transfer, reestablished the HBT-based structure with its emitter contact upward for three-terminal photonic devices. The edge of the planarization polymer is also etched through, contributing some minor resputtering. The eutectic bond appears across the entire interface of the III-V island, assuring that good contact is formed between the underlying substrate and preventing localized heating or thermal gradients across the integrated structure (Figure 10a). The bond is void-less, confirming strong mechanical strength as per the optimized shear strength testing, while the close-up micrograph of the eutectic bond interface distinguishes the two metal stacks and shows them both to have maintained good uniformity throughout processing and transfer (Figure 10b). The interface of Pd/Ge and Ti/Al shows good adhesion to both the III-V island as its collector contact and also to the underlying host wafer, assuring that there is no degradation of electrical or thermal performance of any resulting devices.

Additional inspection of the bond is performed to assess the bond interface for thermal and electrical conduction. An infrared (IR) test is used to penetrate past the surface of the integrated material and see the uniformity of the embedded contact between electronic and photonic materials after transfer. A tungsten-filament halogen lamp that has been filtered of visible and near-IR spectrum by use of double-polished GaAs is coupled into a microscope fiber and illuminated normally onto the surface of the integrated III-V material. The results of the infrared inspection of the bond collected in a silicon-based camera are shown in Figure 11, where integrated material is atop aluminum and is surrounded by planarizing BCB. The overall bond is shown to be highly uniform in two separate inspections, void-free with only minor variations in the eutectic formation that would not degrade the overall thermal or electrical path to a CMOS host wafer. This leads to the conclusion that a uniform bond can be formed that allows for proper thermal sinking of photonic devices formed into the integrated epitaxial structure. The high thermal conductivity of the bond interface between aluminum and germanium (Al-Ge, 1.26 W cm$^{-1}$K$^{-1}$) placed between the III-V and silicon allows for good thermal characteristics of any resulting photonic devices, whereas integrated bonds formed on SOI can be expected to have thermally insulating characteristics (thin film SiO$_2$, $\sim$0.0005 W cm$^{-1}$K$^{-1}$) that can impede photonic device performance at scalable system levels. It is further expected that the choice of integrating III-V on silicon substrate via eutectic bond will have improved thermal characteristics as compared to III-V devices on a native GaAs substrate, due to the low thermal conductivity of bulk GaAs relative to silicon. The thermal mismatch between III-V and Si is therefore alleviated by the embedded metallic layer. Work is underway to compare integrated photonic devices to their native substrate counterpart.

**Discussion**

This work outlines a complete methodology for creating integrated material that is suitable for electronic-photonic circuitry, but may also be extended to the integration of other types of devices and materials.
Bulk III-V wafers are converted into integrated epitaxial layers atop a silicon host wafer in a CMOS-compatible fashion, establishing the blueprint for a network of photonic devices that can be patterned and interconnected in tandem with BEOL processing for patterned electronic gates. Owing to the metal contact that bonds the third-terminal of the photonic epitaxial material, there is the potential for directly improved thermal characteristics, improved high-speed performance, and incorporation of electronic controls for resulting photonic devices. This establishes a fundamentally scalable platform for designing complex electronic-photonic circuitry, where the processes outline may be extended to other III-V materials and other photonic device designs to allow for even wider heterogeneity in an integrated system. Other epitaxial material structures, such as based on InP or GaN, can be utilized by this process with only minor refinement of the substrate removal and metalization processes. Work has begun on investigating this for GaN-based material designs, but further work is needed to verify the possibility of extending beyond three-terminal GaAs-based epitaxial structures. Additional variations for other types of device designs are possible with the same epitaxial bonding and transfer methods. Devices desiring high thermal conductivity with low electrical conductivity are implementable with this same technique given that, though the metal-eutectic bond layer is intrinsically both electrically and thermally conductive, a portion of a semi-insulating (SI) substrate can be left intentionally as part of a designed epitaxial stack to ensure that electrical isolation is maintained for an integrated III-V island. The epitaxial bonding and transfer process shown is also extendable for creating optical interconnects between active III-V photonic material, where epitaxial material made of dielectric or wide-bandgap semiconductor may be similarly patterned into islands and transferred in the same manner, followed by the definition of this material into passive waveguide or coupling structures. Alignment between the active and passive material for good optical transmission is ensured given that the definition of photonic devices occurs after all material has been integrated. This resulting network of three-terminal active photonic material has the advantage of interfacing directly with a CMOS system containing electronic or memory structures and allows for the collector terminal to link between electronic and photonic domains in sharing logic functions as needed. As such, epitaxial bonding and transfer hold promise in addressing the bottleneck in scaling up photonic devices from discrete to system-level by establishing new methods of bonding that can line up with CMOS-compatible interconnect methods.

Conclusions

Epitaxial bonding and transfer processes are developed and characterized to allow for the full integration of III-V material onto a CMOS-compatible host wafer. A temporary bonding polymer is used for epitaxial bonding to establish a large-scale distribution of fine-aligned III-V islands in a compatible manner with post-FEOL CMOS processing, while a permanent metal-eutectic alloy is formed and analyzed to ensure that an embedded interconnect between the third-terminal of HBT-based epitaxial structures and a CMOS host wafer can be formed while acting as the ohmic contact, thermal path, and mechanical bond for the III-V material. The heterogeneous integration of III-V onto silicon allows for the subsequent patterning of photonic devices atop silicon substrate as a separate chip layer for emerging multi-functional circuit designs.

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