A New Three-Phase Multi-Level Asymmetrical Inverter With Optimum Hardware Components

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ABSTRACT In this article, a novel three-phase asymmetrical multilevel inverter is presented. The proposed inverter is designed with an optimal hardware components to generate three-phase nineteen output voltage levels. The proposed inverter exhibits various advantages like a suitable output voltage waveform with improved power quality, lower total harmonic distortion (THD), and more moderate complexity, reduction in cost, reduced power losses, and improved efficiency. A comparison of the proposed topology in terms of several parameters with existing methods illustrates its merits and features. The proposed inverter tested with steady-state and dynamic load disturbances. Various experimental results are included in this article to validate the performance of the proposed inverter during various extremities. In addition, a detailed comparison is tabulated between simulation and experimental results graphically. The proposed inverter has been stable even during load disturbance conditions. The simulation and feasibility model are verified using a prototype model.

INDEX TERMS Multilevel inverter (MLI), total harmonic distortion, asymmetrical multilevel inverter.

I. INTRODUCTION

The multilevel inverter is gaining a lot of importance in industrial and high-power applications because of the usage of low-level inverter results in an output with more significant harmonics. So, the research and study of these multilevel inverters are gaining a lot of importance. There are different methods to realize the working of multilevel inverters [1]–[6]. The most prominent among these topologies is neutral point clamped inverters, the flying capacitors, and the cascaded inverters [2]. These topologies are aided with different switching patterns like single pulse width modulation SPWM, multi-carrier pulse width modulation MCPWM, and staircase modulation technique to achieve AC output voltage waveform with lower harmonics. With an increased number of levels of the inverter, the THD improves. In a neutral point clamped method [7]–[9], diodes are used to facilitate multiple voltage levels to the capacitor bank connected in cascade mode via various phases. The diodes are the clamping devices that allow limited voltage to transfer through them, reducing the stress from other devices. The peak voltage of these inverters is half of the energy supplied, which is one shortfall and the same can be eliminated by aggregating the number of diodes, switches, and condensers, the output voltage is limited and for over three-levels the charge balance gets disturbed. The applications of these inverters include static Var compensation, variable motor speed drives, high voltage DC and AC transmission lines, high voltage system interconnection. Flying capacitors [10] topology is quite similar to the diode-clamped multilevel inverter, but capacitors clamping devices in this method, unlike the diode-clamped MLI [23]–[39].

In recent past, modular multilevel converters (MMC) are suited for high-voltage applications and these are introduced with various sub-modules, where each sub-module comprises two switches with a DC capacitor. The switching losses and harmonics are less. Number of switches and capacitors are used in this topology, which increases the control complexity.
and cost [11], [12]. There are three types of multilevel inverters neutral point clamped (NPC) [13], Cascade H-bridge inverter (CHB) [14] and flying capacitor (FC) [15]. Number of switches and clamping diodes are used in diode-clamped inverter for higher levels, moreover the balancing of capacitors is a challenging task as these are connected in series. Even for higher levels, larger number of capacitors are used in flying capacitor where the balancing of voltage is complex [16].

The advantage of symmetric structures is modularity that can able to design and extend easily. Two such inverter structures are presented in [17], [18], where the mixture of basic units and H-bridge used based on non-isolated DC sources require number of switches, increases the control complexity, size and cost. A new multilevel inverter topology with insulated driver circuit and reduced number of switches has been presented in [19]. In addition, the calculation of DC voltage sources is proposed, and it comprises four high rating switches. This requires a bi-directional switch for the blocking voltage and conducting current in both directions.

In [20], a three-phase multilevel inverter suited for electrical drive applications has been presented. Counterpart of the CHB inverters, power cells are cascaded, and each cell is having two series legs. The design equations for the load voltage with steps carried out using pulse-width modulation phase shifting multi-carrier modulation technique are analyzed. There are several DC voltage sources in this topology results in the increase in the total cost of the inverter which is a disadvantage of this structure.

A new topology of multilevel inverter is presented in [21]. This structure mainly focuses on reducing the power transistors regarding the number of levels. Various equations are derived mathematically. This requires a bi-directional switch for the blocking voltage and conducting current in both directions.

This article presents a reduced circuit part for renewable energy applications, counting inverter topology at nineteen levels. This manuscript presents a 19-level asymmetric cascaded MLI with reduced DC sources and switches with relativity low THD. The proposed inverter is implemented and tested only with a resistive, inductive load, and dynamic variations in the load from R to L and vice versa. The analysis of total standing voltage can be done [22]. During the dynamic load period conditions, the proposed inverter is well stabilized [23]–[41], and this inverter is suitable for renewable energy applications [23]–[41].

The article was structured as follows. Section II that follows can the details of the proposed topology of 19-levels. Part III presents the parameter calculations, section IV presents the loss and efficiency, section V presents TSV calculation, and section VI and section VII present the findings of the analysis and experiment along with the simulation results.

II. PROPOSED THREE-PHASE ASYMMETRICAL INVERTER TOPOLOGY

The proposed three-phase 19-level-inverter is shown in Fig.1. The topology proposed for each phase comprises two bidirectional and nine unidirectional power semiconductor switches for each phase leg is shown in Fig.2. The bidirectional switches are used to avoid short-circuits and to block currents in both directions for the DC supply. In this topology, usually, the desired voltage is realized from different DC voltage links or sources. Based on the DC sources, the cascaded MLIs are classified as symmetrical(equal) and asymmetrical(unequal) inverters. In symmetrical type, the voltage of the DC links is held at the same level. The demerit of symmetrical topology is that with the increase in output voltage levels, the number of switches also increases. In order to overcome this,
TABLE 1. Conduction states of switches.

| Mode | S1 | S2 | S3 | S4 | S5 | S6 | V(V1) | V(V2) | V(V3) |
|------|----|----|----|----|----|----|-------|-------|-------|
| 1    | 0  | 1  | 0  | 1  | 0  | 1  | 0     | 1     | 0     |
| 2    | 0  | 1  | 0  | 1  | 0  | 1  | 0     | 1     | 0     |
| 3    | 0  | 1  | 0  | 0  | 1  | 1  | 0     | 1     | 0     |
| 4    | 1  | 0  | 0  | 1  | 0  | 1  | 0     | 1     | 0     |
| 5    | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 6    | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 7    | 0  | 1  | 0  | 0  | 1  | 1  | 0     | 1     | 0     |
| 8    | 0  | 1  | 0  | 1  | 1  | 1  | 0     | 1     | 0     |
| 9    | 1  | 0  | 1  | 0  | 0  | 1  | 0     | 0     | 0     |
| 10   | 0  | 0  | 1  | 0  | 1  | 0  | 0     | 0     | 0     |
| 11   | 1  | 0  | 1  | 1  | 0  | 0  | 1     | 1     | 0     |
| 12   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 13   | 0  | 1  | 0  | 1  | 0  | 0  | 0     | 0     | 0     |
| 14   | 0  | 0  | 1  | 0  | 1  | 0  | 0     | 0     | 0     |
| 15   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 16   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 17   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 18   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |
| 19   | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |

In Mode-4, the power switches S1, S3, S5, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 + V_3 = +400.5V \) at the load ends. In Mode-5, the power switches S1, S2, S5, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_3 = +222.5V \) at the load ends. In Mode-6, the power switches S3, S4, SA, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_3 = +178V \) at the load ends. In Mode-7, the power switches S2, S4, SA, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_2 = +44.5V \) at the load ends. In Mode-8, the power switches S2, S4, S5, SA, SB, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_2 = +89V \) at the load ends. In Mode-9, the power switches S1, S3, S4, TA, and TB are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_1 = +133.5V \) at the load ends. In Mode-10, the power switches TB, and TP are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_0 = 0V \) at the load ends. In Mode-11, the power switches S1, S3, S4, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is \( V_O = V_1 = +133.5V \) at the load ends. In Mode-12, the power switches S2, S4, S5, SA, SB, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 = +178V \) at the load ends. In Mode-13, the power switches S2, S4, SA, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 = +89V \) at the load ends. In Mode-14, the power switches S3, S4, SA, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 = +222.5V \) at the load ends. In Mode-15, the power switches S1, S2, S5, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 = +267V \) at the load ends. In Mode-16, the power switches S1, S3, S4, TC, and TD are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \( V_O = V_1 + V_2 = +267V \) at the load ends. In Mode-17, the power switches S2, S4, SB, TC, and
T\(_D\) are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \(V_0 = -(V_1 - V_2 + V_3) = -311.5\) V at the load ends. In Mode-18, the power switches \(S_2, S_5, S_A, T_c,\) and \(T_D\) are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \(V_0 = -(V_1 + V_3) = -356\) V at the load ends. In Mode-19, the power switches \(S_3, S_5, S_A, T_c,\) and \(T_D\) are turn-on(conduction state) and remaining switches will turn-off then, the output voltage is the sum of \(V_0 = -(V_1 + V_2 + V_3) = -400.5\) V at the load ends. The expected (typical) output and gate pulse waveform are shown in Fig.22 and simulation output voltage, current, THD, and gate pulses are generated by staircase pulse width modulation technique are shown in Fig.23 to Fig.27 respectively. The proposed 19 level asymmetrical MLI is designed in such a way that the desired output voltage to be 400V. This can be achieved by the proper design of DC sources, such as \(V_1=133.5\) V, \(V_2=44.5\) V and \(V_3=222.5\) V based on the number of levels and proposed topology. The selection of bidirectional switches at a specific location avoids the short circuit and blocks the current in both directions for a DC supply. The selected DC sources are tested with various modes of operation based on the conduction of switches regarding the switching frequency, and the expected output is achieved, which is explained in Table.1.

A. DEVELOPMENT OF POTENTIAL MLI PARAMETERS

Parameters for the proposed topology circuit are set as:

The switches number(No. of switches) are calculated as:

\[
N_{\text{switches}} = 3k + 2 \quad (1)
\]

If \(k\) is the no. of sources, then the switches no. of switches = \(3 \times 3 + 4 = 13\) by taking \(k=3\).

The sources no. of are calculated as:

\[
N_{\text{source}} = k \quad (2)
\]

Then the sources are \(N_{\text{source}}=3\), taking \(k=3\)

The output level No. of is got as:

\[
N_{\text{levels}} = 2\left(2^k\right) + 3 \quad (3)
\]
Then the level no. of is \( N_{\text{level}} = 2(2^3 + 3) = 19 \) with \( k = 3 \)

The voltage from the output is defined as;

\[
V_{\text{output}} = \left[ \left( 2^k \right) + 1 \right] \times V_2 \tag{4}
\]

Then the voltage of the output is

\[
V_{\text{output}} = (2^3 + 1) \times 44.5 = 400.5V, \text{ taking } k = 3 \text{ and } V_2 = V_{\text{dc}} = 44.5V.
\]

III. POWER LOSS AND EFFICIENCY CALCULATION OF MLI

The losses can be calculated in both cases, the losses of conduction and losing switching are the two key losses that follow switches. The conduction losses can be got as follows;

\[
P_{\text{Cl,IGBT}(t)} = \left[ V_{\text{IGBT}} + R_{\text{IGBT}}i^2(t) \right] \times i(t) \tag{5}
\]

where \( V_{\text{IGBT}} \) is IGBT forward voltage drop, and \( V_{\text{diode}} \) is diode drop forward voltage. The \( \alpha \) is a constant for the
FIGURE 18. Mode-16 $V_O = -(V_2 + V_3) = -267V$.

FIGURE 19. Mode-17 $V_O = -(V_1 - V_2 + V_3) = -311.5V$.

FIGURE 20. Mode-18 $V_O = -(V_1 + V_3) = -356V$.

FIGURE 21. Mode-19 $V_O = -(V_1 + V_2 + V_3) = -400.5V$.

IGBT specification [41], [42], and $R_{IGBT}$ is the equivalent resistance of the IGBTs and $R_{d}$ is the equivalent resistance of the diodes [41], [42]. The average value of the conductive power loss ($P_{cl}$) of the multilevel inverter can be given as follows [41], [42], considering that the current path includes both $N_{IGBT}$ transistor and $N_{d}$ diodes at the moment $t$ [47].

$$P_{cl} = \frac{1}{2\pi} \int_0^{2\pi} \left[ N_{IGBT} (t) P_{cl,IGBT} (t) \right] dt$$

Switching loss can be calculated according to the capacity used in the switches. Losses may be got depending on the turn-on and turn-off times of the switches. The losses from switching can be estimated based on linear differences in switching current and voltage. The energy figures are: Where $E_{on}$ and $E_{off}$ are respectively the switch $k$ turn-ON and turn-OFF losses. The losses from switching are equal to the sum of power losses from turn-on and turn-off, calculated:

$$P_{sl} = f \sum_{K=1}^{N_{switch}} \left[ \sum_{j=1}^{N_{on,k}} E_{on,kj} + \sum_{j=1}^{N_{off,k}} E_{off,kj} \right]$$

The total power losses calculated as follows ($P_{total}$ loss)

$$P_{total} = P_{cl} + P_{sl}$$

The efficiency of the Inverter given below

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{P_{out} + P_{loss}}{P_{in}}$$

where the output power and the input power are $P_{out}$ and $P_{in}$, respectively.
Using equation (10) ($V_{\text{rms}} = 282.4$V \& $I_{\text{rms}} = 2.828$A) the experimental output power of 799.87 W is got. For measurement, the parameter values are taken from the IGBT CM75DU-12 datasheet [41], [42]. The $V_{\text{switch}}$ value (0.6V) is taken from the plot of performance characteristics and RIGBT is 0.4-ohm, turn-on delay as 100 ns, turn-on up time as 250 ns, turn off delay time as 200 ns and turn off fall time as 300 ns for 11 switches [41], [42]. The proposed inverter architecture would require 37 measures in one full cycle. The conduction losses are determined by using equation 1; $P_{\text{cl}} = 53.854$ W, and $E_{\text{on}}, E_{\text{off}}$ are 0.124W and 0.1625W respectively, from equation 7 the switching losses are 0.2865 W, therefore, the total losses are calculated during the conduction time and switching time by using equation 8 is 54.14W, finally from equation 9 efficiency is 93.67%. 

**IV. COMPARISON WITH RECENT INVERTERS**

The proposed inverter contrasted with related topologies of new inverters. Table.2 and Fig.28 to Fig.34 provides a comparison of different component parameters such as several electrical power switches (NSW), several DC sources (NDCS), driver circuits (NDC), clamping diodes (NCMP), clamping capacitors (NCP), efficiency (Eff), TSV, THD and higher output voltage levels required for the inverter proposed. thirteen power switches and three DC sources were used in this topology. Next, the sum of gate driver circuits is thus the same as the number of switches. Then, compared
to existing topologies, the suggested asymmetrical topology, each part was calculated for a similar voltage level. While all current topologies will need 10 to 22 switches [43]–[48] and 1 to 8 DC sources to provide an output voltage of 19 rates, the proposed topology needs only 13 switches and three sources with low THD. Compared with traditional topology, the drastically reduced need for switches in the proposed topology to produce better results makes it more suitable for a potential renewable application. Since the DC-link condensers are not required for the proposed topology, they are free from the question of voltage balance. Besides that,
it doesn’t require any capacitor clamping and diodes clamping. Every topology, therefore, has its own merits and demerits. The topology suggested has several benefits, such as fewer switching devices, DC source count and driver circuits, and a minimum number of switches per voltage point. For asymmetric topology, the value of 3.89 percent total harmonic distortion (THD) follows the IEEE 519 requirement. Therefore, it concluded that the proposed topology requires a minimum switch count using both high and fundamental switching frequencies, thus minimizing power losses and costs.

V. TSV (TOTAL STANDING VOLTAGE) CALCULATION
The maximum voltage stress across all switches is the important parameter for the topology, and it can be represented as the total standing voltage (TSV), which is equal to the sum of maximum voltage stress across the switches [49], [50]. This is an important factor for the selection of switches. Total standing voltage (TSV) is the term which is determined regarding the blocking voltages across all the switches with all voltage levels considered. The voltage stresses across each pair of the complementary switch will be same. However, the TSV is calculated for the proposed topology and is compared with various topologies and found to be the best in having the least standing voltage because of which the losses get decreased. As the blocking voltage capability is less, the rating of the switches is fewer results in cost effective. The voltage stress of the switches in different units is given as: The bidirectional switch voltages are \( V_{Sbi} = V_i \) and the unidirectional switch voltages are \( V_{Sui} = 2V_i \) where \( i = 1, 2, \ldots, n \) and \( n \) is the number of complementary switches. With tertiary mode, the maximum output voltage \( V_{o,max} \) of the proposed topology is:

\[
V_{o,max} = 400V
\]  

(11)

The total standing voltage (TSV) is an important factor for the selection of switches. TSV is the addition of the maximum blocking voltage across each semiconductor device [22]. The look-up table for 19-level inverter is shown in Table.3. Therefore, the voltage across the switches are:

\[
\begin{align*}
V_{S1} &= 6V_{dc} \\
V_{S2} &= V_{S5} = 10V_{dc} \\
V_{S3} &= V_{S4} = 8V_{dc} \\
V_{TA} &= V_{TC} = 9V_{dc} \\
V_{TB} &= V_{TD} = 10V_{dc}
\end{align*}
\]

The voltage stress of unidirectional switches of a bidirectional switch is given as: \( V_{SA} = 6V_{dc} \) and \( V_{SB} = 2V_{dc} \). As two unidirectional switches are used for the two bidirectional switches, blocks the voltage of 8Vdc. Therefore,

\[
T_{SV} = 2(V_{S1} + V_{TD} + V_{TB}) + V_{SA} + V_{SB} = 52V_{dc} + 8V_{dc} = 60V_{dc}
\]  

(12)

The TSV (total standing voltages) of the proposed inverter is compared with existing inverters is shown in Fig.34.

VI. EXPERIMENTAL RESULTS
The prototype for 19 level inverter hardware setup systems is recognized and confirmed it experimentally. Fig. 44 specifies the prototype of the multilevel inverter proposed for
TABLE 3. The look up table for 19-level inverter.

| Level | ON Switches |
|-------|-------------|
| 1     | $S_3, S_4, S_A, T_A, T_B$ |
| 2     | $S_2, S_3, S_A, T_A, T_B$ |
| 3     | $S_2, S_A, S_B, T_A, T_B$ |
| 4     | $S_1, S_3, S_A, T_A, T_B$ |
| 5     | $S_1, S_2, S_A, T_A, T_B$ |
| 6     | $S_5, S_4, S_A, T_A, T_B$ |
| 7     | $S_5, S_A, S_B, T_A, T_B$ |
| 8     | $S_2, S_4, S_A, S_B, T_A, T_B$ |
| 9     | $S_1, S_3, S_A, T_B, T_D$ |
| 10    | $T_A, T_B$ |
| 11    | $S_7, S_8, S_A, T_C, T_D$ |
| 12    | $S_2, S_8, S_A, T_C, T_D$ |
| 13    | $S_2, S_8, S_A, T_C, T_D$ |
| 14    | $S_8, S_A, S_B, T_C, T_D$ |
| 15    | $S_1, S_8, S_A, T_C, T_D$ |
| 16    | $S_1, S_8, S_B, T_C, T_D$ |
| 17    | $S_8, S_A, T_C, T_D$ |
| 18    | $S_7, S_8, S_A, T_C, T_D$ |
| 19    | $S_8, S_A, T_C, T_D$ |

FIGURE 35. Experimental Gates Pulses of 19 MLI.

FIGURE 36. Experimental Output waveform of Phase Leg-A 19 MLI.

FIGURE 37. Experimental Output voltage & current waveform of 19 MLI.

FIGURE 38. Experimental Output waveform of Three-Phase 19 MLI.

FIGURE 39. Experimental Output waveform of Phase Leg-A with R Load.

this. Simulink block sets are dumped in to the digital I/O ports by dSPACE RTI 1104, and the MATLAB-Simulink is used to implementing the PWM form of staircase modulation (for gate pulses). Use 20 output pins, which are calculated using physical I/O ports, and real-time interfacing applications are facilitated. The pulse is created from the TLP 250 instrument, which is mined to input the RTI 1104 dSPACE. Gate driver is used to boosting the 5 V to 15 V PWM pulse setup. The control switch is turned on with a 15 V pulse. The specifications of the prototype model part are shown in Table 5, the results of the prototype investigation are verified at a steady-state, load disturbance situations are conducted with the help of resistive, inductive loads, and THD is shown in Figures 35 to 43, respectively.
The pulses from the gate produced using Driver Circuit TLP250 is shown in Figure.35. The steady-state study was verified with 400 V resistive load (R load), with 4 A attaining output current. The RMS output and voltage found at 282.84 V and 2.828 A current, respectively. The hardware tests are shown respectively in Figure.36, Figure.37, Figure.38 and Figure.39. The experimental prototype results show notably that with 19 output voltage levels. Spéciously, the waveform shows that the angle of the transition between the charge current and the charge voltage is zero.

After the achievements of steady-state testing with resistive load, we presented 400 V motor (inductive value is 98mH with 50ohm internal resistance) load (loading power factor) and 6.8 A current. The output current and voltage RMS value are respectively reached with 282.84 V and current 4.808 A. The experimental findings are given in Figure.40. The results show that, with 19 output voltage levels. The phase angle between the lagging charge current and the lagging load voltage is shown in the waveform. To be sure, tons rarely happen distinctly. These can happen continuously in resistive and inductive loads. Typically, where a resistive load is present, an unforeseen addition of inductive load is likely to match the resistive load in parallel or vice versa. The output...
the sizing of the circuit components. The proposed inverter balanced well during complex charging (load disturbance) conditions. This inverter is highly adaptive for high-power and renewable energy systems.

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