The design of large image rejection and wideband CMOS active polyphase filter for BeiDou RF receiver

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Abstract In this letter, a new circuit structure for CMOS active polyphase filter is proposed and analyzed. In the proposed structure, the currents produced from two cascode stage with a capacitor and single cascode stage in a single-stage are used to realize high-pass and low-pass functions, respectively. Compared to other conventional active polyphase filters, the proposed polyphase filter uses a simpler structure to achieve strong image rejection at the higher frequency while obtaining lower power consumption, respectively. Compared to other conventional active polyphase filters, the proposed active polyphase filter occupies less than 0.36mm² of chip area. From the measurements, the four-stage active polyphase filter shows an image rejection ratio of more than 58.2dB at frequencies of 26MHz to 65MHz, a voltage gain of 5.8dB and an IIP3 of 1.5dBm at 45 MHz while consuming only 2.64mA from a 1.8-V supply.

Keywords: active polyphase filter, complex filter, image rejection, low intermediate receiver

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Currently, the low intermediate frequency (IF) quadrature down-conversion architecture [1, 2, 3, 4, 5, 6] have been adopted as excellent RF receiver topologies to realize to highly integrated, high-performance, low-cost RF integrated circuits, such as the global navigation satellite systems (GNSS) RF receiver [7, 8, 9, 10, 11]. Image interferences has important effect on the final required signal-to-noise ratio (SNR) outputted to the baseband. In order to achieve high selectivity between the desired and image signals, we can select higher intermediate frequency and use an on-chip polyphase filter (PPF). Moreover, polyphase filters in some applications require wide bandwidths. For example, more than 20 MHz of channel bandwidth is required for Compass (also known as BeiDou) B3 band. Furthermore, the low-power design adopted is important for the RF receivers as the battery lifetime is limited by the power consumption of the electronics circuit. Therefore, the design of high-performance, wideband, and low-power on-chip polyphase filters for these applications are critically needed.

In most applications, polyphase filters are divided into passive polyphase filters and active polyphase filters. The passive polyphase cascading several stages can exhibit high image rejection ratio (IRR) and wide bandwidth [12, 13, 14, 15, 16, 17, 18]. However, they should consume more power and occupy more chip area. Firstly, additional buffers be employed to compensate the loss caused by cascading. Secondly, more stages should be used to compensate process and temperature variations, because the on-chip passive device is difficult to be adjusted. In contrast with passive polyphase filters, active polyphase filters have the general advantages of small chip area, high signal gain and easy tuning. Many active polyphase filters have also been discussed in some literature [19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30], but few of them achieve strong image rejection at high operating frequency and low-power dissipation.

In this letter, a new tunable CMOS active polyphase filter with a higher operating frequency and lower power consumption is proposed. The basic architecture based on cascode structure is used to realize the same function of the passive polyphase filter mentioned in [12]. Compared with the conventional active polyphase filter [19], the proposed polyphase filter structure effectively enhances the matching of pole frequencies and gains of high-pass and low-pass filters to achieve strong image rejection at higher operating frequency while obtaining lower power consumption, wide bandwidth and smaller chip area.

2. Model for polyphase filters

Fig. 1 [13] shows the signal flowgraph for the realization of the polyphase filter which is a complex filter. The transfer function of the one-stage polyphase filter can be represented as

\[ H(s) = H_L(s) + jH_H(s) = \frac{A_L \cdot \omega_L}{s + \omega_L} + \frac{A_H \cdot s}{s + \omega_H} \]  \hspace{1cm} (1)

where \( A_L, A_H \) and \( \omega_L, \omega_H \) are the gain and pole frequency of first-order low-pass filter \( H_L(s) \) and the high-pass filter \( H_H(s) \), respectively. In the low IF receiver, the image and desired signals are down-converted by quadrature LO phases...
to the same frequency but into two opposite sequences [12], which are negative frequency and positive frequency. The image and desired signals are presented in differential and quadrature phases. According to (1), the desired signal with negative frequency \((s = -j\omega_p)\) falls in the filter’s passband while the image signal at positive frequency \((s = j\omega_p)\) is attenuated. If the gains and pole frequencies of \(H_L(s)\) and \(H_H(s)\) are perfectly matched, assuming \(s = -j\omega_p\) or \(s = j\omega_p\), \(\omega_L = \omega_H = \omega_p\) and \(A_L = A_H = A\) then (1) can be rewritten

\[
H(-j\omega_p) = A - \frac{\omega_p + j\omega_p}{-j\omega_p + \omega_p} = A \frac{2}{1-j}
\]

\[
H(j\omega_p) = A \frac{-\omega_p - j\omega_p}{j\omega_p + \omega_p} = 0
\]

As may be seen from (2) and (3), the gain of the desired signal and the image signal can equal to \(\sqrt{2}\) and zero at \(\omega_p\) respectively, i.e., the polyphase filter completely rejects image signals.

In practical applications, due to impairment of the device and the circuit design structure, it is difficult to achieve the accurate matching of gains and pole frequencies of \(H_L(s)\) and \(H_H(s)\). As shown in Fig. 2(a), it is observed that the pole frequencies of the filters are shifted to the opposite directions and the resulting IRR is degraded at the desired frequency. Assuming \(\Delta A\) and \(\Delta \omega\) are the mismatch quantities of \(A\) and \(\omega_p\), the literature [19] demonstrates that if \(|\Delta A/A| > 12\%\) or \(|\Delta \omega/\omega_p| > 5\%\), then the IRR at \(\omega_p\) is degraded to \(-30dB\).

Fig. 2(b) shows the low-pass filter circuit which is used to realize the conventional active polyphase filter circuit mentioned in [19]. Some non-ideal factors of the circuit may affect the magnitude and phase of \(H_H(s)\) and \(H_L(s)\) thus degrade the IRR of the polyphase filter, especially in high frequency signal processing field. Firstly, the parasitic capacitance \(C_P\) at node A has the large value, which consists of the parasitic capacitance of \(C_C\) and the device capacitance of \(M_4\) and \(M_5\), because the value of \(C_C\) needs to be big enough for reducing signal loss and the minimum length of the MOS devices is not used in this design to reduce the gain mismatch caused by copying currents. Secondly, in the conventional circuit structure, the multiple current mirrors are used to combine the functions of low-pass and high-pass filters, the kind of structure not only consumes more current but also produces some mismatches in copying currents even without minimum-length transistors.

Fig. 3 plots the simulated IRR curves of the single stage polyphase filter with different \(\omega_p\), which is set at 25MHz, 45MHz and 65MHz. The results show that the conventional structure could not get satisfactory effects of image rejection. Meanwhile, IRR is severely degraded from \(-40dB\) to \(-32dB\) with the increasing of \(\omega_p\). Therefore, the new polyphase filter circuit structure should be proposed in this letter, of which the gains and pole frequencies in \(H_L(s)\) and \(H_H(s)\) can be kept highly consistent to achieve the desired image rejection performance at high operating frequency.

3. Proposed active polyphase filter

As discussed in the previous section, the proposed polyphase filter structure consists of a low-pass circuit and a high-pass circuit. Therefore, a low-pass trans-conductance stage \((Gm_1)\) and a high-pass trans-conductance stage \((Gm_H)\) should be designed to realize the proposed active polyphase filter. A pseudo differential structure which consists of four cascode stages and two capacitors represented by \(C_L\), shown in Fig. 4, are the basic kernel of the proposed \(GmL\) cell. The differential output current \(i_L = i_{L+} - i_{L-}\) can be written as

\[
i_L(s) = \frac{v_I g_{m1}}{s+g_{m2}/C_L}
\]

where \(v_I = (V_{IP} - V_{IN})\) is the differential input voltage; \(g_{m1}\) and \(g_{m2}\) are the transconductances of \(M_1\) and \(M_2\). As shown in Fig. 4, the cross-coupled pseudo-differential structure is adopted to realize the proposed \(Gm_H\) cell, which consists of a cascode pseudo differential pairs and a proposed \(Gm_L\) cell. The differential output current \(i_H = i_{H+} - i_{H-}\) can be written as can be derived as
and H, A node C analyzed. When consider the parasitic capacitance this design, the parasitic effects of the circuit in Fig. 4 are consumption but also can achieve strong image rejection. In fore, the proposed polyphase filter not only has lower power consumption, it also has a more symmetric circuit structure. Moreover, the conventional circuit structure, the low-high-pass output currents are produced directly by simpler and more symmetric circuit structure. Moreover, the conventional circuit structure needs more current path between the rails to output low-pass differential currents (i_L+) and high-pass differential currents (i_H-). Therefore, the proposed polyphase filter not only has lower power consumption but also can achieve strong image rejection. In this design, the parasitic effects of the circuit in Fig. 4 are analyzed. When consider the parasitic capacitance of node A, assuming C_L ≫ C_P, the transfer function of H_L(s) and H_H(s) can be derived as

\[
H_L(s) = \frac{g_{m1}}{g_{mL}} \frac{g_{m2}/C_L}{s + g_{m2}/C_L} \tag{5}
\]

\[
H_H(s) = \frac{g_{m1}}{g_{mL}} \frac{s}{s + g_{m2}/C_L} \tag{6}
\]

Where \(g_{mL}\) is the trans-conductance of transistor \(M_L\). The pole \(\omega_p\) of \(H_L(s)\) and \(H_H(s)\) shown in (6), which is also called as the rejected center frequency \(F_C\) (\(F_C = \omega_p/2\pi\)), are determined by \(g_{m2}\) and \(C_L\). Therefore, the \(F_C\) can be adjusted to required frequency point by changing \(g_{m2}\) and \(C_L\). Unlike the conventional circuit structure, the low-high-pass output currents are produced directly by simpler and more symmetric circuit structure. Moreover, the conventional circuit structure needs more current path between the rails to output low-pass differential currents and the high-pass differential currents. Therefore, the proposed polyphase filter not only has lower power consumption but also can achieve strong image rejection. In this design, the parasitic effects of the circuit in Fig. 4 are analyzed. When consider the parasitic capacitance of node A, assuming \(C_L ≫ C_P\), the transfer function of \(H_L(s)\) and \(H_H(s)\) can be derived as

\[
H_L(s) = \frac{g_{m1}}{g_{mL}} \frac{g_{m2}/(C_L + C_P)}{s + g_{m2}/(C_L + C_P)} \tag{7}
\]

As (7) shows, the second pole, which is generated at \(\omega_{p2} = g_{m2}/C_P\), may degrade the IRR of the polyphase filter. However, the impact will be much smaller than that of conventional circuit structure, because \(C_P\) at node A in proposed polyphase filter has smaller value. The parasitic capacitance \(C_P\) only consists of device capacitance of \(M_1\) and \(M_2\) without the parasitic capacitance of \(C_C\) in conventional structure. Moreover, minimum-length transistors are used so as to minimize the device capacitance of \(M_1\) and \(M_2\). Fig. 5(b) plots the simulated transfer curves at desired and image signals and the IRR of the designed one-stage polyphase filter. The IRR at 25 MHz and 65 MHz can exceed 57dB and 52dB.

According to the Beidou RF receiver requirements, the proposed polyphase filter is required to provide more than 50dB of the image rejection at 46MHz of the center frequency and more than 30MHz of the bandwidth which are determined by the final required signal-to-noise ratio of the receiver, as shown in Fig. 6(a).

The block diagram of the entire four-stage polyphase filter is depicted in Fig. 6(b). Several stages of the polyphase filter

Fig. 4 Circuit of \(Gm_H\) and \(Gm_L\).

Fig. 5 (a) Complete circuit of the one-stage polyphase filter, (b) simulated transfer curve and IRR of the one-stage polyphase filter with two different \(\omega_p\).

Fig. 6 (a) Block diagram of the entire GNSS receiver, (b) block diagram of entire four-stage polyphase filter.

Fig. 7 Simulated transfer curve and IRR of the four-stage polyphase filter.
must be cascaded if strong image rejection is required across a wide band. Four stages polyphase filters are required by calculation from more than 50dB of the image rejection and more than 30MHz of the bandwidth over which this rejection is required. The rejected center frequencies are set at 25, 33.7, 49.2 and 65 MHz, respectively. Fig. 7 plots the simulated transfer curves at desired and image signals and the IRR of the designed four-stage polyphase filter which exceeds 66dB over the band-width from 25MHz to 65MHz.

In this receiver, the circuit following the polyphase filter, a trans-conductance amplifier, is differential. Therefore, the IQ output of the polyphase filter should be combined to be a differential signal by a sum circuit, shown in Fig. 6(b).

4. Measurement results

The microphotograph of the compass RF receiver including the proposed four-stage polyphase filter is shown in Fig. 8, which is fabricated in the 0.18-μm CMOS process. The four-stage polyphase filter occupies less than 0.36 mm² of chip area and dissipates an average current per stage of 0.66 mA from a 1.8-V supply. As shown in Fig. 9, the measured IRR of 58.2dB can be achieved in the frequency range 25MHz to 65MHz through the four-stage polyphase filter. From the measurement, the four-stage polyphase filter shows that the voltage gain, the IP1dB and IIP3 are 5.8dB, −8.6dBm and 1.5dBm at 45MHz, respectively. The performance is compared with [12, 19] and [29], which is shown in Table I. At the higher operating frequency, the proposed polyphase filter has the stronger IRR per stage and wider bandwidth while maintaining relatively small current dissipation per stage.

5. Conclusion

In this letter, we have proposed an active polyphase filter that uses a simpler structure to achieve strong image rejection in a wide band while obtaining lower power consumption, higher operating frequency and smaller chip area. Due to the advantage of easy tuning, the proposed active polyphase filter can be used in other low IF receiver, such multi-mode GNSS receiver and Bluetooth receiver, which need be adjusted the center frequency and bandwidth for different operating mode.

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