An Experimental Evaluation of Machine Learning Training on a Real Processing-in-Memory System

Juan Gómez-Luna$^1$ Yuxin Guo$^1$ Sylvan Brocard$^2$ Julien Legriel$^2$
Remy Cimadomo$^2$ Geraldo F. Oliveira$^1$ Gagandeep Singh$^1$ Onur Mutlu$^1$

$^1$ETH Zürich $^2$UPMEM

ABSTRACT

Training machine learning algorithms is a computationally intensive process, which is frequently memory-bound due to repeatedly accessing large training datasets. As a result, processor-centric systems (e.g., CPU, GPU) suffer from costly data movement between memory units and processing units, which consumes large amounts of energy and execution cycles. Memory-centric computing systems, i.e., computing systems with processing-in-memory (PIM) capabilities, can alleviate this data movement bottleneck.

Our goal is to understand the potential of modern general-purpose PIM architectures to accelerate machine learning training. To do so, (1) implement several representative classic machine learning algorithms (namely, linear regression, logistic regression, decision tree, K-Means clustering) on a real-world general-purpose PIM architecture, (2) rigorously evaluate and characterize them in terms of accuracy, performance and scaling, and (3) compare to their counterpart implementations on CPU and GPU. Our experimental evaluation on a real memory-centric computing system with more than 2500 PIM cores shows that general-purpose PIM architectures can greatly accelerate memory-bound machine learning workloads, when the necessary operations and datatypes are natively supported by PIM hardware. For example, our PIM implementation of decision tree is between 27× and 113× faster than a state-of-the-art CPU version on an 8-core Intel Xeon, and between 1.34× and 4.5× faster than a state-of-the-art GPU version on an NVIDIA A100. Our PIM implementation of K-Means clustering is 2.8× and 3.2× faster than CPU and GPU implementations, respectively.

To our knowledge, our work is the first one to evaluate training of machine learning algorithms on a real-world general-purpose PIM architecture. We conclude this paper with several key observations, takeaways, and recommendations that can inspire users of machine learning workloads, programmers of PIM architectures, and hardware designers and architects of future memory-centric computing systems. We open-source all our code and datasets at https://github.com/CMU-SAFARI/pim-ml.

KEYWORDS

machine learning, processing-in-memory, regression, classification, clustering, benchmarking, memory bottleneck

1 INTRODUCTION

Machine learning (ML) algorithms [1–6] have become ubiquitous in many fields of science and technology due to their ability to learn from and improve with experience with minimal human intervention. These algorithms train by updating their model parameters in an iterative manner to improve the overall prediction accuracy. However, training ML algorithms is a computationally intensive process, which requires large amounts of training data [7–9]. Accessing training data in current processor-centric systems (e.g., CPU, GPU) requires costly data movement between memory and processors, which results in high energy consumption and a large percentage of the total execution cycles. This data movement can become the bottleneck of the training process, if there is not enough computation and locality to amortize its cost [10–15].

One way to alleviate the cost of data movement is processing-in-memory (PIM) [16–20], a data-centric computing paradigm that places processing elements near or inside the memory arrays. PIM has been explored for decades [7, 18, 21–154]. However, memory technology challenges prevented its successful materialization in commercial products. For example, the limited number of metal layers in DRAM [155, 156] makes conventional processor designs impractical in commodity DRAM chips [157–160].

Real-world PIM systems have only recently been manufactured [161–170]. The UPMEM company, for example, introduced the first general-purpose commercial PIM architecture [161–165], which integrates small in-order cores near DRAM memory banks. High-bandwidth memory (HBM)-based HBM-PIM [166, 167] and Acceleration DIMM (AxDIMM) [168] are Samsung’s proposals that have been successfully tested via real prototypes. HBM-PIM features Single Instruction Multiple Data (SIMD) units, which support multiply-add and multiply-accumulate operations, near the banks in HBM layers [171, 172], and it is designed to accelerate neural network inference. AxDIMM is a near-rank solution that places an FPGA fabric on a DDR module to accelerate specific workloads (e.g., recommendation inference). Accelerator-in-Memory (AiM) [169] is a DDR6-based PIM architecture from SK Hynix with specialized units for multiply-accumulate and activation functions for deep learning. HB-PNM [170] is a 3D-stacked-based PIM architecture from Alibaba, which stacks a layer of LPDDR4 memory and a logic layer with specialized accelerators for recommendation systems.

Our goal in this work is to quantify the potential of general-purpose PIM architectures for training of machine learning algorithms. To this end, we implement four representative classic machine learning algorithms (linear regression [173, 174], logistic regression [173, 175], decision tree [176], K-Means clustering [177]) on a general purpose memory-centric system containing PIM-enabled memory, specifically the UPMEM PIM architecture [161–165]. We do not include training of deep learning algorithms in our study, since GPUs and TPUs have a solid position as the preferred and highly optimized accelerators for deep learning training [98, 178–183] due to their extremely high floating-point performance.$^1$

$^1$The UPMEM PIM architecture (used in this study) currently does not have native support for floating-point operations [157, 161–165].
Our PIM implementations of ML algorithms follow PIM programming recommendations in recent literature [162–164, 184]. We apply several optimizations to overcome the limitations of existing general-purpose PIM architectures (e.g., limited instruction set, relatively simple pipeline, relatively low frequency) and take full advantage of the inherent strengths of PIM (e.g., large memory bandwidth, low memory latency).

We evaluate our PIM implementations in terms of training accuracy, performance, and scaling characteristics on a real memory-centric system with PIM-enabled memory [161, 184, 185]. We run our experiments on a real-world PIM system [161] with 2,524 PIM cores running at 425 MHz, and 158 GB of DRAM memory.

Our experimental real system evaluation provides new observations and insights, including the following:

- ML training workloads that show memory-bound behavior in processor-centric systems can greatly benefit from (1) fixed-point data representation, (2) quantization [186, 187], and (3) hybrid precision implementation [169, 188] (without much accuracy loss) in PIM systems, in order to alleviate the lack of native support for floating-point and high-precision (i.e., 32- and 64-bit) arithmetic operations in the evaluated PIM system.
- ML training workloads that require complex activation functions (e.g., sigmoid [189]) can take advantage of lookup tables (LUTs) [107, 190, 191] in PIM systems instead of function approximation (e.g., Taylor series) [192], when PIM systems lack native support for those activation functions.
- Data can be placed and laid out such that accesses of PIM cores to their nearby memory banks are streaming, which enables better exploitation of the internal PIM memory bandwidth.
- ML training workloads with large training datasets can greatly benefit from scaling the size of PIM-enabled memory with PIM cores attached to memory banks. Training datasets can remain in memory without being moved to the host processor (e.g., CPU, GPU) in every iteration of the training process. Even if PIM cores need to communicate intermediate results via the host processor, this communication overhead is tolerable.

We compare our PIM implementations of linear regression, logistic regression, decision tree, and K-Means clustering to their state-of-the-art CPU and GPU counterparts. We observe that memory-centric systems with PIM-enabled memory can significantly outperform processor-centric systems for memory-bound ML training workloads, when the operations needed by the ML workloads are natively supported by PIM hardware (or can be replaced by efficient LUT implementations).

We aim to open-source all our PIM implementations of ML training workloads, training datasets, and evaluation scripts in our GitHub repository [193].

2 BACKGROUND

In this section, we first present a general classification of machine learning workloads, and the motivation for accelerating them in processing-in-memory (PIM) systems. Second, we give an introduction to PIM, and the current real-world PIM systems (as of April 2023) with a focus on the UPMEM PIM architecture, which we employ in our study.

2.1 Machine Learning Workloads

Machine learning (ML) [1–6] is a family of algorithms that learns a target function (or model) that best maps the input variables to an output variable. ML algorithms build (train) a model using the observed data (training dataset). The model is then used to make (infer) predictions or decisions.

Machine learning is commonly divided into three main categories of algorithms: (1) supervised learning, (2) unsupervised learning, and (3) reinforcement learning, as shown in Figure 1. Supervised algorithms train a model using training datasets that contain input features with expected labeled outputs. We divide supervised learning into classification, regression, and neural networks. Unsupervised algorithms learn to find structure or commonalities in the data (e.g., grouping, clustering) without using labeled or classified data. We divide unsupervised learning into clustering and dimensionality reduction. Reinforcement learning algorithms train an agent to achieve an objective by interacting with its environment. Thus, they gather training data from this interaction.

ML training with large amounts of data is a computationally expensive process [7–9]. This process requires several iterations to update an ML model’s parameters. Therefore, hardware accelerators (e.g., general-purpose GPU [178], domain-specific accelerators [182, 194, 195]) are widely used to speed up training. Recent research [196, 197] proposes PIM approaches to deal with the frequent data movement between memory and processing elements (either general-purpose cores or accelerators) that is needed to access training data. PIM approaches are especially effective for ML algorithms (or parts of an ML algorithm) where the amount of computation is not enough to amortize the cost of moving training data to the processing elements. Such workloads typically have (1) low arithmetic intensity (i.e., arithmetic instructions executed per byte accessed from memory), (2) low temporal locality, and/or (3) irregular memory accesses (e.g., due to sparsity of data) [7]. However, PIM-based accelerator proposals are usually tailored to specific ML algorithms (e.g., CNNs [196, 197]). As a result, they are less efficient for other types of ML workloads.
Our goal in this study is to analyze how real-world general-purpose PIM architectures can accelerate training of representative ML algorithms, and generate insights and recommendations that are useful to programmers and architecture designers. We select four representative classic machine learning algorithms (linear regression, logistic regression, decision tree, K-Means clustering) from three of the subcategories (regression, classification, clustering) in Figure 1.

These four workloads have been shown to be memory-bound in processor-centric systems (e.g., CPU, GPU) due to their low arithmetic intensity and low data reuse. Linear regression and logarithmic regression make use of gradient descent [198] or stochastic gradient descent [199] as optimization algorithms during training. Recent literature [10–13] shows that both are memory-bound. Decision tree and K-Means clustering are also memory-bound [14, 15] due to their frequent memory accesses and lightweight computation (mainly comparisons in decision tree, or a few additions and multiplications in K-Means).

We employ the roofline model [200] to quantify the memory boundedness of the CPU versions of the four workloads. Figure 2 shows the roofline model on an Intel Xeon E3-1225 v6 CPU [201] with Intel Advisor [202]. We observe from Figure 2 that all of the CPU versions of the four workloads are in the memory-bound area of the roofline model (i.e., the shaded region on the left side of the intersection between the DRAM bandwidth roof and the peak compute performance roof). Hence, we confirm that the four workloads are limited by memory access. As a result, these ML workloads are potentially suitable for PIM.

We implement various versions of the four algorithms (with different datatypes and optimizations) on the first commercially-available PIM architecture, the UPMEM PIM architecture (Section 2.2). We describe our implementations in Section 3 and evaluate them in Section 5.

We do not include any neural network (or deep learning algorithm) or reinforcement learning algorithm in our study for two main reasons. First, training of neural networks (e.g., CNN, RNN, GAN) can generally benefit from large caches and register files in processor-centric computing systems, since they expose high temporal locality [7]. Together with their inherent data-level parallelism and very high floating-point operation intensity, they are a good fit for GPUs [179]. In fact, the state-of-the-art ML-targeted PIM architecture [166, 167] shows performance improvements for neural network inference (not training) and with small batch sizes. Second, reinforcement learning (RL) [203] is an inherently sequential process, where an agent learns to make decisions by receiving a reward at timestep \( t + 1 \) for an action that was performed at timestep \( t \) on an environment. As a result, RL does not appear as a natural fit for PIM systems with many parallel processing elements, such as the one depicted in Figure 3. For deep reinforcement learning (DRL), the state-of-the-art approaches [204] accelerate only the neural network training part in RL (neural network training is out of the scope of our work as explained above). However, there are three limitations of such proposals [205]: (1) a major part in reinforcement learning is spent on sequential interaction between the agent and the environment, while also collecting the training dataset for the neural network, (2) the network sizes used in reinforcement learning are usually small and the weights perfectly fit in on-chip caches of the CPU, and (3) training in DRL can be done asynchronously in the background on the host CPU, while the agent is sequentially interacting with its environment.

### 2.2 Processing-in-Memory

Processing-in-memory (PIM) is a computing paradigm that advocates for memory-centric computing systems, where processing elements (general-purpose cores and/or accelerators) are placed near or inside the memory arrays. Firstly proposed more than 50 years ago [21, 22], processing-in-memory is a feasible solution to alleviate the data movement bottleneck [16, 17], caused by (1) the need for moving data between memory units and compute units in processor-centric systems, which causes a huge performance loss and energy waste, and worsened by (2) the increasing performance disparity between fast processor units and slow memory units.

Recent innovations in memory technology (e.g., 3D-stacked memories [171, 206], nonvolatile memories [207–211]) represent an opportunity to redesign the memory subsystem and equip it with compute capabilities. Recent research proposes processing-in-memory solutions that can be grouped into two main trends. Processing-near-memory (PNM) places processing elements (e.g., in the logic layer of 3D-stacked memories or in the same chip as memory banks in 2D memories). Processing elements can be general-purpose cores [67, 72–75, 149], application-specific accelerators [68–70, 77, 96, 97, 123, 138], simple functional units [71, 92, 212], GPU cores [86, 88, 93, 95], or reconfigurable logic [76, 81, 83]. Processing-using-memory (PUM) leverages the analog operational principles of memory cells in SRAM [32–35], DRAM [19, 36, 39, 41–44, 46, 48, 50, 108], or nonvolatile memory [52–66, 78, 111, 122, 213–217]. PUM enables different operations such as data copy and initialization [39, 44, 50], bulk bitwise operations [32, 36, 43, 52–54], and arithmetic operations [32–34, 46, 48, 56–61].

Real-world processing-in-memory architectures are finally becoming a reality, with the commercialization of the UPMEM PIM architecture [161–163], and the announcement of Samsung HBM-PIM [166, 167], Samsung AxDIMM [168], SK Hynix AiM [169], and Alibaba HB-PNM [170] (all four prototyped and evaluated in real systems). The five of them are PNM architectures. UPMEM places...
small general-purpose in-order cores (called DPUs) near the memory banks in the same DDR chip. HBM-PIM features 16-lane 16-bit floating-point SIMD units (called PCUs) near the banks in the memory layers of an HBM stack [171]. The SIMD units execute a only reduced set of instructions (e.g., multiplication, addition), since the architecture targets machine learning inference. AxDIMM with processing elements near the memory ranks is a DIMM-based solution. Its prototype places an FPGA fabric inside the buffer chip on the DIMM. The FPGA implements an accelerator for recommendation inference. AIm [169] is a GDDR6-based PIM architecture with near-bank processing units (PUs) for multiply-and-accumulate and activation functions for deep learning applications. HB-PNM [170] is a 3D-stacked based PIM solution for recommendation systems. With hybrid bonding (HB) technology [218], HB-PNM stacks one layer of LPDDR4 DRAM [219] on one logic layer. The logic layer embeds two types of specialized engines for matching and ranking, which the memory-bound steps of the evaluated recommendation system.

These five real-world PIM systems have some important common characteristics, as depicted in Figure 3. First, there is a host processor (CPU or GPU), typically with a deep cache hierarchy, which has access to (1) standard main memory, and (2) PIM-enabled memory (i.e., UPMEM DMIMs, HBM-PIM stacks, AxDIMM DMIMs, AIm GDDR6s, HB-PNM LPDDR4). Second, the PIM-enabled memory chip contains multiple PIM processing elements (PIM PEs), which have access to memory (either memory banks or ranks) with higher bandwidth and lower latency than the host processor. Third, the PIM processing elements (either general-purpose cores, SIMD units, FPGAs, or specialized processors) run at only a few hundred megahertz, and have a small number of registers and relatively small (or no) cache or scratchpad memory. Fourth, PIM PEs may not be able to communicate directly with each other (e.g., UPMEM DPUs, HBM-PIM PCUs or AIm PUs in different chips), and communication between them happens via the host processor. Figure 3 shows a high-level view of such a state-of-the-art processing-in-memory system.

In our study, we use the UPMEM PIM architecture [157, 161–163, 184, 185], the first PIM architecture to be commercialized in real hardware. The UPMEM PIM architecture uses conventional 2D DRAM arrays and combines them with general-purpose processing cores, called DRAM Processing Units (DPUs), on the same chip. In the current architecture generation (as of April 2023), there are 8 DPUs and 8 DRAM banks per chip, and 16 chips per DIMM (8 chips/rank). DPUs are relatively deeply pipelined and fine-grained multithreaded [220–222]. DPUs run software threads, called tasklets, which are programmed in Single Program Multiple Data (SPMD) manner.

DPUs have a 32-bit RISC-style general-purpose instruction set [184]. They feature native support for 32-bit integer addition/subtraction and 8-bit multiplication, but some complex operations (e.g., 32-bit integer multiplication/division) and floating-point operations are emulated [163, 164].

Each DPU has exclusive access to its own (1) 64-MB DRAM bank, called Main RAM (MRAM), (2) 24-KB instruction memory, and (3) 64-KB scratchpad memory, called Working RAM (WRAM). The host CPU can access the MRAM banks for copying input data (from main memory to MRAM) and retrieving results (from MRAM to main memory). These CPU-DPU/DPU-CPU transfers can be performed in parallel (i.e., concurrently across multiple MRAM banks), if the size of the buffers transferred from/to all MRAM banks is the same. Otherwise, the data transfers should be performed serially. Since there is no direct communication channel between DPUs, all inter-DPU communication takes place through the host CPU by using DPU-CPU and CPU-DPU data transfers.

Throughout this paper, we use generic terminology, since our implementation strategies are applicable to PIM systems like the generic one described in Figure 3, and not exclusive of the UPMEM PIM architecture. Thus, we use the terms PIM core, PIM thread, DRAM bank, scratchpad, and CPU-PIM/PIM-CPU transfer, which correspond to DPU, tasklet, MRAM bank, WRAM, and CPU-DPU/DPU-CPU transfer in UPMEM’s terminology [184].

3 ML TRAINING AND PIM IMPLEMENTATION

We select four widely-used machine learning workloads (i.e., linear regression, logistic regression, K-Means clustering, and decision tree) as representative ones for our benchmarking and analysis of machine learning training on real-world processing-in-memory architectures. We consider them representative because they are diverse in terms of learning approach and application. They have also diverse computational characteristics (i.e., memory access pattern, computation pattern, synchronization needs), as Table 1 shows.

3.1 Linear Regression

Linear regression [173, 174] is a supervised learning algorithm where the predicted output variable has a linear relation with the input variable. Linear regression is widely used to model relationships between variables in biological and social sciences (e.g., epidemiology, environmental sciences, finance, etc.) [174].

Algorithm Description. Linear regression obtains a linear model that predicts an output vector \( \mathbf{y} \) from an input matrix \( \mathbf{X} \) based on some coefficients or weights, vector \( \mathbf{w} \). We implement linear regression with gradient descent [198], as the optimization algorithm to find the minimum of the loss function. During training, we repeatedly refine the values of vector \( \mathbf{w} \) based on the vector of observed values \( \mathbf{y} \) for the inputs in matrix \( \mathbf{X} \) (row vectors \( \mathbf{x}_i \)). In each iteration, we first calculate the predicted output for each row vector \( \mathbf{x}_i \), i.e., the dot product of \( \mathbf{x}_i \) and \( \mathbf{w} \). Second, we calculate the gradient for the predicted output, i.e., we evaluate the error of the predicted output with respect to the observed value \( \mathbf{y} \). Third, we update the weights \( \mathbf{w} \) using the calculated gradient. We repeat the above process convergence (i.e., the gradient of loss function is zero or close to zero).

PIM Implementation. Our PIM implementation of linear regression with gradient descent divides the training dataset \( \mathbf{X} \) so that each PIM core is assigned an equal number of row vectors \( \mathbf{x}_i \). If the training dataset resides initially in the main memory of the host processor, we need to transfer the corresponding partitions of the training dataset to the local memories (e.g., DRAM banks) of the PIM cores. Inside a PIM core, we proceed as follows. First, we further distribute the assigned row vectors \( \mathbf{x}_i \) across the running threads, which compute the dot products of row vectors and weights (\( \mathbf{x}_i \cdot \mathbf{w} \)). Second, each dot product result is compared to the observed value \( \mathbf{y} \) to compute a partial gradient value. Third, we
reduce partial gradient values, and return the results to the host. Finally, the host (1) performs final reductions of gradient values from PIM cores, (2) updates the weights $w$, and (3) redistributes them to the PIM cores for the next training iteration.

We implement four different versions of linear regression with different input datatypes and optimizations: (1) 32-bit floating-point ($\text{LIN-FP32}$), (2) 32-bit fixed-point ($\text{LIN-INT32}$), (3) fixed-point with hybrid precision ($\text{LIN-HYB}$), and (4) fixed-point with hybrid precision and built-in functions ($\text{LIN-BUI}$).

- $\text{LIN-FP32}$ trains with input datasets of real values (32-bit precision).
- $\text{LIN-INT32}$ uses 32-bit fixed-point representation of input datasets. It uses 32-bit integer arithmetic.
- $\text{LIN-HYB}$ is applicable to input datasets of a limited value range that can be represented in 8 bits. The dot product result is 16-bit width, and the final gradient is represented in 32 bits. This hybrid implementation is motivated by the fact that real-world PIM cores only feature arithmetic units of limited precision. For example, DPUs in the UPMEM PIM architecture [184] run native 8-bit integer multiplication, but emulate 32-bit integer multiplication using shift-and-add instructions [163]. PCUs in HBM-PIM [166] and PUs in AiM [169] have 16-bit floating-point arithmetic units.
- $\text{LIN-BUI}$ replaces compiler-generated 16-bit and 32-bit multiplications with a custom multiplication based on 8-bit built-in multiplication functions [185] (this optimization is specific to the UPMEM PIM architecture). This optimization, which is based on the assumption that input data is encoded in 8 bits, reduces the number of instructions for each multiplication from 7 instructions (compiler-generated multiplication) to 4 (custom multiplication). Listing 1 shows the default integer multiplication code (C-based (a) and compiled code (b)) and our custom integer multiplication code (C-based (c) and compiled code (d)).

In Section 5, we evaluate all LIN versions in terms of accuracy (Section 4.1), performance for different numbers of threads per PIM core (Section 5.2), and performance scaling characteristics (Section 5.3). We also compare our LIN versions to custom CPU and GPU implementations of linear regression (Section 5.4), which use Intel MKL [223] and NVIDIA cuBLAS [224], respectively.

### 3.2 Logistic Regression

Logistic regression [173, 175] is a supervised learning algorithm used for classification, which outputs probability values for each input observation variable or vector. This probability values represent the likelihood of belonging to a certain class or event. Logistic regression is used in various fields (e.g., medical, marketing, engineering, economics, etc.) [175].

**Algorithm Description.** Logistic regression uses the sigmoid function to map predicted values (output vector $y$ obtained from an input matrix $X$ and a weights vector $w$) to probabilities. Our implementation of logistic regression uses gradient descent, same as our linear regression implementation (Section 3.1). First, in the beginning of each training iteration, we obtain the dot product of row vectors $x_i$ and weights $w$. Second, we apply the sigmoid function to the

---

### Table 1: Machine learning workloads.

| Learning approach | Application | Algorithm      | Short name | Memory access pattern | Computation pattern | Communication/synchronization |
|-------------------|-------------|----------------|------------|-----------------------|---------------------|-----------------------------|
| Supervised        | Regression  | Linear Regression | LIN       | Sequential, Strided   | mul, add, exp, div   | barrier                     |
|                   | Classification | Logistic Regression | LOG       | Sequential, Random    | float, int32_t      | barrier, mutex              |
|                   | Decision Tree | Decision Tree    | DTH       | Yes, No               | compare, add        | float                       |
| Unsupervised      | Clustering  | K-Means         | KME       | Yes, No               | mul, compare, add   | int16_t, uint64_t           |

---

Figure 3: High-level view of a state-of-the-art processing-in-memory system. The host CPU has access to $M$ standard memory modules and $N$ PIM-enabled memory modules.
\begin{verbatim}
result = X[i] * W[i]; // X and W are in WRAM (scratchpad)

(a) Default integer multiplication: C-based code.
  lsl, r3, r2, 0 // Load 1 byte from X[i]
  lsl, add, r2, r20, r1, 1 // Address of W[i]; r2=r20+(r1 <<1)
  lsh, r4, r2, 0 // Load 2 bytes from W[i]
  mul_sh_ul, r2, r4, r3, small, 0, x280000378 // r2=r4(1)+r3(1)
  mul_sh_ul, r5, r4, r3 // r5=r4(1)+r3(1)
  lsl, add, r2, r2, r5, 8 // r2=r2+r5<<8
  mul_sh_ul, r5, r3, r4 // r5=r3(1)+r4(1)
  lsl, add, r2, r2, r5, 8 // r2=r2+r5<<8
  mul_sh_sh, r3, r4, r3 // r3=r4(1)+r3(h)
  lsl, add, r2, r2, r5, 8 // r2=r2+r5<<8

(b) Default integer multiplication: Compiled code in UPMEM ISA.
  __builtin_mull_sl_urrr(temph, X[i], W[i]);
  __builtin_mull_sl_uerr(temph, X[i], W[i]);
  result = (temph << 8) + templ;

(c) Custom integer multiplication: C-based code (with built-in functions).
  lsl, r4, r2, 0 // Load 1 byte from X[i]
  lsl, add, r5, r20, r3, 1 // Address of W[i]; r5=r20+(r3 <<1)
  lsh, r5, r5, 0 // Load 2 bytes from W[i]
  mul_sh_ul, r6, r4, r5 // r6=r4(1)+r5(1)
  mul_sh_sh, r4, r5 // r4=r5(1)+r5(1)
  add, r2, r6, r2 // r2=r2+r6
  lsl, add, r2, r2, r4, 8 // r2=r2+r4<<8

(d) Custom integer multiplication: Compiled code in UPMEM ISA.

Listing 1: Default integer multiplication (C-based code (a) and compiled code (b)) vs. custom integer multiplication (C-based code (c) and compiled code (d)). The default multiplication compiles to 7 instructions (blue and green lines) while our custom multiplication compiles to 4 instructions.
\end{verbatim}

dot product results. Third, we calculate the gradient to evaluate the error of the predicted probability. Fourth, we update the weights $w$ according to the gradients.

**PIM Implementation.** Our PIM implementation of logistic regression follows the same workload distribution pattern as our linear regression implementation. First, row vectors $x_i$ are distributed across PIM cores and threads in each PIM core. Second, each thread computes the dot product of a row vector and the weights $(x_i, w)$, and applies the sigmoid function to the dot product result. Third, the thread computes partial gradient values. Fourth, partial gradient values from different threads are reduced, and the results are returned to the host. Finally, the host computes the final reductions, and updates the weights before redistributing them to the PIM cores.

We implement six different versions of logistic regression with different input datatypes and optimizations: (1) 32-bit floating-point (LOG-FP32), (2) 32-bit fixed-point (LOG-INT32), (3) 32-bit fixed-point with LUT-based sigmoid calculation and LUT in DRAM (LOG-INT32-LUT (MRAM)), (4) 32-bit fixed-point with LUT-based sigmoid calculation and LUT in scratchpad (LOG-INT32-LUT (WRAM)), (5) fixed-point with hybrid precision and LUT-based sigmoid calculation (LOG-HYB-LUT), and (6) fixed-point with hybrid precision, LUT-based sigmoid calculation, and built-in functions (LOG-BUI-LUT).

- LOG-FP32 trains with input datasets of real data (32-bit precision). If the PIM architecture does not support exponentiation (needed for sigmoid), this operation can be approximated by Taylor series [192]. This is true for the UPMEM PIM architecture.
- LOG-INT32 uses 32-bit fixed-point representation of input datasets. It uses 32-bit integer arithmetic, and Taylor series for the sigmoid function.
- LOG-INT32-LUT versions use a lookup table (LUT) per PIM core for sigmoid values, instead of Taylor series. Figure 4 represents our LUT-based sigmoid calculation. The size of the LUT depends on the sigmoid boundary and the number of bits for the decimal part of the fixed-point representation. We take advantage of the fact that the sigmoid function is symmetric. Thus, for a sigmoid boundary of 20 and 10 bits for the decimal part, the size of the LUT is $20 \times 1024$ entries. To represent this range of values, we can fit the entries in 16 bits. As a result, the size of our LUT is 40 KB. This small size can comfortably reside in the small scratchpads/caches of PIM cores (e.g., 64-KB WRAM in the UPMEM PIM architecture). However, occupying too much of a scratchpad may reduce the number of possible active threads [163]. We analyze this version in Section 5.2, and compare it to a version that accesses the LUT directly from DRAM (e.g., MRAM in the UPMEM PIM architecture). Depending on where the LUT resides, we have two different versions: LOG-INT32-LUT (MRAM) and LOG-INT32-LUT (WRAM).
- LOG-HYB-LUT is applicable to input datasets of a limited value range that can be represented in 8 bits, same as explained for LIN-HYB, and uses LUT-based sigmoid (LUT in scratchpad).
- LOG-BUI-LUT uses 8-bit builtin multiplication functions (Listing 1), same as explained for LIN-BUI, and uses LUT-based sigmoid (LUT in scratchpad).

In Section 5, we evaluate all LOG versions in terms of accuracy (Section 4.1), performance for different numbers of threads per PIM core (Section 5.2), and performance scaling characteristics (Section 5.3). We also compare our LOG versions to custom CPU and GPU implementations of logistic regression (Section 5.4), which use Intel MKL [223] and NVIDIA cuBLAS [224], respectively.

### 3.3 Decision Tree

Decision trees [176] are tree-based methods used for classification and regression. They are frequently referred to as CART (Classification and Regression Trees). A decision tree partitions the feature space into leaves, with a simple prediction model in each leaf, typically a comparison to a threshold (e.g., an average value in regression problems, a majority class in classification problems).

**Algorithm Description.** The training process of a decision tree builds a binary-search tree, which represents the partitioning of
the feature space. Each tree node splits the current rectangular sub-

space further based on a feature and a threshold. The prediction

is later done by following the correct path in the tree, up to a leaf

which contains the predicted value.

There are different flavors of decision tree algorithms, but the
two main steps are typically:

(1) Split a tree leaf, thus creating two children connected to

their parent node (i.e., the old leaf). A split is represented

as a tuple \((l, f, \text{thresh})\), where \(l\) is the tree leaf index, \(f\)
is the feature index, and \(\text{thresh}\) is the feature threshold.

After a split, the left child contains the points \(p\) of the training set
for which \(p[f] \leq \text{thresh}\), and the right child contains the
points for which \(p[f] > \text{thresh}\).

(2) Evaluate the quality of a tree leaf split. The quality of a split is

measured with a specific score, e.g., the Gini impurity \([176]\), a
probability measure of a randomly chosen element being
incorrectly labeled if it was randomly labeled.

In this work, we implement decision trees for classification prob-
lems. Each feature vector of the training set is associated with a
value referred to as its class, and the goal of the training process is to
create a tree which correctly predicts the class of previously unseen
feature vectors. At each step, we choose one candidate threshold
at random for every feature, and the best threshold-feature pair is
used to generate the split. The resulting tree is known as extremely
randomized tree \([225]\). This type of tree displays a larger bias and
smaller variance than regular trees, and is meant to be used as the
building block for forests of randomized trees \([226]\).

PIM Implementation. Our PIM implementation of a decision tree
partitions the training set into subsets of equal size, which the host
processor transfers to the PIM cores. The host processor maintains
the tree representation and makes splitting decisions, while the
PIM cores compute partial Gini scores to evaluate the splits. The
partial Gini scores computed by PIM cores are returned to the host
and aggregated, in order to make splitting decisions based on the
total Gini score.

The host maintains an active frontier of nodes, i.e., the cur-
rent leaves of the tree. In each training iteration, the host decides
whether (1) to split a tree leaf, an operation called split commit, or
(2) to evaluate a split, an operation called split evaluate, or (3) to
query the minimum and maximum values of a feature in a tree leaf,
an operation called min-max. The minimum value \((\text{min})\) and
the maximum value \((\text{max})\) are needed by the host to randomly select
a candidate split threshold in the \([\text{min}, \text{max}]\) interval. Then, the host
sends commands (i.e., split commit, split evaluate, min-max) to the
PIM cores. The host can send multiple commands at once (with the
only restriction that there must be at most one command per tree
leaf), thus exploiting task-level parallelism in the PIM cores.

Inside a PIM core, a split evaluate command is also parallelized,
as different PIM threads work on different batches of feature
values. PIM threads move batches of feature values of the points in
the training datasets from the DRAM bank to the scratchpad (i.e.,
from MRAM to WRAM in UPMEM DPUs), compare them to the

Page 7

corresponding threshold, and update the partial Gini score accord-

ingly. This operation has low arithmetic intensity, since only one
floating-point comparison and one integer addition are needed.

Consequently, a key point for performance is to load and handle
multiple feature values at once, in order to hide the latency of ac-

cesses to DRAM banks (e.g., in UPMEM DPUs, the MRAM-WRAM
transfers are handled by a DMA engine with a deterministic cost
for each transfer \([163]\)). Streaming memory accesses (using large
MRAM-WRAM transfers in UPMEM DPUs) sustain higher mem-
ory bandwidth than fine-grained strided/random accesses (using
short MRAM-WRAM transfers \([163]\)). In order to access memory in
streaming during split evaluate operations, we lay out the training
data in split commit operations as follows (see Figure 5):

(1) Points are stored by features (leaf 0 in Figure 5). If we denote

\(p[f]\) the value of feature \(f\) of point \(p\), the first feature
values are \(p[0]p[1]...p[n]\), then \(p[1]p[1]...p[n]\), etc.

(2) For all features, the feature values of points belonging to the

same tree leaf are kept consecutive in memory (leaves 1 and

2 in Figure 5). This means that for a leaf node \(l\) containing

the subset of points \(p^l_0\), \(p^l_1\), ... \(p^l_k\), and a feature \(f\), the values

of \(p^l_0[f]p^l_1[f]...p^l_k[f]\) are stored consecutively in memory.

The same applies to the class values.

Figure 5 illustrates the split commit operation on a dataset of 5

points with 2 features. Initially (LO), the points are stored in memory
with \(p_0\)’s feature 0 values, and then feature 1 values. After the

Page 7

Figure 4: LUT-based sigmoid calculation. The red dots repre-

sent the sigmoid values stored in the LUT.
split commit of L0 on feature 0 with threshold 5, two new leaves are created, L1 with \( p_0, p_3, p_4 \) (feature 0 value = 5) and L2 with \( p_1, p_5 \) (feature 0 value > 5). The split commit operation reorders the values\(^2\) in memory, so that the same leaf are stored consecutively. This way, PIM threads can perform streaming data accesses during the split evaluate operation. The cost of reordering is largely compensated by the benefits of this data layout, since split commit is less frequent than split evaluate. The reordering is a parallel operation where a different PIM thread reorders a different feature.

In Section 5, we evaluate DT in terms of accuracy (Section 4.1), performance for different numbers of threads per PIM core (Section 5.2), and performance scaling characteristics (Section 5.3). We also compare our DT implementation to state-of-the-art CPU and GPU implementations of decision tree (Section 5.4). The CPU version is from Scikit-learn [227] and the GPU version is from RAPIDS [228].

3.4 K-Means Clustering

K-Means [177] is a classic iterative clustering method used to find groups which have not been explicitly labeled in a dataset. K-Means can be used to identify unknown groups in complex multidimensional datasets useful to business data segmentation, and with a prominent use in image processing in an effort of simplifying images ahead of more complex classification models and compression algorithms.

Algorithm Description. A K-Means algorithm attempts to partition the dataset into \( K \) pre-defined distinct non-overlapping subgroups (clusters) where each data point belongs to only one group. Points within a cluster are meant be as similar (close) as possible while in comparison to points belonging to other clusters, their differences (distance) should be maximized. A cluster is identified by its centroid, a point with coordinates determined as the minimum total distance between itself and each point of the cluster. Our K-Means algorithm follows Lloyd’s method [177].

PIM Implementation. Our PIM implementation of K-Means partitions the training set and distributes it evenly over the PIM cores. The host processor sets initial random values of the centroids and broadcasts them to all PIM cores. The algorithm follows an iterative process in which (1) each PIM core assigns points of its part of the training set to the clusters, and then (2) the host processor adjusts the centroids based on the new assignment of points.

First, inside a PIM core, PIM threads evaluate which centroid is the nearest one to each point of the training set. Distance calculations are done using 16-bit integer arithmetic. Input data are quantized over a range of \( \pm 32767 \) (16-bit signed integers) to avoid overflowing when doing summations. Second, after finding the nearest centroid to a point, a PIM thread increments a counter and updates one accumulator per coordinate. The counter and the accumulators are associated to the corresponding cluster. Each per-coordinate accumulator contains the sum of values of the corresponding coordinate for all points belonging to a cluster. After all points are processed, each PIM core has partial sums of the coordinate values of the points in each cluster, and the number of points in each cluster. Third, the host processor then retrieves all per-cluster partial sums and counts from all PIM cores, and reduces them in order to compute the new coordinates of the centroids (calculated as the total sum of each coordinate divided by the total count). If these new centroid coordinates are far enough from the previous ones, they are sent over to the PIM cores for another iteration. The process continues until a centroid’s coordinates converge to a local optimum, i.e., when the updated coordinates are within a threshold distance to the previous coordinates. The threshold distance used to check for convergence is the Frobenius norm [229]. Fourth, once a clustering is completed, the PIM cores computes the inertia (also known as within-cluster sum-of-squares) of the clustering for their assigned points, and the host processors sums them up. The entire K-Means algorithm is repeated with different random starting centroids. The host processor chooses the clustering with the lowest inertia as the final result.

In Section 5, we evaluate KME in terms of quality and similarity (Section 4.1), performance for different numbers of threads per PIM core (Section 5.2), and performance scaling characteristics (Section 5.3). We also compare our KME implementation to state-of-the-art CPU and GPU implementations of K-Means (Section 5.4). The CPU version is from Scikit-learn [227] and the GPU version is from RAPIDS [228].

4 METHODOLOGY

We make our implementations of ML workloads for a real-world PIM system compatible with Scikit-learn [227], an open-source machine learning library, by deploying them as Scikit-learn estimator objects.

We run our experiments on a real-world PIM system [161] with 2,524 PIM cores running at 425 MHz, and 158 GB of DRAM memory.\(^3\) Table 2 shows the main characteristics of this PIM system. The table also includes characteristics of the CPU and the GPU that we use as baselines for comparison (Section 5.4). We compare our PIM implementations of ML workloads to state-of-the-art CPU and GPU implementations of the same workloads in terms of performance and quality (Section 5.4). For linear and logistic regression, we implement CPU versions with Intel MKL [223] and GPU versions with NVIDIA cuBLAS [224]. For decision tree and K-Means, CPU versions are from Scikit-learn [227] and GPU versions from RAPIDS [228].

Table 3 presents the datasets that we use in different experiments. For analysis of PIM kernel performance and performance scaling (both weak and strong scaling) experiments (Sections 5.2 and 5.3), we use synthetic datasets, since we can generate them as large as needed for the scaling experiments. For comparison to CPU and GPU (Section 5.4), we use state-of-the-art real datasets. For LIN, we use the SUSY dataset [232] available at [233]. This dataset contains 5 million samples with 18 floating-point attributes. For LOG, we use the SUSY dataset and the Skin segmentation dataset [234]. This dataset contains 245,057 samples with 3 integer attributes. For DTR and KME, we use the Higgs boson dataset [232] available at [235]. This dataset consists of 11 million points with 28 floating-point features, and one binary target label. For DTR, the last 500,000 points are used as the test set. For KME, the whole set is used for clustering. For DTR and KME, we also use the Criteo 1TB Click

---

\(^2\)The reordering is partial in the sense that we only need to place points of the same leaf together, not to sort them.

\(^3\)The UPMEM-based PIM system can have up to 2,560 PIM cores and 160 GB of DRAM.
To train our models, we use the Logs dataset [236]. The entire dataset contains 24 days of feature values and click feedback for millions of display ads. Samples in this dataset have 40 attributes. Given the huge size of the entire dataset, we only use parts of it in two different experiments. In the first experiment, we use one quarter of day 0 (49 million samples). This is the maximum size that we can use in the GPU that we use in our experiments (Table 2). In the second experiment, we use 2 days (days 0 and 1, i.e., 395 million samples). We can only run this experiment on the CPU and the PIM system.

### 4.1 ML Training Quality Metrics

We evaluate the training quality of the different versions of our ML workloads. We use synthetic datasets (with uniformly distributed (Section 3) on a real-world PIM system [161], according to our evaluation methodology (Section 4). First, we evaluate the quality of our implementations (Section 4.1). Second, we analyze the performance of the different versions of our ML workloads on a single PIM core for different numbers of PIM threads (Section 5.2). Third, we evaluate the performance scaling characteristics of our ML workloads on the PIM system (Section 5.3). Fourth, we compare the performance and energy consumption of our implementations for the PIM system to their state-of-the-art CPU and GPU counterparts (Section 5.4).

#### 5.1 ML Training Quality

##### 5.1.1 Linear Regression (LIN)

Figure 6 shows the training error rate of our four versions of LIN for varying numbers of training iterations between 1 and 1000. We observe that the training error rate flattens after 500 iterations for the four versions. LIN-FP32 achieves a training error rate as low as 0.55% (same as the CPU version). This is the comparison point for the integer versions (i.e., LIN-INT32, LIN-HYB, LIN-BUI). The training error rate of the integer versions remains low (1.02% for LIN-INT32 and 1.29% for LIN-HYB and LIN-BUI) and close to that of the 32-bit floating-point version, as shown in the figure. LIN-HYB and LIN-BUI show the same behavior, since they use the same datatypes.

![Figure 6: Training error rate (%) of LIN versions.](image)

##### 5.1.2 Logistic Regression (LOG)

Figure 7(a) presents the training error rate of our six versions of LOG for numbers of training iterations between 1 and 1000. The training error of LOG-FP32, which we use as the comparison point for the integer versions (i.e., LOG-INT32, LOG-INT32-LUT (MRAM), LOG-INT32-LUT (WRAM), LOG-HYB-LUT (WRAM), LOG-BUI-LUT (WRAM)), is almost flat after 100 iterations, and is as low as 1.20% after 1000 iterations (same as the CPU version). We observe that the training error rate of LOG-INT32 (2.42%) is higher than that of LOG-INT32-LUT (MRAM) and LOG-INT32-LUT (WRAM) (2.14%). The reason is that LOG-INT32 approximates exponentiation (hence, sigmoid) with Taylor series, while LOG-INT32-LUT (MRAM) and LOG-INT32-LUT (WRAM) store exact sigmoid values in a LUT.

![Figure 7(a): Training error rate (%) of LOG versions.](image)
and LOG–BUI–LUT (WRAM) increase the training error rate significantly (14.12%) due to the use of reduced-precision datatypes (i.e., 8- and 16-bit integers). In another experiment using samples with 2 decimal numbers (Figure 7(b)), the training error rate of these two versions decreases to 4.49%.

Figure 7: Training error rate (%) of LOG versions.

5.1.3 Decision Tree (DTR). We limit the tree depth to 10. The tree is built by splitting leaf nodes until no node can be split. A node cannot be split if it holds fewer than two data points, or if it contains only points belonging to the same class, or if its depth exceeds the maximum tree depth. To account for the effect of different synthetic datasets (with randomly generated samples) on both PIM and CPU implementations, we restart the algorithm 10 times, and average the resulting accuracies. We register a training accuracy of 0.90008 for the PIM implementation, against 0.90175 for the CPU version.

5.1.4 K-Means Clustering (KME). We perform a K-Means clustering with 16 clusters to match the dataset generation. The clustering iterates for a maximum of 300 iterations, or until the relative Frobenius norm between the cluster centers of two consecutive iterations is lower than 0.0001. In practice, the clustering always converges after less than 40 iterations on both the PIM and CPU implementations. To account for the effect of synthetic datasets (with randomly generated samples), we average the metrics on 10 runs with different random seeds. We register an average Calinski-Harabasz index [238] between the PIM and CPU clusterings is 0.999347 on average, showing that the clusterings are nearly identical despite the quantization.

5.2 Performance Analysis of PIM Kernels
We analyze in this section the performance of the different PIM kernel versions of our ML workloads on a single PIM core (i.e., an UPMEM DPU). This way, we understand the effect of (1) different optimizations we apply, and (2) increasing the number of PIM threads.

5.2.1 Linear Regression (LIN). Figure 8 shows the PIM kernel time of our four versions of LIN. The upper plot (Figure 8(a)) represents the PIM kernel time of LIN–FP32. The lower plot (Figure 8(b)) shows the PIM kernel time of the integer versions. We make four observations. First, all LIN versions result in their best performance with 11 or more PIM threads. Eleven is the minimum number of PIM threads that keep the pipeline of the PIM core (i.e., UPMEM DPU) full [157, 163]. For this PIM core, a workload with performance saturation at 11 PIM threads can be considered a compute-bound workload on this PIM architecture, since the latency of instructions executed in the pipeline hides the latency of memory accesses [163].

Second, using fixed-point representation instead of floating-point (i.e., LIN–INT32 instead of LIN–FP32) reduces the kernel time by an order of magnitude. The PIM cores used in our evaluation do not natively support floating-point arithmetic. Thus, floating-point operations are emulated, since the PIM cores only have integer arithmetic units [157, 163].

Third, LIN–HYB accelerates the PIM kernel by 41% over LIN–INT32. The speedup comes from the use of 8-bit integer multiplication, instead of the emulated 32-bit integer multiplication.

Fourth, LIN–BUI achieves an additional 25% speedup over LIN–HYB due to our custom multiplication operation (see Listing 1). These results demonstrate that applying quantization on the training dataset can greatly increase the performance of PIM implementations without sacrificing much accuracy (see Section 4.1).

Figure 8: Execution time (ms) of four versions of linear regression using 1-24 PIM threads in 1 PIM core.
5.2.2 Logistic Regression (LOG). Figure 9 shows the PIM kernel time of our versions of LOG. Figure 9(a) shows the results for the two versions (LOG-FP32, LOG-INT32) that estimate sigmoid based on Taylor series. Although the 32-bit integer version reduces the kernel time by 65% with respect to the 32-bit floating-point version, which uses emulated floating-point operations, the kernel time of both versions is very high due to the use of Taylor series, which require multiple iterations to achieve the necessary precision. Figure 9(b) shows the PIM kernel time of the LUT-based versions. We make five observations. First, the performance of all LOG versions saturates at 11 PIM threads, for the same reason as LIN versions.

Second, LOG-INT32-LUT (WRAM) results in a speedup of 53× over LOG-INT32. This demonstrates the benefit of converting computation to memory accesses using LUTs in PIM architectures.

Third, there is very little speedup (3%) coming from placing the LUT in the scratchpad (WRAM of UPMEM DPUs). The LUT query is just one memory access and its cost is negligible compared to the rest of computation.

Fourth, the use of 8-bit integer multiplication allows LOG-HYB-LUT (WRAM) to outperform LOG-INT32-LUT (WRAM) by 28%.

Fifth, the custom multiplication used by LOG-BUI-LUT (WRAM) provides an extra 43% speedup over LOG-HYB-LUT (WRAM).

5.2.3 Decision Tree (DTR). Figure 10(a) shows the PIM kernel time of DTR. We make three observations. First, the performance of DTR saturates at 11 PIM threads, for the same reason as LIN versions.

Second, the optimized data layout of DTR (Section 3.3) ensures that data is accessed at maximum bandwidth and, thus, the pipeline latency hides the latency of memory accesses.

Third, the maximum possible number of PIM threads is 16. This is due to the usage of the local scratchpad memory in the PIM core. The amount of memory needed by each PIM thread limits the maximum number of PIM threads to 16.

5.2.4 K-Means Clustering (KME). Figure 10(b) shows the PIM kernel time of KME. The performance of KME saturates at 11 PIM threads, for the same reason as LIN versions.

In summary, the four workloads saturate at 11 PIM threads, as it is expected in the PIM cores we use in our experiments (i.e., UPMEM DPUs) for workloads where the pipeline latency hides the memory access latency [163]. As a result, these workloads behave as compute-bound on these PIM cores (with high memory bandwidth but relatively slow pipeline), as opposed to their memory-bound behavior on processor-centric systems (see Section 2).

5.3 Performance Scaling

We evaluate performance scaling characteristics of our ML workloads using weak scaling and strong scaling experiments. For weak scaling (Section 5.3.1), we run experiments on 1 rank (from 1 to 64 PIM cores). Our goal is to evaluate how the performance scales with the number of PIM cores for a fixed problem size per processing element. For strong scaling (Section 5.3.2), we run experiments on 32 ranks (from 256 to 2,048 PIM cores). Our goal is to evaluate how the performance of our ML workloads scales with the number of PIM cores for a fixed problem size.

5.3.1 Weak Scaling. Figure 11 shows weak scaling results on 1-64 PIM cores for all versions of our ML workloads. Each bar presents the total execution time broken down into (1) execution time of the PIM kernel (i.e., PIM Kernel), communication time between the host CPU and the PIM cores (i.e., CPU-PIM and PIM-CPU times), and communication time between PIM cores (i.e., Inter PIM Core). We make the following observations from the figure.

First, we observe linear scaling of the PIM kernel time of all LIN versions, all LOG versions, and DTR. However, the PIM kernel time of KME reduces as we increase the number of PIM cores. This is caused by the fact that the K-Means algorithm on average converges with fewer iterations on a larger dataset. The PIM kernel time per iteration does scale linearly.

Second, the fraction of total execution time spent on communication between the host CPU and the PIM cores (i.e., CPU-PIM and
Figure 11: Execution time (ms) of ML workloads on 1, 4, 16, and 64 PIM cores using weak scaling. Inside a PIM core, we use the best performing number of PIM threads (Section 5.2).

PIM-CPU times) and between PIM cores (i.e., Inter PIM Core) is negligible compared to the PIM kernel time for all versions. For all LIN versions, all LOG versions, DTR, and KME, the sum of CPU-PIM, Inter PIM Core, and PIM-CPU times takes less than 7% of the total execution time.

5.3.2 **Strong Scaling.** Figure 12 shows strong scaling results on 256-2,048 PIM cores for all versions of our ML workloads. Each bar (left y-axis) presents the total execution time broken down into (1) execution time of the PIM kernel (i.e., PIM Kernel), communication time between the host CPU and the PIM cores (i.e., CPU-PIM and PIM-CPU times), and communication time between PIM cores (i.e., Inter PIM Core). Each red line (right y-axis) represents the speedup of a PIM kernel normalized to the performance of 256 PIM cores. We make the following observations.

First, we observe that the PIM kernel time scales linearly with the number of PIM cores. The speedup of 2,048 PIM cores over 256 PIM cores is between $6.37 \times$ and $7.98 \times$.

Second, the overhead of communication between PIM cores (i.e., Inter PIM Core) is tolerable for all ML workloads. The largest fraction of Inter PIM Core over the total execution time is 36% for KME with 2,048 PIM cores. Even so, 2,048 PIM cores provide the lowest total execution time of KME.

Third, the communication time between the host CPU and the PIM cores (i.e., CPU-PIM and PIM-CPU times) represents a negligible fraction of the total execution time of all ML workloads.

---

FOOTNOTES:

1. DTR and KME do not need final PIM-CPU transfer. For DTR, the reason is that the tree is built iteratively on the host side, and the algorithm ends when the CPU declares termination on the tree build. For KME, the CPU is in charge of the final cluster assignment once convergence has been declared.
5.4 Comparison to CPU and GPU

We compare our implementations of ML workloads on a PIM system to state-of-the-art CPU and GPU implementations of the same workloads in terms of performance and quality. Table 4 indicates the sources of these CPU and GPU implementations.

Table 4: CPU and GPU implementations of ML workloads.

| ML workload     | CPU implementation | GPU implementation |
|-----------------|--------------------|--------------------|
| Linear regression | Intel MKL [223]    | NVIDIA cuBLAS [224] |
| Logistic regression | Intel MKL [223]    | NVIDIA cuBLAS [224] |
| Decision tree   | Scikit-learn [227] | RAPIDS [228]       |
| Kmeans          | Scikit-learn [227] | RAPIDS [228]       |

Our goal is to evaluate the potential of a general-purpose PIM system (Table 2) for acceleration of ML workloads. We use an Intel Xeon Silver 4215 CPU [230] and an NVIDIA A100 GPU [231] based on the Ampere architecture [239] as baseline processor-centric architectures. Table 2 summarizes their key characteristics.

For the PIM system performance measurements, we include the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-PIM-core synchronization ("Inter PIM"), and the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-architecture. Table 2 summarizes their key characteristics.

For the PIM system performance measurements, we include the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-PIM-core synchronization ("Inter PIM"), and the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-PIM-core synchronization ("Inter PIM"), and the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-PIM-core synchronization ("Inter PIM"), and the time spent in the PIM cores ("PIM Kernel"), the time spent for inter-PIM-core synchronization ("Inter PIM"). For the GPU performance measurements, we include the kernel time ("GPU Kernel"), and the initial CPU-GPU and the final GPU-CPU transfers ("CPU-GPU", "GPU-CPU"). The results that we show in this section correspond to the best configurations in terms of CPU threads (for the CPU versions), GPU threads per block and thread blocks (for the GPU versions), and PIM cores and PIM threads (for the PIM versions). We open-source all configurations for reproducibility [193].
We apply symmetric quantization [186, 187] to this dataset, in order without being burdened by other costly arithmetic operations. Sec-

5.4.1 Linear Regression (LIN). Figure 13 shows the execution times of LIN versions on PIM, CPU, and GPU with the SUSY dataset [233]. We apply symmetric quantization [186, 187] to this dataset, in order to be able to evaluate our integer versions. We make the following observations. First, LIN-FP32 is heavily burdened by the use of floating-point arithmetic, which is not natively supported by the PIM system we use in our evaluation (i.e., UPMEM-based PIM system) [163]. Despite that, LIN-FP32 is 13% faster than the CPU version. Second, LIN-INT32 is 8.5× faster than LIN-FP32. This is the result of using natively supported instructions (even though 32-bit integer multiplication is emulated in the UPMEM PIM architecture) [163]. Third, LIN-HYB and LIN-BUI further improve the performance. The kernel time of LIN-HYB is 10% lower than that of LIN-INT32 due to the use of hybrid precision. Our custom multiplication in LIN-BUI reduces the kernel time by an additional 4%. Fourth, the GPU version is 4.1× faster than our LIN-BUI, since the A100 (1) has much higher compute throughput than the PIM system that we use in our experiments, and (2) its memory bandwidth is only 39% lower than the bandwidth of the PIM system (Table 2).

5.4.2 Logistic Regression (LOG). Figure 14 shows the execution times of LOG versions on PIM, CPU, and GPU with the Skin segmentation dataset [234]. We make four observations from these results. First, LOG-FP32 and LOG-INT32 PIM versions are almost 10× slower than the CPU version. The reason is the high cost of sigmoid estimation with Taylor series due to their iterative nature (as mentioned in Section 5.2.2). Second, LOG-INT32 is 17% faster than LOG-FP32 due to the faster integer arithmetic [163]. Third, replacing Taylor series with the use of LUTs (in LOG-INT32-LUT (MRAM), LOG-INT32-LUT (WRAM), LOG-HYB-LUT (WRAM), and LOG-BUI-LUT (WRAM)) to estimate sigmoid accelerates the PIM versions by almost two orders of magnitude. For example, LOG-INT32-LUT (WRAM) is 3.3× and LOG-BUI-LUT (WRAM) is 3.9× faster than the CPU version. Fourth, even though the GPU version is significantly faster than all PIM versions (e.g., 16.5× faster than LOG-BUI-LUT (WRAM)), the gap between GPU and PIM is greatly reduced by using appropriate optimizations in PIM codes (e.g., LUTs, custom multiplication).

Table 5 shows the training error rate (%) of all versions of LIN (with the SUSY dataset) and LOG (with the Skin segmentation dataset). We make several observations. First, the training error rates of the 32-bit floating-point versions (i.e., LIN-FP32, LOG-FP32) is the same as that of the CPU and the GPU versions. Second, the training error rates of the PIM versions of LIN and LOG that use quantized datasets are greater than those of the CPU and GPU versions, but they may still be acceptable (i.e., < 20% for LIN and < 9% for LOG) for some applications [240–246].

Table 5: Training error rate (%) of LIN and LOG versions on PIM, CPU, and GPU.

| ML workload | Version     | Training error rate (%) |
|-------------|-------------|------------------------|
| Linear regression | LIN-FP32    | 13.88                  |
|             | LIN-INT32   | 18.68                  |
|             | LIN-HYB     | 18.68                  |
|             | LIN-BUI     | 18.68                  |
|             | CPU [223]   | 13.88                  |
|             | CPU [224]   | 13.88                  |
| Logistic regression | LOG-FP32    | 7.58                   |
|             | LOG-INT32   | 8.72                   |
|             | LOG-INT32-LUT (MRAM) | 8.72          |
|             | LOG-INT32-LUT (WRAM) | 8.98          |
|             | LOG-HYB-LUT (WRAM) | 8.98         |
|             | LOG-BUI-LUT (WRAM) | 8.98         |
|             | CPU [223]   | 7.58                   |
|             | CPU [224]   | 7.58                   |

5.4.3 Decision Tree (DTR). Figure 15(a) shows the execution times of DTR versions on PIM, CPU, and GPU with the Higgs boson dataset [235]. We make two observations. First, the PIM version of DTR outperforms the CPU version and the GPU version by 27× and 1.34×, respectively. Since DTR mostly uses comparison operations (e.g., comparing a feature value to a threshold), the PIM version can take advantage of the large internal bandwidth of the PIM system without being burdened by other costly arithmetic operations. Second, 70% of the execution time of the GPU version of DTR is spent on moving data between the host CPU and the GPU, while only 27% of the execution time of the PIM version is due to communication between the host CPU and the PIM cores or between PIM cores. The fact that the host CPU and the PIM cores are connected through memory channels is an advantage over the GPU, which uses PCIe bus, as the memory channels provide higher bandwidth.

For DTR, we also run experiments using the Criteo dataset [236]. Figure 16(a) shows the execution times of DTR versions on PIM, CPU, and GPU with a quarter of day 0. We make two observations in line with the observations from the results with the Higgs boson dataset (Figure 15(a)). First, the speedup of the PIM version of DTR over the CPU version and the GPU version increases to 62× and 4.5×, respectively. Since the part of the Criteo dataset that we use is significantly larger than the Higgs boson dataset, there is enough work to keep all 2,524 PIM cores busy (the best performing number of PIM cores for the Higgs boson dataset is 1,024). This explains the increased speedups with respect to those for the Higgs boson dataset. Second, the percentage of the execution time devoted to communication remains 27% for the PIM version, while it increases to 77% for the GPU version. This also explains the increased speedup of the PIM version over the CPU version.

Figure 17(a) shows the execution times of DTR versions on PIM and CPU with two days (days 0 and 1) of the Criteo dataset [236]. A main observation is that the PIM version outperforms the CPU version by 113×. A possible explanation for this high speedup is that the large dataset size causes many page faults on the CPU.

Using the Criteo dataset [236], we also compare the PIM version of DTR to another, more optimized, CPU baseline, the Intel extension for Scikit-learn [247, 248]. For a quarter of day 0, the PIM version is 21× faster than Intel’s CPU version. For days 0 and 1, the PIM version is 36× faster than Intel’s CPU version. Despite the Intel extension for Scikit-learn [247, 248] is significantly faster than the original Scikit-learn [227], the speedups that our PIM version of DTR provides are still considerable.

Table 6 shows the training accuracy of DTR versions on PIM, CPU, and GPU for the Higgs boson dataset. We observe that the accuracy of our PIM version (0.65635) is very similar to the accuracy of the CPU version (0.65581), and only slightly smaller than that of the GPU version (0.70462).
Table 6: Training accuracy of DTR versions on PIM, CPU, and GPU.

| ML workload | Version | Training accuracy |
|-------------|---------|-------------------|
| Decision tree | DTR (PIM) | 0.65635 |
| CPU [227] | 0.65581 |
| GPU [228] | 0.70462 |

5.4.4 **K-Means Clustering (KME).** Figure 15(b) shows the execution times of KME versions on PIM, CPU, and GPU with the Higgs boson dataset [235]. We observe that the PIM version of KME is 2.8× faster than the CPU version and 3.2× faster than the GPU version. Similar to DTR, KME does not use costly arithmetic operations but mainly 16-bit integer arithmetic.

For KME, we also run experiments using the Criteo dataset [236]. Figure 16(b) shows the execution times of DTR versions on PIM, CPU, and GPU with a quarter of day 0. Figure 17(b) shows the execution times with two days (days 0 and 1) of the Criteo dataset. We observe that the speedups of the PIM version over the CPU version (2.7× with a quarter of day 0, and 2.4× with two days) and the GPU version (3.2× with a quarter of day 0) remain similar to the speedups with the Higgs boson dataset (Figure 15(b)). This can be explained by the fact that the best performing number of PIM cores is the maximum (2,524) for both datasets. Thus, for KME, a larger dataset does not increase the speedup of the PIM version over the CPU and the GPU versions.

We also compare the PIM version of KME to the Intel extension for Scikit-learn [247, 248] using the Criteo dataset [236]. The Intel extension for Scikit-learn [247, 248] is almost twice as fast as the original Scikit-learn [227], but our PIM version of KME is still faster. For a quarter of day 0, the PIM version is 1.42× faster than Intel’s CPU version. For days 0 and 1, the PIM version is 1.37× faster than Intel’s CPU version.

Table 7 shows the similarity of the clusterings (given by the adjusted Rand index) produced by KME versions on PIM, CPU, and GPU for the Higgs boson dataset. The adjusted Rand index between the PIM version and the CPU version is 0.999985, while the adjusted Rand index between the GPU version and the CPU version is significantly lower (0.758579).

Table 7: Adjusted Rand index of KME versions on PIM, CPU, and GPU.

| ML workload | Version | Adjusted Rand index |
|-------------|---------|---------------------|
| K-means     | KME (PIM) | 0.999985 |
| CPU [227]   | 1       |
| GPU [228]   | 0.758579 |

6 **KEY TAKEAWAYS AND RECOMMENDATIONS**

In this section, we summarize our key observations, takeaways, and recommendations that stem from our analysis of four ML training workloads on a state-of-the-art general-purpose PIM architecture. There are four subsections that are titled after four widely-accepted facts about near-bank PIM architectures. For each of them, we first state general key observations that are derived from the particular...
PIM cores [157, 166, 167, 169] are wimpy processors (operating at relatively low frequency) with high memory bandwidth, especially for streaming memory access patterns [163]. As a result, for real-world workloads, the compute throughput tends to saturate much more frequently than the memory bandwidth, and the pipeline latency hides the memory access latency.

**Key Takeaway #1.** Even ML training workloads (e.g., linear regression, logarithmic regression, decision tree, K-Means) that are bound by memory access due to their low arithmetic intensity in processor-centric systems (e.g., CPU, GPU) behave as compute-bound when running on PIM cores.

**Recommendation #1.** Maximize the utilization of PIM cores by keeping their pipeline fully busy. For example, in the UPMEM PIM architecture [157], which has fine-grained multithreaded scalar cores, we recommend to schedule 11 or more PIM threads (Section 5.2), which is the minimum number of PIM threads to saturate the pipeline throughput. In SIMD-based PIM architectures [166, 167, 169], a recommendation would be to maximize SIMD utilization by minimizing divergence across SIMD lanes [249].

### 6.2 PIM Cores Have Limited Instruction Sets

PIM cores [157, 166, 167, 169] have limited instruction sets. As such, they do not support natively a large variety of arithmetic operations and datatypes. For example, the UPMEM PIM architecture [157] does not support floating-point operations or 32-bit integer multiplication/division (only emulated by the runtime library) [163]. AiM [169] and HBM-PIM [166, 167] only support multiplication and addition of 16-bit floating-point values.

**Key Takeaway #2.** Workloads that require arithmetic operations or datatypes that are not natively supported by PIM cores...
will either (1) run at low performance due to instruction emulation (e.g., floating-point operations in UPMEM PIM), or (2) cannot be implemented on those PIM architectures (e.g., workloads requiring operations other than multiplication and addition in AiM or HBM-PIM).

**Recommendation #2.** ML workloads (e.g., L1N, LOG) can employ fixed-point representation if PIM cores do not support floating-point operations (e.g., UPMEM PIM) without sacrificing much accuracy (Section 4.1).

**Recommendation #3.** Quantization can be used to take advantage of native hardware support, if PIM cores natively support only limited precision. For example, using hybrid precision after quantizing the training dataset can provide significant performance improvements in the UPMEM PIM architecture (Section 5.2).

**Recommendation #4.** Programmers (or better compilers) can optimize code at low level to better leverage the available native instructions and hardware (e.g., 8-bit integer multiplication in UPMEM DPUs). For example, we show that our custom 16-bit and 32-bit integer multiplications (Listing 1) significantly improve performance over compiler-generated code for quantized training datasets (Section 5.2).

**Key Takeaway #3.** Memory-bound ML workloads that require mainly operations natively supported by the PIM architecture (e.g., 32-bit integer addition/subtraction in UPMEM PIM), such as decision tree and K-Means clustering, leverage the large PIM bandwidth, and perform better than their state-of-the-art CPU and GPU counterparts. For example, DTR only requires comparison and 32-bit integer addition. Our PIM version of DTR outperforms the CPU and GPU versions by 27x and 1.34x, respectively. Our PIM implementation of KME employs mainly 16-bit integer arithmetic. As a result, it outperforms the CPU and GPU version by by 2.8x and 3.2x, respectively.

### 6.3 PIM Cores Have High Memory Bandwidth

Near-bank PIM cores leverage high aggregated memory bandwidth and low latency memory access. As a result, memory accesses are typically cheaper than computation (in particular, 32- or 64-bit integer arithmetic, floating-point arithmetic, transcendental functions) for workloads that are memory bound in processor-centric systems due to the relatively low frequency and simple pipelines of PIM cores [163].

PIM cores exploit memory bandwidth better when they perform streaming memory accesses to the memory banks, especially if memory arrays have large row buffers (e.g., DDR4 memory in UPMEM PIM).

**Recommendation #5.** Programmers can convert computation to memory accesses in PIM architectures by keeping pre-calculated operation results (e.g., LUTs, memoization) in memory. For example, our use of LUTs for sigmoid calculation in LOG results in a speedup of 53x (LOG-INT32-LUT (MRAM) over LOG-INT32, Section 5.2).

**Recommendation #6.** For data structures of more than one dimension, programmers can optimize the data layout in a way that memory accesses are in streaming, thus exploiting higher sustained bandwidth. We show in this paper one example of optimized data layout for DTR on the UPMEM PIM architecture (Section 3.3).

### 6.4 PIM Throughput Scales with Memory Capacity

Since near-bank PIM cores are directly attached to the memory arrays, their number scales at the same pace as the number of memory arrays, banks, and chips in the memory subsystem. Consequently, the overall PIM throughput scales linearly.

Large PIM-enabled memory allows training datasets to remain in memory during the whole training process. This represents an inherent advantage over processor-centric systems (e.g., CPU, GPU) where the whole training dataset needs to be moved to the processor in every iteration of the training process.

**Key Takeaway #4.** Memory-bound ML training workloads, which need large training datasets, benefit from large PIM-enabled memory with many PIM cores. Even if PIM cores need to communicate via the host processor (e.g., in UPMEM PIM), the amount of data movement needed for intermediate results is minimal with respect to the size of the whole training dataset. Our strong scaling and weak scaling characterization of four ML training workloads (Section 5.3) demonstrates that.

### 7 RELATED WORK

To our knowledge, this is the first work that comprehensively evaluates the benefits of a real general-purpose processing-in-memory (PIM) system for ML training workloads. We briefly summarize prior works on PIM acceleration of Deep Learning (DL) and other ML algorithms.

**PIM for DL inference.** Many prior works focus on accelerating DL inference using different PIM solutions. This includes both proposals from Academia [47, 73, 98, 136, 150, 151, 250–257] and Industry [166–170], targeting various types of DL models, including convolutional neural networks [47, 73, 98, 136, 150, 151, 166, 167, 250, 252–255], recurrent neural networks [136, 169, 257], and recommendation systems [168, 170, 251, 256]. Our work differs from such works since we focus on classic ML algorithms (i.e., regression, classification, clustering) using a real-world general-purpose PIM architecture (i.e., the commercially-available UPMEM PIM architecture [161]).

**PIM for DL training.** Another body of works leverages PIM techniques to accelerate DL training [197, 258–269]. These works mainly utilize the analog computation capabilities (e.g., for matrix vector multiplication) of non-volatile memory (NVM) technologies to implement training of deep neural networks [258–261, 263, 265, 266, 268]. In contrast, executing DL training using DRAM-based PIM architectures is challenging, since the area and power constraints of such architectures lead to performance bottlenecks when executing key operations (e.g., multiplication) required during training [270].

**PIM for other ML algorithms.** Few related prior works [80, 271–275] propose solutions for ML algorithms other than DL inference and training (e.g., regression, classification, clustering). Such works leverage different memory technologies (e.g., 3D-stacked DRAM [80, 271, 274], ReRAM [275], SRAM [272, 275]) to accelerate ML workloads such as linear regression [271–274], logistic regression [271, 273], support vector machines [271], and K-nearest
neighbors [272, 275]. None of these works provide comprehensive implementation and evaluation of ML algorithms using a real processing-in-memory architecture.

8 CONCLUSION

Machine learning training frequently becomes memory-bound in processor-centric systems due to repeated accesses to large training datasets. Memory-centric systems (i.e., systems with processing-in-memory (PIM) capabilities) can overcome this memory boundedness.

We implement several representative classic machine learning algorithms on a real-world general-purpose PIM architecture with the aim of understanding the potential of memory-centric systems for ML training. We evaluate our PIM implementations on a memory-centric computing system with more than 2500 PIM cores in terms of accuracy, performance, and scaling characteristics, and compare to state-of-the-art implementations for CPU and GPU.

To our knowledge, our work is the first one to evaluate training of machine learning algorithms on a real-world general-purpose PIM architecture. We show that PIM systems can greatly outperform CPUs and GPUs for memory-bound ML training workloads when the PIM processing elements have native support for the arithmetic operations and datatypes required by the ML training workloads. Compared to CPUs, PIM systems feature significantly higher memory bandwidth and many more parallel processing elements, the number of which scales with memory capacity. Compared to GPUs, PIM systems benefit from higher host-accelerator bandwidth given that PIM processing elements are connected to the host CPU via memory channels (as opposed to PCIe like GPUs). We believe that our work shows great promise for PIM systems as widely-used accelerators for ML training workloads, and this promise can materialize in future PIM systems with more mature architectures, hardware, and software support.

ACKNOWLEDGMENTS

We acknowledge the generous gifts provided by our industrial partners, including ASML, Facebook, Google, Huawei, Intel, Microsoft, and VMware. We acknowledge support from the Semiconductor Research Corporation, the ETH Future Computing Laboratory, and the European Union’s Horizon programme for research and innovation under grant agreement No. 101047160, project BioPIM (Processing-in-memory architectures and programming libraries for bioinformatics algorithms). This research was partially supported by ACCESS – AI Chip Center for Emerging Smart Systems, sponsored by InnoHK funding, Hong Kong SAR.

A much shorter version of this paper appears as an invited paper at the 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

REFERENCES

[1] A. Géron, Hands-on Machine Learning With Scikit-Learn, Keras, and TensorFlow: Concepts, tools, and techniques to build intelligent systems, 2019.
[2] El Alpaydın, Introduction to Machine Learning, 2020.
[3] I. Goodfellow et al., Deep Learning, 2016.
[4] M. Mohri et al., Foundations of Machine Learning, 2018.
[5] S. Shalev-Shwartz and S. Ben-David, Understanding Machine Learning: From Theory to Algorithms, 2014.
[6] S. Raschka and V. Mirjalili, Python Machine Learning: Machine Learning and Deep Learning with Python, Scikit-Learn, and TensorFlow 2, 2019.
[7] G. F. Oliveira et al., “DAMOV: A New Methodology and Benchmark Suite for Evaluating Data Movement Bottlenecks,” IEEE Access, 2021.
[8] M. Wang et al., “A survey on large-scale machine learning,” IEEE Transactions on Knowledge and Data Engineering, 2020.
[9] C. Dünner et al., “Snap ml: A hierarchical framework for machine learning,” Advances in Neural Information Processing Systems, vol. 31, 2018.
[10] X. Xie et al., “CuMF: SGD-Parallelized Stochastic Gradient Descent for Matrix Factorization on GPUs,” in HPCD, 2017.
[11] C. De Sa et al., “Understanding and Optimizing Asynchronous Low-precision Stochastic Gradient Descent,” in ISCA, 2017.
[12] H. Kim et al., “GradPIM: A Practical Processing-in-DRAM Architecture for Gradient Descent,” in HPCA, 2021.
[13] D. Mahajan et al., “Tabla: A Unified Template-based Framework for Accelerating Statistical Machine Learning,” in HPCA, 2016.
[14] B. Peng et al., “HarpgBDT: Optimizing Gradient Boosting Decision Tree for Parallel Efficiency,” in CLUSTER, 2019.
[15] M. A. Bender et al., “K-Means Clustering on Two-Level Memory Systems,” in MEMSYS, 2015.
[16] O. Mutlu et al., “Processing Data Where It Makes Sense: Enabling In-Memory Computation,” MidPro, 2019.
[17] O. Mutlu et al., “A Modern Primer on Processing in Memory,” Emerging Computing: From Devices to Systems - Looking Beyond Moore and Von Neumann, 2021, https://arxiv.org/pdf/2012.03112.pdf.
[18] S. Ghose et al., “Processing-in-Memory: A Workload-Driven Perspective,” IBM JRD, 2019.
[19] V. Seshadri and O. Mutlu, “In-DRAM Bulk Bitwise Execution Engine,” arXiv:1905.08822 [cs.AR], 2020.
[20] O. Mutlu et al., “Enabling Practical Processing in and near Memory for Data-Intensive Computing,” in DAC, 2019.
[21] H. S. Stone, “A Logic-in-Memory Computer,” IEEE TC, 1970.
[22] W. H. Kautz, “Cellular Logic-in-Memory Arrays,” IEEE TC, 1969.
[23] D. E. Shaw et al., “The NON-VON Database Machine: A Brief Overview,” IEEE Database Eng. Bull., 1981.
[24] P. M. Kogge, “EXECUBE - A New Architecture for Scalable MPPs,” in JTCP, 1994.
[25] M. Gokhale et al., “Processing in Memory: The Terasys Massively Parallel PIM Array,” IEEE Computer, 1995.
[26] D. Patterson et al., “A Case for Intelligent RAM,” IEEE Micro, 1997.
[27] M. Oskin et al., “Active Pages: A Computation Model for Intelligent Memory,” in ISCA, 1998.
[28] Y. Kang et al., “FlexRAM: Toward an Advanced Intelligent Memory System,” in ICCD, 1999.
[29] K. Mai et al., “Smart Memories: A Modular Reconfigurable Architecture,” in ISCA, 2000.
[30] R. C. Murphy et al., “The Characterization of Data Intensive Memory Workloads on Distributed PIM Systems,” in Intelligent Memory Systems. Springer.
[31] J. Draper et al., “The Architecture of the DIVA Processing-in-Memory Chip,” in SC, 2002.
[32] S. Aga et al., “Compute Caches,” in HPCA, 2017.
[33] C. Eckert et al., “Neural Cache: Bit-serial In-cache Acceleration of Deep Neural Networks,” in ISCA, 2018.
[34] D. Fujiki et al., “Duality Cache for Data Parallel Acceleration,” in ISCA, 2019.
[35] M. Kang et al., “An Energy-Efficient VLSI Architecture for Pattern Recognition via Deep Embedding of Computation in SRAM,” in ICASSP, 2014.
[36] V. Seshadri et al., “Ambit: In-Memory Accelerator for Bulk Bitwise Operations Using Commodity DRAM Technology,” in MICRO, 2017.
[37] V. Seshadri et al., “Buddy-RAM: Improving the Performance and Efficiency of Bulk Bitwise Operations Using DRAM,” arXiv:1611.09988 [cs.AR], 2016.
[38] V. Seshadri et al., “Fast Bulk Bitwise AND and OR in DRAM,” CAL, 2015.
[39] V. Seshadri et al., “RowClone: Fast and Energy-Efficient In-DRAM Bulk Data Copy and Initialization,” in MICRO, 2013.
[40] S. Angizi and D. Fan, “Graphide: A Graph Processing Accelerator Leveraging In-DRAM-computing,” in GLSVLSI, 2019.
[41] J. Kim et al., “The DRAM Latency PUF: Quickly Evaluating Physical Unclonable Functions by Exploiting the Latency–Reliability Tradeoff in Modern DRAM Devices,” in HPCA, 2018.
[42] J. Kim et al., “D-RaNgE: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput,” in HPCA, 2019.
[43] F. Gao et al., “ComputeDRAM: In-Memory Computing Using Off-the-Shelf DRAMs,” in MICRO, 2019.
[44] K. K. Chang et al., “Low-Cost Inter-Linked Subarrays (LISA): Enabling Fast Inter-Subarray Data Movement in DRAM,” in HPCA, 2016.
[45] X. Xu et al., “ELP2IM: Efficient and Low Power Bitwise Operation Processing in DRAM,” in HPCA, 2020.
[46] S. Aga et al., “DRISA: A DRAM-Based Reconfigurable In-Situ Accelerator,” in MICRO, 2017.
[47] Q. Deng et al., “DaAec: A DRAM Based Accelerator for Accurate CNN Inference,” in DAC, 2018.
Y. Zha and J. Li, "Hyper-AP: Enhancing Associative Processing Through A

D. Fujiki et al., "GIRAF: General Purpose In-Storage Resilient Associative Frame-
work," IEEE TPDS, 2021.

B. Asgari et al., "FASFNR: Accelerating Sparse Gathering by Using Efficient Near-Memory Intelligent Reduction," in HPCA, 2021.

A. Boroumand et al., "Google Neural Network Models for Edge Devices: Analy-
lyzing and Mitigating Machine Learning Inference Bottlenecks," arXiv preprint
arXiv:2109.14320, 2022.

A. Boroumand et al., "Google Neural Network Models for Edge Devices: Analy-
lyzing and Mitigating Machine Learning Inference Bottlenecks," in PACT, 2021.

A. Boroumand, "Practical Mechanisms for Reducing Processor-Memory Data
Movement in Modern Workloads," Ph.D. dissertation, Carnegie Mellon Univer-
sity, 2020.

G. Singh et al., "NERO: A Near High-Bandwidth Memory Stencil Accelerator for
Weather Prediction Modeling," in BIBM, 2020.

Y. Seohadri and G. Mutlu, "Simple Operations in Memory to Reduce Data Move-
ment," in Advances in Computers, Volume 106, 2017.

S. Dai et al., "High-throughput Pairwise Alignment with the Wavefront Algo-

rithm using Processing-in-memory," arXiv preprint arXiv:2204.02085, 2022.

S. Dai et al., "High-throughput Pairwise Alignment with the Wavefront Algo-

rithm using Processing-in-memory," in HICOMB, 2022.

D. Fujiki et al., "In-Memory Data Parallel Processor," in ASPLOS, 2018.

Y. Zha and J. Li, "Hyper-AP: Enhancing Associative Processing Through A
Full-Stack Optimization," in ISC, 2020.

G. Mutlu, "Memory Scaling: A Systems Architecture Perspective," IMW, 2013.

G. Mutlu and L. Subramanian, "Research Problems and Opportunities in Memory
Systems," SuperFBE, 2014.

H. Ahmed et al., "A Compiler for Automatic Selection of Suitable Processing-in-
Memory Instructions," in DATE, 2019.

S. Jain et al., "Computing-in-Memory with Spintronics," in DATE, 2018.

N. M. Ghiasi et al., "GenStore: A High-Performance and Energy-Efficient In-
Storage Computing System for Genome Sequence Analysis," in ASPLOS, 2022.

G. F. Oliveira et al., "DAMOV: A New Methodology and Benchmark Suite for
Evaluating Data Movement Bottlenecks," arXiv:2105.03725 [cs.AR], 2021.

S. Cho et al., "McDRAM v2: In-Dynamic Random Access Memory Systolic Array
Accelerator to Address the Large Model Problem in Deep Neural Networks on the
Edge," IEEE Access, 2020.

H. Shin et al., "McDRAM: Low latency and energy-efficient matrix compu-
ting in DRAM," IEEE TCDAC, 2018.

P. Gu et al., "UPDM: Programmable In-Memory Image Processing Accelerator
using Near-Bank Architecture," in ISCA, 2020.

D. Lavenier et al., "Variant Calling Parallelization on Processor-in-Memory
Architecture," in BIBM, 2020.

V. Zois et al., "Massively Parallel Skyline Computation for Processing-in-
Memory Architectures," in PACT, 2018.

D. Weber et al., "Current and Future Challenges of DRAM Metallization," in
IFTC, 2005.

Y. Peng et al., "Design, Packaging, and Architectural Policy Co-optimization for
DC Power Integrity in 3D DRAM," in DAC, 2015.

F. Devaux, "The True Processing In Memory Accelerator," in Hot Chips, 2019.

M. Yu et al., "A Fully Integrated Multi-CPU, GPU and Memory Controller
32nm processor," in JSICC, 2011.

R. Christy et al., "8.3 A CHG ARM Neoverse N1 CPU in 7nm FinFET for Infra-
structure Applications," in JSICC, 2020.

T. Singh et al., "3.2 Zen: A Next-generation High-performance x86 Core," in
JSICC, 2017.

UPMEM, "UPMEM Website," https://www.upmem.com, 2020.

UPMEM, "Introduction to UPMEM PIM, Processing-in-memory (PIM) on DRAM
Architecture (White Paper)," 2016.

J. Gómez-Luna et al., "Benchmarking a New Paradigm: An Experimental Anal-
ysis of a Real Processing-in-Memory Architecture," arXiv:2105.03814 [cs.AR],
2021.

J. Gómez-Luna et al., "Benchmarking a New Paradigm: Experimental Analysis
and Characterization of a Real Processing-in-Memory System," IEEE Access,
2022.

J. Gómez-Luna et al., "Benchmarking Memory-Centric Computing Systems: Analysis of Real Processing-In-Memory Hardware," in ISCC, 2021.

Y.-C. Kwon et al., "25.4 A 20nm 6GB Function-In-Memory DRAM, Based on
HBM2 with a 1.2 TFLOPS Programmable Computing Unit Bank-Level Parallel-
ism, for Machine Learning Applications," in ISCC, 2021.

S. Lee et al., "Hardware Architecture and Software Stack for PIM Based on
Commercial DRAM Technology: Industrial Product," in ISCA, 2021.

L. Ke et al., "Near-Memory Processing in Action: Accelerating Personalized
Recommendation with AIxDMA," IEEE Micro, 2021.

S. Lee et al., "A 1ynm 1.25V 8Gb, 16GB/s pin GDDR6-based Accelerator-in-
Memory supporting 1TFLOPS/MAC Operation and Various Activation Functions
for Deep-Learning Applications," in ISCC, 2022.

D. Niu et al., "164QPI/P 64MHz 3D Logic-to-DRAM Hybrid Bonding with
Process-Near-Memory Engine for Recommendation System," in ISCC, 2022.

JEDEC, "High Bandwidth Memory (HBM) DRAM," Standard No. JESD235, 2013.

D. Lee et al., "Simultaneous Multi-Layer Access: Improving 3D-Stacked Memory
Bandwidth at Low Cost," TACO, 2016.

D. A. Freedman, Statistical Models: Theory and Practice, 2009.

Y. Xu and X. Su, Linear Regression Analysis: Theory and Computing, 2009.

D. W. Hosmer Jr et al., Applied Logistic Regression, 2013.

S. Sathaharan, "Decision Tree Learning," in Machine Learning Models and Algo-
rithms for Big Data Classification, 2016.

S. P. Lloyd, Least Squares Quantization in PCM, IEEE Transactions on Informa-
tion Theory, 1982.

B. Birk et al., "Programming Massively Parallel Processors, 3rd Edition, Chapter
16 - Application Case Study: Machine Learning," Morgan Kaufmann, 2017.

S. Chetlur et al., "cudNN: Efficient Primitives for Deep Learning," arXiv preprint
arXiv:1410.0794, 2014.

S. P. Jouppi et al., "Tensorflow: A System for Large-scale Machine Learning," in
OSDI, 2016.

Run:AI, "Best GPU for Deep Learning," https://www.run.ai/guides/gpu-deep-
learning-best-gpu-for-deep-learning/, 2021.

M. P. Jouppi et al., "In-Datascience Performance Analysis of a Tensor Processing
Unit," in ISCA, 2017.

M. P. Jouppi et al., "Ten Lessons from Three Generations Shaped Google’s
TPUv4: Industrial Product," in ISCA, 2021.

UPMEM, "UPMEM User Manual: Version 2021.3.0," 2021.

UPMEM, "UPMEM Software Development Kit (SDK)," https://sdk.upmem.com,
2021.

N. Zmora et al., "Achieving FPS2 Accuracy for INT8 Inference Using Quantization Aware Training with NVIDIA TensorRT," https://developer.nvidia.com/blog/achieving-fp32-accuracy-for-int8-inference-
using-quantization-aware-training-with-tensorrt/.

A. Glomm et al., "A Survey of Quantization Methods for Efficient Neural
Network Inference," in Low-Power Computer Vision.

NVIDIA, "NVIDIA H100 Tensor Core GPU Architecture. White Paper," https://
nvidia.widen.net/9fe8d674d7e/tgp2-whitepaper-hopper-2022.

J. Han and C. Moraga, "The Influence of the Signifidt Parameter Computational
Speed of Backpropagation Learning," in IWANN, 1995.

Q. Deng et al., "L2ac: Exploring Lookup Table-based Fast and Accurate Vector
Multiplication in DRAM-based CNN Accelerator," in DAC, 2019.

M. Gao et al., "DRA: A Low-power DRAM-based Reconfigurable Acceleration
Architecture for Deep Learning Workloads," in ISCA, 2016.

E. W. Weisstein, "Taylor Series," https://mathworld.wolfram.com/TaylorSeries.
hmtl, 2004.

SAFARI Research Group, "PIM Machine Learning Training Benchmarks,"
https://github.com/CMU-SAFARI/pim-ml.

D. Abt et al., "Think fast: a tensor streaming processor (tsp) for accelerating
dee pi learning workloads," in ISCA, 2020.

K. Rocki et al., "Fast Stencil Code Computation on a Wafer-Scale Processor," in
SC, 2020.

D. Kim et al., "Neurocube: A Programmable Digital Neuromorphic Architecture
with High-Density 3D Memory," in ISCA, 2016.

J. Liu et al., "Processing-in-Memory for Energy-Efficient Neural Network Train-
ing: A Heterogeneous Approach," in MICRO, 2018.

B. T. Polya, "Introduction to Optimization, 1987.

S. Boyd and L. Vandenberghe, Convex Optimization, 2004.

S. Williams et al., "Roofline: An Insightful Visual Performance Model for Multi-
core Architectures," CACM, 2009.

Intel, "Intel Xeon Processor E3-1225 v6," https://ark.intel.com/content/www/en/
ark/products/97476/intel-xeon-processor-e3-1225-v6-fm-cache-3-30-
ghz.html, 2017.

Intel, "Intel Advisor," 2020.

R. S. Sutton and A. G. Barto, Reinforcement Learning: An Introduction, 2018.

H. Cho et al., "FaSc: Fpga-accelerated deep reinforcement learning," in Proceed-
ings of the Twenty-Fourth International Conference on Architectural Support for
Programming Languages and Operating Systems, 2019, pp. 499–513.

G. Singh et al., "Sibyl: Adaptive and extensible data placement in hybrid storage
systems using online reinforcement learning," in ISCA, 2022.

Hybrid Memory Cube Consortium, "HMC Specification 2.0," 2014.
