Design, Simulation and Characteristics Research of the Interface Circuit based on nano-polysilicon thin films pressure sensor

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Abstract. This paper presents a interface circuit for nano-polysilicon thin films pressure sensor. The interface circuit includes consist of instrument amplifier and Analog-to-Digital converter (ADC). The instrumentation amplifier with a high common mode rejection ratio (CMRR) is implemented by three stages current feedback structure. At the same time, in order to satisfy the high precision requirements of pressure sensor measure system, the 1/f noise corner of 26.5 mHz can be achieved through chopping technology at a noise density of 38.2 nV/sqrt(Hz).Ripple introduced by chopping technology adopt continuous ripple reduce circuit (RRL), which achieves the output ripple level is lower than noise. The ADC achieves 16 bits significant digit by adopting sigma-delta modulator with fourth-order single-bit structure and digital decimation filter, and finally achieves high precision integrated pressure sensor interface circuit.

1. Introduction
With the development of microelectronics mechanical system (MEMS) technology and the improvement of integrated circuit technology, integrated sensor with signal processing circuit has been applied in car electronics, aeronautics and astronautics, etc. Due to the output of pressure sensor is about a few tens of millivolt, amplifier often uses to amplify the output then utilizing the ADC to convert the analog signal into digital signal. However, the output signal of pressure sensor is always effected by noise and offset of interface circuit, which seriously reduced the pressure sensor performance. To maintain interface circuit of pressure sensor accuracy, the instrumentation amplifier should be low noise and high CMRR. The input noise and offset of typical complementary metal oxide semiconductor (CMOS) amplifiers is at the millivolt level, limiting their accuracy severely. The need for precise pressure measurement is the driving force behind a continuous effort to reduce the offset and noise of CMOS amplifier. The technology can be taken use of includes chopping and auto-zero technology. Because auto-zero technology adopts sampling, so noise aliasing will be induced to signal band, which would reduce circuit performance. Therefore, chopping technology is more suitable for low-noise instrumentation amplifier. In addition, in order to facilitate subsequent digital circuit processing, a ADC with high signal to noise ratio (SNR) for high precision measurement system is needed. Among various ADC architectures, the Sigma-Delta ADC can realize high SNR by using oversampling and noise shaping technologies [1], which trade speed for accuracy and low requirement to integrated circuit
manufacturing process as well as reduce the difficulty of the analog integrated circuit design. Those properties exactly fit for pressure sensor interface circuit.

Based on characteristics of nano-polysilicon thin films pressure sensor, a high CMRR and high precision interface circuit presents in this paper. Chopping technology was chosen in this design to achieve low-noise instrumentation amplifier. For the complete realization of digital output interface circuit, a Sigma-delta ADC was designed in the system.

2. Principle of pressure sensor interface circuit

2.1. Characteristics of pressure sensor

In order to measure the environment pressure, a block diagram of pressure sensor interface circuit was present in figure 1(a). The sensitive element of pressure sensor is four nano-polysilicon thin films piezoresistors (R1, R2, R3 and R4) connected by the Wheatstone bridge structure, which has been represented in the dashed block (as shown figure 1(a)). The characteristics of the pressure sensor is shown in figure 1(b). The sensitivity of pressure sensor is 0.146 mV/kPa, when the supply is 3 V [2]. The pressure sensor interface circuit is generally divided into two parts: instrumentation amplifier and ADC. The instrumentation amplifier can amplify the output signal of pressure sensor and the ADC can digitize the output of amplifier.

![Figure 1](image)

**Figure 1.** An interface circuit block diagram and sensitive characteristics of pressure sensor based on nano-polysilicon thin films

(a) the overall block diagram of interface circuit  (b)the characteristics of the pressure sensor

2.2. Principle of instrumentation amplifier

The instrumentation amplifier adopts current feedback instrumentation amplifier (CIFA) structure is shown in figure 2. This structure has high CMRR, meanwhile output common-mode voltage has no relationship with input common-mode voltage, which is fit for sensor interface circuit with the advantage of low power consumption. In order to satisfy the characteristic of low noise required by the system, chopping technology is used to reduce low frequency noise and offset. By using a three stage nested-Miller topology, and chopping both the input stage and intermediate stage as well as the third stage noise is too small to neglect, which can satisfied the requirements of the system. The ripple induced by chopping technology adopts continuous time ripple-reduce-loop (RRL) to suppress the influence of ripple on the system [3-4], achieving the demands of system on noise and offset.

The principle of the whole instrumentation amplifier is as follows: the input voltage is corresponding to the current through Gm1, and the feedback voltage is converted to corresponding current through Gm4, then, the current difference between the output current of Gm1 and Gm4 is nulled by Gm2 and Gm3.

According to principle of instrumentation amplifier, the gain (A_v) of proposed instrumentation amplifier can be indicated as eq. (1),

\[ A_v \approx \frac{G_{m1}}{G_{m4}} \cdot \frac{G}{G + R_{21} + R_{22}} \]

where \( G_{m1} \) and \( G_{m4} \) is amplifier transconductance of input stage, \( R_G \), \( R_{21} \) and \( R_{22} \) are resistances which use to modify the gain.
Figure 2. The overall block diagram of instrumentation amplifier circuit

As shown in the figure 2, CH1, CH5, CH2 and CH6 is chopper, the noise and offset of the input stage and the intermediate stage are modulated to high frequency by chopper CH2, transmitted to the output end through capacitance (C11, C12). Without RRL circuit, the ripple in output end will be large, which will influence the performance of measuring circuit. The principle of RRL is: output high frequency ripple current is converted into high frequency voltage through two capacitance (C31, C32), and then converted into direct voltage through chopper CH6, and take use of Gm5 to convert voltage into current to make the feedback of the output end of Gm1 and Gm4 so as to achieve the goal of negative feedback. Signal transfer function of the whole loop can be presented as:

\[ H(s) = \frac{1}{1 + L(s)} \]  \hspace{1cm} (2)

\[ L(s) = \frac{A_v G_{m5}}{C_2 f_{ch1}} \]  \hspace{1cm} (3)

where \( H(s) \) is the signal transfer function of RRL and \( L(s) \) is the transfer function from input end of chopper CH3 to output end of chopper CH2, \( A_v \) is the gain of integration amplifier, \( C_2 \) is high frequency path capacitance, \( f_{ch1} \) is chopping frequency.

Through feedback loop, the output voltage of ripple is:

\[ V_{out,ripple} = \frac{V_{ref} G_{m3}}{2 A_v G_{m5}} \]  \hspace{1cm} (4)

where the \( V_{ref} \) is the input offset.

The unity-gain bandwidth \( f_{notch} \) of the loop can be derived from eq. (2) by setting \( L(s) = 1 \):

\[ f_{notch} = \frac{G_{m3} C_3}{2 \pi C_2 C_{int}} \]  \hspace{1cm} (5)

where \( C_{int} \) is integration capacitance, \( C_3 \) is capacitance that using to transfer current to voltage.

Therefore, RRL achieves notch-filtering function with the \( 2 f_{notch} \) bond width of chopping frequency. So, the ripple can be filter out within frequency at chopping frequency \( f_{ch} \) around \( 2 f_{notch} \). The magnitude of output ripple would be determined by \( G_{m3}, G_{m5} \) and \( A_v \).

2.3. Details implementation of the instrumentation amplifier

Because output noise equivalent to the input needs to be divided by the first-level gain, so the first-level gain must be very large. This design employed a folded cascode gain-boosted topology as shown in the figure 3(a), \( G_{m1} \) and \( G_{m4} \) use the same output stage, which lowers the influence of device mismatching on system, at the same time omits the difficulty of designing feedback transconductance and saves power dissipation. The auxiliary amplifiers also adopt full differential folded-cascode
operational amplifier structures. The gain of such structure can implement over 140 dB, and the 1/f noise is about 10 μV/sqrt(Hz).

Then, the second stage is implemented using a folded-cascode topology. The schematic diagram of the second and output stages is shown in figure 3(b). In order to increasing the range of output voltage, a class-AB output stage is implemented to achieve rail-to-rail output. Because the noise of output stage is suppressed by the gain of the preceding stages, the output stage does not use chopping technology.

The detailed implementation of the cascade buffers (CB) is shown in figure 3(c), CB isolates from C3 to enhance the ripple reduction. To increase the output impedance of CB, a gain-boosting topology is employed.

Figure 3. The schematic diagram details implementation of the instrumentation amplifier

(a) schematic diagram of the input stage
(b) schematic diagram of second and output stages circuit
(c)Implementation of the gain-boosted Cascades buffer

2.4. Principle of Sigma-Delta ADC

For implementing high precision analog-to-digital converter, Sigma-delta modulator is chosen. Four-order single-bit modulator is selected to achieve signal bandwidth with 10kHz and ADC with 16 bits resolution. Sigma-delta modulator mainly adopts over-sampling technology and noise-shaping technology to achieve high resolution. The SNR can be indicated as eq. (6)

\[
SNR = 6.02N + (2L+1)10\log_{10} OSR - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right)
\]

where L is the modulator order, N is the number of quantizer bit and OSR is oversampling ratio [5].
Quantized noise within signal bandwidth can be modulated to the high frequency through these two technologies, then acquire the interest signal by using digital decimation filter to remove the useless noise, and finally accomplish the design of pressure sensor interface circuit.

2.5. The details implementation of the Sigma-Delta ADC

2.5.1. Sigma-Delta Modulator

The structure of Sigma-delta Modulator is shown in figure 4. The design of Sigma-delta Modulator is mainly the design of NTF, which determines the upper limit of system and minimizes the influence of non-ideal factors on system as much as possible. The CIFF structural fourth-order single bit is adopted in the design, with Simulink ideal model simulation, the preliminary structure and structural coefficients are obtained, as shown in table 1. Considering non-ideal factors (e.g. the influence of operational amplifier, switch, capacitance, clock and other modules in Sigma-delta system), the circuit structural parameters are designed based on non-ideal model. In addition, according to the requirements of system for every module parameters, the specific module is designed.

The integrator adopts switch capacitance structure which can reduce the affect of clock jitter. As show in the figure 4, the amplifier of the first stage integrator employed by gain-boosting structure, which can reduce the effect that amplifier gain changed by output voltage. Due to the noise floor of Sigma-delta modulator mainly determined by the first stage amplifier, the chopping technology also fit for reduce the noise of the first stage amplifier. The amplifier of rest of integrator can be shaping by noise-shaping technology, so the basic structure of fully differential folded-cascode amplifier can realize the system requirements. By appropriate designing the timing, the circuit that satisfy the system requirements is designed finally.

Figure 4. Implementation of CIFF fourth-order single bit Sigma-delta Modulator

| Table 1. Structural coefficients of Sigma-Delta Modulator |
|-------------------|---|---|---|---|---|---|---|
|                  | C1 | C2 | C3 | C4 | A1 | A2 | A3 |
| C_{S1}/C_{I1}    | 1/3| 1/3| 1/3| 1/3| A1 | A2 | A3 |
| C_{S2}/C_{I2}    | 1/3| 1/3| 1/3| 1/3| A1 | A2 | A3 |
| C_{S3}/C_{I3}    | 1/3| 1/3| 1/3| 1/3| A1 | A2 | A3 |
| C_{S4}/C_{I4}    | 1/3| 1/3| 1/3| 1/3| A1 | A2 | A3 |
| C_{F1}/C_{F0}    | 1/5| 1/5| 1/5| 1/5| A1 | A2 | A3 |
| C_{F2}/C_{F0}    | 1/5| 1/5| 1/5| 1/5| A1 | A2 | A3 |
| C_{F3}/C_{F0}    | 1/5| 1/5| 1/5| 1/5| A1 | A2 | A3 |
| C_{F4}/C_{F0}    | 1/5| 1/5| 1/5| 1/5| A1 | A2 | A3 |

2.5.2. Digital decimation filter
Considering to reduce the cost and power consumption of digital circuit, the cascaded integrator comb (CIC) filter was use as decimation filter which can be implement by integrator and differentiators. In order to filter the out-band-noise, five order comb filter was selected. For downsampling ration is N, the transfer function of comb filter in Z domain can be indicated as eq. (7)

$$\frac{1}{H(z)} = \frac{(1-z^{-N})^5}{N(1-z^{-1})} = \frac{1}{1-Z^{-1}} \frac{1}{1-Z^{-1}} \frac{1}{1-Z^{-1}} \frac{1}{1-Z^{-1}} \frac{1}{1-Z^{-1}} \frac{1-Z^{-N}}{N} \frac{1-Z^{-N}}{N} \frac{1-Z^{-N}}{N} \frac{1-Z^{-N}}{N} \frac{1-Z^{-N}}{N} \frac{1-Z^{-N}}{N}$$

(7)

The expression can be transfer to block structure as shown in figure 5.

![Figure 5. Block structure of CIC filter](image)

However, after the CIC filter processing, the passband damping is serious, a Finite Impulse Response (FIR) trimming filter is needed. Then through Verilog language describes the behavior then transfer into digital circuit.

3. Results and Discussion

3.1. simulation results of AC response and noise

The pressure sensor interface circuit was realized in a 0.35μm CMOS process. By scanning the input signal frequency range from 1 Hz to 1 GHz, simulation result presents that the unity-gain bandwidth of CIFA is 336 kHz and the gain is 40 dB. A notch around chopping frequency can be seen in the figure6, which is 6.1 kHz notch width. The outcomes satisfy the designed requirement.

![Figure 6. The periodic AC response of instrumentation amplifier](image)

The noise simulation result is shown in figure 7, under 20 μV offset, the 1/f noise corner is 26.5 mHz at a noise density of 38.2 nV/sqrt(Hz) of the amplifier can be achieved through chopping technology. So the noise effect induced by interface circuit can be neglected.

![Figure 7. The equivalent input noise of instrumentation amplifier](image)
3.2. Simulation results of Sigma-Delta ADC

The voltage and frequency of input signal (amplified output signal of pressure sensor) in simulation condition are 1 V and 488.28125 Hz, respectively. By computing 65536 points simulation data, the simulation result of Sigma-delta modulator is shown in figure 8. The power spectral density figure shows that the design goal of 16 bits (effective number of bits) was realized.

![Figure 8. The Sigma-delta modulator output power spectral density](image)

The simulation result of digital decimation filter is shown in figure 9, realizing the 16 bits significant digit output.

![Figure 9. The input signal and output of digital decimation filter](image)

4. Conclusions

Based on nano-polysilicon thin films pressure sensor, an integrated interface circuit was designed in the paper. After discussing the principle of instrumentation amplifier and Sigma-delta ADC, the details of design is given in the paper. The simulation result shows that the instrumentation amplifier with low noise 100 times of magnification and the ADC integrated with 16 bits significant digit is implemented. The instrumentation amplifier only consumes supply current of 620μA. The 1/f noise density is 38.2 nV/sqrt(Hz) at 26.5 mHz. While, the Sigma-delta ADC consumes 55 mW supply, realizing 99.49 dB SNR. The output of pressure sensor was fully high precision converted into digital signal, after the digital decimation filter. The design of high precision integrated pressure sensor interface circuit is completed.

References

[1] B.E. Boser, S.EJ. Wooley. The design of Sigma-Delta Modulator analogy-to-digital converters[J].
IEEE Journal of Solid-State Circuits, 1988, 23:1298-1308.

[2] Zhao Xiaofeng, Wen Dianzhong. Fabrication and characterization of nano-polysilicon thin film pressure sensor[J]. Journal of Semiconductors, 2008,29(10):2038-2042.

[3] Rong Wu, Kofi A. A. Makinwa, Johan H. Huijsing. A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an AC-coupled ripple reduction loop[J]. IEEE Journal of Solid-State Circuits, 2009,44(12).

[4] Rong Wu, Johan H. Huijsing and Kofi A. A. Makinwa. A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error[J]. IEEE Journal of Solid-State Circuits, 2011, 46(12).

[5] Richard Schreier, Cabor C.Temes. Understanding delta-sigma data converters[M]. IEEE Press. 2005:91-121.

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