A Machine Learning Pipeline Stage for Adaptive Frequency Adjustment

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Abstract—A machine learning (ML) design framework is proposed for adaptively adjusting clock frequency based on propagation delay of individual instructions. A random forest model is trained to classify propagation delays in real time, utilizing current operation type, current operands, and computation history as ML features. The trained model is implemented in Verilog as an additional pipeline stage within a baseline processor. The modified system is experimentally tested at the gate level in 45 nm CMOS technology, exhibiting a speedup of 70% and energy reduction of 30% with coarse-grained ML classification. A speedup of 89% is demonstrated with finer granularities with 15.5% reduction in energy consumption.

Index Terms—Computer Systems Organization, Microprocessors and microcomputers, Hardware, Pipeline, Processor Architectures, Pipeline processors, Pipeline implementation, VLSI Systems, Impact of VLSI on system design, VLSI, System architectures, integration and modeling, Design Methodology, Cost/performance, Machine learning, Classifier design and evaluation

1 INTRODUCTION

The primary design goal in computer architecture is to maximize the performance of a system under power, area, temperature, and other application-specific constraints. Heterogeneous nature of VLSI systems and the adverse effect of process, voltage, and temperature (PVT) variations have raised challenges in meeting timing constraints in modern integrated circuits (ICs). To address these challenges, timing guardbands have constantly been increased, limiting the operational frequency of synchronous digital circuits. On the other hand, the increasing variety of functions in modern processors increases delay imbalance among different signal propagation paths. Bounded by critical path delay, these systems are traditionally designed with pessimistically slow clock period, yielding underutilized IC performance. Moreover, power efficiency of these underutilized systems also degrades due to the increasing power leakage. Alternatively, when designed with relaxed timing constraints, integrated systems are prone to functional failures. To simultaneously maintain correct functionality and increase system performance, numerous optimization techniques as well as offline and online models have recently been proposed including: pipelining, multicore computing, dynamic frequency and voltage scaling (DVFS), and ML driven models [1], [2], [3], [4], [5], [6], [7], [8], [9].

Propagation delay in a processor is a strong function of the type, input operands, and output of the current operation, and computation history [1]. Computation history accounts for data overwrite and crosstalk noises. Intuitively, majority of operations are completed within a small portion of the clock period, as determined by the slowest path in the circuit. Based on path delay distribution, as reported in [5], the operational frequency can be doubled for majority (e.g., 86.7% in [5]) of instructions in a typical program.

While multicore approaches have been proposed to enhance system performance, the scalability of modern multicore systems is limited by the design complexity of instruction level parallelism and thermal design power constraints [10], [11]. Thus, speeding a single thread execution is an important cornerstone for enhancing performance in modern ICs [12]. This is, therefore, the primary focus of the proposed approach. To the best of the authors’ knowledge, this paper is the first to employ ML for adaptively adjusting the clock frequency at the instruction-level. Note that with the proposed method, the clock frequency is adaptively adjusted per instruction in real time, yielding a fundamentally different approach as compared with the traditional, task-based dynamic frequency scaling. The main contributions of this work are as follows:

1) A systematic flow is proposed and implemented as a unified platform for extracting ML input features from an instruction and classifying the instruction execution delay in real time.
2) A random forest (RF) model is trained to classify individual instructions into delay classes based on their type, input operands, and the computation history of the system.
3) A new pipeline stage is integrated within a pipelined MIPS processor.
4) The proposed method is synthesized and verified on LegUp [13] benchmark suite of programs with Synopsys Design Compiler in 45 nm CMOS technology node.

The rest of the paper is organized as follows. Section 2 describes prior and related work. Section 3 explains the proposed unified platform and the design methodology. ML algorithms for classification of instruction delay are described in Section 4. In Section 5 the implementation details of the system are introduced. Experimental results are presented in Section 6. Conclusions and future work

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are discussed in Section 7 and the paper is summarized in Section 8.

2 Prior and Related Work

Multiple approaches have been proposed for efficiently tuning the operating point (i.e., voltage supply and clock frequency) of a system at various levels of a computing system, including application- and task-based methods and instruction-level speculations.

Predicting timing violations in a constraint-relaxed system is impractical with deterministic approaches, due to the wide dynamic range of input and output signals (typically 32 or 64 bits), variety of operations in a modern processor, and delay dependence on the runtime and physical characteristics of the system (e.g., crosstalk noise). ML based approaches for predicting timing violations of individual instructions have recently been proposed, which consider the impact of input operands and computation history on timing violations [4], [14], [15]. While significant for the design process of next generation scalable high performance systems, these approaches have several limitations:

1) Instruction output is considered as a ML feature and exploited in these systems for predicting the timing characteristics of the individual instructions. These predictions are, however, carried out before the instruction execution, when the instruction output is not yet available, limiting the effectiveness of these methods in practical systems.

2) The modules under the test are studied separately and evaluated in an isolated test environment without the effects of other processing elements (e.g., arithmetic modules, buffers or multiplexers). The high reported accuracy is, therefore, expected to degrade if the methods are applied to a complex system (e.g., a practical execution unit).

3) Power and timing overheads due to additional hardware are not considered in these papers.

Granularity of prediction is another primary concern. A bit-level ML based method has been proposed in [16] for predicting timing violations with reduced timing guardbands. While up to 95% prediction accuracy has been reported with this method, the excessively high, per bit granularity of the ML predictions is expected to exhibit substantial power, area, and timing overheads. These overheads are, however, not evaluated in [16]. Furthermore, a procedure for recovery upon a timing error is not provided and the recovery overheads are also not considered.

An alternative to fine-grain high-overhead ML methods, multiple coarse-grain schemes for timing error detection and recovery have been proposed to mitigate the adverse effect of the pessimistic design constraints. A better-than-worst-case design approach has been introduced in [5]. With this approach, the clock period is set to a statistically nominal value (rather than worst-case propagation delay) and the history of timing erroneous program counters is kept in a ternary content-addressable memory (TCAM). The TCAM is exploited for predicting timing violations of the instructions based on previous observations. Note that the system only warns against those timing violations that have been previously recorded. Alternatively, unseen violations are not predicted with this approach. Owning to the apparent simplicity of this approach, only bi-state operating conditions (i.e., nominal and worst-case clock frequencies) can be efficiently utilized with this method. Alternatively, the design complexity and system overheads are expected to significantly increase with the increasing number of frequency domains.

In BandiTS [17], a reinforcement learning approach has been proposed to estimate the timing error probability (TEP) within a program time interval, given timing speculation (TS) ratios, \( TS_R = t_{clk}/t_{nom} \) for various values of the reduced clock period \( t_{clk} \), and the worst-case clock period \( t_{nom} \). The TS-based TEP problem is modeled in [17] as the classical multi-armed bandit problem [18], where the TS ratios and TEPs correspond to, respectively, the arms and stochastic rewards. The primary limitation of that work is the lack of details about the hardware implementation and overheads. In addition, the maximum achievable performance gain of only 25% has been reported. Furthermore, BandiTS approach exhibits per-task clock granularity and scales the clock frequency for a batch of instructions. Higher performance gain is possible with fine-grain, per instruction clock frequency adjustment, as shown in this paper.

A thermal-aware voltage scaling has been proposed in [19]. Voltage selection algorithm has been developed and integrated within FPGA synthesis process to aggressively scale the core and block RAM voltages, utilizing the available thermal headroom of the FPGA-mapped design. As a result, 36% reduction in power consumption has been demonstrated. Driven by workload and thermal power dissipation, this method, however, supports only coarse-grain voltage and frequency scaling.

Predicting program error rate in timing-speculative processors has been proposed in [20]. A statistical model is developed for predicting dynamic timing slack (DTS) at various pipeline stages. The predicted DTS values are exploited to estimate the timing error rate in a program. The implementation overheads, and the potential performance or power consumption gains are, however, not reported with this approach.

An offline model for TS processors has been introduced in [21]. This probabilistic model is trained to optimally select a better-than-worst-case, nominal clock frequency. The provided hardware-based speculation, however, does not consider the overall workload or specific finer units, limiting the fidelity of the method. Alternatively, the adverse effect of process variations on the propagation delay is considered, strengthening the approach in [21]. Note that PVT variations are also considered with the proposed approach of classifying instructions into delay intervals in real time, as described in the following sections.

Finally, ML based methods for modeling system behavior have also been proposed. For example, in [6], linear regression has been leveraged for modeling the aging behavior of an embedded processor based on current instruction and its operands, as well as the computation history and overall circuit switching activity. As a result, the timing guardband designed to compensate for aging in digital circuits can be effectively reduced, in presence of graceful degradation [6]. Reallocation of delay budget has, however, not been considered with this method.
ML ICs can exhibit a prohibitively high power consumption and physical size. Furthermore, ML ICs can introduce additional delay and increase design complexity, depending upon the application characteristics. To efficiently exploit ML methods for managing frequency in modern processors, delay, power, and area of ML ICs should be considered.

3 The proposed ML based frequency adjustment

In this paper, a design methodology is proposed for ML driven adjustment of operational frequency in pipeline processors. With the proposed method, individual instructions are classified into the corresponding propagation delay classes in real time, and the clock frequency is accordingly adjusted to reduce the gap between the actual propagation delay and the clock period. The classes are defined by segmenting the worst-case clock period into shorter delay fragments. Each class is characterized by a specific supply voltage and clock frequency. The primary design objective is to maximize system performance within an allocated energy budget. The overall delay and energy consumption are evaluated with the additional ML components, and both the correct and incorrect predictions. The proposed scalable framework allows for other control configurations to be defined in a similar manner for different design objectives. The real-time clock adjustment is enabled by the recent advancement in clock management circuits [24].

In order to evaluate this method, a pipelined, 32-bit MIPS processor (TigerMIPS [22]) is utilized as the baseline processor. The ML classifier is designed as an additional pipeline stage within the pipelined MIPS processor, as shown in Fig. 1. The inputs to the additional ML pipeline stage are the current instruction and its operands, as well as the computation history, as defined by the toggled inputs bits (i.e., current inputs are XORed with the previous inputs) and output of the previous operation. The choice of these parameters is in accordance with the results in [4] and [6]. These inputs are utilized as ML features for predicting the delay class of the current instruction based on the trained ML model. It is important to note that more complex, slower ML models can also be trained with this methodology, as long as the design complexity and hardware costs of the final system meet the specified constraints. To meet the overall system throughput constraints, the trained models can be implemented as multiple pipeline stages, mitigating the additional latency introduced by the ML functions.

3.1 Phase 1: Baseline processor synthesis and profiling

First, the high-level hardware description language (HDL) model of the baseline processor is synthesized into gate-level description model. During this phase, timing information is generated in the IEEE standard delay format (SDF). Based on this information, the gate-level simulation (GLS) is performed and the instruction-level execution profile is generated. A profile comprises a list of instructions, the fetched or forwarded operands, the output of the operations, and the propagation delays. In addition to the execution profile, post place-and-route (PAR) reports, including timing and power information, are collected in this phase.

3.2 Phase 2: ML training

In this phase, the gate-level profiles from Phase 1 are parsed and utilized as ML features. Based on the extracted features, a preferred ML model is trained in Python with Scikit-learn ML library [23]. A HDL code (e.g., Verilog in this paper) of the trained model is generated and integrated within the baseline processor as a single (or multiple) pipeline stage(s) between the decode and execute stages (see Fig. 1).

3.3 Phase 3: Verification and Evaluation

During this phase, the modified high-level HDL model of the system with the ML pipeline stage is synthesized and profiled, as described in Phase 1. To guarantee functional correctness, the output signal is double-sampled to detect timing violations, and timing-erroneous instructions are re-executed with the worst-case clock frequency. Similar to the baseline iteration, the post PAR reports are extracted for evaluating the timing and energy characteristics of the system. Finally, the profiling of the modified system is executed during this phase to evaluate the overall speedup of the system.

To optimize the final solution in terms of the operational frequency and energy consumption, the proposed flow is executed iteratively with various ML algorithms and clock fragments, as shown with the feedback in Fig. 2. The clock signal of the pipeline registers is assumed to be near-instantly switched based on the individual classification results, as has been experimentally demonstrated in [24].

4 Machine learning models

Owing to the unique learning characteristics and hardware trade-offs of neural networks (NNs), support vector machines (SVMs), and random forest (RF) models, all these ML models are considered in this paper. Each model is trained based on the instruction profiles extracted from a
synthetically generated dataset of 3,000 random instructions per class. The delay boundaries of the individual classes are experimentally determined with respect to the worst-case delay of 4 ns as follows: 

\[
\{[0.0, 2.2], (2.2, 4.0]\} \text{ for the two-class configuration, }
\{[0.0, 1.8], (1.8, 2.6], (2.6, 4.0]\} \text{ for the three-class configuration, and }
\{[0.0, 1.0], (1.0, 2.0], (2.0, 3.0], (3.0, 4.0]\} \text{ for the four-class configuration.}
\]

The feature vector of the \(i\)th instruction comprises six elements, \(x_i = (\text{instr}, \text{op}_1, \text{op}_2, \text{Xop}_1, \text{Xop}_2, \text{output})\). The first feature, \(\text{instr}\), comprises four subfeatures, representing the type of the operation in one-hot format,

\[
\text{instr} = \begin{cases} 
1000, & \text{if arithmetic} \\
0100, & \text{if arithmetic with immediate operand} \\
0010, & \text{if logical} \\
0001, & \text{if multiplication or division}
\end{cases}
\]

The subsequent four elements are defined by the operands. The features \(\text{op}_1\) and \(\text{op}_2\) are the first and second operands of the instruction, and the features \(\text{Xop}_1\) and \(\text{Xop}_2\) are the XORed values of the first and second operands with their respective previous values. The last feature, \(\text{output}\), is the output of the preceding instruction. The last three elements of the feature vector are exploited to capture the effect of computation history on the instruction delay. Note that the operands and output of the preceding instruction are 32-bit long, as determined by the 32-bit baseline processor utilized in this work. Thus, the distribution of these features significantly differs from the distribution of the operation type subfeatures. To balance the overall distribution of the individual features, the input features are preprocessed and scaled to follow a normal distribution using quantile transformer in Python scikit-learn library. An example of operand and output features with and without the transformation is shown in Fig. 3 for arithmetic and logical instructions. Note that the type subfeatures remain unchanged.

To evaluate the efficiency and efficacy of the proposed method, propagation delay classification is investigated with three common ML algorithms: NN, SVM, and RF. The configuration of each of the three ML models is described in the following subsections, including the hyperparameters, performance, and hardware costs of the individual ML algorithms. All the algorithms are five-fold cross-validated based on three thousand randomly generated instructions per class. While finding an effective metric for stability of the evaluation is still an open question, k-fold cross-validation with \(5 \leq K \leq 20\) is typically used, as these \(K\) values have been demonstrated to simultaneously minimize the bias and variance across many studied test sets \cite{25}, \cite{26}, \cite{27}, \cite{28}. Thus, \(K = 5\) is used in this work. ML accuracy is reported as the F1-score of delay classification and the resultant speedup for each benchmark program has been considered in determining the performance of each ML algorithm. Hardware cost is evaluated as the number of additional transistors required for implementing the individual ML algorithms and has also been considered in determining the performance of the ML algorithms. Among the evaluated ML algorithms, the RF classifier is preferred in this work due to the favorable tradeoff between the performance gain and hardware costs, as well as the relative simplicity of the RF algorithm, as explained in the following subsections.

### 4.1 Neural Networks

NNs excel in learning complex hidden patterns in large datasets and have exhibited a particular supremacy in vision and text applications as compared with classical ML algorithms. Following this success, promising results have been shown with NNs in various hardware related applications \cite{29}, \cite{30}, \cite{31}.

To determine the preferred set of hyperparameters for the two-, three-, and four-class NN models, a grid search is executed for each multiclass NN over the following ranges:

**Phase 1**
- **Start**
- **Baseline processor**
- **High-level HDL model**
- **Technology library**
- **Synopsys design compiler**
- **Timing and power reports**

**Phase 2**
- **Extract ML features and transform into the data structure**
- **Select ML model and train**
- **Trained ML model**
- **Evaluate the trained model**
- **No Constraints met?**
  - **Yes**
  - **Transform ML model into HDL**
  - **ML model HDL**
  - **Integrate HDL model into the baseline processor**

**Phase 3**
- **High-level HDL model**
- **Technology library**
- **Gate-level hardware model**
- **Synopsys design compiler**
- **Place & route**
- **ModelSim gate-level simulation**
- **Evaluate**
  - **Instruction-level execution profile**
  - **No Constraints met?**
  - **Yes**
  - **Finish**

Fig. 2: Systematic flow for designing ML predictor within a typical pipelined processor.
1) Identity, tanh, logistic, and ReLu activation functions,
2) Stochastic gradient descent [32], lbfgs (a limited memory BFGS quasi-Newton optimization algorithm [33]), and Adam (an adaptive learning rate optimization algorithm [34]) solvers, and
3) A single $m$-neuron hidden layer ($m \in \{5, 10, 15, 20\}$) and two hidden NN layers with $m_1$ and $m_2$ neurons in, respectively, the first and second layers ($m_1 \times m_2 \in \{20 \times 5, 20 \times 10, 20 \times 15\}$).

The networks are trained using backpropagation algorithm for 200 epochs until convergence with quasi-newton optimizer. Note that the number of neurons in the input and output layers is determined by, respectively, the number of ML features (nine, including the four instruction type subfeatures) and the number of ML classes (two, three, and four). The top ten grid search results (within 1% of the highest F1-score) are listed in Table 1 for each of the NN configurations. These top NN results are compared with the SVM and RF top results, and speedup per hardware metric (SPH).

The speedup per hardware cost (SPH) is also listed in Table 1 for each of the NN configurations. These top NN results are compared with the SVM and RF top results, as described at the end of this section. As a general rule,
learning capacity of a NN increases with the network complexity (i.e., number of neurons and number of layers). For a NN to be competitive with or outperform a classical ML algorithm, a large number of neurons and layers is required, significantly increasing the system complexity and hardware overhead of the NN based solutions.

### 4.2 Support Vector Machines

SVM classifier generates an optimal hyperplane which separates data samples in feature space with the objective to minimize the classification error. Linear SVM can only classify a linearly-separable data. Alternatively, to learn complex nonlinear data patterns, SVM can be combined with a kernel trick, enabling the feature transformation into linearly separable space \([36]\). In this work, a grid search is performed over the following kernel SVM hyperparameters:

1. Linear, polynomial, and radial basis function (rbf) kernels,
2. Integer degree of flexibility of the polynomial decision boundary, \(d \in [2, 15]\), and
3. The influence on the model of a single sample in a training set with \(N\) features and variance \(\text{Var}\) by scaling (i.e., \(\gamma = 1/(N \cdot \text{Var})\) or not scaling (i.e., \(\gamma = 1/N\)) the kernel coefficient, \(\gamma\).

The sets of hyperparameters with the highest F1-scores are listed in Table 2. The speedup, hardware cost, and SPH metric are also listed in the table for all the SVM configurations. SVM hardware cost is determined as the number of transistors, based on the method presented in [37]. SVM often exhibits excellent performance as compared with other learning algorithms at the expense of higher computational and design complexity, and accordingly higher power and area overheads [38]. These tradeoffs are discussed at the end of this section.

### 4.3 Random Forest

RF classifier is an ensemble of decision tree classifiers. The input samples are split into multiple sample subsets and each decision tree is trained on one training subset. The final classification decision for each sample is made based on the result of averaging the individual tree decisions (i.e., ensembling). RF models benefit from the accuracy, training speed, and interpretability of the decision tree model, while the ensembling mitigates the overfitting, otherwise common to decision tree classifier. RF is often preferred in scientific and practical applications [4], [39].

The computational and hardware complexity of RF is a strong function of the number and depth of the decision trees. The depth of the individual trees is dependent on the number of features and their correlation. In this work, a RF grid search is performed over the following ranges of hyperparameters:

1. Number of trees in the forest, \(n_{\text{estimators}} \in \{1, 10, 50, 100, 200\}\),
2. Maximum number of levels in each tree, \(\text{max\_depth} \in \{10, 20, 30, 40, 50\}\).

The results of the top estimators (within 1% of the highest F1-score) are listed in Table 3. The hardware cost of an
TABLE 3: Top (within 1% of the highest F1-score) RF configurations and their respective performance metrics (i.e., speedup, hardware cost (in million transistors), and speedup per hardware metric (SPH)).

|       | max_depth | n_estimator | F1-score | Speedup  | HW cost | SPH       |
|-------|-----------|-------------|----------|----------|---------|-----------|
| 4 classes | 0.120    | 3.515       | 0.980    | 0.947    | 0.843   | 200       |
| 3 classes | 0.846    | 1.856       | 0.407    | 4.554    |         |           |
| 2 classes | 0.840    | 1.902       | 0.120    | 15.859   |         |           |

Average F1-score: 0.847
Positive standard deviation: 0.002
Negative standard deviation: 0.008

5 IMPLEMENTATION

The proposed framework is implemented with RF model within TigerMIPS and evaluated based on LegUp benchmarks. The details of the implementation are described in this section.

5.1 Unified Platform

A holistic platform is developed based on the proposed system design methodology, as illustrated in Fig. 2. The framework is unified within a shell programming platform supported with several peripheral programs developed in C++ and Python. The synthesis steps, as described in Fig. 2, are sequentially executed from Start to Finish.

During the first phase, Synopsys Design Compiler is called with the high-level HDL model of the baseline processor. The profiler triggers are added to the system and GLS is performed in Modelsim.

The second phase is triggered upon the completion of the instruction profiling. An external parser program is called to transform the instruction profiles into the ML feature data structure and eliminate outliers. The model is trained to classify propagation delays into user-defined number of classes based on a user-specified learning algorithm and delay boundaries. The ML accuracy and estimated speedup are evaluated upon the training completion. If the design requirements are met, the ML software model is transformed into the high-level HDL code. Otherwise, ML model is retrained with new parameters.

Upon training completion, the HDL code of the ML model is instantiated within the original HDL model of the baseline processor. Finally, the procedure in Phase 1 is repeated in Phase 3 with the modified processor model, and the overall system performance and overheads are evaluated.

5.2 Baseline Processor

The proposed framework is demonstrated on TigerMIPS. In addition to the basic MIPS units, such as Instruction Fetch (IF), Instruction Decode (ID), Execute (Exe), Memory access (Mem), and Write-back (WB), TigerMIPS comprises advanced units, such as, forwarding unit, branch handling unit, stall logic, and instruction and data caches, which are common in modern pipeline processors.
5.3 Synthesis and Profiling

The baseline model is synthesized in 45 nm NanGate CMOS technology node with Synopsys Design Compiler. Upon completion of the synthesis, triggers are implemented in Verilog HDL, enabling data and timestamp sampling at the input and output of the execution unit within the MIPS pipeline. The profiling is performed based on GLS with Modelsim simulator.

5.4 Integration, Verification and Evaluation

The trained ML model is first validated in Python. The HDL code of the validated ML model is integrated into the baseline processor. Finally, the modified processor is synthesized and its functionality is verified through GLS.

The post PAR reports are utilized to evaluate the modified system with respect to specified design constraints.

6 Experimental Results

To demonstrate the framework, LegUp high-level synthesis benchmark suite coupled with LLVM compiler toolchain is utilized for profiling and verification during GLS. The trained RF model is tested with nine standard benchmark programs available within the LegUp benchmark suite and an additional synthetically generated benchmark with one million random instructions. The F1-score is shown in Fig. 6 for two, three, and four ML delay classes, yielding above 95% F1-score for majority of the programs with two delay classes. Resultant speedup for the individual benchmarks is shown in Fig. 7 including the practical speedup (with the misclassification penalty), no-penalty speedup (without the misclassification penalty), and ideal speedup (with 100% classification accuracy). The energy overhead due to the additional ML hardware and classification errors is listed in Table 4. To account for delay overheads due to the misclassification of a slow instruction into a higher performance class, a re-execution penalty of four clock cycles (compensating for IF, ID, ML, and EX stages) is considered within the performance results, as reported in Fig. 7. The no-penalty speedup is also presented in Fig. 7, visualizing the penalty due to the misclassification of a fast instruction into a slow class. Note that the overall speedup with four-class configuration is higher than the speedup with two-class configuration, albeit the higher classification accuracy with two delay classes. Alternatively, higher misclassification rate with four delay classes yields higher re-execution energy consumption, as listed in Table 4. Also, note that a negative energy overhead indicates a reduction in the overall energy consumption (i.e., power-delay product).

Performance comparison between the proposed method and state-of-the-art (ML and non-ML) DVFS approaches is listed in Table 5. For example, both the proposed framework and the approach in [5] consider binary classification with two execution delay classes. The proposed method exhibits 3.5 times higher speedup gain and 33% energy savings as compared with 3% energy overhead, as reported in [5]. As compared with the adaptive approach in [24], the proposed method exhibits up to 4.9 times increase in performance gain with 50% less energy savings. Alternatively, a 3.85 times higher performance gain is demonstrated as compared to [24] with similar energy savings.

Power overhead per instruction for two-, three-, and four-delay class configurations are also determined for the programs in the LegUp benchmark suite. The average power overhead (due to the additional ML stage and re-execution of misclassified instructions) is shown in Fig. 8. The average power is linearly reduced with the increasing number of program instructions, exhibiting an overhead of less than 0.02 microwatts in practical applications with more than one million instructions. Furthermore, the additional average power consumption rapidly converges for various number of classes, as shown in Fig. 7. Thus, when optimizing the number of delay classes in processors with large workload, power overhead is a secondary factor. Finally, the steeper decrease in the power overhead with the four-class configurations.
configuration supports the previous assertion regarding the gain-overhead tradeoff with finer granularity of delay classes: as the number of instructions increases, the higher accuracy with four-class configuration mitigates the adverse effects of misclassifications on the overall system frequency.

7 CONCLUSIONS AND FUTURE WORK

The proposed unified framework facilitates efficient utilization of the time and hardware recourses in the system. In addition, this approach enables the design of ML pipeline stages, while satisfying design constraints, as shown in Fig. 2. Finally, classification of instructions into delay intervals in real time alleviates the path propagation variances imposed by PVT variations and system aging. To enhance the performance gain, the proposed approach should be preferred with those applications and systems characterized by considerable variations in the propagation delay of the individual instructions.

This method is practical with pipelined, MIPS-like pro-
TABLE 4: Experimental power and energy overhead of the proposed ML method.

| Benchmark | Practical speedup | Power overhead | Energy overhead | Instruction count |
|-----------|------------------|----------------|----------------|------------------|
| rand1M    | 1.923            | 38.5%          | -27.99%        | 1000000          |
| adpcm     | 1.497            | 56.49%         | 4.55%          | 30197            |
| aes       | 2.087            | 45.14%         | -30.46%        | 11223            |
| blowfish  | 1.633            | 65.01%         | 1.02%          | 199759           |
| fft       | 1.165            | 42.43%         | 22.28%         | 11001            |
| fir       | 2.905            | 25.94%         | -56.7%         | 70324            |
| gsm       | 1.382            | 45.77%         | 5.45%          | 2621             |
| jpeg      | 1.792            | 55.04%         | -13.49%        | 1133161          |
| sha       | 1.657            | 62.00%         | -2.22%         | 34557            |
| sra       | 2.840            | 20.62%         | -57.33%        | 1775             |
| Average   | 1.889            | 45.7%          | -15.51%        | 274387           |

Positive standard deviation (σ⁺) = 0.35, 5.81%, 8.70% = 374831.68
Negative standard deviation (σ⁻) = 0.17, 6.58%, 15.50% = 92682.62

TABLE 5: Comparison between the proposed method and existing state-of-the-art methods.

| Algorithm                        | Performance gain | Energy overhead | ML based |
|----------------------------------|------------------|----------------|----------|
| SLot [4]                         | 23%              | N/A            | Yes      |
| Early Prediction [5]             | 20%              | 3%             | No       |
| Clim [14]                        | 24%              | N/A            | Yes      |
| SLBM [16]                       | 15%              | N/A            | Yes      |
| Adaptive Clock Management [24]   | 18.2%            | -30.4%         | No       |
| This work                       | 2 classes        | 70%            | -30%     | Yes      |
|                                  | 3 classes        | 83%            | -28.6%   |         |
|                                  | 4 classes        | 89%            | -15.5%   |         |

multicore systems on performance and energy efficiency in commercial class processors, the following methodologies should be considered.

7.1 Single-Core, Single-Clock Delay-Based Out-of-Order Execution

To support out-of-order execution, instructions within a delay class should be bundled into a delay-class specific reservation station (RS). Instructions stored in an RS are individually executed at a constant frequency until the RS is emptied or a dependency is determined, preventing further execution of instructions in the RS. Such bundling of instructions reduces the number of clock signal transitions among various frequencies, increasing the performance and power efficiency of the system.

7.2 Single-Core, Multi-Clock Delay-Based Out-of-Order Execution

As previously, to support out-of-order execution, instructions should be bundled based on the delay classes and stored within the matching RS’s. To support multi-clock execution, the ALUs and FPUs within the execution unit should be operated at different clock frequencies, as determined by the granularity of the delay classes. Intuitively, the parallelization of execution from different delay classes with this approach decreases the number of clock adjustments, increasing the system performance and energy efficiency.
7.3 Multi-Core, Multi-Clock Delay-Based Out-of-Order Execution

To leverage the advantages provided by processing with multiple clock domains in multicore systems, bundled instructions within the individual clock domains (as defined in subsection 7.1) should be shared among all the system clock domains, mitigating the additional cost of multiple clocking (as described in subsection 7.2). To enable the sharing of bundles, efficient bundle scheduling and low overhead communication channels are required. While the number of clock adjustments is expected to further reduce with this approach, additional overheads due to intelligent communication of bundles among the cores should be considered. Alternatively, by partially or fully replacing the traditional DFS, DVFS, and thread scheduling mechanisms, additional savings are expected with the proposed approach. Finally, the proposed method can be adjusted in a similar manner to classify instruction propagation delay of various pipeline stages.

Existing approaches are focused on offline speculations, statistical models, per-task (workload-based) frequency scaling, and prediction of timing errors at an operating point of a system. Alternatively, the proposed method demonstrates the benefits of fine-grained, instruction-level frequency adjustment, simultaneously utilizing most of the clock period slack and mitigating the adverse effects of PVT variations and aging.

8 SUMMARY

In this work, an additional ML pipeline stage is proposed for increasing the overall system performance by enhancing the temporal resource utilization. This additional stage is designed to classify instructions into propagation delay classes. The system clock frequency is adaptively adjusted based on the individual delay class predictions. Pipelining is exploited to mitigate the effect of the ML stage latency on the overall system performance. Practical ML features are extracted based on current instruction and computation history. ML hardware and misclassification power and delay overheads are considered within the reported results. Tiger-MIPS is utilized as the baseline processor. The processor is enhanced with the ML predictor and simulated with the LegUp benchmark suite. Based on the experimental results, up to 89% performance gain is achieved with four delay classes with 15.5% energy saving. Alternatively, the reduction of 30% in energy consumption with 70% performance gain is demonstrated with two delay classes. A unified shell programing platform with peripheral programs is designed to provide a systematic design flow for ML driven pipelined processors.

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