Interleaved Ultra-High Step-Up DC-DC Converters With Extendable Voltage Gains and ZVS Performance

PARHAM MOHSENI1, MORTEZA DEZHBORD2, MD. RABIUL ISLAM1, (Senior Member, IEEE), WEI XU3, (Senior Member, IEEE), AND KASHEM M. MUTTAQI1, (Senior Member, IEEE)

1School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, NSW 2522, Australia
2Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666, Iran
3State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China

Corresponding author: Wei Xu (weixu@hust.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 51877093, in part by the National Key Research and Development Program of China under Grant 2018YFE0100200, and in part by the Key Technical Innovation Program of Hubei Province under Grant 2019AAA026.

ABSTRACT This paper introduces eight novel interleaved non-isolated dc-dc converters with ultra-high step-up and zero voltage switching (ZVS) capabilities for renewable energy systems. To increase the voltage gain, the proposed converters benefit coupled inductors, high-frequency (HF) transformer, and voltage multiplier (VM) techniques. In comparison to other converters, which just benefit coupled inductors or HF transformers, these combinations of the techniques make an additional degree of freedom to achieve high voltage gains (more than 25 without extreme duty cycle). Besides, two active clamp circuits, including two stages of switch-capacitor VM cells, not only increase the voltage gain of the proposed converters but also act as an auxiliary circuit to provide ZVS. Moreover, the stored energy in the leakage inductances is absorbed and passed to the output by the clamp capacitors. The input current ripple is reduced by applying the interleaved technique. The voltage stresses across the power switches are clamped to lower values and can be controlled by the turn ratios of the coupled inductors and the HF transformer. The theoretical performance of the proposed converters is fully explained. Also, the proposed converters are compared with more than twenty latest interleaved high step-up and ultra-high step-up dc-dc converters. Finally, a 1 kW, 20 V/500 V laboratory prototype is built to prove the advantages of the proposed converters.

INDEX TERMS Interleaved structure, DC-DC converter, ultra-high step-up converter, zero-voltage switching.

I. INTRODUCTION Nowadays, the growing demand for energy from fossil fuels causes air pollution, global warming, and other environmental concerns. These problems motivate research communities to find alternative or clean energy sources. Renewable energy sources such as solar energy and wind energy are the best response to these growing demands. Among different types of renewable energy sources, photovoltaic (PV) energy is one of the most attractive types of clean energy sources [1]–[4]. Usually, the PV array terminal voltage is low. Therefore, high step-up dc-dc converters are commonly used to step-up the PV array voltage to the grid voltage level. Besides, the high step-up dc-dc converters are widely used in many applications such as fuel cells, batteries, servo motors, etc. [5]–[8].

In these applications, in order to increase power sources’ lifetime, input current ripples should be stabled in lower levels. To decrease current ripples, interleaved converters are presented [9]–[13]. In [9] and [10], two simple circuits for interleaved converters are investigated. However, due to the hard switching condition, the efficiencies of these converters are lower than similar converters. The interleaved converter, as presented in [11], uses a high frequency (HF) transformer to provide high voltage gain. In [12] and [13], the combination of coupled inductors with voltage multiplier
cells is utilized to increase the presented converters’ voltage gain. The circuit, as illustrated in [14], is based on coupled inductors, and due to interleaved structure, the input current ripple of this converter is low. Converters in [11]–[14] suffer from high cost and volume. Also, the efficiencies of these converters are low.

In high step-up converters, high frequency provides low volume but increases switching losses. Under high frequencies, switching losses are more elevated and decrease efficiencies of converters [15]–[18]. Therefore, in order to achieve high efficiency with low cost and volume, switching losses should be eliminated or reduced. There are various techniques to minimize switching losses that are classified into three main types: zero voltage switching (ZVS), zero current switching (ZCS), and zero current zero voltage switching (ZCZVS). Presented converters in [19]–[21] use the ZVS technique to decrease switching losses. In these converters, switches turn on under ZVS conditions, but they turn off under hard switching conditions, which provides switching losses. Also, in [20] and [21], the reverse recovery problem of diodes is solved. In [22]–[25], in the presented interleaved converters, switches turn on under ZVS condition, and the reverse recovery problem of diodes is solved, but switches turn off under hard switching conditions. ZVS turn-on condition for switches will be more effective than the ZCS turn-on condition in reducing switching losses. Structures in [26]–[31] can provide a fully soft-switching condition for switches. Also, the reverse recovery problem is eliminated in these converters.

In previous works, some kinds of diode-capacitor voltage multiplier cells have been presented to step up a low voltage to a high output voltage [32]. Figs. 1(a) and 1(b) illustrate one of the diode-capacitor voltage multiplier techniques with AC non-isolated/isolated and DC input voltages, respectively. The diode-capacitor VM techniques have been used in a number of current fed structures as dual-input and single-input interleaved structures [15]–[18]. One of these structures is illustrated in Fig. 1(c). The voltage gain of this kind of converter depends on the number of diode-capacitor VM cells. To increase the converter voltage gain, decrease the voltage stress across the semiconductors, reduce the switching losses, and add another designing freedom degree, an HF transformer is added to the converter and combined with the diode capacitor voltage multiplier stages [22]. The combination method is presented in Fig. 1(d). In the proposed converter in this figure, the power switches turn on under ZCS conditions. In addition to the mentioned techniques, to further increase the converter voltage gain and the designing freedom degrees and decrease the voltage stress across the semiconductors, coupled inductors can be utilized instead of inductors. In this technique, the coupled inductors are combined with the HF transformer and diode-capacitor voltage multiplier cells to provide three designing freedom degrees. By adding two auxiliary switch-capacitor voltage multiplier cells, the leakage inductances of the coupled inductances and HF transformer can be utilized to provide ZVS for the power switches, ZCS for the power diodes, and increase the converter voltage gain significantly.

This paper presents eight new ultra-high step-up interleaved converters with various combinations of coupled inductors, HF transformer, and diode-capacitor VM cells.
In the presented converters, two different auxiliary active switch-capacitor VM circuits are utilized to provide ZVS for all of the power switches. Also, in the proposed converter all of the power diodes turn off and on under ZCS conditions. The presented converters provide three freedom degrees for their designers to work with low-rated semiconductors and provide ultra-high voltage gain with optimum duty cycles. Also, the utilized active auxiliary VM cells act as a clamp circuit to clamp the voltage stresses across the power switches and absorb the leakage inductances' energy to pass it to the output.

In this paper, section 2 describes the eight proposed converters along with different operational modes associated with one of them. Section 3 explains the steady-state analysis. In this section, the voltage gain of one of the proposed converters is calculated. Also, components, turn ratios, and the number of VM stages are designed. Section 4 presents efficiency analysis. In section 5, the control system of the proposed converter is presented. In section 6, the proposed structures are compared with more than twenty related converters. Also, in section 7, in order to validate the theoretical analysis, experimental results of a 1kW laboratory prototype are discussed. Finally, in section 8, a brief conclusion is presented.

II. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLES

The equivalent circuits of the eight presented converters with $M$ number of diode-capacitor VM cells are illustrated in Figs. 2 and 3. The proposed converters are composed of two coupled inductors, an HF transformer, two main power switches, some stages of diode-capacitor VM cells, and two stages of active clamp switch-capacitor VM cells. In these converters, utilizing the active auxiliary switch-capacitor VM stages not only enhances the output voltage but also provides ZVS turn-on for the main power switches.

The turn ratios of the coupled inductors, $n_1 = n_{s1}/n_{p1}$ and $n_2 = n_{s2}/n_{p2}$, and HF transformer, $N = N_{s}/N_{p}$ can be utilized to regulate the output voltage. Besides, the diode-capacitor VM stages are utilized to increase the voltage gain. As a result, the number of used stages depends on the required output voltage. Therefore, the turn ratios $n_1 = n_2 = n$, $N$, and the number of diode-capacitor VM stages $M$ provide three degrees of freedom to the designer, which makes the...
design more flexible. In Figs. 2 and 3, S1 and S2 are the main power of the metal oxide semiconductor field-effect transistors (MOSFETs), and SAux1 and SAux2 are the auxiliary power MOSFETs, C1 and C2 are the clamp capacitors, \( V_{in} \) and \( V_{out} \) are the input and output voltages, respectively, and \( R_{out} \) is the equivalent resistance of the load.

In Figs. 2 and 3, two combination patterns to combine the coupled inductors and the HF transformer with diode-capacitor VM cells are presented. In the first pattern, the secondary sides of the coupled inductors and HF transformer are connected in series. In the second pattern, the secondary sides of the coupled inductors are connected in series with the primary side of the HF transformer. In the secondary side of the HF transformer, VM cells are utilized where the diode and capacitor of the \( j \)th cell are introduced with \( D_j \) and \( C_{VMj} \), respectively. To simplify describing the operational modes, a sample of the proposed converters (the converter presented in Fig. 2(a)) with four stages of diode-capacitor VM cells is selected. The key waveforms of the proposed converter are illustrated in Fig. 4. As illustrated in the figure, the gate signal of each auxiliary switch is the reverse form of its corresponding main switch. This converter has ten operational modes. The equivalent circuits of the proposed converter in different operational modes are shown in Figs. 5. In this figure, \( L_{LK1}, L_{LK2}, \) and \( L_{LK} \) are the leakage inductances of the coupled inductors and HF transformer, \( L_{m1} \) and \( L_{m2} \) are the magnetizing inductances of the coupled inductors.

**Mode 1** \( (t_0 < t < t_1) \) (see Fig. 5(a)): In this mode, both the main power switches \( S_1 \) and \( S_2 \) are in the ON state. Also, all the other semiconductors are in the OFF state. Therefore, it can be written as follows,

\[
i_{LKj}(t) = i_{Lmj}(t) = i_s(j = 1, 2)
\]

\[
i_{LK}(t) = i_{LKj}(t_0) + \frac{V_{in}}{L_{LKj} + L_{mj}}(t - t_0), \quad j = 1, 2
\]  

**Mode 2** \( (t_1 < t < t_2) \) (see Fig. 5(b)): At \( t_1 \), the power switch \( S_2 \) turns OFF. The parallel parasitic capacitors of \( S_2 \) and the auxiliary switch \( S_{Aux2} \) start being charged and discharged by \( i_{Lm2} \), respectively. The main power switch \( S_2 \) turns off with ZVS condition because of the existence of the parallel parasitic capacitor \( C_{S2} \). Due to the small values of parasitic capacitors \( C_{S2} \) and \( C_{SAux2} \), their charging and discharging time is very short, and it can be calculated as,

\[
t_2 - t_1 \approx (C_{S2} + C_{SAux2})(V_{C2} - V_{C1})/i_m(t_1)
\]  

**Mode 3** \( (t_2 < t < t_3) \) (see Fig. 5(c)): At \( t_2 \), the voltage across the auxiliary switch \( S_{Aux2} \) reaches zero, and its anti-parallel body diode starts conducting. Also, the gate to source signal of the auxiliary MOSFET \( S_{Aux2} \) is applied, and this switch turns on when the current direction changes from negative to positive. Therefore, the power switch \( S_{Aux2} \) turns on under ZVS condition. The stored energy in the magnetizing inductance of the second coupled inductor \( L_{m2} \) causes charging in capacitor \( C_2 \) and discharging in capacitor \( C_1 \). The conducting current through the secondary windings of the coupled inductors and transformer starts to charge the even-numbered VM capacitors (\( C_{VM2}, C_{VM4}, \ldots \)) and discharge the odd-numbered VM capacitors (\( C_{VM1}, C_{VM3}, \ldots \)).

The currents through the leakage inductances can be obtained as,

\[
i_{LK1} = i_{Lm1} + n_1(i_{D2} + i_{D4})
\]  

\[
i_{LK2} = i_{Lm2} - n_2(i_{D2} + i_{D4}) = -i_{SAux2} - N(i_{D2} + i_{D4})
\]  

\[
i_{LK} = -N(i_{D2} + i_{D4})
\]  

**Mode 4** \( (t_3 < t < t_4) \) (see Fig. 5(d)): At \( t_3 \), the auxiliary power switch \( S_{Aux2} \) turns off. The currents value \( i_{LK1} \) and \( i_{LK2} \) start to decrease and increase, respectively. The current which flows through the secondary side windings starts to decrease to zero. The negative value of the current \( i_{LK} \) is more than the positive value of \( i_{L2} \). Therefore, parasitic capacitors \( C_{S2} \) and \( C_{SAux2} \) start being discharged to zero and being charged to \( V_{C2} - V_{C1} \), respectively. As a result, due to the existence of \( C_{SAux2} \), ZVS turn-off for the power MOSFET \( S_{Aux2} \) is achievable. The duration of this mode can be achieved as,

\[
t_4 - t_3 \approx (C_{S2} + C_{SAux2})(V_{C2} - V_{C1})/i_{LK}(t_3) - i_{LK2}(t_3)
\]  

**Mode 5** \( (t_4 < t < t_5) \) (see Fig. 5(e)): At \( t_4 \), the voltage across the power switch \( S_2 \) reaches zero, and its anti-parallel body diode starts conducting. The currents through the secondary side windings and VM diodes continue decreasing to zero. In order to realize the ZVS turn-on for \( S_2 \), its gate signal should be applied in this mode.

**Mode 6** \( (t_5 < t < t_6) \) (see Fig. 5(f)): At \( t_5 \), the power switch \( S_2 \) turns on under ZVS condition because its parallel body diode has been conducted before. Also, all the other semiconductors are in the OFF state.

**Mode 7** \( (t_6 < t < t_7) \) (see Fig. 5(g)): At \( t_6 \), the power switch \( S_1 \) turns off. The parallel parasitic capacitors of the main switch \( S_1 \) and the auxiliary switch \( S_{Aux1} \) start to be
charged and be discharged by \( i_{Lm1} \), respectively. The main power switch \( S_1 \) turns off under ZVS condition, because of the existence of the parallel parasitic capacitor \( C_{S1} \).

Due to the small values of capacitors \( C_{S1} \) and \( C_{SAux1} \), their charging and discharging duration is very short, and it can be obtained as,

\[
t_7 - t_6 \approx \frac{(C_{S1} + C_{SAux1}) V_{C1}}{i_{Lm2}} (t_6) \tag{7}
\]

**Mode 8 \( t_7 < t < t_8 \) (see Fig. 5(h)):** At \( t_7 \), the voltage across the main switch \( S_1 \) reaches \( V_{C1} \), which causes the conduction of the anti-parallel body diode of the auxiliary switch \( S_{Aux1} \). Also, the gate to source signal of the MOSFET \( S_{Aux1} \) is applied, and it starts to conduct when its current direction changes from negative to positive. Therefore, the power switch \( S_{Aux1} \) turns on under ZVS condition. The stored energy in the magnetizing inductance of the first coupled inductor \( L_{m1} \) charges the capacitor \( C_{1} \). The conducting current through the secondary windings of the coupled inductors and the transformer starts to charge the odd-numbered VM capacitors \( (C_{VM1}, C_{VM3}, \ldots) \) and discharge the even-numbered VM capacitors \( (C_{VM2}, C_{VM4}, \ldots) \) through the odd-numbered diodes \( (D_1, D_3, \ldots) \), respectively. The current through the leakage inductance can be achieved as,

\[
i_{LK1} = n_1 (i_{D1} + i_{D3}) \tag{8}
\]

\[
i_{LK2} = n_2 (i_{D1} + i_{D3}) = n (i_{D1} + i_{D3}) - i_{SAux1} \tag{9}
\]

\[
i_{LK} = N (i_{D1} + i_{D3}) \tag{10}
\]
**Mode 9** \((t_S < t < t_9)\) (see Fig. 5(i)): At \(t_S\), \(S_{Aux1}\) turns off. The currents value \(i_{Lk1}\) and \(i_{Lk2}\) start to increase and decrease, respectively. The current that flows through the secondary side windings starts to decrease to zero. Also, the positive value of the current \(i_{Lk}\) is more than the negative value of the current \(i_{Lk}^{−}\). As a result, the parasitic capacitors \(C_S1\) and \(C_{Aux1}\) start to discharge to zero and charge to \(V_{C1}\), respectively. Therefore, the existence of \(C_{Aux1}\) provides ZVS conditions for the power MOSFET \(S_{Aux1}\). The duration of this mode can be expressed as follows:

\[
t_0 − t_8 \approx \frac{(C_{S1} + C_{Aux1}) V_{C1}}{(i_{Lk}^{−} (t_0) − i_{Lk} (t_0))} \tag{11}
\]

**Mode 10** \((t_9 < t < t_{10})\) (see Fig. 5(j)): At \(t_0\), the voltage across \(S_1\) reaches zero and its anti-parallel body diode starts conducting. The currents through the secondary side windings and VM diodes continue decreasing to zero. In order to achieve the ZVS turn-on for \(S_1\), its gate signal should be applied in this mode. At \(t_{10}\), \(S_1\) turns on, and the converter’s operational cycle is repeated.

### III. STEADY-STATE OF THE PRESENTED CONVERTER

To simplify the analysis, the short time intervals \((t_1 − t_2, t_3 − t_5, t_6 − t_7, \text{ and } t_8 − t_{10})\) and the leakage inductances of the coupled inductors and HF transformer are neglected. Also, it is assumed that all the passive elements and switches are ideal, and the voltages of the capacitors are constant during a switching cycle.

#### A. POWER DRIVER TOPOLOGY

By using the volt-second balance law for the magnetizing inductances \(L_{m1}\) and \(L_{m2}\), these relations can be achieved as,

\[
V_{C1} = V_{in}/(1 − d) \tag{12}
\]

\[
V_{C2} − V_{C1} = V_{in}/(1 − d) \tag{13}
\]

\[
V_{CVM1} = V_{CVM3} − V_{CVM2} = (N + n) V_{in}/(1 − d) \tag{14}
\]

\[
V_{CVM2} − V_{CVM1} = V_{CVM4} − V_{CVM3} = (N + n) V_{in}/(1 − d) \tag{15}
\]

where \(d\) is the duty cycle of the main power switches \(S_1\) and \(S_2\).

By utilizing (12-15), the voltages across the VM capacitors are achieved as,

\[
V_{C2} = 2V_{in}/(1 − d) \tag{16}
\]

\[
\begin{align*}
V_{CVM2} &= (2NV_{in})/(1 − d) + (2mV_{in})/(1 − d) \\
V_{CVM1} &= (2NV_{in})/(1 − d) + (3mV_{in})/(1 − d) \\
V_{CVM4} &= (4NV_{in})/(1 − d) + (4mV_{in})/(1 − d)
\end{align*} \tag{17}
\]

The output voltage is the summation of the voltages across the capacitors \(C_2\) and \(C_{VM4}\). Therefore, the output voltage is obtained as,

\[
V_{out} = (2 + 4(N + n)) V_{in}/(1 − d) \tag{18}
\]

The above analysis can be extended to a converter with \(M\) stages of diode-capacitor VM cells. Therefore, the output voltage of the proposed converter with \(M\) stages of VM cells can be expressed as,

\[
V_{out} = ((2 + M(N + n)) V_{in})/(1 − d) \tag{19}
\]

The voltage gain of the converter presented in Fig. 2(b) can be calculated by the method presented in (12-18). Therefore, the voltage gain of the converter is obtained as,

\[
V_{out} = ((2 + N(1 + n)M) V_{in})/(1 − d) \tag{20}
\]

With regards to (19) and (20), it can be concluded that the voltage gains of the proposed converters depend on the turn ratios of the coupled inductors and HF transformer and diode-capacitor VM stages. Therefore, \(n, N,\) and \(M\) are the three variables that make the design of these converters more flexible.

In (18), the obtained voltage gain is ideal, and the actual voltage gain is slightly smaller than (18). In fact, the leakage inductances and transformer cause the duty cycle losses that reduce the voltage gain. Therefore, the precise voltage gain of the proposed converter with four stages of diode-capacitor VM cells can be expressed as,

\[
\frac{V_{out}}{V_{in}} = \frac{2+4(n+N)}{1−d} F \left[\frac{n^2(L_{LK1} + L_{LK2}) + N^2L_{Lk}}{R_{out}(1−d)\sqrt{\left(\frac{2+4(n+N)}{1−d}\right)^2 - \frac{4V_{CM}}{(I_{out} L_{m1} f S)^2}}\right] \tag{21}
\]

### B. REALIZATION OF ZVS CONDITION FOR POWER MOSFETS

Due to the presence of parallel parasitic capacitors, the power MOSFETs turn off under near to soft conditions. The ZVS turn-on for the auxiliary power MOSFETs \(S_{Aux1}\) and \(S_{Aux2}\) are naturally realized due to the conduction of their anti-parallel body diodes. In order to ensure ZVS turn-on for the main power MOSFETs \(S_1\) and \(S_2\), the stored energy in the equivalent leakage inductance \((L_{LKj} L_{Lk})/(L_{LK} + L_{Lk})\), which charges or discharges the parasitic capacitors \(C_{Sj}\) and \(C_{S_{Aux}j}\), should be more than the stored energy in the parallel parasitic capacitors. Therefore, this relation can be achieved:

\[
\frac{L_{LkJ} L_{Lk}}{L_{LK} + L_{Lk}} \geq \frac{4(C_{Sj} + C_{S_{Aux}j}) V_{CM}^2}{(2+4(n+N)) \frac{V_{CM}^2}{(1−d)^2} - \frac{4V_{CM}}{(I_{out} L_{m1} f S)^2}} \quad j = \{1, 2\} \tag{22}
\]

### C. MAGNETIZING COMPONENTS DESIGN

To provide the required conditions for the proposed converter to operate in continuous conduction mode (CCM), the average currents of the magnetizing inductances of the coupled inductors should be more than their half current ripple. The average currents of the magnetizing inductances of the coupled inductors for \(M\) stages of VM cells are achieved as,

\[
I_{Ln_1} = (2 + (M + 1) (n + N)) I_{out}/2(1−d), \quad i = \{1, 2\}
\]

If \(M\) is even

\[
\begin{align*}
I_{Ln1} &= (2 + (M + 1) (n + N)) I_{out}/2(1−d) \\
I_{Ln2} &= (2 + (M - 1) (n + N)) I_{out}/2(1−d)
\end{align*} \tag{23}
\]

If \(M\) is odd

\[
\begin{align*}
I_{Ln1} &= (2 + (M + 1) (n + N)) I_{out}/2(1−d) \\
I_{Ln2} &= (2 + (M - 1) (n + N)) I_{out}/2(1−d)
\end{align*} \tag{24}
\]
The current ripple of the magnetizing inductances is given by:

\[
\Delta i_{Lm_j} = \frac{dV_{in}}{L_{mj}f_S}, \quad j = \{1, 2\} \tag{25}
\]

Therefore, the critical values of the magnetizing inductances to ensure the CCM operation can be obtained as,

\[
\begin{align*}
L_{m1} = L_{m2} &\geq d(1-d)^2R_{out}/[2 + M(n+N)]^2 f_S \\
\text{if } M \text{ is even} \\
L_{m1} \geq d(1-d)^2R_{out}/[2 + (M+1)(n+N)]^2 f_S \\
L_{m2} \geq d(1-d)^2R_{out}/[2 + (M-1)(n+N)]^2 f_S \\
\text{if } M \text{ is odd}
\end{align*}
\tag{26}
\]

In the third operational mode, when \(S_1\) is in on state and \(S_2\) is in off state, the voltage across the primary winding of the HF transformer is expressed as,

\[
V_{p-\text{Trans}} = V_{in}/(1-d) = N_p\Delta BA_e/((1-d)T) \tag{28}
\]

where \(\Delta B\) is the magnetic flux density variation and \(A_e\) is the magnetic core equivalent area. The primary and secondary windings turns can be selected based on the proper transformer designing guidelines. The current through the secondary side of the transformer is the summation of the currents which flow through the diodes. Therefore, the RMS current value of the secondary winding is expressed as,

\[
i_{\text{RMS-Trans}}^{\text{Secondary}} = I_{out}M\sqrt{2(1-d)/2(1-d)} \quad \text{If } M \text{ is even}
\tag{29}
\]

\[
i_{\text{RMS-Trans}}^{\text{Secondary}} = I_{out}\sqrt{0.5(M^2 + 1)(1-d)/(1-d)} \quad \text{if } M \text{ is odd}
\tag{30}
\]

The RMS value of the primary winding’s current is equal to \(N \times i_{\text{RMS-Trans}}^{\text{Secondary}}\). According to (29) and (30), the diameters of the primary and secondary windings of the HF transformer can be obtained. Furthermore, the RMS voltage across the primary winding of the transformer can be expressed as,

\[
V_{\text{RMS-Trans}}^{\text{Primary}} = V_{in}\sqrt{2(1-d)/(1-d)} \tag{31}
\]

The apparent power of the HF transformer can be obtained by multiplying its primary winding RMS voltage and current.

**D. SEMICONDUCTORS DESIGN**

To select proper power semiconductors for the proposed converter, their voltage and current stresses should be calculated. In the proposed converter with \(M\) stages of diode-capacitor VM cells, the voltage stresses on the power semiconductors are obtained as,

\[
\begin{align*}
V_{S1} &= V_{S2} = V_{S\text{Aux2}} = V_{in}/(1-d) \\
V_{S\text{Aux1}} &= 2V_{in}/(1-d) \\
V_D &= V_{D2} = \cdots = V_{DM} \\
&= \frac{2(n+N)V_{in}}{1-d} = \frac{2(n+N)V_{out}}{2 + M(n+N)}
\end{align*}
\tag{32}
\]

Also, the voltage stress across the semiconductors for the presented converter in Fig. 2(b) can be expressed as,

\[
\begin{align*}
V_{S1} &= V_{S2} = V_{S\text{Aux2}} = V_{in}/(1-d) \\
&= V_{out}/((2 + N(1+n)M)) \\
V_{S\text{Aux1}} &= 2V_{in}/(1-d) \\
&= 2V_{out}/((2 + N(1+n)M)) \\
V_D &= V_{D2} = \cdots = V_{DM} \\
&= \frac{2(n+N)V_{in}}{1-d} = \frac{2(n+N)V_{out}}{(2 + N(1+n)M)}
\end{align*}
\tag{35}
\]

The average currents of the power MOSFETs are given by:

\[
\begin{align*}
I_{S1}^{\text{Avg}} &= \frac{2d + M(n+N)}{2(1-d)}I_{out}, \quad I_{S\text{Aux1}}^{\text{Avg}} = -I_{out} \\
I_{S2}^{\text{Avg}} &= \frac{2 + M(n+N)}{2(1-d)}I_{out}, \quad I_{S\text{Aux2}}^{\text{Avg}} = -I_{out}
\end{align*}
\tag{38}
\]

If \(M\) is even

\[
\begin{align*}
I_{S1}^{\text{Avg}} &= \frac{2d + (M+1)(n+N)}{2(1-d)}I_{out}, \\
I_{S\text{Aux1}}^{\text{Avg}} &= -I_{out} \\
I_{S2}^{\text{Avg}} &= \frac{2 + (M+1)(n+N)}{2(1-d)}I_{out}, \\
I_{S\text{Aux2}}^{\text{Avg}} &= -I_{out}
\end{align*}
\tag{39}
\]

If \(M\) is odd

The current stresses of the power diodes are given by:

\[
I_{D1}^{\text{Max}} = I_{D2}^{\text{Max}} = \cdots = I_{DM}^{\text{Max}} = 2I_{out}/(1-d) \tag{40}
\]

**E. TURN RATIOS AND NUMBER OF VM STAGE**

By determining the output voltage and proper duty cycle of the power switches, the values of \(n\), \(N\), and \(M\) can be achieved. As mentioned before, the voltage stress on the power diodes decreases by increasing the number of diode-capacitor VM cells. Therefore, the number of VM cells is selected based on the peak inverse voltage \(V_{D\text{Max}}\) of the available diodes. The number of diode-capacitor stages can be determined as,

\[
M \geq (2(n+N)V_{out} - 2V_{D\text{Max}})/(n+N)V_{D\text{Max}}) \tag{41}
\]

The voltage stresses of the power switches decrease by increasing the turn ratios \(n\) and \(N\). The turn ratio of the coupled inductors \(n\) can be determined based on the voltage stress across the power MOSFETs \(S_1, S_2,\) and \(S_{\text{Aux2}}\) as,

\[
n \geq \left(\frac{V_{out} - 2V_{DM}}{MV_{DM}}\right) - N \
\tag{42}
\]

In (42), \(V_{DM}\) is the peak inverse voltage of the selected power MOSFETs for \(S_1, S_2,\) and \(S_{\text{Aux2}}\).

The turn ratio of the HF transformer can be obtained based on the voltage stress across the auxiliary power MOSFET \(S_{\text{Aux1}}\) as follows:

\[
n \geq \left(\frac{2V_{out} - 2V_{\text{Aux}}}{MV_{\text{Aux}}}\right) - n \
\tag{43}
\]
where \( V_{\text{DS max}} \) is the peak inverse voltage of the selected power MOSFET for \( S_{\text{aux1}} \). Therefore, the selected \( n, N, \) and \( M \) should confirm the obtained values from (41-43).

**F. CAPACITORS DESIGN**

The capacitor values can be designed based on their voltage ripple. Therefore, the values of the capacitors can be determined as,

\[
C_2 = C_{VM4} = C_{VM-M} = \frac{dV_{out}}{\Delta V_{Cout} R_{out} f_S} \quad (44)
\]

\[
C_1 = C_{VM1} = C_{VM2} = \cdots = C_{VM-(M-1)} = \frac{V_{out}}{\Delta V_{Cout} R_{out} f_S} \quad (45)
\]

**IV. EFFICIENCY ANALYSIS**

The efficiency of the proposed converter is calculated by considering the parasitic resistances of different elements. Primary and secondary equivalent series resistances (ESR) of the coupled inductors (primary \( r_{lp1} \) and secondary \( r_{ls1} \)) and HF transformer (primary \( r_{lp2} \) and secondary \( r_{ls2} \)), conductive resistances of the power MOSFETs \( r_{DS} \) and diodes \( r_{DC} \), the forward voltage of diodes \( V_F \), and ESRs of the capacitors \( r_c \) are considered to calculate the efficiency of the proposed converter. To simplify the efficiency calculations, the component’s conduction currents are approximated by their average values. Also, the effects of the leakage inductances and the short time intervals \((t_1 - t_2, t_3 - t_5, t_6 - t_7, \) and \( t_8 - t_{10} \)) are ignored. Therefore, considering the parasitic values, the output voltage can be achieved as,

\[
M = \frac{V_{out}}{V_{in}} = \frac{2 + 4(n + N) 1 - (4(1-d)V_F) / ((2 + 4(n + N))V_{in})}{1 + \alpha + \beta + \gamma + \lambda} \quad (46)
\]

where \( \alpha, \gamma, \beta, \) and \( \lambda \) can be expressed as (47), as shown at the bottom of the page.

The core losses of the magnetic cores are constant and directly depend on the converter switching frequency. Therefore, the core losses should be considered at high frequencies. The core losses for each magnetic core is obtained 3.34 W from its datasheet at 100 kHz switching frequency. As a result, the total core losses at 138 kHz switching frequency is equal to PCore = 13.83 W. Therefore, the theoretical efficiency of the sample proposed converter can be calculated as (48), as shown at the bottom of the next page.

With regards to (46-48), it can be concluded that if the input voltage is considerably higher than the summation of the forward voltages of the VM diodes or the equivalent resistance of the load \( R_{out} \) is significantly larger than the combined parasitic resistance of the components, the efficiency and voltage gain of the proposed converter would be high. Fig. 6 shows the voltage gain and efficiency of the proposed converter with different ESRs of the coupled inductors and the HF transformer versus different duty cycles. (Vout = 500 V and Pout = 1 kW).

![FIGURE 6. Calculated efficiency and voltage gain of the proposed converter with various ESRs of the coupled inductors and the HF transformer versus different duty cycles. (Vout = 500 V and Pout = 1 kW.)](image)
V. CONTROL SYSTEM OF THE PROPOSED CONVERTER

For the proposed converters, the pole placement control method can be a proper method to control the output DC voltage. This control method is completely explained in [2], [4], [13], and [22]. This control method deals with state variables directly to design the control compensators. Therefore, it can be a proper control method in power switching converters because in this kind of converters, state variables are accessible. The control circuit schematic of the mentioned control system is shown in Fig. 7(a). In this figure, $K_x$ and $K_q$ are the control coefficient matrixes of the control system. The closed-loop poles of the desired control system should be determined to reach the optimum phase margin (PM) and gain margin (GM) ($60^\circ \leq PM \leq 80^\circ$ and $GM \geq 10$) in its closed-loop control path. The bode plots of the single-input-single-output system after and before implementing the control system are shown in Fig. 7(b). As it can be seen in the figure, the phase margins of the closed-loop system before and after implementing the control system are obtained 0.188$^\circ$ and 67$^\circ$, respectively. This means that the PM and GM of the control system are in their optimum areas.

VI. COMPARISON STUDY OF THE PROPOSED CONVERTERS

To prove the advantages of the proposed converters, the performances of the selected proposed circuits (Converters presented in Figs. 2(a) and 2(b)) are compared to five recently presented interleaved ultra-high step-up and high step-up topologies, and their results are tabulated in Table 2. The voltage gain comparison versus various turn ratios ($n_1 = n_2 = N = n$) is demonstrated in Fig. 8(a). It is clear that the proposed converters with four number of VM stages $M = 3$ can provide significantly higher voltage gain than the ultra-high step-up and high step-up converters.

The voltage stress comparisons of the power switches and power diodes are presented in Figs. 8(b) and 8(c). Considering these figures, it can be concluded that in the proposed converters, the voltage stresses across the power switches are significantly lower than other compared structures. Also, it is clear in Fig. 8(c) that the normalized voltage stress across the power diodes is low, even lower than 0.5 for $M = 4$.

In comparison to the converters presented in [5] and [24], which are benefited from coupled inductors, HF transformer, and diode-capacitor voltage multiplier techniques, the proposed converters can provide higher voltage gains and lower voltage stresses across the semiconductors with a lower number of components. Also, the proposed converters can provide ZVS for all of the power switches and ZCS for all the power diodes, which cannot be realized in the presented converters in [5] and [24]. Moreover, in the proposed converters the active clamp auxiliary VM circuits provide ZVS condition, enhance the converters’ voltage gain considerably, and clamp the voltage spikes across the power switches. Where in the converters presented in [5] and [24], the mentioned multi-function of the clamp circuits is not realized. Also, the proposed converters provide three designing freedom degrees $n$, $N$, and $M$ for their designer to

\[
\eta = \frac{P_{av}}{P_{tot}} = \frac{P_{out}}{P_{out} + V_{out} (1 - d) V_F / R_{out} + V_{out}^2 (\alpha + \beta + \gamma + \lambda) / R_{out} + P_{Cor}}
\]
TABLE 2. Comparison between the proposed converter and other presented converters in the references.

| Converter | Voltage Gain | Normalized voltage stress on switches | Normalized Max. voltage on diodes | Number of | Soft Switching of | Soft Switching of | Efficiency at output power |
|-----------|--------------|--------------------------------------|-----------------------------------|-----------|-------------------|-------------------------|---------------------------|
|           |              | normalized voltage on diodes |                                   | \(W_{1*}\) | \(M_{C^*}\) | \(S_{*}\) | \(D_{*}\) | \(C_{*}\) | \(T. D_{*}\) | Side |
| [5]       | \[(2+4n)/(1-d)\] | \(1/(2+4n)\) | \((2n+1)/(2+4n)\) | 7 | 3 | 2 | 8 | 7 | 20 | Hard | Hard | 96% at 1kW |
| [24]      | \[(2+3n)/(1-d)\] | \(1/(2+3n)\) | \((1+3n)/(2+3n)\) | 7 | 3 | 2 | 6 | 5 | 16 | ZCS by \(L_{X}\) | ZCS | 97% at 1kW |
| [27]      | \[(4+2n)/(1-d)\] | \(1/(4+2n)\) | \((n+1)/(n+2)\) | 6 | 2 | 3 | 6 | 4 | 15 | ZVS | ZCS | 96% at 200W |
| [21]      | \[(4n)/(1-d)\] | \(1/4n\) | 1/2 | 5 | 4 | 6 | 2 | 5 | 17 | ZVS | ZCS | 95% at 500W |
| [30]      | \[(2+2n)/(1-d)\] | \(1/(2+2n)\) | \((1+2n)/(2+2n)\) | 8 | 4 | 4 | 6 | 9 | 23 | ZVS | ZCS | 95.5 at 1kW |
| Prop.*    | \((2+(n-n^2)M)/(1-d)\) | \(1/(2+(n-n^2)M)\) | \(4n(2+2nM)\) | 6 | 3 | 4 | \(M+2\) | \(M+2\) | \(2M+9\) | ZVS | ZCS | 96.32% at 1kW |

TABLE 3. Comparison results of the eight proposed converters with each other.

| Converter | Voltage gain | Normalized total voltage across capacitors | Same ground | Flexibility in the design of number of diode-capacitor VM cells (M) |
|-----------|--------------|------------------------------------------|-------------|---------------------------------------------------------------|
| Fig.2(a)  | \((2+2nM)/(1-d)\) | \((3+2nM (M+1))/(2+2nM)\) | Yes | Both even and odd |
| Fig.2(b)  | \((2+2nM (n+n)^2)/(1-d)\) | \((3+n(n+n)^2)(M+1))/(2+2nM)\) | Yes | Both even and odd |
| Fig.2(c)  | \((2+2nM)/(1-d)\) | \((2+2nM (M+1))/(2+2nM)\) | No | Both even and odd |
| Fig.2(d)  | \((2+2nM (n+n)^2)/(1-d)\) | \((2+n(n+n)^2)(M+1))/(2+2nM)\) | No | Both even and odd |
| Fig.3(a)  | \((2+2nM)/(1-d)\) | \((6+nM (M+2))/(2+2nM)\) | Yes | Just even |
| Fig.3(b)  | \((2+2nM (n+n)^2)/(1-d)\) | \((12+2(n+n)^2)(M+2))/(4+2(n+n)^2)(M)\) | Yes | Just even |
| Fig.3(c)  | \((2+2nM)/(1-d)\) | \((4+nM (M+2))/(2+2nM)\) | No | Just even |
| Fig.3(d)  | \((2+2nM (n+n)^2)/(1-d)\) | \((8+2(n+n)^2)(M+2))/(4+2(n+n)^2)(M)\) | No | Just even |

The comparison results of the eight proposed converters are summarized in Table 3. Although the voltage gain of the presented converter in Fig. 2(a) is significantly high, it can be increased just by utilizing the second pattern of the coupled inductors and the HF transformer combination. Also, utilizing this combination pattern reduces the voltage stress across the power switches considerably. Besides, the voltage stress across the capacitors can be decreased significantly just by using the second pattern of diode-capacitor VM cells (Figs. 3(a)-3(d)) instead of the first pattern of VM cells (Figs. 2(a)-2(d)). But on the other hand, just an even number of diode-capacitor VM cells can be utilized with the second pattern of diode-capacitor VM cells. Therefore, the design flexibility of the number of VM stages work with low-rated semiconductors at optimum duty cycles. Whereas in the presented converters in [5] and [24], only two designing freedom degrees \(n\) and \(N\) are provided. Consequently, in the proposed converters, the ultra-high voltage gain, optimum efficiency and cost are achievable by selecting the appropriate turn-ratios \(n\) and \(N\), the number of diode-capacitor VM cells \(M\), and the duty cycle.

The comparison results of the eight proposed converters with each other are summarized in Table 3. Although the voltage gain of the presented converter in Fig. 2(a) is significantly high, it can be increased just by utilizing the second pattern of the coupled inductors and the HF transformer combination. Also, utilizing this combination pattern reduces the voltage stress across the power switches considerably. Besides, the voltage stress across the capacitors can be decreased significantly just by using the second pattern of diode-capacitor VM cells (Figs. 3(a)-3(d)) instead of the first pattern of VM cells (Figs. 2(a)-2(d)). But on the other hand, just an even number of diode-capacitor VM cells can be utilized with the second pattern of diode-capacitor VM cells. Therefore, the design flexibility of the number of VM stages \(M\) will be limited to even values. Furthermore, the voltage stress across the clamp capacitors can be decreased by using the second pattern of auxiliary circuit (Figs. 2(c), 2(d), 3(c), and 3(d)). But this pattern separates the input ground port from the output port.

TABLE 4. Hardware prototype specification.

| Components | Values |
|------------|--------|
| Input and Output Voltages \((V_{in}, V_{out})\) | \(V_{in}=20V\), \(V_{out}=500V\) |
| Output Power \((P_{out})\) | \(1kW\) |
| Switching Frequency \((f_{s})\) | \(138 kHz\) |
| Duty Cycle \((d)\) | 0.66 |
| Coupled Inductors and High-frequency Transformer | \(L_{m1}=L_{m2}=50\mu H\), Turn ratios \(n=n=1\) |
| Power Switches \((S_{1}, S_{2}, S_{M1}, S_{M2})\) | IRFP4668PBF |
| Power Diodes \((D_{1}, D_{2}, D_{3}, \text{and} D_{4})\) | SBR10U300CT |
| Voltage Multiplier Capacitors \((C_{V1}, C_{V2}, C_{V3}, \text{and} C_{V4})\) | \(C_{V1}, C_{V2}, C_{V3}, C_{V4}=33 \mu F, 400V\) |
| Clamped Capacitors \((C_{1}, C_{2})\) | \(C_{1}: 33 \mu F, 400V, C_{2}: 100 \mu F, 200V\) |
FIGURE 8. Comparison results of the proposed converter with other related structures.

FIGURE 9. Experimental results at 1 kW output power: (a) Voltage and current waveforms of the main switch $S_1$ (along with zoomed turn-off moment), and (b) Voltage and current waveforms of the main switch $S_2$ (along with zoomed turn-off moment).

VII. EXPERIMENTAL RESULTS

In this section, in order to validate the theoretical analysis, a 1 kW laboratory prototype of the sample proposed converter is built. The parameters of the test converter are tabulated in Table 4. Also, the experimental results of this laboratory prototype are illustrated and analyzed completely.

Figs. 9-13 illustrate the experimental results of the proposed converter at 1kW output power. Table 5 compares the calculated voltage values with experimentally measured values. Figs. 9(a) and 9(b) show the voltage and current waveforms of the main power switches $S_1$ and $S_2$. As it can be seen, before the turn-on moment of these switches, their anti-parallel diodes conduct negative currents. Consequently, these switches turn on under ZVS conditions. At the turn-off moment, the parallel capacitors of the power switches get charged, and the switches’ voltages increase with a mild slope. Therefore, a soft-switching condition is provided for switches’ turn-off. Figs. 10(a) and 10(b) illustrate the voltage and current waveforms of the auxiliary power switches $S_{AUX1}$.
and \( S_{AUX2} \). Similar to the main switches, auxiliary switches turn on under ZVS conditions by discharging their parallel capacitors and conducting their anti-parallel diodes. Also, due to charging of their parallel capacitors with mild slopes, the soft-switching condition is provided for the auxiliary switches’ turn-off.

The experimental voltage and current waveforms of the VM diodes \( D_3 \) and \( D_4 \) are illustrated in Figs. 11(a) and 11(b). As it can be observed, the VM diodes turn on under ZCS condition, and their current falling rates are controlled by the equivalent leakage inductance of the coupled inductors and HF transformer. Therefore, the reverse recovery losses are decreased significantly. Figs. 12(a) and 12(b) show the current waveforms of the leakage inductances of HF transformer (\( i_{Lk} \)) and coupled inductors (\( i_{Lk1} \) and \( i_{Lk2} \)), respectively. From 13(b), it can be seen that the currents \( i_{Lk1} \) and \( i_{Lk2} \) have reverse changes that reduce the input current ripple noticeably.

Fig. 13(a) illustrates the input current and the voltage waveform of the capacitor \( C_2 \). As can be seen, due to the reverse changes of leakage inductances’ current, the input current ripple is very low. Also, the capacitor \( C_2 \) has an almost constant voltage that provides a constant dc voltage in output. Fig. 13(a) shows the input and output voltages. From this figure, it can be seen that when the duty cycle and the input voltage are 66% and 20 V, respectively, the proposed converter can provide 500 V output voltage. Finally, it can be concluded that the experimental results confirm the theoretical analysis.

The experimental and theoretical efficiencies of the proposed converter versus different output powers (0.2 kW-1 kW) with a 20 V input voltage are illustrated in Fig. 14. As can be seen, the maximum efficiency is measured 96.41% at 700 W output power. The experimental efficiency of the laboratory prototype is obtained 96.32% at 1000 W output power which is 0.76% lower than the calculated value (97.08%).

### VIII. CONCLUSION

In this paper, eight interleaved ultra-high step-up dc-dc converters with ZVS performance are proposed. A detailed steady-state analysis, comparison study, and experimental results of one of the interleaved ultra-high step-up dc-dc converters are presented to verify the following features of the proposed converters:

1. The number of diode-capacitor VM cells \( M \), turn ratios of the coupled inductors \( n \) and the HF transformer \( N \) are three designing degrees of freedom to extend the voltage gain for operating with optimum duty cycles and work with low rated semiconductors at high voltage gains.

2. The active auxiliary switch-capacitor ZVS circuit is implemented not only to provide ZVS conditions for the main power switches \( S_1 \) and \( S_2 \) but also to clamp the voltage spikes across the power switches and increase the voltage gain.

3. The voltage stresses across the power switches are low and can be lower by increasing the number of the diode-capacitor VM stages \( M \) and turn ratios \( n \) and \( N \). Therefore, MOSFETs with low conducting resistance can be adopted, which decreases the conduction losses and cost.

4. The ZVS performance is achieved for the power switches, and the reverse recovery losses of the power diodes are reduced.

5. Utilizing coupled inductors instead of inductors leads to optimum utilization of cores which improves the power density.

6. According to (26) and (27), the magnetizing inductances of the coupled inductors are reduced to ensure the CCM operation by simultaneous implementation of the HF transformer and coupled inductors. Therefore, the coupled inductors’ core volume is reduced.

7. Recycling the stored energy in the leakage inductances and passing it to the output, which helps to achieve high efficiency.

8. Simple control and triggering the gate signals like the conventional interleaved converter.

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| Table 5. Comparison of the calculated and measured voltages. |
|-----------------|-----------------|-----------------|-----------------|
| Output voltage \((V_{\text{mea}})\) | Calculated | Equation | Measured |
|-----------------|-----------------|-----------------|-----------------|
| Voltage stress across switches \(V_{S1} \) and \(V_{S2} \) | 58.8 V | (32) | 55 V |
| Voltage stress across the auxiliary switches \(V_{D/E AUX1}, V_{D/E AUX2} \) | 117.6 V | (33) | 110 V |
| Voltage stress across the capacitor \(C_2 \) | 235.3 V | (34) | 195 V |
| Voltage stress across the capacitor \(C_2 \) | 117.6 V | (16) | 110 V |

**FIGURE 14.** The experimental and theoretical efficiencies at different output powers.
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MD. RABIUL ISLAM (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Technology Sydney (UTS), Sydney, Australia, in 2014.

He was appointed as a Lecturer at RUET, in 2005, and promoted to a Full Professor, in 2017. In early 2018, he joined the School of Electrical, Computer and Telecommunications Engineering (SECTE), University of Wollongong (UOW), Wollongong, Australia. He has received several funding from government and industries, including in total $5.48 million from the Australian Government through the Australian Research Council (ARC) Discovery Project (DP) 2020 entitled “A Next Generation Smart Solid-State Transformer for Power Grid Applications” and the ARC Industrial Transformation Training Centre Project 2021 entitled “ARC Training Centre in Energy Technologies for Future Grids.” He has authored or coauthored more than 250 articles, including 77 IEEE TRANSACTIONS/IEEE journal articles. He has written or edited five technical books published by Springer and Taylor & Francis. His research interests include in the fields of power electronic converters, renewable energy technologies, power quality, electrical machines, electric vehicles, and smart grid. He has received several best paper awards, including two Best Paper recognitions from IEEE TRANSACTIONS ON ENERGY CONVERSION, in 2020. He has served as a Guest Editor for IEEE TRANSACTIONS ON ENERGY CONVERSION, IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, and IET ELECTRIC POWER APPLICATIONS. He is serving as an Editor for IEEE TRANSACTIONS ON ENERGY CONVERSION and IEEE POWER ENGINEERING LETTERS, and an Associate Editor for IEEE ACCESS. He is also editing the Special Issue on Advances in High-Frequency Isolated Power Converters of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS. He is an Editor of the Book Series entitled ADVANCED IN POWER ELECTRONIC CONVERTERS (CRC Press, Taylor & Francis Group).

WEI XU (Senior Member, IEEE) received the double B.E. and M.E. degrees from Tianjin University, Tianjin, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, in 2008, all in electrical engineering. From 2008 to 2012, he was a Postdoctoral Fellow with the University of Technology Sydney, the Vice Chancellor Research Fellow with the Royal Melbourne Institute of Technology, and a Japan Science Promotion Society Invitation Fellow with Meiji University. Since 2013, he has been a Full Professor with the State Key Laboratory of Advanced Electromagnetic Engineering, Huazhong University of Science and Technology, China. He has more than 110 articles accepted or published in IEEE journals, two edited books published by Springer, one monograph published by China Machine Press, and more than 150 invention patents granted or in pending, all in the related fields of electrical machines and drives. His research interests include design and control of linear/rotary machines. He is a fellow of the Institute of Engineering and Technology (IET). He will serve as the General Chair of the 2021 International Symposium on Linear Drives for Industry Applications (LDIA 2021) and the 2023 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE 2023), Wuhan, China. He has served as an Associate Editor for several leading IEEE TRANSACTIONS/IEEE journals, such as IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY, and IEEE TRANSACTIONS ON ENERGY CONVERSION.

KASHEM M. MUTTAQI (Senior Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 1993, the M.Eng.Sc. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1996, and the Ph.D. degree in electrical engineering from Multimedia University, Selangor, Malaysia, in 2001.

Currently, he is a Full Professor and the Discipline Leader of electrical engineering at the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, Australia. He was associated with the University of Tasmania, Hobart, Australia, as a Research Fellow/Lecturer/Senior Lecturer, from 2002 to 2007, and Queensland University of Technology, Brisbane, Australia, as a Research Fellow, from 2000 to 2002. Previously, he also worked with Multimedia University as a Lecturer for three years. He has more than 22 years of academic experience and authored or coauthored 410 papers in international journals and conference proceedings. He has been cited highly for his work in the control of renewable and distributed power generation. His research interests include distributed generation, solid state transformer, power converters, power electronic applications, renewable energy, solar PV, wind turbines, wave energy, electrical vehicles, smart grids, micro-grids, standalone power supply, power grids, and power system planning and control. He is a fellow of the Institution of Engineers Australia (FIEAust) and U.K. Institution of Engineering and Technology (FIET).