Susceptibility of a microcontroller against electrical fast transients disturbances

Jiawen Nie, Xianchao Chen, Weiheng Shao and Wenxiao Fang

1 Guangdong University of Technology, Guangzhou, China.
2 China Electronic Produce Reliability and Environmental Testing Research Institute, Guangzhou, China.
3 E-mail: fangwx@ceprei.com

Abstract. This paper presents a research on the susceptibility of a microcontroller against electrical fast transients (EFT) and the caused failure of the microcontroller. The susceptibility test method is based on an EFT injection probe. According to the result of test, it is found that the susceptibility threshold of coupling voltage is 25V and the tested IC was damaged due to latch-up effect. The results would be instructive for the IC application with better electromagnetic compatibility performance.

1. Introduction

Integrated circuits (IC) play a key role in modern electronic systems. With the rapid development of manufacturing technique, the trend of ICs are smaller feature size, higher integration, faster operation speed, and lower operation voltage. In this situation, modern ICs are becoming more and more sensitive to external electromagnetic interference (EMI).

Electrical fast transients (EFT) is one of the important EMI in industrial electronics. In recent years, more and more researchers focus on the susceptibility of IC to EFT. [1] and [2] predicted the process that EFT interferences induced errors in IC. On the other hand, [3] introduced four failure types of microcontroller to EFT and the failure root, and [4] described a method for the characterization of IC susceptibility to EFT that propagated across the parasitic path of IC ground net. In addition, [5], [6], [7] mainly discussed modeling injection of EFT. Especially the international electro technical commission (IEC) provided a reference standard for EFT testing of IC [8].

In this paper, we systematically study the effect of EFT interference on a microcontroller IC by using capacitive coupling. We find the susceptibility threshold of the selected pins with EFT injection. With the increase of the injection voltage, the IC failed. To study the failure mechanism, we conducted a failure analysis of the microcontroller IC after the test.

2. Experiment

2.1. Measurement setup

The susceptibility measurement setup consists of a EFT generator (NSG 3040), a capacitive probe (P250) with optional coupling tip, a ground plane, and an oscilloscope (Tektronix TDS 3054C). The tip of the probe can be placed on a pin conductively and then the EFT pulses are injected into the studied IC. The test IC mounted on a test printed circuit board (PCB) is placed on a ground plane and...
monitored by the oscilloscope. The measurement setup and the connection scheme are shown in figure 1.

![Measurement setup (a) and schematic diagram (b) by using P250 probe.](image)

**Figure 1.** Measurement setup (a) and schematic diagram (b) by using P250 probe.

2.2. Test IC and its PCB
The tested IC is a 44 pins commercial microcontroller. The pinout diagrams of the tested ICs are shown in figure 2. Four I/O pins (No. 8, 9, 24 and 34) were selected for susceptibility test. These selected pins are of key concern in the practical application. The IC operates at a 4 MHz clock, and the selected I/O pins are set at a 5V output.

![The diagram of the tested IC.](image)

**Figure 2.** The diagram of the tested IC.

![Front side (a) and back side (b) of the testing board with IC.](image)

**Figure 3.** Front side (a) and back side (b) of the testing board with IC.
To study the effect of EFT interference on the microcontroller IC, a 10cm×10cm test board is fabricated according to the IEC 61967-1 [9]. The tested board has four layers. At layer 1 only the tested IC is mounted, and layer 4 are used as the ground plane. Layer 2 and 3 act as power and signal planes, respectively. Other components are mounted at layer 4. The back side (layer 1) and front side (layer 4) of the tested board are shown in figure 3 (a) and (b), respectively.

In experiment, the test board is mounted on the ground plane and the tip of the probe contacts with the selected pin of IC. Several I/O pins of the IC is monitored by an oscilloscope, so that the failure can be observed in time. The EFT pulses are injected to the Test IC from the P250 probe, and then pass to the ground plane from the ground pin of the microcontroller, finally return to the probe forming a loop, as shown in figure 4.

![EFT test current path](image)

**Figure 4.** EFT test current path.

3. **Experiment results and discussion**

3.1. **Results of EFT experiment**

According to susceptibility performance classification, the error state of the IC is defined in table 1.

| Lever | Response                      |
|-------|-------------------------------|
| A     | No failure                    |
| B     | Short-term sporadic failure   |
| C     | Long-term frequent failure    |
| D     | Re-power on recovery          |
| E     | Damaged                       |

The results of the IC with the injection of EFT pulses to the pins (No. 8, 9, 24, and 34) are shown in figure 5. As shown, the pin of EINT11 (pin 24) is weakest in the four pins. When the coupling voltage reaches 25V at pin EINT11, the state of the IC changes from A to B.

![EFT test results](image)

**Figure 5.** EFT test results.
3.2. Failure analysis of the IC

The failure IC are observed by a metallurgical microscope. As shown in figure 6, a breakdown due to the latch-up effect occurred between the VDD and VSS pins. In CMOS IC, latch-up usually occurs inside the silicon controlled rectifier (SCR) of the device. The equivalent circuit schematic of the SCR structure is shown in figure 7(a), which consists of a lateral NPN and a vertical PNP bipolar transistor to form a PNPN structure. The trigger current induced by the injected EFT pulses flows through substrate parasitic resistance $R_{\text{sub}}$. When the coupling voltage exceeds the turn-on voltage (about 0.7V) of NPN transistor due to a positive bias in the emitter junction, the NPN transistor turns on and then the current of the power supply VDD flows through the parasitic resistance $R_{\text{sub}}$ and NPN transistor to VSS. When the voltage drop $R_{\text{off}}$ are higher than the turn-on voltage of PNP transistor, the PNP transistor will be also turned on. The SCR will be completely triggered into a latching transistor due to the positive-feedback regenerative mechanism [10]. A low resistance path between the power supply and ground is finally built, generating a huge SCR current from VDD to VSS. The I-V characteristic of the SCR device of the studied IC is shown in figure 7(b). When the latch-up effect was triggered, a continuously large current damaged the studied IC finally.

![Figure 6. Failure location between the VDD pad and VSS pad.](image)

![Figure 7. Equivalent circuit schematic of a SCR device (a), and the I-V characteristics (b) of the SCR of the studied IC by using a TLP measurement method.](image)
4. Conclusions
This paper presents an electromagnetic susceptibility study of a microcontroller under the EFT interference. In the experiment, the susceptibility threshold of coupling voltage is 25V, and with a high enough amplitude the positive EFT voltage pulses trigger the latch-up effect of the IC under test. It is proven that a low resistance huge current path is generated, and finally the IC was damaged.

References
[1] Gao X, Sui C, Hemmady S, et al 2015 Predicting EMI induced delay errors in integrated circuits: Sensitivity to the velocity saturation index Electromagnetic Compatibility IEEE PP 102-105
[2] Bauer S, Deutschmann B, Winkler G 2015 Prediction of the robustness of integrated circuits against EFT/BURST IEEE Int Symp on Electromagnetic Compatibility IEEE PP 45-49
[3] Li C, Li J, Wu J, et al 2016 Investigation on the immunity of microcontroller to electrical fast transients IEEE Int Conf on Asic IEEE PP 1-4
[4] Musolino F, Fiori F 2005 Investigation on the susceptibility of microcontrollers to EFT interference Int Symp on Electromagnetic Compatibility IEEE 2 410-413
[5] Zhang J, Koo J, Moseley R, et al 2014 Modeling injection of electrical fast transients into power and IO pins of ICs IEEE Transactions on Electromagnetic Compatibility 56(6) 1576-1584
[6] Zhang J, Koo J, Beetner D G, et al 2010 Modeling of the immunity of ICs to EFTs IEEE Int Symp on Electromagnetic Compatibility IEEE PP 484-489
[7] Koo J, Han L, Herrin S, et al 2009 A nonlinear microcontroller power distribution network model for the characterization of immunity to electrical fast transients IEEE Transactions on Electromagnetic Compatibility 51(3) 611-619
[8] Integrated Circuits 2013 Measurement of impulse immunity Part 3:Non-synchronous transient injection method IEC 62215-3
[9] Integrated Circuits 2005 Measurement of Electromagnetic Emissions Part1:General conditions and definitions IEC 61967-1
[10] Yen C C, Ker M D, Chen T Y, et al 2009 Transient-induced latchup in CMOS ICs under electrical fast-transient Test IEEE Transactions on Device & Materials Reliability 9(2) 255-264