Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficiency, and Power-Intermittency Resilience

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Abstract—Herein, a bit-wise Convolutional Neural Network (CNN) in-memory accelerator is implemented using Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) computational sub-arrays. It utilizes a novel AND-Accumulation method capable of significantly-reduced energy consumption within convolutional layers and performs various low bit-width CNN inference operations entirely within MRAM. Power-intermittence resiliency is also enhanced by retaining the partial state information needed to maintain computational forward-progress, which is advantageous for battery-less IoT nodes. Simulation results indicate \( \approx 5.4 \times \) higher energy-efficiency and \( 9 \times \) speedup over ReRAM-based acceleration, or roughly \( \approx 9.7 \times \) higher energy-efficiency and \( 13.5 \times \) speedup over recent CMOS-only approaches, while maintaining inference accuracy comparable to baseline designs.

I. INTRODUCTION

Due to their impressive performance on image recognition tasks, deep Convolutional Neural Network (CNNs) offer significant potential advantages for use on large-scale datasets. However, the processing demands of high-depth CNNs spanning hundreds of layers face serious challenges for their tractability in terms of memory and computational resources. This so-called "CNN power and memory wall" has been motivating the development of alternative approaches to improve CNN efficiency at both software and hardware levels [1].

In algorithm-based approaches, use of shallower CNN models, quantizing parameters [2], and network binarization [3] have been explored extensively. Recently, utilizing weights with low bit-width and activations reduces both model size and computing complexity. For instance, performing bit-wise convolution between the inputs and low bit-width weights has been demonstrated in [2] by converting conventional Multiplication-And-Accumulate (MAC) operations into their corresponding AND-bitcount operations. However, such conversion cannot necessarily guarantee high efficiency operation in a hardware implementation that may engage various aspects of instruction encoding and operand access. In an extreme quantization, Binary Convolutional Neural Network (BCNN) has achieved acceptable accuracy on both small [4] and large datasets [3] by relaxing the demands for some high precision calculations. Instead, it binarizes weight/input while processing the forward path, providing a promising solution to mitigate aforementioned bottlenecks in storage and computational components [5].

![Figure 1: Proportional relationship for execution time of a CNN on both CPU and GPU][1]

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From the hardware point of view, the underlying operations should be realized using efficient mechanisms. However, within conventional isolated computing units and memory elements interconnected via buses, there are serious challenges, such as limited memory bandwidth channels, long memory access latency, significant congestion at I/O choke-points, and high leakage power consumption [6], [7]. In-memory processing paradigms built on top of non-volatile devices, such as Resistive Random Access Memory (ReRAM) [6], [8], Spin-Transfer Torque Magnetic RAM (STT-MRAM) [9] and recent Spin Orbit Torque MRAM (SOT-MRAM) [10], introduced to address the aforementioned concerns. Due to their interesting features such as non-volatility, near-zero standby power, high integration density, compatibility with CMOS fabrication process, and radiation-hardness, these NV-based systems offer some promising attributes for in-memory processing implementations.

CNNs realize machine learning classifiers that are capable of taking an image as an input and then computing the probability that the image belongs to each designated output class. Typically, a CNN consists of several convolutional layers including convolution, non-linearity, normalization, and pooling steps, followed by a flatten layer connected to fully-connected layers. For feature extraction, each convolutional layer receives a set of features organized into multi-channels referred to as feature maps. It applies feature detectors (filters) by performing high-dimensional convolutions. To increase non-linearity of the pooled feature map, a non-linear activation function, i.e. rectified linear unit (ReLU), will be applied to the results. The convolutional layer occupies the largest portion of running time and consumes significant computational resources in both GPU and CPU implementations, as depicted in Figure [1].
This motivates us to propose an optimized bit-wise CNN in-memory accelerator based on SOT-MRAM computational sub-arrays. In particular, the bit-wise CNN based on AND-bitcount operations presented in [2] can be further accelerated by modifying the algorithm rather than a direct module-by-module mapping such as IMCE [12].

The remainder of this paper is organized as follows. In Section II, the proposed accelerator is designed to be partially power-failure resilient and uses a novel hardware-conforming AND-Accumulation method to further accelerate convolutional layers in CNN. The non-volatile SOT-MRAM based structures provide power failure resiliency feature. Moreover, they are leveraged to develop a bit-wise CNN in-memory accelerator. Extensive simulation results and detailed analysis are summarized in Section III including inference accuracy, energy consumption, and memory storage. Finally, Section IV concludes this paper by highlighting the features and advantages of the proposed in-memory accelerator.

II. INTERMITTENT RESILIENT CNN ACCELERATOR

As mentioned in the previous section, most of the CNN run-time is taken by performing MACs. Therefore, reducing computation complexity of MAC operations are vital for resource-constrained systems such as IoT devices. In order to accelerate MAC operations in convolutional layers, three main processes including AND operation, bitcount, and bitshift are leveraged, which realize a bit-wise convolution. A crude in-memory implementation of such bit-wise operations can be found in [12], where bitcount and bitshift are directly implemented using serial counter and shifter units. We believe such module-by-module mapping not only degrades the bit-wise convolution performance in hardware, but also imposes a large in-memory data-transfer due to its intrinsic serial operations. Hence, we propose a hardware-optimized method inspired by DoReFa-Net [2] to mitigate these drawbacks, in addition to address the power-failure issue:

\[
I * W = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} 2^{n+m} CMP(AND(C_n(W), C_m(I)))
\]

\[
CMP(X) = \sum_{i=1}^{n} x_i, \text{ where } X = x_0x_{n-1}...x_2x_1 \tag{1}
\]

where \( I \) as input and \( W \) weight. The convolution can be implemented by AND, CMP (rather than bitcount), and parallel bitshift operations. A general overview of our proposed CNN accelerator is shown in Figure 2. This architecture mainly consists of an Image Bank, a Kernel Bank, computational sub-arrays, and an Extra Processing Unit (EPU) including three ancillary units, i.e. Quantizer, Activation Function-Active, and Batch Normalization-BN. Each computational sub-array is equipped with three components: CMP as a Compressor unit, ASR as an Adaptive Shift Register, and NV-FA as a Non-Volatile Full Adder. As discussed earlier, the convolutional layer contributes the largest proportion of computation time and complexity to CNNs. Thus, we mainly focus on this layer. However, the proposed system architecture can be leveraged to implement other CNN layers including batch normalization and pooling layers. We assume both feature maps \( I \) and feature weights \( W \) are initially loaded in two sub-banks of memory. In our approach, inputs should be quantized before mapping to the accelerator, which is performed by EPU’s Quantizer. Because of page limit of this paper we cannot thoroughly discuss EPU’s units in details. In the following, we elaborate two main processing phases of the accelerator.

A. Parallel AND Phase

Figure 4 shows the in-memory processing sub-array architecture using SOT-MRAM [10, 12, 13]. The array supports both memory read-write and simple Boolean logic operations such as AND/XOR. The SOT-MRAM structure includes an Magnetic Tunnel Junction (MTJ) that its free layer is directly connected to a Spin Hall Metal (SHM). There are two stable magnetization states, parallel (low resistance), and anti-parallel (high resistance), which denote 0 and 1 in binary information, respectively. Each SOT-MRAM cell requires five signals, which are common among all MRAM cells to perform memory operations. There are Write Word Line (WWL), Write Bit Line (WBL), Read Word Line (RWL), Read Bit Line (RBL), and a Source Line (SL). (For more details, refer to [14])

The SOT-MRAM based computational sub-array can be readily utilized such that the massive AND operations required for convolutions can be handled. Consider \( I \) and \( W \) as input
and kernel of \( m \)- and \( n \)-bit (for simplicity, 3-bit, as Figure 3), \( I \) is covered by kernel \( W \). The bits of each \( I_i/W_i \) element are indexed from least significant bit to most significant bit with \( M = [0, m-1] \) and \( N = [0, n-1] \). Then, a second sequence noted by \( C_m(I) \) can be considered for \( I \) including the combination of \( m^\text{th} \) bit of \( I_i \) elements. For example, \( C_2(I) \) represents the LSBS of all \( I_i \) elements, “0000”. The second sequence for \( W \) can be considered like \( C_n(W) \). Now, by considering the set of all \( m^\text{th} \) value sequences, the \( I \) can be expressed as \( I = \sum_{n=0}^{M-1} 2^n C_m(I) \). Additionally, \( W \) can be expressed as \( W = \sum_{n=0}^{N-1} 2^n C_n(W) \).

To efficiently load the Quantizer unit’s output to computational sub-arrays, \( I \) and \( W \) should be tailored. As illustrated in the data organization and mapping step of Figure 3, \( C_2(W) - C_0(W) \) are consequently mapped to the assigned sub-array. Accordingly, \( C_2(I) - C_0(I) \) are mapped to the following memory rows similarly. Now, the accelerator can perform the parallel bit-wise AND operation depicted in Figure 4 within its computational sub-array.

**B. Accumulation Phase**

The accumulation phase consists of three main components: (1) NV 4:2 compressor, (2) adaptive shift register, and (3) NV full adder.

1. **4:2 Compressor (CMP):** Compressors, especially 4:2 and 5:2, are widely used to reduce the delay of the summation of partial products in multiplier designs. Figure 5a shows the schematic of a 4:2 compressor and its fundamental implementation using two serially connected full adders. The basic equation of the 4:2 compressor is \( x_1 + x_2 + x_3 + x_4 + C_m = \text{sum} + 2 \times (\text{carry} + Cout) \). The following equations express the outputs of the 4:2 compressor:

\[
\text{sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 + c_m
\]
\[
\text{carry} = (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot c_m + (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot x_4
\]
\[
Cout = (x_1 \oplus x_2) \cdot x_3 + (x_1 \oplus x_2) \cdot x_1 \quad (2)
\]

Figure 5: Implementation of (a) 4:2 compressor, and (b) proposed architecture with the MUX and XOR-XNOR modules.

These equations can be reformed in a way that XOR/XNOR modules are only located in a first row and the other XOR/XNOR elements are replaced by MUXs, as shown in Figure 5b. Considering the compressor implementation presented in [15] and the capability of our proposed computational sub-array design to function as an XOR/XNOR operation including MUX elements, the accelerator can be configured to implement an optimized 4:2 compressor. The results of parallel AND operations are written back to the sub-array and passed through the compressor, which can readily count the number of “1”s within each resultant vector and pass it to the next unit. Figure 5 depicts step (1) of the accumulation phase. In our design, we only need to update the memory contents once to implement XOR/XNOR logic, namely in-memory XOR computation. Due to the 4:2 compressor, the bitcount operation can be performed in one clock cycle instead of several clock cycles of shifting operations, yielding considerable reductions in delay and energy. Due to the nonvolatile XOR/XNOR implementation, our 4:2 compressor is power failure resilient. Moreover, it is power efficient, due to the optimum number of write operations equal to the sub-array length. In general, kernel length \((n_k)\) determines the number of compressor’s input \((n + 1)\).

2. **Adaptive Shift Register (ASR):** Since the number of shift operations is different and is determined by the locations of the input and the weight in the sub-array, governed by the expression: \( m + n - 2 \), an adaptive shift register (ASR) is required. One method to implement an ASR is an addition tree approach. In general, this structure is composed of \( 2^{m+n}-1 \) bit full adders (FAs), in which the first layer includes \( 2^{n-1} \) FAs, the second layer has \( 2^{n-2} \) FAs, and finally the last layer consists of one FA. Another approach to designing an ASR, developed herein, is to implement logic expressions using multiplexers (MUXs) and then connect them to the flip-flops (FFs) in an appropriate way. Figure 6 depicts an ASR design for 4-bit input data, which is able to operate with three different numbers of shifts: 00=0, 01=1, and 10=2. It includes seven MUXs, three inverters, four NOR/AND gates, and six FFs. For instance, assume that \( \text{IN}[3:0] = "1001" \) and \( \text{SHIFT}[1:0] = 1 \) (01), which means \( \text{SHIFT}[0]=1 \) (red line) and \( \text{SHIFT}[1]=0 \) (green line). Because of the MUX-based selection structure, “0” is stored in FF#5 and FF#0. Then the applied input is written into FF#1 to FF#4 appropriately/successively, which produces “010010” as an output. The number of FFs is determined by the summation of the number of inputs and the maximum number of possible shift operations. In our

\[\text{The number of shift is determined by the memory array size, i.e. 8 bits.}\]
implementation, a 4-bit ASR is developed, which requires six FFs to perform three possible shift operations.

3) Non-Volatile Full Adder (NV-FA): Due to the usage of NV elements in the AND-Accumulation process, the structure has become partially power-failure resilient, meaning it can restore the system’s operations to the last good/suitable state under most conditions. While it might fail to restore the last configuration if power loss occurs during the addition (shift) operations, the delay for this step is equal to the delays of $m+n$ FAs, $\approx m+n \times 58$ ps, which is negligible to the total delay of calculating one fmap. Finally, the output of this level should be added with the results of the previous inputs ($Is \times Ws$). To make our design more resilient in presence of power failure, we developed a NV-FA (NV-FA), as shown in Figure 7a. The NV-FA includes two NV flip-flops (NV-FFs) in addition to the regular FA. The NV-FF consists of a volatile CMOS FF and a NV element.

To remove the additional overhead and issues caused by the common checkpointing approaches, the summation results will be written into the NV-elements after computing steps for a fixed number of frames, i.e. 20 frames. Otherwise, the states and results of each step store in a volatile FF and sum up with the upcoming results. We can modify the period of writing operation based on the power failure rate. In this case, our checkpointing approach is superior to common energy harvesting systems, which are usually utilized in intermittent computing architectures, in terms of area and complexity. Because herein, common checking-based approaches may suffer from inconsistencies, both internal and external, after each power loss. Moreover, peripheral circuits such as voltage detection systems and capacitor arrays are needed, which is a crucial challenge for area-constrained IoTs. Figure 7b depicts the functionality of NV-FA in presence of power failure.

III. EXPERIMENTAL RESULTS

A. Accuracy

Bit-width: We consider 4 different bit-width of W:I (1:1, 1:4, 1:8, 2:20) to explore the accuracy of our accelerator with an 8-bit gradient. In addition, we consider a 32-bit full-precision case as the base-line with 32-bit gradient. Data-set: Among various data-sets, we select SVHN [16] with 73257 training digits, 26032 testing digits, and 531131 additional digits for extra training data. The images are pre-processed to 40×40 from the original 32×32 cropped version and fed to the model. CNN Layers: We developed a bitwise CNN with 6 convolutional, 2 average pooling and 2 FC layers, which are equivalently implemented by convolutional layers. Such model costs about 80 FLOPs for each 40×40 image. To avert further prediction accuracy degradation, we don’t quantize the first and last layers [2], [3], [5]. Training: We basically modified the open-source DoReFa-Net [2] algorithm by integrating new bit-wise convolution function applying the AND-Accumulation method. To increase the accuracy and avoid over-fitting, we adopted batch normalization, parameter tuning and dropout methods. The CNN design is implemented on TensorFlow [17] running 100 epochs and we extract the test error of each epoch. Results: Table 1 shows the computation complexity and test error of the under-test model. We used $W \times I$ and $W \times I + W \times G$ to achieve the computation complexity of inference and training, respectively. Our results replicate the conclusion drawn by [2], [12] whereby kernels weights and inputs are progressively more vulnerable to bit-width reductions.

Table I: Test error of the CNN model on SVHN.

| Bit-width | Computation Complexity | Error (%) |
|-----------|------------------------|-----------|
| W:32:32  | Inference              | Training  |
| 1:1       | 2.4                    |
| 1:4       | 2.3                    |
| 1:8       | 2.1                    |
| 2:20      | 1.8                    |

B. Storage

Five bit-width of W:I (32:32, 1:1, 1:4, 1:8, and 2:2) are selected to evaluate memory storage requirements. The breakdown of memory storage is shown in Figure 8a. We observe that as the CNN model’s bit-width decreases, less memory storage is required. For instance, the 1:4 configuration, with higher inference accuracy compared to 32:32, shows $\sim$11.7× memory reduction. To investigate the memory usage in large data-sets, we implement three different bit-width of W:I (64:64, 32:32, and 1:1) using AlexNet model on ImageNet data-set on the proposed accelerator in [8]. We observe that 1:1 bit-width configuration demands $\sim$40MB memory which is $\sim$6× and $\sim$12× smaller in comparison with the single and double precision CNNs, respectively.

C. Energy Consumption

In this subsection, we estimate the energy-efficiency of the CNN model implemented by the proposed accelerator and state-of-the-art inference acceleration solutions, i.e. ReRAM, SOT-MRAM, and CMOS-only ASIC. To evaluate the performance of the proposed design, the circuit level simulation is implemented in Cadence Spectre using NCSU 45nm CMOS PDK [18] in conjunction with a SOT-MRAM resistive model. The NEGF approach is utilized to extract the MTJ resistance
(R_{MTJ}) \ [19], whereas the heavy metal resistance (R_{SHM}) is determined based on the resistivity and device dimension. Accordingly, we extensively modified the system-level memory evaluation tool NVSim \ [20] to co-simulate with an in-house developed C++ code simulator based on circuit-level results. We configure the memory sub-array organization with 256 rows and 512 columns per mat organized in a H-tree routing manner, 2×2 mats per bank, 8×8 banks per group; in total 16 groups and 512Mb total capacity.

For comparison, a ReRAM-based in-memory accelerator based on \ [6] was developed with 64 fully-functional sub-arrays. For each mat, there are 256×256 ReRAM cells and eight 8-bit reconfigurable SAs. For evaluation, NVSim simulator \ [20] was modified to estimate the system energy and performance. We adopted the default NVSim’s ReRAM cell file (.cell) for the assessment. Besides, we developed an IMCE-like \ [12] design with the same sub-array configuration as our design. To compare the result with ASIC accelerators, we developed a YodaNN-like \ [21] design with 8×8 tiles for 33MB eDRAM. Accordingly, we synthesized the design with Design Compiler \ [22] under a 45 nm process node. The eDRAM and SRAM performance were estimated using CACTI \ [23]. In order to have a fair comparison, the area-normalized results (performance/energy per area) will be reported henceforth.

Figure 9 demonstrates the proposed accelerator energy-efficiency results with batch sizes of 1 and 8 in different configuration spaces of weight and input. We observe that the proposed accelerator offers the highest energy-efficiency normalized to area compared to others owing to its fast, energy-efficient, and parallel operations. Our design shows \sim 2.1 \times better energy-efficiency compared to IMCE. This energy reduction comes mainly from using a fast, efficient, in-memory compressor instead of a serial counter in the accumulation phase. In addition, 5.4\times and 9.7\times better energy efficiencies are reported over ReRAM and ASIC accelerators, respectively.

D. Performance Estimation

Figure 10 compares the throughput in frames per second normalized to area of the proposed design with other accelerators. We observe that the AND-Accumulation method leads to \sim 3\times higher performance than AND-bitcount employed in IMCE. In addition, it is 9\times and 13.5\times faster on average than ReRAM and ASIC-64 solutions. This arises from two sources: (1) ultra-fast and parallel in-memory operations of the proposed design compared to multi-cycle ASIC and ReRAM solutions and (2) the existing mismatch between computation and data movement in ASIC design. In addition, the ReRAM design uses matrix splitting approach because of the intrinsically limited bit levels of ReRAM devices so that excessive sub-arrays are occupied. This can further limit parallelism methods \ [6].

E. Area-Energy trade-off

In this subsection, we evaluate the energy/area of BCNN resistive processing-in-memory accelerators based on ReRAM \ [8] and SOT-MRAM \ [12]) for inference of one single image over three well-known data-sets under a 45nm technology node. Table II demonstrates that the proposed SOT-MRAM-based accelerator can process BCNN very efficiently compared to others. Its worth pointing out that the energy reported in
Table II consists of the energy of convolution computation of all layers. We observe that our design can execute binary-weight AlexNet [3] on ImageNet favorably with 471.8 \mu J/img where \sim 4.8 \times and 3.5 \times smaller energy and area are obtained, respectively, compared to the ReRAM-based design. In addition, the proposed accelerator exhibits 1.6 \times better energy savings compared to SOT-MRAM IMCE on ImageNet even though it imposes larger overhead to the memory chip.

Table II: Energy-area comparison of different NVM-based BCNN accelerators.

| Designs   | ImageNet Energy (\mu J/img) | Area (mm²) | SVHN Energy (\mu J/img) | Area (mm²) | MNIST Energy (\mu J/img) | Area (mm²) |
|-----------|-----------------------------|------------|-------------------------|------------|--------------------------|------------|
| ReRAM [3] | 2275.34                     | 9.19       | 425.21                  | 0.085      | 13.55                    | 0.060      |
| IMCE [13] | 785.25                      | 2.12       | 135.26                  | 0.01       | 0.92                     | 0.009      |
| Proposed  | 471.8                       | 2.60       | 84.31                   | 0.039      | 0.68                     | 0.012      |

IV. CONCLUSION

In this work, a bit-wise CNN in-memory accelerator based on SOT-MRAM computational sub-arrays was proposed. This new architecture could be leveraged to greatly reduce energy consumption dealing with convolutional layers and accelerate low bit-width CNN inference within non-volatile MRAM. Our device-to-architecture co-simulation results show that the proposed accelerator can attain \sim 5.4 \times higher energy-efficiency and 9 \times speedup compared to ReRAM-based, and \sim 9.7 \times higher energy-efficiency and 13.5 \times speedup over ASIC accelerators holding almost the same inference accuracy to the baseline CNN on different data-sets.

We plan to extend our future work to mitigate the write-operations issue for NV elements, which consumes a large amount of power. Choosing a proper thermal barrier, i.e. 30kT, for MTJ devices could provide retention times ranging from minutes to hours and achieve at least 50% energy reduction compared to nanomagnets with a thermal barrier around 40kT. The other approach to reduce performance overhead caused by NV elements is to leverage one NV-FF instead of two NV-FFs within each FA. After a specified duration, only Cout will be stored in a NV-FF while sum is saved in a regular FF. If power failure occurs, the stored value is considered as both sum and Cout for the next add operation. In this scenario, PDP improvements can be achieved at the cost of lower accuracy. Generally, in a situation with a high occurrence rate of power failure, the number of completed tasks for a CMOS-only implementation is significantly reduced, which degrades performance of the system [14]. Hence, utilizing the power failure resilient architecture even without further optimization can avoid high bulk-write energy costs of Flash pages and complexities from checkpointing/restore protocols.

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