A comparative Analysis of Multi-Level Inverters Supplied by Photovoltaic Panels based on THD and Filter Size by using POD-SPWM Technique

Haider Ali Khalif 1, Jameel Kadhim Abed 2 and Ali Jafer Mahdi 3
1, 2 Elect. Eng. Technical College, Middle Technical University, Baghdad, Iraq
3 Department of Elect. and Electronics Eng., University of Karbala, Karbala, Iraq

Abstract. Solar Photovoltaic (PV) power is one of the favourable renewable energy resources in the globe especially in Iraq. The main benefits of solar energy are dependability and availability. The important roles for construction of a PV power plant are decreasing the cost of its components, simplifying the complexity of its controllers and improving its performance to meet the grid standards. In this paper, single stage PV Generators (PVGs) connected with Cascaded H-Bridge Multilevel Inverter (CHB-MLI) are designed and analyzed. Four MLI topologies are demonstrated, which are three, five, seven and nine levels, for improving the efficiency of multilevel inverter, reducing drop voltage and total harmonic distortion (THD) value for the output voltage and current by decreasing the inductance value of L filter in load side. In this paper, Phase Opposition Disposition based on Sinusoidal pulse width modulation (POD-SPWM) technique is used to control the proposed MLI circuits. In this technique, the reference signal is a modulating sine of 50 Hz frequency is compared with a carrier signals of 50 kHz to produce optimal switching combinations that achieve numerous levels of output voltage. Simulation work is done using the MATLAB software. The simulation results confirm that the performance and the cost of nine-level topology is improved compared with the three, five and seven levels topologies.

Keywords: Multilevel inverter; PV array; Sinusoidal pulse width modulation; Performance-Enhancing.

1. Introduction

In the past few decades, because of the fast increase in population and universal industrialization, The demand for electricity has increased dramatically, Due to generosity of renewable resources in nature, solar energy is considered as one of the most promising energies of renewable energy resources. Solar energy does not use fuel and therefore it decreases the cost and also it is an environmentally friendly source of energy [1]. Photovoltaic energy is a form of green energy. A high performance on this energy is required in order to benefit from great energy produced by solar cells. Also there must be a constant adaptation for the continuous changes of energy production[18]. Renewable energy source(RES) such as solar and wind energies can be used to generating the power in residential buildings and transportation applications because it has environmental advantages [2]. RES is going ever-significant with the current drive to sustainable and environment friendly power generation techniques. DC-AC converters (i.e. inverters) are used with PV power generator to convert input (DC) to output (AC) and improving PV system efficiency [3]. Multi-level inverter can be used in PV systems applications for various reasons such as producing high-quality voltage output, can operate at a frequency close to fundamental frequency, consists of several DC-links That makes it easy to control...
the DC-voltage and implement MPPT in each source [4]. Multilevel inverters are becoming recent trends, because of its modularity and simplicity of control to generate particular number of levels. Multilevel inverters have a lot of applications like ups, in power grid, as solar inverter, induction heating and number of other applications. With increasing dc voltage sources can be obtained a sinusoidal like waveform. Thus, THD decreases which has a great importance in power grid applications. A sine wave output is desirable due to a lot of electrical products are designed to work best with a sine wave ac power source [27]. The demand for high voltage, high power inverters are increasing and it is impossible to connect a power semiconductor switch to high voltage network directly. Therefore, the multilevel inverters had been introduced and are developing now. With an increasing the number of dc voltage sources in input side, the sinusoidal like waveform can be created at the output side. As a outcome, (THD) decreases and the output waveform quality increasing, which are two main usefulness of the multilevel inverters [24]. The staircase output waveform and a low electromagnetic emission, this make it uses in industrial applications that need high voltage and high output characteristics [5]. MLI can be classified to diode-clamped flying capacitor inverter and cascaded H-bridge MLI (symmetrical DC sources, asymmetrical DC sources). Cascaded H-bridge MLI has been used for improving the performance of RES, voltage organization, VAR compensation and for decreasing harmonics in output voltage [6]. Cascaded H-bridge MLI is the most used in the applications in comparing with others MLI because it does not need clamping diode and flying capacitors. Additionally, PWM control of cascaded H-bridge MLI is simple in construction and implementation [7]. In H-bridge circuit, levels of output voltage can be increased by using a smaller number of DC-voltage sources. The rate of change of voltage \((dV/dt)\) decreases, that leads to reducing electromagnetic interference. Cascaded H-bridge MLI has disadvantages such as: number of switches are increased with increasing levels of output voltage, this leads to difficult in control, increasing size and cost of inverter[8]. The cascaded H-bridge MLI needs more panels connected in cascade and that increase the output voltage levels with separate DC voltage sources for each panels. This is the easiest way to producing waveform close to sinusoidal waveform and then filter the output to get the THD required [9]. Most studies focus on design and analysis of single-phase grid-connected solar power system without using DC-link capacitor and inductor filter. Ref. [10] Single Phase Grid-Connected Inverter for Photovoltaic System with Maximum Power Point Tracking. The paper[10], focus on using boost converter to increasing DC voltage of inverter, to getting maximum power tracking in order to increasing efficiency of the system. Also LC filter used to decreasing THD of output. In[11], seven and nine levels are designed with reducing number of switches. Boost converter uses to increasing DC voltage of PV-array. THD of output voltage decreases by using L filter. The paper in [12] deals with nine-level, PV system is designed with DC/DC boost converter and nine level inverter. The main purpose of paper in [12] is to reducing the switches to seven switches in compared with conventional method, 16 switches were used. SPWM technique is used to trigger the switches of inverter. It consists of one carrier wave and one reference wave. The pulses are generated by comparing two waves to getting PWM. In [25], different-levels cascaded H-bridge inverter are implemented for PV grid-connected systems which are five, seven and nine levels to minimizing THD of output voltage. THD of output voltage in the five level was (29.92%), for the seven level was (25.01%) and for the nine level was (22.75%). The paper in [26], deals with the design and putting into practice of single-phase nine-level MLI for R-load with multi-carrier PWM method. THD of output voltage is minimized to (17.93%).

2. PV Power System Configuration

PV panel is a device used to convert irradiance from the sun directly into DC power [2]. PV system consists of solar cells connected in series and parallel circuits to getting high power is called PV module. A group of modules are electrically connected in series-parallel combinations to produce desired voltage and current as a PV array [13]. Table 1 shows the parameters of solar cell. The basic equation that describe the characteristics of current-voltage of PV module is described by (1) [19]. The electrical circuit of PV is shown in Figure 1.

\[
I = I_{ph} - I_s \left( \exp(\alpha(R_s I + V)) - 1 \right) - \frac{R_s I + V}{R_{sh}}
\]

(1)
where \( \alpha = \frac{q}{nN_sKT} \) \((2)\)

Where \( \alpha \) represents the thermal equivalent voltage, \( q \) is the charge of the electron \((1.602 \times 10^{-19} \text{C})\), \( K \) is the Boltzman constant \((1.381 \times 10^{-23} \text{J/K})\), \( N_s \) is the number of series connected cells, \( T \) is the panel temperature, \( n \) is the ideality factor, \( R_s \) is the series resistance, \( R_{sh} \) is the shunt resistance, \( I_{ph} \) is the photo current, \( I_s \) is the reverse saturation current.

| Table 1. solar system characteristics |
|--------------------------------------|
| Parameters                        | Specifications |
| maximum number of PV panels        | 16             |
| maximum Power \((P_{mpp})\)         | 135 W          |
| maximum Voltage \((V_{mpp})\)       | 17.7 V         |
| maximum Current \((I_{mpp})\)       | 7.63 A         |
| Open circuit voltage \((V_{dc})\)   | 22.1 V         |
| short circuit current \((I_{sc})\)  | 8.37 A         |

3. MLI Topology

The cascaded H-Bridge MLI has many benefits and important technique of power electronic systems which are analyses output voltage with number of dc sources as inputs. The cascaded H-Bridge MLI requires a smaller number of components in comparing with others MLIs. It gives high-quality output voltage close to sine wave. With several levels of MLI topologies, THD can be decreased. Cascaded H–bridge MLI consists of \((N)\) H-bridge converters connected in series. Each H-bridge is connected to a string of PV panels as DC voltage sources. Each H-bridge has four switches, by different methods to control the four switches in each H-bridge can produce three voltage levels. Number of input dc sources are equal to number of H-Bridge \((N)\). With \((N)\) input dc source can produce \((2N+1)\) levels to composition AC output voltage. This is decreased THD of output voltage and current as well as decreasing filter size and cost[14]. Single phase three-level cascaded H–bridge MLI consists of single bridge has four power IGBT switches from \( S_1 \) to \( S_4 \). This Circuit gives three level voltage \((V_{dc}, 0, -V_{dc})\) across the output. There are four possible states for switches which can generate voltages across the output of the inverter as shown in the Table 2 [23]. Five-level cascaded H–bridge MLI consists of two bridges connected in series. Each bridge has four power IGBT switches. This Circuit gives five level voltage \((V_{dc}, 2V_{dc}, 0, -V_{dc}, -2V_{dc})\) across the output. There are five possible states for switches which can generate voltages across the output of the inverter as shown in the Table 3 [22]. Seven-level cascaded H–bridge MLI consists of three bridges connected in series. Each bridge has four power IGBT switches. This Circuit gives seven level voltage \((V_{dc}, 2V_{dc}, 3V_{dc}, 0, -V_{dc}, -2V_{dc}, -3V_{dc})\) across the output. There are seven possible states for switches which can generate voltages across the output of the inverter as shown in the Table 4 [16]. Nine-level cascaded H–bridge MLI consists of four bridges connected in series. Each bridge has four power IGBT switches. This Circuit gives nine level voltage \((V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 0, -V_{dc}, -2V_{dc}, -3V_{dc}, -4V_{dc})\) across the output of the inverter. There are nine possible states for switches which can generate voltages across the output of the inverter as shown in the Table 5 [20]. Number of DC voltage sources for each level are equal to the number of H-bridges as shown in Figure 2.
Figure 2. Cascaded H-bridge multilevel inverter.

Table 2. Switches states of 3-level MLI.

| Level  | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
|--------|-------|-------|-------|-------|
| $V_{dc}$ | on    | on    | off   | off   |
| $-V_{dc}$ | off   | off   | on    | on    |
| 0      | on    | off   | on    | off   |
| 0      | off   | on    | off   | on    |

Table 3. Switches states of 5-level MLI.

| Level  | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| $V_{dc}$ | on    | on    | off   | off   | off   | off   | off   | off   |
| $2V_{dc}$ | on    | on    | off   | off   | on    | on    | off   | off   |
| 0      | off   | on    | off   | on    | off   | on    | off   | on    |
| $-V_{dc}$ | off   | off   | on    | on    | off   | off   | on    | off   |
| $-2V_{dc}$ | off   | off   | on    | on    | off   | off   | on    | on    |

Table 4. Switches states of 7-level MLI.

| Level  | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|
| $V_{dc}$ | on    | on    | off   | off   | off   | on    | on    | off   | on    | off      | on       | on       |
| $2V_{dc}$ | on    | on    | off   | off   | on    | off   | on    | on    | off   | on       | on       | on       |
| $3V_{dc}$ | on    | on    | off   | on    | off   | off   | on    | off   | on    | off      | on       | on       |
| 0      | off   | on    | off   | on    | off   | on    | off   | on    | off   | on       | on       | on       |
| $-V_{dc}$ | off   | on    | off   | on    | off   | on    | off   | on    | off   | on       | on       | on       |
| $-2V_{dc}$ | off   | on    | off   | off   | on    | off   | on    | on    | off   | on       | on       | on       |
| $-3V_{dc}$ | off   | on    | off   | off   | off   | on    | off   | on    | off   | on       | on       | on       |
Table 5. switches states of 9-level MLI.

| Level | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{15}$ | $S_{16}$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $V_{dc}$ | on | off | off | off | off | off | off | off | off | off | on | off | off | off | on | on |
| 2$V_{dc}$ | on | on | off | off | on | off | on | off | on | off | on | off | on | off | on | on |
| 3$V_{dc}$ | on | on | off | off | on | on | off | off | on | off | on | off | on | off | on | on |
| 4$V_{dc}$ | on | on | off | off | on | on | on | off | on | off | on | off | on | off | on | on |
| 0$V_{dc}$ | off | on | off | on | off | on | off | on | off | on | off | on | off | on | on | on |
| −2$V_{dc}$ | off | on | off | on | off | on | off | on | off | on | off | on | off | on | on | on |
| −3$V_{dc}$ | off | on | off | on | off | on | off | on | off | on | off | on | off | on | on | on |
| −4$V_{dc}$ | off | off | on | off | on | off | on | off | on | off | on | off | on | on | on | on |

4. Modulation Techniques

Pulse Width Modulation (PWM) technique is used to giving the desired current and voltage to the load. PWM techniques are widely utilized for AC drives because it decreases harmonic current and get maximum output voltage to the load. This is the purpose from all PWM techniques are to getting the required voltage and frequency with decreasing THD. There are different techniques of control and modulation methods utilized for MLI. These techniques classified according to the switching frequency. Selecting the modulation technique is very useful as it decides the harmonic content of the output voltage waveform and current [15]. There are many types of PWM techniques such as SPWM, SVPWM and Selective Harmonic Elimination (SHE). SPWM is the most easy method that can be implemented [16]. In SPWM strategy a reference signal waveform is compared with carrier signal waveform and the intersections between two generate the ‘ON’ & ‘OFF’ states of the switches utilized in the MLI [17]. SPWM technique is divided to the following: (a) In phase disposition (IPD); (b) Phase opposition disposition (POD); and (c) Alternate phase opposition disposition (APOD). In this paper, POD-SPWM method is used to controlling the proposed MLI circuits for various reasons such as: this technique gives better harmonics performances at lower modulation indices [16], to reducing common-mode voltage (CMV) at the output multilevel inverters [21]. Output power and voltage can be changed by modulation index ($M_i$). $M_i$ of the MLI is given by equation (3) [17].

$$M_i = \frac{A_r}{(N - 1)A_c}$$  \hspace{1cm} (3)

where $A_r$ is amplitude of the reference signal (sine wave), $A_c$ is amplitude of the carrier signal (triangular wave), $N$ is number of the levels the frequency modulation index is given by equation (4)

$$M_f = \frac{F_{cr}}{F_m}$$  \hspace{1cm} (4)

where $F_{cr}$ is frequency of carrier wave, $F_m$ is frequency of modulating wave. In three-level cascaded H–bridge MLI, POD-SPWM method consists of two carrier waves (carrier1, carrier2) have the same value of amplitude and frequency (50 kHz). The carrier wave bellows the zero reference (carrier1) is in same phase with carrier wave up the zero reference (carrier1) but it is shifted by 180° from the carrier wave up the zero reference (carrier1) as shown in Figure 3. In the Five, seven and nine level cascaded H–bridge MLI, POD-SPWM method consists of (N-1) carrier waves. The carrier waves bellows the zero reference are in same phase with the carrier waves up the zero reference but they are shifted by 180° from the carrier waves up the zero reference. The pulses are generated by comparison of carrier signals with modulating signal at modulation index ($M_i = 1$) to trigger the switches of inverter for each level.
5. Results and Discussions

The PV-generator system discussed in this paper was simulated in MATLAB and Simulink. A 135 kW PV-array was carried out with this characteristics: \( V_{\text{mpp}} \) was 17.7V x 16 connected in series and \( I_{\text{mpp}} \) was 7.63A (for three, five and nine) levels while for seven level, \( V_{\text{mpp}} \) was 17.7V x 15 connected in series and \( I_{\text{mpp}} \) was 7.63A. DC-link capacitor is connected in parallel with PV to reducing dc voltage ripple and improving the output. The value of DC-link capacitor was 4000\mu F. the load was resistive \( (R_{\text{load}}) \) and is selected to equals the DC resistance of the PV-array at 1000 W/m2 and 25\degree C. The value of \( (R_{\text{load}}) \) is calculated by the equation (5).

\[
R_{\text{load}} = \frac{V_{\text{mpp}}}{I_{\text{mpp}}}
\]  

(5)

In this paper, the Fourier series of output voltage for each levels are implemented to calculating harmonic voltage \( (V_{H}) \) and THD of output voltage theoretically. Angles of output voltage are increased with increasing levels of MLI topologies. Number of angles are equal to the number of H-bridges of MLI. With increasing H-bridges of MLI, \( V_{H} \) decreases and that leads to minimizing THD of output voltage as shown in Table 6 and 7. The switching angles \( (\alpha_{1} , \alpha_{2} , \alpha_{3} , \alpha_{4}) \) used in the numerical calculations are estimated from the simulation of stairs voltage waveforms. The Fourier series of output voltage for three level MLI \( V_{H} \) is RMS harmonic voltage

\[
V_{H} = \sqrt{\left(V_{rms}^{2} - (V_{1rms})^{2}\right)^{1/2}}
\]  

(7)

The Fourier series of output voltage for five level MLI

\[
V_{H} = \frac{4V_{dc}}{n\pi} \left[ \cos(n\alpha_{1}) + \cos(n\alpha_{2}) \right]
\]  

(9)

The Fourier series of output voltage for seven level MLI

\[
V_{H} = \frac{4V_{dc}}{n\pi} \left[ \cos(n\alpha_{1}) + \cos(n\alpha_{2}) + \cos(n\alpha_{3}) \right]
\]  

(10)

The Fourier series of output voltage for nine level MLI

\[
V_{H} = \frac{4V_{dc}}{n\pi} \left[ \cos(n\alpha_{1}) + \cos(n\alpha_{2}) + \cos(n\alpha_{3}) + \cos(n\alpha_{4}) \right]
\]  

(11)

THD of output voltage for each level is calculated by using equation 7 & 8

| Table 6. analysis of RMS voltage and angles. |
|---------------------------------------------|
| level | \( V_{1}(\text{rms}) \) | \( V_{2}(\text{rms}) \) | \( V_{3}(\text{rms}) \) | \( \alpha_{1} \) | \( \alpha_{2} \) | \( \alpha_{3} \) | \( \alpha_{4} \) |
|-------|-------------------------|-------------------------|-------------------------|---------------|---------------|---------------|---------------|
| 3-level | 228 V | 260 V | 125.38 V | 0.688\degree | – | – | – |
| 5-level | 230 V | 238 V | 61.2 V | 0.89\degree | 30\degree | – | – |
| 7-level | 215 V | 218.3 V | 37.8 V | 0.76\degree | 19.224\degree | 41.4\degree | – |
| 9-level | 229 V | 231.2 V | 31.8 V | 0.414\degree | 14.6\degree | 30\degree | 48.8\degree |
Table 7. THD of output voltage without filter.

| THD% | Level of voltage |
|------|------------------|
|      | 3-level | 5-level | 7-level | 9-level |
| Numerical | 55      | 26.8    | 17.6    | 13.9    |
| Simulation | 57.55   | 28.74   | 19.34   | 14.73   |

The harmonics in the output voltage inverter can be decreased by connecting output L, LC or LCL filters as well as MLI. Accordingly, several levels of MLI topologies are utilized to minimizing THD and the drop voltage due to the high inductance of the filters. By using MLI, the THD and the drop voltage of the output voltage are minimized by decreasing the inductance value of L filter used in load side. In this paper, two states of L filter are implemented, variable inductance of L filter and fixed inductance of L filter for the proposed MLI circuits. In case selecting the appropriate inductance value of L filter for the three, five and seven levels to minimizing THD of the output voltage to less than (5%), THD of the output voltage decreases while drop voltage (∆V) increases because using high value of inductance of L filter as shown in Table 8.

If using the inductance value of L filter used in the nine level for the three, five and seven levels, THD of output voltage increases while drop voltage (∆V) decreases because using small value of inductance of L filter as shown in Table 9.

The two above tables show that the inductance value of L filter affects the drop voltage and THD of the output voltage. With minimizing the inductance value of L filter, drop voltage of output voltage minimizes while THD increases. For this reason, MLI is used to minimizing the drop voltage and improving THD of output voltage by decreasing the inductance value of L filter. In the nine level, drop voltage minimizes to (0.06) and THD improves to (1.2) by decreasing the inductance value of L filter to (6 mH) compared with the three, five and seven levels topologies. Drop voltage can be calculated by using equation (12).

\[ ∆V(\%) = \frac{V_{\text{rms (inverter)}} - V_{\text{rms (load)}}}{V_{\text{rms (inverter)}}} \]  

(12)

In this paper, FFT analysis of output voltage is implemented by using the inductance value of L filter used in the nine level for the three, five and seven levels. THD is decreased with increasing level of output voltage. In the three level, THD of output voltage without filter is (57.55%) and with filter is (6.9%) as shown in Figure 4 and 7. In the five level, THD of output voltage without filter is (28.74%) and with filter is (4.13%) as shown in Figures 5 and 8. In the seven level, THD of output voltage without filter is (19.34%) and with filter is (2.93%) as shown in Figures 6 and 9. In the nine level, THD of output voltage without filter is (14.73%) and with filter is (1.2%) as shown in Figures 10 and 11.
In addition, in the nine level, the efficiency is improved to (99.7%) due to the inductance value of L filter is small. In the case of using the inductance value of L filter used in the nine level for the three, five and seven levels, efficiency remains almost constant because the inductance value of L filter is constant. When the inductance value of L filter is large value, the efficiency decreases as show in Table 10.

| Voltage level | Fixed inductance of L-filter | Efficiency | variable inductance of L-filter | Efficiency |
|---------------|-----------------------------|-----------|---------------------------------|-----------|
| 3-level       | 6 mH                        | 99.6      | 30 mH                           | 96        |
| 5-level       | 6 mH                        | 99.67     | 20 mH                           | 97.3      |
| 7-level       | 6 mH                        | 99.6      | 10 mH                           | 98.5      |
| 9-level       | 6 mH                        | 99.7      | 6 mH                            | 99.7      |

The results (drop voltage and efficiency) can be improved by using levels more than the nine level. There are several disadvantages of using level more than nine level such as: increasing size of inverter, cost and increasing number of switches, that makes the process of controlling the switches are difficult and complex.

6. Conclusion

In this paper four MLI topologies are designed and analyzed to improving THD and drop voltage of output voltage for (PVGs) which are (three, five, seven and nine) levels. with using several levels of MLI topologies, THD and drop voltage of output voltage are minimized due to using small value of inductance of L filter used in load side. Also using small value of inductance of L filter, efficiency improves. Here, proved that the nine level is better as compared with others MLI topologies which are three, five and seven levels for this system in terms of THD, drop voltage and efficiency. THD and efficiency are improved and drop voltage reduces with the nine level by using a small value of inductance of L filter. Also, the output voltage reaches to the steady state in less time as compared with others MLI topologies.

7. References

[1] S. Fahad, N. Ullah, A. J. Mahdi, A. Ibeas, and A. Goudarzi, “An advanced two-stage grid connected PV system: A fractional-order controller,” Int. J. Renew. Energy Res., vol. 9, no. 1, pp. 504–514, 2019.

[2] A. J. Mahdi, “Design and Performance Analysis of an on-Grid Photovoltaic Power System Under Iraqi Solar,” J. Eng. Sustain. Dev. Vol., vol. 21, no. 04, pp. 46–57, 2017.

[3] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, “Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H-Bridge Inverter for Photovoltaic System,” IEEE Access, vol. 7, pp. 16504–16524, 2019, doi: 10.1109/ACCESS.2019.2894757.

[4] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, “Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems,” IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4399–4406, 2009, doi: 10.1109/TIE.2009.2029579.

[5] S. J. Lee, H. S. Bae, and B. H. Cho, “Modeling and control of the single-phase photovoltaic grid-connected cascaded H-bridge multilevel inverter,” 2009 IEEE Energy Convers. Congr. Expo. ECCE 2009, no. October, pp. 43–47, 2009, doi: 10.1109/ECCE.2009.5316126.

[6] I. B. F. Citarsa, I. N. W. Satiawan, I. K. Wirajati, and Supriono, “Performance analysis of cascaded h-bridge multilevel inverter using mixed switching frequency with various dc-link voltages,” IOP Conf. Ser. Mater. Sci. Eng., vol. 105, no. 1, 2016, doi: 10.1088/1757-899X/105/1/012003.

[7] S. H. Hosseini, A. Farahkhor, and S. K. Haghighian, “New cascaded multilevel inverter topology with reduced number of switches and sources,” ELECO 2013 - 8th Int. Conf. Electr. Electron. Eng., vol. 2, no. 6, pp. 97–101, 2013, doi: 10.9790/1676-0262636.

[8] K. Dhineshkumar, C. Subramani, A. Geetha, and C. Vimala, “Performance analysis of PV powered multilevel inverter,” Int. J. Electr. Comput. Eng., vol. 9, no. 2, p. 753, 2019, doi:
10.11591/ijece.v9i2.pp753–760.

[9] P. S. Sanjay, P. R. Tanaji, and S. K. Patil, “Symmetrical Multilevel Cascaded H-Bridge Inverter Using Multicarrier SPWM Technique,” 2018 3rd Int. Conf. Converg. Technol. I2CT 2018, pp. 1–4, 2018, doi: 10.1014/I2CT.2018.8529331.

[10] A. H. Mollah, P. G. K. Panda, and P. P. KSaha, “Single Phase Grid-Connected Inverter for Photovoltaic System with Maximum Power Point Tracking,” Int. J. Adv. Res. Electr. Electron. Instructum. Eng., vol. 04, no. 02, pp. 648–655, 2015, doi: 10.15662/ijareecie.2015.0402021.

[11] T. JALA and G. RAO, “A Novel Nine Level Grid-Connected Inverter for Photovoltaic System,” Ijmer.Com, vol. 2, no. 2, pp. 154–159, 2012, [Online]. Available: http://ijmer.com/papers/vol2_issue2/AA022154159.pdf.

[12] A. Ramesh, O. Chandra Sekhar, and M. Siva Kumar, “A novel three phase multilevel inverter with single DC link for induction motor drive applications,” Int. J. Electr. Comput. Eng., vol. 8, no. 2, pp. 763–770, 2018, doi: 10.11591/ijece.v8i2.pp763–770.

[13] A. J. Mahdi, W. H. Tang, and Q. H. Wu, “Improvement of a MPPT algorithm for PV systems and its experimental validation,” Renew. Energy Power Qual. J., vol. 1, no. 8, pp. 611–616, 2010, doi: 10.24084/repq08.419.

[14] B. Xiao, F. Filho, and L. M. Tolbert, “Single-phase cascaded H-bridge multilevel inverter with nonactive power compensation for grid-connected photovoltaic generators,” IEEE Energy Convers. Congr. Expo. Energy Convers. Innov. a Clean Energy Futur. ECCE 2011, Proc., pp. 2733–2737, 2011, doi: 10.1109/ECCE.2011.6064135.

[15] J. Sabarad and G. H. Kulkarni, “Comparative analysis of SVPWM and SPWM techniques for multilevel inverter,” Proc. 2015 IEEE Int. Conf. Power Adv. Control Eng. ICPACE 2015, pp. 232–237, 2015, doi: 10.1109/ICPACE.2015.7274949.

[16] P. Udakhe, D. Atkar, S. Chiriki, and V. B. Borghate, “Comparison of different types of SPWM techniques for three phase seven level cascaded H-Bridge inverter,” 1st IEEE Int. Conf. Power Electron. Intell. Control Energy Syst. ICPEICES 2016, pp. 1–5, 2017, doi: 10.1109/ICPEICES.2016.7853286.

[17] Swagata Banerjee and Biswamoy Pal, “Design of a Three Phase Reduced Switch Multilevel Inverter Based on Different SPWM Techniques,” Int. J. Eng. Res., vol. V4, no. 04, pp. 1418–1424, 2015, doi: 10.17577/ijertv4is041432.

[18] Mdsafia, “Design and Simulation of Grid Connected PV system Using Multilevel Inverters,” Int. J. Electr. Electron. Eng., no. 42, pp. 2231–5184, 2013.

[19] H. Mokhliess et al., “An accurate method for parameters determination of current voltage characteristics of photovoltaic modules,” Proc. 2019 Int. Conf. Comput. Sci. Renew. Energies, ICCSRE 2019, pp. 1–7, 2019, doi: 0.1109/ICCSRE.2019.8807725.

[20] A. A. Zulkefle et al., “Modeling and simulation of nine-level cascaded H-bridge multilevel inverter,” Indones. J. Electr. Eng. Comput. Sci., vol. 11, no. 2, pp. 696–703, 2018, doi: 10.11591/ijeecs.v11.i2.pp696–703.

[21] M. M. Renge and H. M. Suryawanshi, “Multilevel inverter to reduce common mode voltage in AC motor drives using SPWM technique,” J. Power Electron., vol. 11, no. 1, pp. 21–27, 2011, doi: 10.6113/JPE.2011.11.1.021.

[22] N. Rajavinu et al., “Modeling and Design of Five Level Cascaded H-Bridge Multilevel Inverter with DC / DC Boost Converter,” 2013 8th Int. Conf. Electr. Electron. Eng., vol. 4, no. 6, pp. 97–101, 2014, doi: 10.1109/ELECO.2013.6713811.

[23] N. H. Selman and J. R. Mahmood, “Design and Simulation of two Stages Single Phase PV Inverter operating in Standalone Mode without Batteries,” Int. J. Eng. Trends Technol., vol. 37, no. 2, pp. 102–109, 2016, doi: 10.14445/22315381/ijett-v37p102.

[24] E. Babaei, S. Laali, and Z. Bayat, “A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches,” IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 922–929, 2015, doi: 10.1109/TIE.2014.2356601.

[25] A. H. Ali, H. S. Hamad, and A. A. Abdulrazzaq, “An adaptable different-levels cascaded H-bridge inverter analysis for PV grid-connected systems,” Int. J. Power Electron. Drive Syst., vol. 10, no. 2, pp. 831–841, 2019, doi: 10.11591/ijpeds.v10.i2.831–841.
[26] T. Aishwarya, R. Preethi, and R. Boopathi, “FPGA Implementation of Power Quality Improvement Strategy for MLI,” IEEE Int. Conf. Intell. Tech. Control. Optim. Signal Process. INCOS 2019, pp. 1–4, 2019, doi: 10.1109/INCOS45849.2019.8951374.

[27] R. Anand and M. Kamatchi, “A Fifteen Level Cascaded H-Bridge Multilevel Inverter with Reduced Number of Switches,” Int. J. Adv. Eng. Res. Sci., vol. 2, no. 11, 2015.