Strained Germanium Quantum Well PMOSFETs on SOI with Mobility Enhancement by External Uniaxial Stress

Yan Liu¹, Jiebin Niu², Hongjuan Wang¹, Genquan Han¹*, Chunfu Zhang¹, Qian Feng¹, Jincheng Zhang¹ and Yue Hao¹

Abstract

Well-behaved Ge quantum well (QW) p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) were fabricated on silicon-on-insulator (SOI) substrate. By optimizing the growth conditions, ultrathin fully strained Ge film was directly epitaxially grown on SOI at about 450 °C using ultra-high vacuum chemical vapor deposition. In situ Si2H6 passivation of Ge was utilized to form a high-quality SiO2/Si interfacial layer between the high-κ dielectric and channels. Strained Ge QW pMOSFETs achieve the significantly improved effective hole mobility $\mu_{\text{eff}}$ as compared with the relaxed Si and Ge control devices. At an inversion charge density of $Q_{\text{inv}}$ of 2 × 10^{12} cm$^{-2}$, Ge QW pMOSFETs on SOI exhibit a 104% $\mu_{\text{eff}}$ enhancement over relaxed Ge control transistors. It is also demonstrated that $\mu_{\text{eff}}$ of Ge pMOSFETs on SOI can be further boosted by applying an external uniaxial compressive strain.

Keywords: Germanium, MOSFET, Mobility, Quantum well

Background

Germanium (Ge) has been attracting tremendous research interests for future pMOSFET applications due to it possesses the higher hole mobility over Si. Theoretical and experimental results proved that in order for Ge channel transistors to have significantly improved mobility and driving current over their Si and SiGe channel competitors, compressive strain is essential [1–3]. A great deal of efforts were devoted to demonstrating bi-axially strained Ge-based ultrathin quantum well (QW) pMOSFETs [2, 4, 5], which have exhibited the advantages of confining hole in the undoped quantum well, eliminating dopant impurity scattering, and accommodating very high strain in channel. Nonetheless, the development of defect-free SiGe buffer with smooth surface on Si raised a major challenge for Ge devices. It was reported that, by optimizing the growth condition and controlling the film thickness precisely, fully strained Ge channel could be pseudomorphically grown directly on Si and silicon-on-insulator (SOI) [6–8].

Methods

Material Growth

Ge channel was epitaxially grown on lightly doped p-type SOI wafer using ultra-high vacuum chemical vapor deposition tool. Before loading into the growth chamber, the top Si layer was thinned down to about 7 nm using dry oxidation followed by the dilute HF etching. It is well known that, as Ge is epitaxially grown on the low thermal budget device fabrication process, the strain in channel region was maintained, which substantially boosted the transistor performance. Studies showed that the uniaxial compressive strain is also promising for improving the mobility of Ge pMOSFETs [9–11]. However, there is still lack of the study on the combination effects between uniaxial and biaxial strain on Ge pMOSFETs.

In this paper, ultrathin strained Ge QW pMOSFETs on SOI are realized and characterized. Devices achieve the superior hole mobility to the relaxed Si and Ge control transistors. Electrical performance of Ge QW transistors is further improved by applying the external uniaxial compressive strain being parallel to channel direction.

* Correspondence: hangenquan@ieee.org; gqhan@xidian.edu.cn
1 State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China
Full list of author information is available at the end of the article

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Si, Ge islands tend to form in Stranski-Krastanow mode due to the 4.2% lattice mismatch between Ge and Si. The formation of Ge islands could be prevented by decreasing the growth temperature; nevertheless, the misfit dislocations are preferred to appear in Ge layer to release the strain energy. To achieve the continuous and defect-free epitaxial Ge film, we carried out the growth of Ge (the growth of Ge) on ultrathin SOI with different substrate temperatures. During the growth, the flow rate of GeH₄ in a H₂ carrier gas is 20 sccm, the pressure in growth chamber is about 10⁻⁴ Pa, and the growth duration is 5 min. Figure 1 shows the atomic force microscope (AFM) images of Ge film on SOI samples grown at various temperatures. The formation of large numbers of Ge islands was observed on the sample grown at 500 °C. With the reduction of growth temperature to 400 °C, it was found that many nanopits were yielded in Ge layer with the self-assembled growth, which partially released the strain energy. A flat surface was achieved for the Ge layer grown at 450 °C without the observation of any nanostructure. Experiments demonstrated that, as 3~5 nm Ge channel was epitaxially grown on SOI, the transition from 2 to 3D growth mode can be effectively suppressed with the growth temperature ranging from 420 to 450 °C.

Device Fabrication

The key process steps for fabricating ultrathin fully strained Ge QW pMOSFETs are shown in Fig. 2a. After the epitaxial growth of strained Ge layer, Ge channel was treated using in situ Si₂H₆ passivation at 350 °C for 15 min. Gate stack comprising hafnium dioxide (HfO₂) by atomic layer deposition and metal gate by physical vapor deposition was formed. After the gate patterning and etching, BF₂⁺ was implanted into drain and source regions at an energy of 10 keV and a dose of 1 × 10¹⁵ cm⁻². Self-aligned metallic source/drain (S/D) was formed by depositing 10 nm nickel followed by a thermal anneal (RTA) at ~450 °C for 30 s. During the Ni germanosilicide, the p-type dopants in S/D regions were partially activated by the dopant segregation. The residual Ni was removed by the concentrated H₂SO₄ cleaning. Using the similar process, Si and Ge control pMOSFETs on bulk substrates were also fabricated.

Figure 2b shows the cross-sectional schematic of a fabricated Ge pMOSFET. Figure 2c depicts the high-resolution transmission electron microscope (HRTEM) image of metal gate stack on strained Ge channel on SOI. The thicknesses of defect-free Ge channel and HfO₂ dielectric layer are 3.7 and 4.0 nm, respectively.

Fig. 1 AFM images of epitaxially grown Ge on ultrathin SOI at a 500, b 400, and c 450 °C.
Excellent interface quality and a uniform SiO_2/Si interfacial layer (IL) are observed.

**Flexure-Based Bending Setup**

Uniaxial compressive strain was introduced into the Ge QW pMOSFETs on SOI through a mechanical flexure-based wafer bending apparatus. The apparatus is able to perform four-point bending upon chips positioned between loads and support, as shown in Fig. 3. The uniaxial strain was always applied parallel to the channel direction. The channel direction is calculated by \( \sigma = E\gamma t/[2a-(L/2 -2a/3)], \) where \( E \) is the Young’s Modulus, \( y \) is the sample vertical displacement, \( t \) is the total thickness of the sample, \( L \) is the distance between the two supports, and \( a \) is the distance between the support and load [12]. The setup was calibrated with a load cell under the mounting platform and a strain gauge bonding on the sample.

Before measurement, the handle Si of SOI wafer was thinned down to about 300 \( \mu \)m by back side polishing to make sure it can accommodate the large strain. The values of Young’s modulus for Ge along [110] direction is 138 GPa [13].

**Results and Discussion**

Figure 4a depicts the transfer characteristics of a typical Ge QW pMOSFET on SOI with and without external uniaxial compressive stress. The stress is along [110] and parallel to the channel direction. The gate length \( L_G \) of the device is 3.5 \( \mu \)m. Device has a subthreshold swing (SS) of \( \sim 90 \) mV/decade. The uniaxial stress has the negligible impact on the SS and the leakage floor characteristics of the Ge transistor. Here, \( V_{TH} \) is defined as the \( V_{GS} \) at a constant drive current of \( 10^{-7} \) A/\( \mu \)m and a \( V_{DS} \) of \( -0.1 \) V. \( V_{TH} \) is shown to be affected by the applied uniaxial compressive stress. As uniaxial stress is applied, devices exhibit a right shift of \( V_{TH} \). \( I_{DS} = V_{DS} \) curves at different \( V_{GS} = V_{TH} \) for the devices are illustrated in Fig. 4b, which demonstrate the \( I_{DS} \) enhancement in devices under the uniaxial compressive stress. A \( \sim 250 \) MPa uniaxial stress provides a 17% Ge \( I_{DS} \) enhancement in ultrathin Ge pMOSFET on SOI at \( V_{DD} \) of 1.5 V. Figure 4c shows the linear intrinsic transconductance \( G_M \) of the same pair of transistors in Fig. 4a. At \( V_{DS} \) of \( -0.1 \) V, a 24% peak \( G_M \) is achieved in devices under \( -250 \) MPa external uniaxial strain compared to the Ge QW transistor without uniaxial strain.

To evaluate the intrinsic channel piezoresistance characteristics for the Ge QW pMOSFETs, large amount of devices with and without external uniaxial compressive strain were measured with \( L_G \) ranging from 3.5 to 9.5 \( \mu \)m. The total resistance \( R_{total} \) as a function of \( L_G \) extracted at a gate overdrive of \( -1.5 \) V and \( V_{DS} \) of \( -0.1 \) V are plotted in Fig. 5. The intercept of the fitted lines with the \( y \)-axis yields the value of source/drain resistance \( R_{SD} \). \( R_{SD} \) of Ge QW pMOSFETs on SOI is about 14 k\( \Omega \mu \)m, and it is observed that the external uniaxial stress has little impact on \( R_{SD} \). The slope of \( \Delta R_{total}/\Delta L_G \) represents the channel resistance \( R_{ch} \) which is related to the effective hole mobility \( \mu_{eff} \) and inversion charge density. The uniaxially strained pMOSFETs achieve a 24% reduction in \( \Delta R_{total}/\Delta L_G \) slope i.e. \( R_{ch} \) compared to the devices without uniaxial compressive strain. Experiment demonstrates that the impact of external uniaxial strain on inversion capacitance of Ge QW pMOSFETs is negligibly small. Therefore, the decreasing of \( R_{ch} \) is attributed to the improvement in \( \mu_{eff} \) for the transistors with the external uniaxial compressive stress.

\( \mu_{eff} \) is a crucial factor, which affects the drive current and \( G_M \) of the devices. We extracted the \( \mu_{eff} \) using the \( \Delta R_{total}/\Delta L_G \) method. \( \mu_{eff} \) was calculated by \( \mu_{eff} = 1/\left[ WQ_{inv}(\Delta R_{total}/\Delta L_G) \right] \), where \( W \) is the channel width,
$Q_{\text{inv}}$ is the inversion charge density in Ge QW channel, and $\Delta R_{\text{total}}/\Delta L_G$ is the slope of the $R_{\text{total}}$ as a function of $L_G$ plots as shown in Fig. 5. $Q_{\text{inv}}$ in the channel was calculated by integrating the measured $C_{\text{inv}}$ versus $V_{\text{GS}}$ curves. Figure 6 illustrates the $\mu_{\text{eff}}$ as function of $Q_{\text{inv}}$ characteristics of the Ge QW pMOSFETs on SOI with and without a $-250$ MPa uniaxial stress. Comparison of $\mu_{\text{eff}}$ for the Ge QW pMOSFETs with Si and Ge control on bulk wafers is also presented. Ge QW pMOSFETs under uniaxial compressive strain achieve a peak $\mu_{\text{eff}}$ of $897 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. At the low $Q_{\text{inv}}$, Ge QW pMOSFETs under uniaxial compressive strain demonstrate an 18 times higher $\mu_{\text{eff}}$ as compared with Si control devices. At the $Q_{\text{inv}}$ of $2 \times 10^{12} \text{ cm}^{-2}$, Ge QW pMOSFETs without external uniaxial strain demonstrate a 104% $\mu_{\text{eff}}$ enhancement of over the relaxed Ge control device. This is attributed to the fact that the biaxial compressive strain in ultrathin Ge channel leads to the splitting of valence bands, and top valence band populated by carrier has a reduced effective mass than relaxed Ge [14, 15]. It is noted that, under the external uniaxial compressive strain, the Ge QW devices demonstrate a 24% $\mu_{\text{eff}}$ enhancement in comparison with the transistors without external strain. It is speculated that the external uniaxial
compressive strain further decreases the effective hole mobility, leading to the additional mobility enhancement, along transport direction in strained Ge channel.

Conclusions
High-mobility strained Ge QW pMOSFETs with high channel crystallinity on SOI platform are realized. Devices exhibit good transfer and output characteristics and a significantly improved $\mu_{\text{eff}}$ over Si and Ge control pMOSFETs. Ge QW pMOSFETs on SOI obtain a 104% improvement in $\mu_{\text{eff}}$ in comparison with the relaxed Ge control transistors at a fixed $Q_{\text{inv}}$ of $4 \times 10^{12} \text{cm}^{-2}$. Ge QW pMOSFETs on SOI under an external uniaxial compressive strain achieve a further $\mu_{\text{eff}}$ enhancement, contributing to the reduced $R_{\text{ch}}$ and the improved drive current over the transistors without external uniaxial compressive strain.

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Authors’ contributions
YL, HW, and GH carried out the experiments and drafted the manuscript. CZ, QF, JZ, and YH provided constructive advice in the drafting. JN gave kind suggestions about the experiment. GH and YL conceived the study and participated in the experiment design. All the authors read and approved the final manuscript.

Competing interests
The authors declare that they have no competing interests.

Author details
1State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi’an 710071, China. 2Laboratory of Nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China.

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