Performance enhancement by an improved compact design for self-powered synchronous switching harvesting circuits

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Abstract. In the self-powered synchronous switching circuits, the electronic breakers for producing the desired switching control signal consumes a significant part of harvested energy. Moreover, the capacitors used in the electronic breakers brings the effect of decreasing the electromechanical coupling level thus hinders the available power. In this paper, a novel circuit design by combining two separate electronic breaker into a unified one in which only a single capacitor is required and the introduced parasitic capacitance is cut to half. Besides, the diodes in the envelope detectors are also removed. Consequently, both performance enhancement and cost reduction are achieved with this new circuit.

1. Introduction

Interface circuit is an important part of the piezoelectric generator and will significantly affect the performance. The synchronous switching circuits, such as SSHI (Synchronous Switching Harvesting on an Inductor) [1], SECE (Synchronous Electric Charge Extraction) [2], OSECE (Optimized SECE) [3] and so on, are considered as effective approaches for enhancing the generator’s performance in the case of low electromechanical coupling level and providing better adaptability for load variations. A critical issue for these synchronous switching circuits is the self-powered realization. Various methods including electronic breaker [4-6], velocity control [7], mechanical switches [8-10], integrated control circuits [11] etc. were proposed. Among them, the electronic breaker possesses the advantage of simplicity and reliability. Generally, a part of the extracted energy from the generator is consumed by the electronic breaker. Moreover, the parasitic capacitance in the electronic breaker, mainly referred to the envelope detector capacitance, imposes an equivalent effect of connecting a parallel capacitor of several times the parasitic capacitance to the generator, thus decreasing the coupling level. Consequently, the generator’s performance degenerates in contrast with the ideal case.

Reducing the components of the self-powered circuit components while keeping the function could save the energy consumption and would be helpful to the performance. Recently, an alternative SSHI self-powered design has been proposed with fewer diodes used and better performance [12]. However, two capacitators are still used in the circuit for peak detectors. Compared with the diodes, the capacitance plays a more critical role in the by introducing the switching phase lag and decreasing the coupling level.

In this paper, we propose a simpler and more efficient circuit breaker for synchronous switch techniques dedicated to piezoelectric vibration energy harvesters. In comparison with the regular electronic breaker design for the SP-OSECE (Self-Powered OSECE) [6], this new CSP-OSECE (Compact SP-OSECE) circuit multiplexes the comparator in the envelope detector instead of the diode.
More important, only a single capacitor is used for both positive and negative peak detection. The parasitic capacitance of the electronic breaker is thus reduced to half so that the performance is improved.

2. Principle and analysis

Fig. 1 (a) presents the regular SP-OSECE design with the usual electronic breaker. In the circuit, the piezoelectric element is represented by an equivalent current source $i_{eq} = a_0 \dot{u}$ in parallel with an intrinsic capacitance $C_0$ and a leakage resistor $R_0$. Here, $a_0$ is the piezoelectric force factor and $u$ is displacement of the piezoelectric generator. Two separate envelope detectors are used for determining the positive and negative piezoelectric voltage peak respectively. Each envelope detector is composed of an filtering RC network ($R_{pi}$ an $C_{pi}$) and a diode $D_{pi}$. In addition, a PNP transistor $T_{p1}$ is used as the comparator for the positive breaker and a NPN transistor $T_{p2}$ is used as the negative comparator. At the beginning of the positive half-period, both switches $S_1$ and $S_2$ are opened which $C_0$ is charged by $i_{eq}$ with the piezoelectric voltage $V_p$ increasing. Meanwhile, $C_{p1}$ is charged through $R_{p1}$ and $D_{p1}$ with $V_{p1}$ follows $V_p$ while $C_{p2}$ is charged through $R_{p2}$ and $T_{p2}$ as well. After $V_p$ reaches the maximum value and starts to decline, $V_{p1}$ keeps this maximum value. As $V_p$ decreases further, the comparator $T_{p1}$ conducts and output the switching control signal to turn on $S_1$. Consequently, the piezoelectric voltage $V_p$ in the positive half can be approximated as

$$V_p = V_{load} + \frac{a_0 \dot{u}}{m} \int_i^{t+T/2} dt + \frac{a_0 \dot{u}}{C_0} \int_i^{t+T/2} dt$$

in which $a_1 = a_0 C_0 / (C_0 + 2C_p)$ is the modified piezoelectric force factor with $C_{p1} = C_{p2} = C_p$, $t_1$ is the start time of the positive half-period and $T$ is the period. It can be inferred that the piezoelectric force factor $a$ is decreased to $a_1$ by $C_{p1}$ and $C_{p2}$.

Figure 1 (a) SP-OSECE circuit with regular electronic breakers; (b) CSP-OSECE circuit.

In order to enhance the performance, the CSP-OSECE is proposed with a more compact design as seen in Fig. 1 (b). Instead of two separate electronic breakers, a unified one is constructed for both
positive and negative half-periods with a single capacitor $C_p$. Moreover, the comparator transistor $T_{p1}$ of the positive half-period is multiplexed for not only producing the switching signal but also rectifying the current instead of the diode $D_2$ in Fig. 1 (a) while $T_{p2}$ covers the function of $D_2$ in the negative half-period as well. Two friction diodes are plotted with dotted lines in Fig. 1 (b) to indicate the multipurpose usage of the comparators. The current source $I_e$ charges $C_p$ through $T_{p2}$ and $R_b$ in the positive half-period and reversely charge $C_p$ through $T_{p1}$ and $R_b$ in the negative half-period. Both positive and negative voltage peak are reserved on the same capacitor while the comparators works similarly to detect the peak position as before. Fig. 2 presents the voltage waveforms and the switching signal of the two circuits. Easy to find, the CSP-OSECE circuit works the same as the regular SP-OSECE circuit in Fig. 1 (a) with fewer components. Moreover, due to the single capacitor configuration, we can write down the piezoelectric voltage in the positive half-period as

$$V_p = \frac{V_{\text{load}}}{m} + \int_{t_i}^{t_f+T/2} \alpha \frac{\dot{u}}{C_0 + C_p} \, dt = \frac{V_{\text{load}}}{m} + \int_{t_i}^{t_f+T/2} \alpha \frac{\dot{u}}{C_0} \, dt$$

in which $\alpha_2 = \alpha C_p/(C_0 + C_p)$.

By comparing eq. (1) and eq. (2), it is found that $\alpha_2$ is larger than $\alpha_1$, which means that better power performance is expected. It is also seen in Fig. 2 that the CSP-OSECE obtains higher load voltage than the regular SP-OSECE does.

3. Results

In order to verify the performance, a piezoelectric generator is subjected to both SP-OSECE and CSP-OSECE circuits as shown in Fig. 1 (c). The generator’s parameters have been identified as follow: $C_0=14 \text{nF}$, $\alpha=3.1 \text{e-3 N V}^{-1}$, and $M=0.006 \text{kg}$. Here, $M$ is the inertial mass. The resonant frequency is measured to be $41 \text{Hz}$ in the short-circuit case. In addition, the envelope capacitance $C_p$ is selected to be $1.75 \text{nF}$ for both circuits and $R_b$ is set to $3.3 \text{k}\Omega$. The value of $C_p$ is selected to obtain the optimal power performance of the circuits.

The constant displacement case is firstly investigated with the magnitude of $u$ fixed as $1.25 \text{mm}$ and the excitation frequency is selected to be $41 \text{Hz}$ at the resonant frequency. Fig. 3 (a) shows the power results of the two circuits. Clearly, the load dependence properties of the two circuits is close to each other while the optimal power is obtained around $470 \text{k}\Omega$ in both cases. However, the CSP-OSECE obtains much better performance than the SP-OSECE except the small load case. A maximum power
of 0.301mW is obtained for CSP-OSECE with a power increase of 30% in consideration that the SP-OSECE circuit has a maximum power of 0.233mW.

The test with a constant acceleration amplitude of 0.5g was also performed with the optimal load of 470kΩ from 20Hz to 60Hz with the power plotted in Fig. 3 (b). Similar to the constant displacement case, the CSP-OSECE circuit always shows better performance. A power boost of 38% is found around the resonant frequency. Moreover, wide bandwidth is also obtained with the CSP-OSECE circuit.

Fig. 3 Power performance of the generator using two self-powered circuits: (a) in the case of constant displacement amplitude; (b) in the case of constant acceleration.

4. Conclusion

A compact design of the self-powered synchronous switching circuit is proposed in this paper. Compared with the regular SP-OSECE design, the new CSP-OSECE circuit brings two improvements: First, the parasitic capacitance is reduced to half; Second, the circuit has fewer component by excluding the envelope detector diodes. The former improvement is especially useful about the enhancement of the power performance. It is validated by experiments in both constant displacement and constant acceleration cases. Meanwhile, the latter one saves the cost and also assembling space.

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