Research Article

One Clock-Cycle Response 0.5 μm CMOS Dual-Mode ΣΔ DC-DC Bypass Boost Converter Stable over Wide $R_{ESR}$ LC Variations

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Power supplies in portable applications must not only conform and adapt to their highly integrated on-chip and in-package environments but also, more intrinsically, respond quickly to fast load dumps to achieve and maintain high accuracy. The frequency-compensation network, however, limits speed and regulation performance because it must cater to all combinations of filter capacitor $C_O$, inductor $L$, and $C_O$’s equivalent series resistance $R_{ESR}$ resulting from tolerance and modal design targets. As such, it must compensate the worst-case condition and therefore restrain the performance of all other possible scenarios, even if the likelihood of occurrence of the latter is considerably high and the former substantially low. Sigma-delta (ΣΔ) control, which addresses this issue in buck converters by easing its compensation requirements and offering one-cycle transient response, has not been able to simultaneously achieve high bandwidth, high accuracy, and wide $R_{ESR}$ LC compliance in boost converters. This paper presents a dual-mode ΣΔ boost bypass converter, which by using a high-bandwidth bypass path only during transient load-dump events was experimentally 1.41 to 6 times faster than the state of the art in current-mode ΣΔ boost supplies, and this without any compromise in $R_{ESR}$ LC compliance range (0–50 mΩ, 1–30 μH, and 1–350 μF).

1. Introduction

In portable applications like cellular phones, PDAs, and the like, integrated BiCMOS and CMOS switching dc-dc supply circuits reduce cost, size, component count, and design complexity (from a user’s perspective). One of the critical bottlenecks in obtaining a fully integrated solution, however, is the frequency-compensation circuit, which is designed around off-chip power LC filter devices to obtain optimal performance [1]. The fact is mode-rich state-of-the-art applications, manufacturing tolerances, and parameter drifts expose dc-dc converter integrated circuits (ICs) to wide variations in output capacitance $C_O$, power inductance $L$, and $C_O$’s equivalent series resistance $R_{ESR}$, inducing considerable changes in loop-gain and transient response, compromising feedback stability or transient response. As a result, to guarantee stability and high bandwidth with a fixed on-chip frequency-compensation circuit, the design necessarily constrains $R_{ESR}$ LC values within a narrow target range [1]. This is especially detrimental in compact high-performance multiple input-output converters [2, 3], where the on-chip or in-package LC filter is variable by design to dynamically accommodate the diverse loading conditions of the system.

Unclocked or asynchronous sigma-delta (ΣΔ) buck converters [4–8] are self-compensating and free of the speed-stability tradeoffs of most dc-dc converters because the control loop in these converters resembles current-mode control by indirectly sensing the inductor current ripple via the ripple voltage it drops across $C_O$’s $R_{ESR}$. In other words, the ESR voltage mostly sets the terminal ripple voltage of $C_O$, impressing the inductor ripple current information on the output voltage and achieving current-mode-like control. The resulting single-pole-like response yields higher bandwidth and more explicit control over the output ripple voltage [7].
Extending this technique and its benefits to boost converters, which are popular in portable electronics for boosting battery voltages to 3.3–5 V, is not straightforward because the inductor current does not fully flow to \( C_O \). Consequently, in realizing \( \Sigma \Delta \) control in boost converters, the feedback circuit must explicitly sense and mix inductor current with the sensed output voltage [9]. Such techniques, however, resuscitate the limiting speed-stability tradeoffs \( \Sigma \Delta \) control averted in buck converters in the first place, forcing the designer to adjust current and voltage gains thereby reducing the loop bandwidth in order to accommodate large \( R_{\text{ESR}} \) LC filter values.

This paper presents a dual-mode boost \( \Sigma \Delta \) bypass controller IC that overcomes the aforementioned speed-stability compromise by introducing a high-speed bypass mode (and circuit) that engages only during transient load-dump events, achieving both high bandwidth and wide \( R_{\text{ESR}} \)LC compliance. To this end, Section 2 first reviews and discusses the stability requirements of \( \Sigma \Delta \) converters and their resulting transient response to fast load dumps. Section 3 then describes the proposed dual-mode technique and the design of its IC-prototype embodiment, followed by experimental results in Section 4; Section 5 draws relevant conclusions.

2. \( \Sigma \Delta \) Converters

2.1. \( \Sigma \Delta \) Control in Buck Converters. A \( \Sigma \Delta \) buck converter, as shown in Figure 1, controls the frequency and duty cycle of PMOS switch \( S_M \) by comparing ripple output voltage \( v_O \) via sensed voltage \( v_S \) against dc reference \( V_{\text{REF}} \) with comparator \( CP_V \). Operationally, ac inductor ripple current \( i_l \) flows into \( C_O \) and its \( R_{\text{ESR}} \) (which is relatively large in these converters at 100–250 mΩ) to ensure its voltage —\( v_{\text{err}} \)— overpowers ac capacitor voltage \( v_C \) [7] as capacitor displacement current \( i_C \), forcing ac output ripple voltage \( v_O \) to mimic \( i_l \) (\( v_O \approx v_{\text{err}} = i_l R_{\text{ESR}} \)). As a result, in regulating \( v_O \), the converter also regulates \( i_l \), which in the process simplifies the frequency response of the converter to that of a single-pole system, as in current-mode control, guaranteeing stability, irrespective of \( R_{\text{ESR}} \)LC values.

In a positive load-step transient event, when load current \( i_O \) suddenly rises, comparator \( CP_V \) detects the voltage drop. The now larger \( i_O \) induces on \( V_O \) and consequently switches \( S_M \) on indefinitely (i.e., at 100% duty cycle) until \( V_O \) returns within \( CP_V \)’s predefined hysteretic window, which is, within an acceptably low margin of \( V_{\text{REF}} \). During \( S_M \)’s on time, the inductor voltage being nearly constant at \( V_{IN} - V_O \), inductor current \( i_l \) slews in a single switching cycle until it fully supplies \( i_O \) and recharges \( C_O \) back to \( V_{\text{REF}} \) [8]. In other words, only the inductor and capacitor slew-rate limits and second-order delays across the comparator and switch set the response time (effective bandwidth) of the system. Note a negative load dump undergoes a similar but reversed response.

2.2. \( \Sigma \Delta \) Control in Boost Converters. Unlike buck converters, ac inductor ripple current \( i_l \) in boost converters does not flow completely to output capacitor \( C_O \) because reverse-biased diode \( D \) (shown in Figure 2) temporarily disconnects \( L \) from \( V_O \) (and \( C_O \)) when switch \( S_M \) conducts all of \( i_l \) to ground. The resulting ac ripple voltage in \( V_O \) does not fully reflect the behavior of \( i_l \), as it does in buck converters with nonnegligible \( R_{\text{ESR}} \) values, which means that \( \Sigma \Delta \) control in boost converters cannot rely on \( v_O \) alone [9]. The negative feedback loop in a boosting supply must therefore sense, scale, and mix \( i_l \) with \( V_O \) explicitly (e.g., mix \( i_l R_{\text{ESR}} \) and \( v_O s_{\text{LM}} \) into \( R_S \) as scaled sum \( s_{\text{UM}} \)) to achieve current-mode-like control characteristics. A hysteretic comparator then modulates \( S_M \)’s frequency and duty cycle based on how the scaled sum \( s_{\text{SUM}} \) of the ripples compares against a user-defined hysteresis window. Note the voltage feedback loop modulates the effective inductor reference current \( v_{\text{REF}} R/S_{\text{IL}} \), which is also the average inductor current \( i_l \) (or low-pass filtered —LPF— version of \( i_l \)) to whatever is necessary to fully supply \( i_O \).

Within the context of averaged small-signal analysis, the relatively high-gain, low-bandwidth voltage control loop (V Loop) of the system effectively embeds a higher bandwidth, lower gain current loop (I Loop), as shown Figure 3 [10]. At low frequencies, below low-pass filter pole \( p_{\text{LPF}}, i_l R/S \) nearly equals \( v_{\text{REF}} R \) and the gain of the current loop is practically zero, but increasing with frequency until reaching its highest possible gain at frequencies past \( p_{\text{LPF}} \). The current loop’s gain again drops at high frequencies, past the complex LC double poles, when the ac voltage across \( L \) decreases. Given that \( i_l \) is, for all practical purposes, regulated to higher frequencies and therefore is a current source to the outer voltage loop at moderate-to-high frequencies, \( C_O \) and effective load resistance \( R_S \) set the dominant low-frequency pole of the system while \( L \) and \( R_O \) invoke right-half plane zero \( z_{\text{RHP}} \) [11].

For stable conditions to prevail, the unity-gain frequency of the voltage loop (i.e., the system —\( f_{V,0dB} \)—) must fall below \( z_{\text{RHP}} \) and \( i_l \) must remain a current source (i.e., current loop must stay closed with considerable loop gain) for the frequency range of interest to the voltage loop [10]. As such, \( f_{V,0dB} \) must stay below both \( z_{\text{RHP}} \) and current-loop bandwidth \( f_{I,0dB} \):

\[
f_{0dBV} = \frac{g_{mv} D_M}{2\pi R g_{mi} C_O} \ll f_{0dBI} = \frac{R g_{mi} R_S M V_O}{2\pi L}, \quad (1)
\]

\[
f_{0dBV} = \frac{g_{mv} D_M}{2\pi R g_{mi} C_O} < z_{\text{RHP}} = \frac{D_M V_O}{2\pi L_I}, \quad (2)
\]

or

\[
\frac{L_I}{V_O C_O} = \frac{L_I}{C_O V_O D_M} < \frac{R g_{mi}}{g_{mv}}, \quad (3)
\]

where \( D_M \) is the duty-cycle of \( S_M \), \( D_I \) is \((1 - D_M)\), and \( M \) is the modulator gain. Note that \( z_{\text{RHP}} \) and \( f_{I,0dB} \) shift to lower frequencies with increasing inductance values, which means that \( f_{V,0dB} \) must also decrease accordingly, in an ideal case. LPF pole \( p_{\text{LPF}} \), whose location indicates the lowest frequency at which the current loop is closed, must also be below
the worst-case value of $f_{V,0\,db}$ to ensure there is enough gain for $i_L$ to remain a current source:

$$p_{LPF} \approx f_{V,0\,db}[\min] = \frac{D_M^2 V_O}{2\pi L I_L}.$$

Ultimately, the system responds to a load dump at the speed of the voltage loop, whose bandwidth is $f_{V,0\,db}$, allowing switch $S_M$ to cycle multiple times before restoring $v_O$ back to its target window. LPF pole $p_{LPF}$ limits the extent to which $i_L$ naturally responds to a load dump by allowing moderate-to-high frequency ac error-correcting signals through the current loop. In other words, the current loop limits (while attempting to regulate) the rising and falling rates of average $i_L$ below $i_L$’s maximum possible slew-rates of $V_{IN}/L$ and $(V_O - V_{IN})/L$. Because $f_{V,0 \, db}$ and $p_{LPF}$ both decrease with increasing $L$, with the former also decreasing with decreasing $C_O$, the worst-case LC combination, from the perspective of stability, occurs at the highest $L$ and lowest $C_O$, the condition for which gains $R_{J\, g_m \, R_S}$ and $g_m \, R_S$ and pole $p_{LPF}$ are adjusted and transient-response performance over the entire LC filter range is sacrificed.

3. Proposed Dual-Mode $\Sigma\Delta$ Controller IC

The proposed $\Sigma\Delta$ boost controller IC in Figure 4 overcomes the transient-response degradation associated with the worst-case LC combination by bypassing the main voltage loop (and its $f_{V,0\,db}$) with a fast (and lower low-frequency loop gain) feed-forward path only during transient events. The stability requirements of the main loop set the acceptable $R_{ESR,LC}$ range for the system while the high-bandwidth bypass path allows the system to respond in one cycle at the maximum possible inductor current slew rate, the response of which is similar to $\Sigma\Delta$ buck converters. The transient improvement is achieved on chip (i.e., without an off-chip frequency compensation circuit) and without sacrificing LC compliance.

3.1. Steady-State and Bypass Operation. The basic objective of the bypass mode is to override nominal equivalent average inductor current reference $I_{L,(nom)}$ ($V_{REF}/R_I$) to a higher value almost instantly only during load dumps and allow the bypass voltage loop to control and limit how much of the extra current in $L$ flows to $v_O$. Initially, during steady-state conditions, the bypass circuit is inactive and load current $i_O$ and $S_M$’s average off duty cycle $D_M$ (i.e., one minus $S_M$’s average on duty cycle $D_M$) set the nominal average inductor current $I_{L,(nom)}$ required to support a given $i_O$, which is higher than $i_O$ because $S_M$ steers a portion of $i_L$ away from $v_O$ to ground according to $D_M$:

$$I_{L,(nom)} = \frac{I_O}{1 - D_M}.$$ 

In the bypass mode, however, independent loops regulate $i_L$ to a value higher than $I_{L,(nom)}$ and sensed output voltage $v_S$ to $V_{REF}$, as depicted in the equivalent circuit of Figure 5.

The current loop, which modulates switching frequency $f_{SW}$ and $S_M$’s duty cycle $d_M$, has higher bandwidth and appears as a current source for frequencies of interest to the lower bandwidth bypass voltage loop controlling auxiliary switch $S_A$. In the bypass mode, inductor current $i_L$ is regulated at a value $i_{PK}$ or $V_{PK}/R_I$ that is greater than $I_{L,(nom)}$ (i.e., $I_L$ required to support $I_O$). This means, unless otherwise limited, average diode current $i_D$ is now higher than $I_O$, as a result of which $C_O$ recharges quickly. Once $v_O$ is back within the hysteretic window limit of bypass comparator $CP_B$ and about to surpass its upper boundary, $CP_B$ and $S_A$ divert excess current away from $D$ through $S_A$ until $i_O$ again discharges $v_O$ to $CP_B$’s lower window limit. The switching cycle repeats as average inductor current $i_L$ gradually drops back to $I_{L,(nom)}$, at which point the bypass loop stops switching and $S_A$ remains open. Note as long as $I_L$ exceeds $I_{L,(nom)}$, the bypass voltage loop, by independently regulating $v_O$ with higher loop gain than the current loop, ensures that the voltage inputs of summing comparator $CP_S$ are virtually short-circuited (i.e., $v_S \approx V_{REF}$), as shown in Figure 6, allowing $CP_S$ to regulate $i_L$ exclusively.
With respect to stability, as already mentioned, the unity-gain frequency of the current loop \( f_{i,0,\text{dB}} \) must exceed that of the bypass voltage loop \( f_{b,0,\text{dB}} \) so the inductor appears as a current source in the voltage loop, eliminating the complex conjugate pair associated with LC in the voltage loop [12]. Because the unity-gain bandwidth of a \( \Sigma\Delta \) loop is its switching frequency, \( S_M \)'s switching frequency \( f_{i,0,\text{dB}} \) must exceed that of \( S_A \) \( f_{b,0,\text{dB}} \). Therefore, since \( f_{i,0,\text{dB}} \) depends on the rising and falling rates of \( i_L / R_I \) as it traverses \( CP_S \)'s hysteretic current window \( H_I \),

\[
f_{i,0,\text{dB}} = f_{b,0,\text{dB}} = \left( \frac{H_I}{R_I} \right)^{-1} \left( \frac{L}{V_{IN}} + \frac{L}{V_{O} - V_{IN}} \right)^{-1} = \frac{V_{IN}(V_{O} - V_{IN})R_I}{V_{O}H_IL}
\]

\(6\)

and \( f_{b,0,\text{dB}} \) on how fast excess \( i_D \) (i.e., \( D_M I_L - I_D \)) and \( I_O \) charge and discharge output capacitor \( C_O \) between \( CP_B \)'s hysteretic voltage window \( H_V \),

\[
f_{b,0,\text{dB}} = \frac{(H_V(R_1 + R_2))^{-1}}{R_2} \left( \frac{C_O}{I_O} + \frac{C_O}{(D_M R_L - I_O)} \right)^{-1},
\]

\(7\)

to force \( f_{i,0,\text{dB}} \) to be greater than \( f_{b,0,\text{dB}} \), \( C_O \) must exceed

\[
C_O \geq \left( \frac{H_I}{H_V} \right) \left( \frac{I_O L}{V_{O}R_1D_M} \right) \left( \frac{R_2}{R_1 + R_2} \right) \equiv C_{(O,\text{min})},
\]

\(8\)

where the \( R_1-R_2 \) divider represents the effect of the resistive feedback factor on \( H_V \) and \( C_{(O,\text{min})} \) the minimum stable output capacitance.

3.2. Transient Response and Mode Transition. During a positive load-dump event, when \( I_O \) suddenly rises and \( V_O \) droops in response, as shown in Figure 7, the dual-mode converter enters its bypass mode, raising \( i_L \) to peak value \( i_{PK} \) (or \( V_{PK}/R_I \)) in a single switching cycle of \( S_M \). Subsequently \( V_O \) (or \( V_S \)) is pulled back to \( V_{REF} (R_1+R_2)/R_2 \) (or \( V_{REF} \)) in a single switching cycle of \( S_A \). Transient-detect comparator \( CP_T \) in Figure 4 perceives the load dump and engages the bypass mode by sensing when \( V_S \) drops below \( V_{REF} \) by a preset threshold value of \( \Delta V_{BP} \) (e.g., 2.5% of \( V_{REF} \)) (after the delay the comparator requires to switch: \( t_d \)). Then, \( CP_T \) clamps \( V_{REF} \) to peak voltage \( V_{PK} \), the value of which sets the maximum current the circuit can drive. Switch \( S_M \) therefore remains closed \((t_{(M,\text{on})})\) until \( i_L \) reaches \( V_{PK}/R_I \) \((I_{PK})\), the new value of \( v_{REF}/R_I \). After \( S_M \) resumes switching and regulating \( i_L \) about \( I_{PK} \), \( S_A \) remains open and allows all diode current \( i_D \) to flow to \( V_O \) until \( C_O \) recharges to \((V_{REF} + \Delta V_{BP}/2) \cdot (R_1+R_2)/R_2 \). Beyond this point, \( CP_A \) and \( S_A \) regulate \( V_S \) about \( V_{REF} \) by switching \( S_A \), in other words, by steering excess inductor current away from \( C_O \).

Ultimately, output voltage \( V_O \) droops in response to load dump \( \Delta i_O \) until \( i_L \) reaches \( I_{PK} \). First, excess current \( i_O \) discharges \( C_O \) during delay \( t_d \) while \( V_S \) reaches \( V_{REF} - \Delta V_{BP} \). Then, while \( S_M \) raises \( i_L \) from \( I_{L,\text{avg}} \) (or \( V_{REF}/R_I \) or \( I_{L,\text{nom}}(1) \)) to

\[\text{Figure 4: Simplified schematic of the proposed dual-mode } \Sigma\Delta \text{ boost converter.}\]

\[\text{Figure 5: Equivalent circuit of the proposed } \Sigma\Delta \text{ converter in the bypass mode.}\]
$I_{PK}$ (or $V_{PK}/R_1$), $i_D$ is zero and full load current $I_O$ discharges $C_O$, yielding a total variation ($\Delta V_O$) of

$$\Delta V_O = \Delta V_{BP} + \left( \frac{I_O}{C_O} \right) i_{L(M(on)}}$$

$$= \Delta V_{BP} + \left( \frac{I_O}{C_O} \right) \left[ \left( I_{PK} - I_{L(nom)} \right) L \right]$$

$$= \Delta V_{BP} + \left( \frac{I_O}{C_O} \right) \left( V_{PK} - v_{LREF} \right) L$$

(9)

Note that the ratio of $L$ and $C_O$ sets the dominant part of $\Delta V_O$.

Once sensed output voltage $v_S$ is within the hysteric voltage window of $C P_B$, to transition back to steady state, $i_{L(avg)}$ must somehow fall back to whatever value ($I_{L(nom)}$) is necessary to sustain $I_O$, reducing to zero the amount of excess current $i_L$ that bypass comparator $C P_B$ steers away from $v_O$ through $S_A$. To that end, introducing a series negative offset voltage $V_{LOS}$, as shown in Figure 8, ensures that $i_L$ is always above its target (i.e., $i_{L(avg)}$ is greater than $v_{LREF}/R_1$), forcing the loop to gradually decrease both $i_{L(avg)}$ and the excess current. Finally, when $i_L$ is low enough to be able to fully supply $i_O$ and the excess current ($D_{H,L(–I_O)}$) is zero, the bypass loop stops switching (i.e., disengages), which means that the main voltage loop now regulates $v_O$ via $S_M$ (Figure 4) to its target. In other words, henceforth, $i_{L(avg)}$ equals $I_{L(nom)}$.

Note that the transition is continuous, allowing $S_A$ to stop switching without incurring irregularities in $S_M$.

During a negative load dump, when $i_O$ suddenly drops, as also shown in Figure 7, $i_{L(avg)}$ automatically exceeds its new steady-state target and $v_O$ rises above its target. As a result, bypass comparator $C P_B$ engages and diverts current away from $v_O$ until $v_S$ again drops to $v_{LREF} – H/2$ (in one cycle of $S_A$). The circuit gradually transitions back to steady state in the same manner as described earlier, through $V_{LOS}$.

4. Experimental Results and Discussion

4.1. IC Design. The proposed dual-mode $\Sigma \Delta$ bypass converter was designed, fabricated, and evaluated using a 0.5 $\mu$m, 5 V CMOS process. The circuit embodiment of the converter, as shown in Figure 9, employs a differential-signal processing scheme to attenuate the effects of substrate noise on the high-bandwidth $\Sigma \Delta$ loops [10]. For simplicity, series resistor
operating conditions, when \(v_0\) is higher than \(V_{IN}\), as the body diode of the first blocks the current of the second.

The proposed \(\Sigma\Delta\) controller 0.5 \(\mu\)m IC was designed to supply power from a 2.7–4.2 V Li-ion battery and drive a 0–1 A load at 5V \(\pm 5\%\) with as wide an \(R_{ESR/LC}\) range as possible (0–50 m\(\Omega\), 1–30 \(\mu\)H, and 1–350 \(\mu\)F was achieved). The total silicon surface area the IC occupied was 1.9 \(\times\) 2.6 mm (Figure 10). The peak efficiency of the converter was 93% at 0.4A with a biasing quiescent current of 1.5 mA. The total output voltage variation of the converter in response to a 0.1–1A load dump (\(\Delta I_0\)) with 5 m\(\Omega\), 5.6 \(\mu\)H, and 53 \(\mu\)F of \(R_{ESR/LC}\) was 200 mV, which constitutes a 4x improvement over its nonbypassed counterpart under similar conditions (800 mV).

### 4.2. LC Compliance

The measured \(R_{ESR/LC}\) space for which the converter was stable is 0–50 m\(\Omega\), 1–30 \(\mu\)H, and 1–350 \(\mu\)F, as illustrated in Figure 11. This range was determined by subjecting the converter to 0.1–1A load dumps with 100 nanoseconds rise and fall times. The stability limit was observed as a loss of regulation for the proposed \(\Sigma\Delta\) converter in the bypass mode, as the bypass loop was no longer able to control the loop, and subharmonic oscillations for the nonbypassed (state-of-the-art) \(\Sigma\Delta\) boost converter [14].

The stability limits for both converters, with and without the bypass path, are reached when their respective current-loop bandwidths \((f_{BL0 dB})\) approach their voltage-loop counterparts \((f_{V0 dB}\) and \(f_{V0 dB}^{\text{dB}}\)), as that is when \(L\) ceases to be a current source for the voltage loop, be the main loop, or the bypass loop. As a result, because \(f_{V0 dB}\) and \(f_{BL0 dB}\) increase with decreasing \(C_O\) and increasing \(I_O\) and \(f_{BL0 dB}\) and RHP zero \(\Delta H\) decrease with increasing \(L\) and decreasing \(V_{IN}\), the highest \(L-I_O(30 \mu H-1A)\) and lowest \(C_O-V_{IN}\) (12 \(\mu F-2.7\) V) combination constitutes worst-case conditions. Since \(R_{ESR}\) essentially introduces a left-half plane zero in the voltage loop, increasing \(R_{ESR}\) also increases \(f_{V0 dB}\) and \(f_{BL0 dB}\), which means that the above-mentioned limits along with the highest \(R_{ESR}\) value (50 m\(\Omega\)) describe the worst-case stability point of the converter. In other words, \(C_O(\text{min})\) increases with increasing \(L\), \(I_O\), and \(R_{ESR}\) and decreasing \(V_{IN}\).

The maximum capacitance was limited to 350 \(\mu\)F as a practical limit for the intended portable application space (the circuit is stable at higher \(C_O\) values). Similarly, the maximum \(R_{ESR}\) value was limited to 50 m\(\Omega\) to keep the output voltage ripple acceptably low under a 1A load. Under these conditions and constraints, the stability spaces for the proposed and the state-of-the-art converters are approximately equal in “volume.”

### 4.3. Transient Load-Dump Performance

As shown in Figure 12(a), the transient-response variation of \(v_0\) (\(\Delta v_0\)) in response to 0.1–1A load dumps (\(\Delta I_0\)) with 100 nanoseconds rise and fall times under 2.7 V, 5.6 \(\mu H\), 53 \(\mu F\), and 5 m\(\Omega\) of \(V_{IN}\), \(L\), \(C_O\), and \(R_{ESR}\) was 200 mV for the proposed dual-mode scheme and 800 mV for its single-mode state-of-the-art counterpart. While the proposed converter responds by increasing \(i_L\) above its target (to \(I_{PK}\) or \(V_{PK}/R_1\))
in one switching cycle of $S_M$, the state-of-the-art circuit increases $i_L$ gradually, pulling $v_O$ back to regulation in several cycles of $S_M$, which is why the proposed solution exhibits a fourfold improvement over its predecessor. In a negative load-step (Figure 12(b)), while the excess inductor current is immediately bypassed by switch $S_A$ in the proposed converter keeping the output voltage overshoot low (<75 mV), the excess inductor energy causes a large voltage overshoot (600 mV) in the state-of-the-art converter.

Decreasing (increasing) $L$ increases (decreases) the rate at which $i_L$ responds to a load dump, as shown in Figure 13, thereby decreasing (increasing) the time $v_O$ slews (reducing $\Delta v_O$). Similarly, increasing (decreasing) $C_O$ decreases (increases) $v_O$’s droop rate in response to a load dump (Figure 14). Note that increasing (decreasing) $C_O$ also increases (decreases) the delay time between the load step and the onset of bypass threshold voltage $\Delta V_{BP}$ ($t_d$) (Figure 7), which is why the onset of $i_L$ rising shifts with $C_O$.

Although transient-response performance for the proposed dual-mode scheme improves with decreasing $L$, the same is not true for the single-mode converter whose $i_L$ response time is limited by the bandwidth of the loop, not $L$’s slew rate. As a result, as illustrated in Figure 15, the percentage improvement that the dual-mode enjoys over its single-mode counterpart increases with decreasing $L$: 6- and 1.43-fold improvement at 1 μH–36 μF and 30 μH–36 μF, respectively.
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Figure 15: Measured transient output voltage variation \( \Delta v_O \) under various LC combinations in response to 0.1–1 A load dumps (\( \Delta i_O \)) for the proposed dual-mode and state-of-the-art single-mode \( \Sigma \Delta \) converters.

Increasing \( C_O \) decreases \( v_O \)'s transient droop in both converter cases, except that bypass threshold voltage \( \Delta V_{BP} \) effectively limits the extent to which a larger \( C_O \) decreases \( \Delta v_O \) in the proposed scheme. In the limit, increasing \( C_O \) to such an extent that \( \Delta v_O \) is less than \( \Delta V_{BP} \) would prevent the bypass mode from ever engaging. As a result, the performance improvement in \( \Delta v_O \) is lower between the proposed and state-of-the-art solutions at higher \( C_O \) values: \( \Delta v_O \) for the proposed and state of the art asymptotically converge as \( C_O \) increases.

4.4. Mode Transition. Figures 16 and 17 illustrate how the proposed dual-mode \( \Sigma \Delta \) bypass boost converter transitions from steady state to bypass mode and back in response to positive and negative 0.1–0.6 A load dumps with an LC combination of 15 \( \mu \)H and 53 \( \mu \)F. As designed, the bypass mode...
ripple is larger at ±70 mV (±(H_v/2)·(R_1 + R_2)/(R_2 A_{DV}) ≈ ±140 mV/2) or ±1.4% than the steady-state counterpart, which is at ±15 mV or ±0.3%. During a positive load dump (Figure 16), when I_O suddenly rises, a load-induced drop in V_O exceeding the ΔV_{BP} limit engages the bypass mode and increases I_L to 2.5 A (I_{PK}) in one switching cycle of S_M. As determined by offset V_{LOS}, the circuit then takes approximately 2.5 ms to gradually decrease I_L back to its new target of roughly 1.3A, at which point S_A stops switching and the converter is back in steady state. During a negative load dump (Figure 17), I_L is automatically above its target and S_A consequently starts diverting some of I_L back to V_{IN} almost immediately, until 2.5 ms later, when I_L drops to its new target.

The main drawbacks of the auxiliary bypass path are the silicon real estate, power, and switching noise associated with power switch S_A. The latter two shortcomings, however, are more often than not inconsequential because they only occur during transient events, which are typically sporadic, short, and seldom occur without significantly affecting the steady-state power efficiency (Figure 18). The prominent disadvantage of the proposed solution is therefore additional silicon real estate for S_A because it carries substantial current. The transient-performance benefits of S_A and the bypass path that drives it, however, offset this cost.

5. Conclusion
A dual-mode ΣΔ bypass boost dc-dc controller 0.5μm CMOS IC that is stable for an R_{ESR}LC filter range of 0–50 mΩ, 1–30 μH, and 1–350 μF and responds to positive and negative load dumps in one switching cycle has been proposed, designed, fabricated, and evaluated. The driving feature of the foregoing solution is a robust on-chip (i.e., smooth transitioning) ΣΔ bypass path that responds only during transient load dumps. While the converter increases inductor current I_L in one switching cycle in response to a sudden rise in load current I_O and uses it to quickly slew output capacitor C_O back to its target, it also limits how much of I_L flows to C_O in the case of a negative load dump, when I_O drops, limiting the total transient variation of output voltage V_O and therefore improving accuracy performance. The transient-response benefits of the proposed scheme, as compared to state-of-the-art single-mode ΣΔ converters, are the highest at low values of L (e.g., 6x at 1 μH and 1.41x or 40% improvement at 30 μH) because L limits how fast I_L rises and falls to its targets. The main drawback of the proposed technique is the additional silicon real estate required for auxiliary power switch S_A, which is partially (and often completely) offset by its improved accuracy performance. In summary, the proposed dual-mode ΣΔ bypass boost converter is fast, widely LC compliant (robust), and easily implementable.

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