A mechanism for balancing accuracy and scope in cross-machine black-box GPU performance modeling

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Abstract
The ability to model, analyze, and predict execution time of computations is an important building block that supports numerous efforts, such as load balancing, benchmarking, job scheduling, developer-guided performance optimization, and the automation of performance tuning for high performance, parallel applications. In today’s increasingly heterogeneous computing environment, this task must be accomplished efficiently across multiple architectures, including massively parallel coprocessors like GPUs, which are increasingly prevalent in the world’s fastest supercomputers. To address this challenge, we present an approach for constructing customizable, cross-machine performance models for GPU kernels, including a mechanism to automatically and symbolically gather performance-relevant kernel operation counts, a tool for formulating mathematical models using these counts, and a customizable parameterized collection of benchmark kernels used to fit models to GPUs in a black-box fashion. With this approach, we empower the user to manage trade-offs between model accuracy, evaluation speed, and generalizability. A user can define their own model and customize the fitting process, making it as simple or complex as desired, and as application-targeted or general-purpose as desired. As application examples of our approach, we demonstrate both linear and nonlinear models; these examples are designed to predict execution times for multiple variants of a particular computation: two matrix-matrix multiplication variants, four Discontinuous Galerkin (DG) differentiation operation variants, and two 2-D first-order finite difference computation variants. For each variant, we present accuracy results on GPUs from multiple vendors and hardware generations. We view this highly user-customizable approach as a response to a central question arising in GPU performance modeling: how can we model GPU performance in a cost-explanatory fashion while maintaining accuracy, evaluation speed, portability, and ease of use, an attribute we believe precludes approaches requiring manual collection of kernel or hardware statistics.

Keywords
Performance model, GPU, Microbenchmark, Code generation, Black box, OpenCL

1 Introduction
Maximizing computational performance requires tailoring an application implementation to the target architecture. As a result, obtaining and maintaining good performance in a heterogeneous computing environment necessitates the ability to efficiently decide between multiple mathematically equivalent program variants. Being able to model, interpret, and predict the execution time of computational kernels can provide insight into factors contributing to computation cost, and doing so in an automated, architecture-independent fashion is a key step toward the automation of performance tuning for complicated, modern, vector-based, massively parallel processor architectures including recent CPUs and GPUs.

GPUs, originally designed for rapid graphics rendering, have highly parallel single instruction, multiple thread (SIMT) architectures that make them particularly useful for data-parallel problems. Over the last decade, general purpose GPU programming has risen in popularity. GPUs are increasingly prevalent in the worlds fastest supercomputers, and are being utilized in an expanding body of applications including machine learning and artificial intelligence. GPU programming has been facilitated by the release of general purpose GPU programming systems, including Nvidia CUDA in 2007 and the Open Computing Language (OpenCL) in 2009 [Munshi et al. 2011] Nvidia, CUDA 2015.

Tailoring a performance model to a particular computation on a single hardware device may yield high accuracy. When broadening the scope of architectures and computations targeted by a model, achieving high accuracy becomes increasingly difficult. We present a mechanism for putting the user in control of this trade-off between model accuracy and generalizability with an approach for creating custom performance models that is realized on top of, though technically not dependent on, a program transformation system.

We consider this contribution a building block to provide guidance in exploring the vast search space of possible and, from the point of view of the result, equivalent program variants, by either a developer or an auto-tuning compiler. We view the models constructed within our framework as more economical alternatives to evaluating execution time of computational kernels than, for example, using actual on-device timing runs. Our system primarily targets execution on modern GPU

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hardware, as exposed in, for example, the CUDA or OpenCL compute abstractions. To facilitate portability and maximize ease of use, the system makes few assumptions about the internal organization of the hardware, and device-specific parameters are obtained from a black-box model-fitting process that needs to run precisely once per model per hardware device used. We demonstrate that this cross-machine, black-box, microbenchmarking approach to analytical performance modeling can predict kernel execution time well enough to determine which of multiple implementation variants will yield the shortest execution times.

We review related performance modeling work in Section 9. and discuss two recent surveys of the current GPU performance modeling landscape, [Madougou et al. (2016) and Lopez-Novoa et al.] (2015). Like the survey authors, we find that many existing GPU performance models predict well for a particular application or architecture but are not easily portable. Most require knowledge of hardware or application characteristics, often gathered manually, and significant effort to construct and use. Compared to analytical approaches, learning and statistical techniques tend to be more hardware-flexible, but the models produced are less accessible to users from the standpoints of both design and interpretability: assumptions and limitations about model predictive power, fidelity, and range of applicable programs and hardware tend to be less clear. Madougou et al. (2016) conclude that software utilizing these methods may be difficult to use for users without good knowledge of statistical methods. None of the approaches we surveyed provide users any significant control over the model expression or microbenchmark design.

The following combination of factors distinguishes our work from previous GPU performance prediction work:

- Our approach allows a level of customization of the mathematical model not available in previous work. A user can define their own model, making it as simple or as complex as desired, as application-targeted or as general-purpose as desired.
- Similarly, our approach allows for complete customization of the set of measurement computations used to compute the model parameters during the model fitting process.
- We automate the gathering of all performance-relevant kernel features used to model execution time. These features are gathered pre-compilation by examining our polyhedrally-based program representation.
- We model execution time with very limited explicit representation of hardware characteristics and behavior. The only hardware statistic required is the sub-group size, which is 32 on all current Nvidia and AMD hardware generations.
- Models created using our approach are hardware vendor- and generation-independent, and we demonstrate performance on an AMD GPU and four generations of Nvidia GPUs.
- Models created using our approach are amenable to human understanding: through the exposed parameters and their known meanings, it becomes possible to reason about which parts of kernel execution cost are attributed to which specific operations.
- By making use of a polyhedrally-based program representation, we obtain precise counts of various units of work performed by a program. The counts obtained are parametric in the problem size, allowing us to amortize counting work over repeated applications of the model to the same kernels with varying problem size. Possibilities exist for extensions to data-dependent control flow, but are beyond the scope of this contribution.

## 2 Illustrative Example

Consider the following simple, illustrative example use case. Suppose a user wants to model and predict the execution time of square matrix-matrix multiplication on a GPU. In this case, we will only predict execution times for a single program variant employing an algorithm which divides each matrix into 16 × 16 tiles and avoids some repeated access to global memory by prefetching these tiles into local memory shared between threads before performing the multiplication and addition.

We construct this kernel using LOOPY, a programming system for array computations that targets CPUs, GPUs, and other, potentially heterogeneous, compute architectures. This system keeps the mathematical intent of a computation strictly separated from the computational minutiae. To attain that goal, LOOPY realizes programs as objects in a host programming language (Python in this concrete case) that can be manipulated from their initial, “clean,” mathematical statement into highly device-specific, optimized versions via a broad array of transformations.

### 2.1 OpenCL Machine Model

Program representation in LOOPY relies on the OpenCL machine model [Munshi et al. (2011)] for semantics, and typical GPU hardware mappings thereof inspire the models we use to demonstrate our approach. A very brief overview of the OpenCL machine model will introduce terminology used throughout the following discussion.

The OpenCL model considers two levels of concurrency, each explicitly exposed to the abstraction by the programmer in the form of a multi-dimensional grid. Each integer point in the grid is called a work-item. A rectangularly-indexed set of work-items forms a work-group, and a rectangularly-indexed set of work-groups forms a grid (or NDRange), which is the unit in which work is submitted to the abstraction. Aside from barrier synchronization across the work-items in a work-group, individual work items are assumed to be independent.

Item indices within a work-group are termed local indices or local IDs, and indices of a work-group in the grid are termed group indices or group IDs. We will use symbols like lid(0) to denote the local ID along axis 0 and gid(1) to denote the group ID along axis 1. We assume, in keeping with implementations available in the marketplace, that work-groups are
implemented by first mapping contiguous work-items along the lowest-numbered axis to adjacent SIMD lanes, subsequently to simultaneous multithreading (SMT), and finally to sequential execution. Likewise we assume that work-groups are mapped to individual execution cores, potentially mapping multiple work-groups onto one core depending on capacity.

2.2 Kernel Creation and Transformation

The following Python code constructs the matrix multiplication kernel described above using LOOPY. First, we specify the mathematical intent:

```python
knl = lp.make_kernel("[i,j,k]: 0<=i,j,k<n)
  c[i,j] = sum(k, a[i,k]*b[k,j])")
```

Without any code transformations, LOOPY produces a sequential algorithm looping over each index, as in the following OpenCL code:

```opencl
float acc;
for (int j = 0; j <= -1 + n; ++j)
  for (int i = 0; i <= -1 + n; ++i)
    acc = 0.0f;
    acc += a[n*(16*i + j) + k] * b[n*k + j];
  c[n*i + j] = acc;
```

Next, we add loop-splitting transformations:

```opencl
knl = lp.split_iname(knl, "i", 16)
knl = lp.split_iname(knl, "j", 16)
knl = lp.split_iname(knl, "k", 16)
knl = lp.assume(knl, "n >= 1 and n % 16 = 0")
```

Each `split_iname` transformation divides one loop into two nested loops with the inner loop iterating over the specified number of index values (16). Without knowledge about the value of n, LOOPY would need to add several conditional statements to prevent out-of-bounds array access. We avoid these conditionals by adding the `assume` transformation, yielding the following OpenCL code:

```opencl
float acc;
for (int j_out = 0; j_out <= ...)
  for (int i_out = 0; i_out <= ...)
    acc = 0.0f;
    acc += a[n*(16*i_out + j_out) + k] * b[n*k_out + k_in] * c[n*(16*gid(1) + lid(1)) + 16*gid(0) + lid(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
```

Finally, we add prefetching transformations:

```opencl
knl = lp.add_prefetch(knl, "a", ["i_in","k_in"])
knl = lp.add_prefetch(knl, "b", ["k_in","j_in"])
```

The two prefetching transformations load data from the specified array into local memory outside of the specified loop, yielding the following OpenCL kernel:

```opencl
float acc;
acc = 0.0f;
__local float a_fetch[16*16];
__local float b_fetch[16*16];
for (int k_out = 0; k_out <= ...)
  for (int k_in = 0; k_in <= 15; ++k_in)
    acc = acc + a_fetch[16*lid(1) + k_in] * b_fetch[16*gid(1) + k_in] * c[n*(16*gid(1) + lid(1)) + 16*gid(0) + lid(0)];
```

2.3 Model Creation, Fitting, and Evaluation

For simplicity in this example, suppose we only aim to predict execution times for a single program variant, so a very simple mathematical model may suffice. We model the execution time as

\[ t(n) \approx p_{madd} \cdot f_{madd}(n), \]

where \( n \) is matrix width, \( f_{madd}(n) \) is the number of multiply-add (madd) sequences executed by the algorithm, \( p_{madd} \) is a hardware-dependent parameter representing the effective cost (seconds) per madd for this program variant, and \( t(n) \) is execution time. We distinguish madd sequences from isolated multiplication or addition operations since many GPUs provide a specialized fused multiply-add operator. We refer to quantitative kernel characteristics used in our models as kernel features. Input features, e.g., \( f_{madd}(n) \), appear in the model function, and output features, e.g., \( t(n) \), are produced when evaluating a model function.

Our methods for automatically producing symbolic counts like \( f_{madd}(n) \) in the form of piecewise quasi-polynomials will be discussed in Section 5.1. Now we need a value for parameter \( p_{madd} \).

To determine this parameter value while treating the GPU as a black-box, we run measurement computations designed to reveal the appropriate cost. In this simple
example we need the effective madd cost only for this particular program variant, so we determine this cost by running the same matrix multiplication variant on various sizes of matrices, computing $f_{\text{madd}}(n)$ and $t(n)$ for each, and then fitting our model to the data to compute $p_{\text{madd}}$. More complex models that employ a microbenchmark approach to determine parameter values will be discussed in Section 8.

The following code fragments demonstrate how this is accomplished using our framework.

1. Define the model shown in Equation 1 by specifying wall time on the Nvidia GTX Titan X GPU as the output feature $(f_{\text{cl_wall_time_nvidia_geforce})$, and providing the model expression. $p_{\text{f32madd}}$ represents parameter $p_{\text{madd}}$ and $f_{\text{op_float32_madd}}$ specifies input feature $f_{\text{madd}}(n)$:

```python
model = Model("f_cl_wall_time_nvidia_geforce", "p_f32madd * f_op_float32_madd")
```

2. Generate measurement kernels for model calibration using our parameterized collection of kernel generators, UIPiCK, which we describe in Section 7.1. To govern which generators are used and which kernel variants are produced by each generator, we pass filtering tags to the kernel collection identifying the desired computation and describing, for example, the data type of the arrays, the work-group dimensions, whether to prefetch data into local memory, or whether to assume that work-group dimensions divide evenly into the corresponding array dimensions. In this example, we generate square matrix multiplication kernel variants:

```python
filter_tags = [
    "matmul_sq", "dtype:float32", "prefetch:True",
    "lsize_0:16", "lsize_1:16", "groups_fit:True",
    "n:2048,2560,3072,3584",
]
```

```python
m_knls = KernelCollection UIPick.ALL_GENERATORS).
```

```python
m_knls = m_knls.generate_kernels(filter_tags)
```

Generator filter tags, consisting of a single value, e.g., matmul_sq, determine which generators run. This kernel collection includes all UIPiCK generators, but the matmul_sq tag filters out generators not executing a square matmul. In this case, only generators with a tag matching the user-supplied generator tag, matmul_sq, will execute, which leaves us with a single generator. Variant filter tags consist of argument:value pairs, e.g., dtype:float32, and determine which kernel implementation variants are produced by the generators. Each generator maintains criteria defining a set of allowable values for each argument and generates one kernel for each set of arguments in the Cartesian product of allowable argument value sets. By passing a variant filter tag with argument values, the user can reduce the set of allowable values for that argument. In this example, we provide a set of four values for the problem size $n$ and a single value for each of the remaining arguments, so four measurement kernels will be generated. We discuss kernel set generation and filtering further in Section 7.1.

3. Compute input and output feature values for all measurement kernels:

```python
m_knl_feature_values = gather_feature_values(model, m_knls)
```

Here we compute the two feature values found in our model, madd count and execution time, for each of the four measurement kernels. This uses our automatic kernel statistics gathering techniques described in Section 5.1.

4. Fit model to feature value data, producing parameter values:

```python
model_param_values = fit_model(model, m_knl_feature_values)
```

We describe this fitting process in Section 7.2.

5. Use model to predict execution time for a kernel:

```python
exec_time = model.eval_with_kernel(model_param_values, test_knl, ("n": 1024))
```

Figure 1 displays the actual execution times and model predictions obtained in this example on an Nvidia GTX Titan X GPU. OpenCL version and other platform information is available in Table 2. In this case we sacrifice breadth of model applicability to achieve very accurate predictions with a very simple model by using measurement kernels that are very similar to our target computation. Examples in Section 8 will demonstrate more complex models that use large sets of microbenchmark measurement kernels to determine larger numbers of parameter values, and predict execution time for multiple kernel variants.

3 Overview of the Contribution

There are three main components to our framework. UIPiCK, our parameterized collection of kernels, contains kernel generators that produce the customized set of measurement computations used to fit model parameters. LOOPY, our kernel creation and transformation engine, enables both construction of our measurement kernels and extraction of their statistics. PERFLEX, our performance modeling tool, enables custom model construction from user-defined parameters and kernel features, as well as model fitting and evaluation.
Figure 2 shows the process for creating and fitting a model. First, the user creates a model as an arithmetic expression in terms of some subset of the available PerfLEX features. Second, the user provides a list of filtering tags to UIPiCK, which generates a measurement kernel set. Then PerfLEX gathers feature values for each kernel in the set and fits the model to the feature value data. This produces model parameter values, which the user can then use, along with the model, to produce execution time predictions for new kernels. UIPiCK generators use LoopY to create and transform measurement kernels, and PerfLEX uses LoopY’s statistics-gathering routines when computing kernel feature values.

We organize this contribution as follows. In Section 4, we discuss limitations of our approach and a few assumptions we make. In Section 5 we present our procedure for automated extraction of performance-relevant kernel statistics. We include a brief overview of the kernel transformation engine, LoopY. In Section 6 we introduce a set of kernel features derived from these statistics that form the basis of models constructed using our framework. In Section 7 we describe how UIPiCK produces a customized set of measurement kernels based on user-provided filtering tags, and PerfLEX enables custom model creation and fitting. In Section 8 we evaluate the predictive power of several performance models we create using PerfLEX and UIPiCK on five GPUs from various hardware generations and vendors. Lastly, in Sections 9 and 10 we compare our approach to related work and summarize our conclusions.

4 Assumptions and Limitations
The modeling system as presented has considerable generality and extensibility, as the set of expressions usable for modeling is unbounded in size, and the set of program features is user-extensible. For evaluation of our system, we focus on cost-explanatory models of performance, i.e. models that seek to explain execution time of a kernel as a sum of costs, each of which is given by an empirically determined coefficient multiplied by an operation count for a particular type of operation. In keeping with this view, we make only very limited use of nonlinearity. Importantly, this is a feature of our evaluation and our preferred choice of model, not necessarily of the system itself. It is true however that the preference for such models has biased the set of kernel features that are built into the system by default.

The typical use case we envision for the performance models in this paper is to serve as a pruning heuristic for an optimization procedure that considers computationally (or even algorithmically) different but mathematically equivalent versions of a given kernel. This gives rise to our key criterion for evaluation, for which we (here, manually) produce program variants and evaluate the degree to which our model provides correct guidance for ranking the execution time of the kernels presented to it. Succeeding at this task would make the model an effective pruning strategy, as it would permit us to efficiently rule out parts of an autotuning search space, without having to rely on execution of the actual program. This does not mean that the tuning process must be entirely execution-free. In fact, as we demonstrate, important accuracy gains are available if we allow for additional, on-line measurement runs that obtain calibration parameters for features not thus far encountered.

As a secondary objective, we evaluate the accuracy with which our models predict overall execution time, in terms of relative error. In a broad overview of the literature, discussed in Section 5 no known performance model is able to consistently attain better than single-digit percentages of relative error. Thus we evaluate our models to be roughly consistent with this standard and view departures from it as a sign of potential modeling issues.

Lastly, we evaluate the interpretability of our models. While, for our stated purpose, we are most interested in the relative ranking of various program variants, we choose execution time rather than ranking as our primary model output. Ranking-based approaches (e.g., Chen et al. (2018)) have seen considerable success, however discerning contributions to their prediction output poses a considerable challenge. We only consider models that have a simple, mostly linear form in terms of potential cost contributions. We define interpretability of our models as the degree to which the fitted model is consistent with the cost-explanatory point of view. For example, models that require negative weights are inconsistent with the notion of ‘cost’, as carrying out additional operations of any type should never result in a cost reduction. Taken together, these factors enhance reliability and trustworthiness of our methods.

A further aspect of ensuring reliability is a statement of the conditions under which we can expect our models to satisfy the criteria above. An important class of performance effects relate to machine utilization. For example, the peak rate of floating point operations feasible on a given machine varies with the number of cores in use, or, analogously, the number of vector lanes used within a subgroup/warp/wavefront/SIMD vector. The sizes of available on-chip state space (register, scratchpad) may impact utilization of scheduling slots, which in turn may impact the degree to which latency may effectively be hidden. These are examples of effects that our models do not (and cannot) account for. In return, the elementary cost coefficients that our models obtain by fitting are readily interpretable, e.g., by comparisons with the reciprocal of memory bandwidth and peak FLOP rate.

In cases of less than full utilization, our models can still be used as the computation in question remains in steady state, essentially increasing the cost of a single operation to account for less-than-optimal utilization. In cases of genuinely varying utilization, the only viable path is to shrink the modeling granularity (e.g., to a single core or SIMD lane) until the variation in utilization is no longer relevant. We note that this is not at all an uncommon assumption. The ‘execution-cache-memory’ (ECM) family of models (Treibig and Hager 2010) is based around similar considerations and calls this a
Figure 2. An overview of the performance modeling process.

'speed of light' assumption. To maximize probability of achieving full machine utilization, nearly all of the measurement kernels used to fit the models demonstrated here, as well as the kernels whose execution time we model, use work-groups of size 256.

The set of features available by default in our modeling framework is the source of a further set of limitations and assumptions that merit discussion. The majority of these features are based on the detection of a specific type of operation (e.g., a floating point operation, or a specific type of memory access) and an accounting of the number of times that the cost of the operation is incurred through repeated execution of the site of the operation. To estimate the latter quantity, we assume that the program under consideration exhibits static (i.e., non-data-dependent) control flow that is accurately represented by the polyhedrally-given loop domain. Data-dependent loop control flow could in principle be handled by allowing user-supplied ‘average’ trip counts, but we defer this to future work. Further, any conditionals present in the code are accounted for by summing the cost contribution of both branches, matching the cost behavior of GPUs under divergent control flow. All of our kernel generators accept tags allowing a user to specify assumptions, e.g., that the relationship between a particular index bound and relevant workgroup dimensions eliminates the need for conditionals that would otherwise be necessary to avoid out-of-bounds array access. We use these to minimize the number of conditionals in the measurement kernels and test kernels.

The cost of memory access is particularly challenging to predict. Effects that may contribute to this circumstance include the interaction of caches and locality (statement-to-statement as well as vector), and contention in the setting of banked memory. We have further observed that array sizes above a certain threshold (e.g., 1 GiB on our AMD hardware) can severely impact performance. We make no attempt to model the implementation details of each target machine’s memory subsystem. Instead, we take a two-pronged approach (Section 6.1.1). For simple types of memory access whose cost we expect to generalize across programs, we offer descriptive classification by, e.g., interlane stride, utilization ratio, and data width. Notably, our ability to determine these is predicated on the (multi-dimensional) array subscript being quasi-affine, as they rely on polyhedrally-based reasoning. For more complex access patterns, we permit the memory access cost to be measured by executing the memory access in isolation including its loop environment, retaining an additive accounting of cost. Our mechanism enabling this approach will be discussed further in Section 7.1.1.

5 Gathering Kernel Statistics

Our methodology to automatically gather the kernel statistics underlying kernel features that are used by our modeling process leverages the LOOPY (Klöckner 2014, 2015) programming system in a number of ways:

- we express our kernels in its intermediate representation based on a generic OpenCL/CUDA-style machine model,
- we use its program transformation vocabulary to obtain computationally different but mathematically equivalent variants of our measurement kernels,
- we use it to generate OpenCL C-level source code for the various target machines on which we evaluate our model. While LOOPY is able to target a much larger range of output languages (e.g. C, OpenMP+SIMD, OpenCL, ISPC, CUDA), we limit ourselves to only OpenCL in keeping with our focus on GPUs, and finally,
- we make use of LOOPY’s polyhedrally-based internal representation to support the automatic extraction of kernel statistics.
Algorithm 1 Determine per-kernel count of per-statement operation.

for each statement $s$ in the kernel do
  Compute projection $\pi_s(D)$ of loop domain $D$ onto set of loop indices in which $s$ resides.
  Obtain symbolic count $|\pi_s(D)|$ of integer points in projection (piecewise quasi-polynomial representing number of times statement will be executed).
  Count operations $(n_{ops,s})$ occurring in single instance of statement $s$ (e.g. by traversing left- and right-hand-side expressions).
end for

Find the overall count for the desired operation as

$$n_{ops} = \sum_{\text{Statement } s} |\pi_s(D)| \cdot n_{ops,s}. \quad (2)$$

We note that the statistics-gathering piece of our work is notionally independent of our modelling process in the sense that, while it is convenient to have the ability to automatically extract the kernel features being used in our models, it is not technically necessary and could be achieved either by hand or in a technologically different manner.

5.1 Counting Kernel Statistics

The basic mathematical primitive underpinning our data gathering strategy is the ability to count the number of integer points in a subset of the $d$-dimensional integer tuples $\mathbb{Z}^d$ specified by affine inequalities connected in disjunctive normal form (i.e., a disjunction of conjunctions of affine inequalities). The output of this operation is a piecewise quasi-polynomial in terms of problem size parameters that may occur as part of the specification of the set of integers. E.g., the number of integer points $(i,j)$ in 

$$\{ p=c_i \text{\ and } p=c_j+1 \} = 1/2*(n^2 + p^2 - 2*n*p + n - p).$$

We make use of the barvinok library in conjunction with the isl library (Verdoolaege 2010) to perform this operation, with a fallback to a less accurate, simpler counting technique that is used should barvinok not be available. barvinok in turn is based on Barvinok's algorithm (Barvinok 1994).

To obtain a count of, e.g., a certain kind of memory access, we proceed as in Algorithm 1.

Some counting operations require ancillary processing. For instance, determining the number of floating point operations or memory transactions of a certain data type requires knowing the result data type, which is provided by a type inference pass. We also identify multiply-add sequences in expression trees since some processors support a fused multiply-add operation. When counting global memory accesses, we track the global and local stride components, which we obtain via an analysis of the array index components. Counting arithmetic operations within array indices is optional.

Operations counted using Algorithm 1 carry an implicit count granularity specifying whether they are to be counted once per work-item, sub-group, or work-group.

Algorithm 2 Determine accessed index footprint $F_v \subset \mathbb{Z}^d$ for variable $v$.

Let $v$ be a $d$-dimensional array

for each statement $s$ in the kernel do
  Compute the projection $\pi_s(D)$ of the loop domain $D$ onto set of loop indices in which $s$ resides.
  for each access $j$ to $v$ in statement $s$ do
    Determine the multi-dimensional index mapping $I_j : \mathbb{Z}^d \rightarrow \mathbb{N}_0^d$ that takes a tuple of loop variables to the accessed indices. For example, the access $a[2s+1, j+1]$ would have an index mapping of $I_j(s,j) = (2s - 1, j + 1)$.
  end for
end for

Find the overall accessed footprint as

$$F_v = \bigcup_{\text{Statement } s, \text{ access } j} I_j(\pi_s(D)).$$

On-chip operations, i.e., arithmetic and local memory access, are counted per sub-group, and global memory operations are counted per work-item, with the exception of global memory accesses with lid(0) stride 0 (multiple threads access the same memory location), which we refer to as uniform accesses and count on a per-sub-group basis. This counting scheme necessitates the only user-provided hardware statistic required by any part of our approach, the sub-group size.

Practically speaking, many different operation counts are extracted at once and maintained in a mapping of operation kinds to operation counts. The map keys contain characteristics of each operation for later computation of the kernel features discussed in Section 6.1 and the map values are piecewise quasi-polynomials. All arithmetic and the map values are piecewise quasi-polynomials. All arithmetic in Equation 2 is then carried through to the values of the mapping and performed symbolically on the piecewise quasi-polynomials therein. Once these quasi-polynomial counts are determined for a particular kernel, they can be cheaply reevaluated for changed problem sizes, represented as domain and kernel parameters.

In addition to total operation counts, data motion features in PERFLEX models, discussed in Section 6.1.1 may specify the ratio of array access count to accessed data footprint. This footprint is found as shown in Algorithm 2. The construction of the index map $I_j$ and the computation of the union crucially rely on the polyhedral primitives in our approach.

We count local memory accesses just as we do global memory accesses. We can acquire some statistics by simply querying a LOOPY kernel object, like work-group sizes and counts.

Counting barrier synchronizations requires yet another approach, as these are not apparent in LOOPY code without a schedule. The schedule is found automatically by a search procedure and determines the ordering of statements and the nesting of loops, which enables a subsequent procedure that determines synchronization.
locations. Once a schedule is obtained and barriers are placed, the counting process proceeds much as above, using the schedule information to obtain the relevant set of loop indices on which to project. Unlike with data movement and floating point operations, the resulting count is the number of synchronizations encountered by a single work-item.

Aside from enabling automatic computation of kernel features used in PERPLEX models, this operation-counting LOOPY module is a useful tool for code analysis and algorithm development.

6 Modeling Kernel Execution Time

We model execution time, or more generally any feature, as a function of user-defined parameters and other kernel features, i.e.,

\[
T_{\text{wall}}(\mathbf{n}) = \text{feat}^\text{out}(\mathbf{n}) \\
\approx g \left( \text{feat}^\text{in}_0(\mathbf{n}), \ldots, \text{feat}^\text{in}_i(\mathbf{n}), p_0, \ldots, p_k \right),
\]

where \text{feat}^\text{in}(\mathbf{n}) is a kernel-dependent piecewise quasi-polynomial that uses domain parameters in the vector \(\mathbf{n}\) to account for the number of units of a particular characteristic of a kernel (e.g., the number of single-precision flop/s), \(p_i\) is a machine-dependent parameter related to hardware behavior, and \(g\) is a function provided by a user that is differentiable with respect to the parameters. When creating a PERPLEX model, the user provides an output feature and model expression.

6.1 Kernel Features

A kernel feature is a function that accepts a kernel and a set of domain parameters and returns a number. An input feature is a feature that appears in a model expression, like \(f_{\text{madd}}(n)\) in the example model described by Equation [1], and an output feature is a feature produced when evaluating a model, like execution time.

PERPLEX uses the operation counting approach described in Section 6.1 to compute features, most of which are fully parametric in the sense that once a symbolic representation like \(f_{\text{madd}}(n)\) has been determined from a kernel expressed in LOOPY’s internal representation, it can be cheaply reevaluated for changed values of the domain parameter vector \(n\). We cache these symbolic representations for quick reuse, and PERPLEX distinguishes between situations where a cached symbolic representation for a feature can be immediately reevaluated using a changed \(n\), and situations where additional processing using the new problem sizes is required. For example, when a characteristic of a feature is specified using inequality constraints involving a problem size parameter, e.g., stride \(< n\), the count cannot be reused for new values of \(n\) without using the new \(n\) value to checking the inequality.

When creating a model in PERPLEX, the user specifies an output feature and a model equation containing input features. Each feature is denoted by a string beginning with the prefix \(f_\) as shown in the matmul example in Section 2.8. The first section of the string determines the feature class, and the remainder determines specific characteristics of that feature. For example, we might expand our matmul model to incorporate two types of memory access costs as follows:

```
model = Model("f_cl_wall_time_nvidia_geforce",
  "p_f32madd * f_op_float32_madd +",
  "p_f32l * f_mem_access_local_float32 +",
  "p_f32g * f_mem_access_global_float32")
```

This model now contains one operation feature, two memory access features, and one synchronization feature. We provide a built-in set of features, discussed in the following sections, which we have found sufficient to accurately model execution time in a variety of computations. PERPLEX users can also create their own custom features.

6.1.1 Data Motion Features

For most types of computational kernels, data motion is the dominant cost. We account for this with a family of memory access features, each member of which has a set of characteristics affecting its cost. We refer to these characteristics collectively as a memory access pattern; they include

- the memory type, e.g., local or global,
- the direction, e.g., load or store,
- the size of the data type accessed, e.g., 32-bit or 64-bit,
- the local and global strides along each thread axis in the array index, i.e., strides \(gs_0, gs_1, \ldots, ls_0, ls_1, \ldots\) in flattened array index \(\text{array}[gs_0*gid(0) + gs_1*gid(1) + \ldots + ls_0*lid(0) + ls_1*lid(1) + \ldots]\) (recall that we assume these indices are affine),
- and the ratio of memory accesses to accessed data footprint (access-to-footprint ratio, or AFR). I.e., a ratio of 1 means every element in the footprint is accessed one time and a ratio greater than 1 means that some elements are accessed more than once.

Changes to any aspect of a memory access pattern may affect cost, particularly for global memory access. As an extreme example, consider the difference between the patterns for matrices \(a\) and \(b\) in the example in Section 2.8.

```
for (int k_out = 0; k_out <= ((-16 + n) / 16); ++k_out)
  ... 
  a_fetch[...]
  b_fetch[...] 
```

The local strides and AFRs are the same for both arrays, and the loop variable strides and global strides are different, as shown in Table 1. We could incorporate these as separate features into our model as follows:

```
model = Model("f_cl_wall_time_nvidia_geforce",
  "p_f32madd * f_op_float32_madd +",
  "p_f32l * f_mem_access_local_float32 +",
  "p_f32g * f_mem_access_global_float32")
```

We provide a built-in set of features, discussed in the following sections, which we have found sufficient to accurately model execution time in a variety of computations. PERPLEX users can also create their own custom features.
When defining a data motion feature, the user may also specify a memory access tag to match a particular memory access by name. We could tag the global loads in our LOOPY matmul kernel as aLD and bLD as follows:

```
knl = lp.make_kernel(
    "(i,j,k): 0<=i,j,k<n",
    "c[i,j] = sum(k, aLD*a[i,k]*bLD*b[k,j])"
)
```

and then define features counting these loads as follows:

```
model = Model("f_cl_wall_time_nvidia_geforce",
    "p_f32madd * f_op_float32_madd + "
    "p_f32ga * f_mem_access_tag:aLD + "
    "p_f32gb * f_mem_access_tag:bLD + "
    "p_f32gc * f_mem_access_global_float32_store"
)
```

To compare the costs of these two reads from memory, we create two microbenchmark kernels, each of which reads a global array using an access pattern matching the a or b fetch pattern. In Section 7.1.1 we introduce a tool we provide that could be used to create these microbenchmarks. We choose array sizes large enough that overhead and other costs not associated with the read are negligible. When we run them on the Nvidia GTX Titan X GPU varying matrix width n from 2048 to 3584, we observe an average cost per load for the b pattern kernel that is consistently 4-5 times higher than that of the a pattern kernel. Platform information is available in Table 2.

Observe that these two accesses only differ in their global (i.e., work-group-to-work-group) stride and the stride of the loop variable. Analytical models would have to account for many undocumented machine details (e.g., work-group scheduling) to account for these differences. This example provides evidence that aspects of GPU execution not discoverable to a black-box model can strongly influence performance of global memory access. Since it is difficult to rule out the possibility that any change in a global memory access pattern will affect execution cost on some hardware, we create a unique kernel feature for nearly every different global memory access pattern found in kernels we wish to model. With this approach, a universal model for all kernels on all hardware based on kernel-level features like ours would need a prohibitively large number of global memory access features and corresponding measurement.

### 6.1.2 Arithmetic Operation Features

While execution time for many computations is dominated by data movement, arithmetic operations also contribute, sometimes significantly, to overall execution time. We account for these costs with a family of features that count arithmetic operations. Each operation is characterized by the operation type, e.g., addition, multiplication, or exponentiation, and the data type, e.g., float32 or float64. A 32-bit floating point multiplication operation feature, for example, could be specified in a model string as \( f_{op}\_{float32\_mul} \). The models we demonstrate in this work do not include integer arithmetic features; in the kernel variants modeled, integer arithmetic is only used in array index computation, a cost that can be reduced to negligible levels by, e.g., the compiler performing common subexpression elimination.

### 6.1.3 Synchronization Features

Local barriers in GPU kernels halt execution of every thread within a work-group until all threads have reached the barrier and can contribute to execution time. Additionally, launching a kernel incurs a constant overhead cost. We account for these costs with a family of synchronization features. Synchronization types include local barriers and kernel launches. Recall that the statistics gathering module counts the number of synchronizations encountered by a single work-item, so depending on how a user intends to model execution, they may need to multiply a synchronization feature like local barriers by, e.g., the number of work-groups, a feature discussed in the next section. A user might incorporate synchronization features into this model as follows:

```
model = Model("f_cl_wall_time_nvidia_geforce",
    "p_f32madd * f_op_float32_madd + "
    "p_barrier * f_sync_barrier_local + f_thread_groups + "
    "p_launch * f_sync_kernel_launch"
)
```

### 6.1.4 Other Features

We provide a few other built-in kernel features in PERFLEX. By executing OpenCL kernels containing no instructions and varying the number of work-groups launched, we learned that average execution time increases with the work-group count. This was true on all 5 GPUs we tested, listed in Table 2. We allow PERFLEX models to account for this cost by providing a thread groups feature, the total work-group count. We also provide an OpenCL wall time feature, which accepts a platform, e.g., nvidia, and device, e.g., geforce and when evaluated, executes several trials of the kernel on the specified device to obtain an average wall time. We measure kernel execution time excluding any host-device transfer of data. This feature is typically chosen as the output in our model expressions.
Based on the feature examples provided in the preceding sections, a complete model might be expressed as follows:

```python
model = Model("f_cl_wall_time_nvidia_geforce",
    "p_f32madd * f_op_float32_madd + "
    "p_f32l * f_mem_access_local_float32 + "
    "p_f32ga *
    f_mem_access_global_float32_load_lstrides
    :0:1:1:15:0:af:0 + "
    "p_f32gb *
    f_mem_access_global_float32_load_lstrides
    :0:1:1:15:0:af:1 + "
    "p_f32gc *
    f_mem_access_global_float32_load_lstrides
    :0:1:1:15:0:af:0 + "
    "p_barrier * f_sync_barrier_local * f_thread_groups + "
    "p_group * f_sync_barrier_local + "
    "p_launch + f_thread_groups + ")
```

6.2 Model Parameters

Feature values, as discussed in the previous sections, are kernel-dependent, whereas parameter values are hardware-dependent. For example, the parameter \( p_{\text{f32madd}} \) in Equation 1 passed as \( p_{\text{f32madd}} \) to the example PERFLEX model in Section 2.3 is the coefficient of the madd count in the model, representing the effective cost per madd. Identifiers of parameters in model expressions begin with prefix \( p_\) followed by a unique user-defined string of characters used to distinguish the parameter from others. We determine parameter values using the fitting process described in Section 7.

7 Fitting Model Parameters

To avoid the need for machine architecture performance knowledge and to promote model portability and customizability, we treat the GPU as a black box and knowledge and to promote model portability and customizability, we treat the GPU as a black box and facilitate both analysis of kernel cost components and generation of relevant microbenchmarks.

7.1 Parameterized Collection of Kernels

UIPiCK includes a large collection of kernel creation functions, each capable of producing multiple implementation variants of a particular LOOPY kernel. These include computations designed to exercise a particular feature, e.g., single-precision floating point multiplication or a particular memory access pattern, as well as more complex application-oriented computations, e.g., performing a transpose or multiplying two matrices. Arguments passed to a creation function determine which variant of a particular computation is produced. Arguments may include, for example, thread group dimensions, array dimensions, data type, or whether to perform a particular LOOPY transformation like prefetching or loop unrolling. Our transformation engine, LOOPY, discussed briefly and demonstrated in Section 2, enables this automated creation and transformation of kernels.

While a user can use kernel creation functions directly to produce LOOPY kernels, UIPiCK also provides a tag-driven filtering interface to facilitate production of large sets of measurement kernels matching specified characteristics. To do this, we provide a collection of kernel generators, each of which corresponds to a kernel creation function. Each generator maintains a collection of filtering tags of two varieties.

Generator filter tags determine which generators are used and consist of a single value that identifies a characteristic of the computation, e.g., \texttt{matmul_sq} or \texttt{flops_mul_pattern}. The generators matching the user-provided generator filter tags, according to a generator match condition, will execute. The generator match condition specifies whether (1) a generator’s filter tag must be identical to the user-provided tags, (2) a generator’s filter tag must be a subset of the user-provided tags, (3) a generator’s filter tag set must be a superset of the user-provided tags (default), or (4) the intersection of a generator’s filter tag set and the user-provided tags must be non-empty.

Variant filter tags consist of argument:value pairs, e.g., \texttt{dtype:float32}, and determine which kernel variants each generator produces. For each argument, a generator maintains criteria defining a set of allowable values, e.g., the \texttt{prefetch} argument might allow the set \{\texttt{True}, \texttt{False}\}, and the \texttt{lsize0} argument might allow the set \{1, 2, 4, 8, 16, 32, 64, 96, 128, 160, 192, 224, 256\}. When executed, the generator generates one kernel for each set of arguments in the Cartesian product of allowable argument value sets. By passing a variant filter tag with argument values, a user reduces the set of allowable values for that argument.

For example, recall the filter tags used in the matmul example in Section 2.3:

```python
filter_tags = [
    "matmul_sq", "dtype:float32", "prefetch:True",
    "lsize_0:16", "lsize_1:16", "groups_fit:True",
    "n:2048,2560,3072,3584"]
```

Here, the generator filter tag \texttt{matmul_sq} yields a single generator. We then provide a single value for each variant filter tag associated with that generator, except array size \( n \), for which we provide a set of four values. The Cartesian product of these sets contains four sets of argument values. These four sets each contain a different value for \( n \) and are otherwise identical, so all four kernels produced will perform the same square matmul with a different \( n \) value. These variants will all operate on 32-bit floating point data, perform a prefetching operation that fetches 16 \( \times \) 16 tiles from global memory, and assume that workgroup dimensions fit evenly into array dimensions, which prevents conditionals. If we were to omit, for example, the tag \texttt{prefetch:True}, we would instead obtain 8 kernels; for each problem size UIPiCK would generate one kernel that performs prefetching and one that does not. We could include more generators by adding additional generator filter tags and passing the desired generator match condition to our kernel collection.

7.1.1 Kernel Work Remover One tool we provide to facilitate both analysis of kernel cost components and generation of relevant microbenchmarks, is
We can use the work remover as follows to isolate the
global load from b:

```c
knl = remove_work(knl, remove_vars=["a", "c"])
```

This removes as much of the on-chip work as possible, as well as global memory accesses to the variables specified, producing the following OpenCL code:

```c
float acc;
acc = 0.0f;
__local float a_fetch[16*16];
__local float b_fetch[16*16];
for (int k_out = 0; k_out <= ((-16 + n) / 16); ++k_out) {
    barrier(CLK_LOCAL_MEM_FENCE);
    a_fetch[16*1ld(1) + 1ld(0)] = a[n*(16*gid(1) + lid(1)) + 16*k_out + lid(0)];
    b_fetch[16*1ld(1) + 1ld(0)] = b[n*(16*k_out + lid(1)) + 16*gid(0) + lid(0)];
    barrier(CLK_LOCAL_MEM_FENCE);
    for (int k_in = 0; k_in <= 15; ++k_in)
    acc = acc + a_fetch[16*1ld(1) + k_in] + b_fetch[16*k_in + 1ld(0)];
} c[n*(16*gid(1) + 1ld(1)) + 16*gid(0) + 1ld(0)] = acc;
```

Observe that the b access pattern is unchanged. We include the seemingly unnecessary global store to read_tgt_dest to ensure that instructions with unused results are not dropped by an optimizing compiler. To maximize model accuracy, this store will also need to be represented by a feature in the model; it uses a fairly typical access pattern for which we can automatically generate measurement kernels. We also include writes to global memory matching this pattern in our arithmetic operation and local memory access measurement kernels (discussed in the next section) for the same reason.

7.1.2 Measurement Kernel Design UIPiCK users can choose from generators that we provide, and may also create measurement kernel generators to fit a specific purpose. To fit the models demonstrated in Section 8 we use measurement kernels designed to reveal the cost of individual kernel features. A few fundamental examples of these microbenchmarking kernels follow.

Global memory access: We employ two varieties of measurement kernels designed to exercise global memory access. First, for access patterns simple enough to be fully specified by the local strides, global strides, and data size, we provide a generator that automatically constructs measurement kernels exercising the desired access pattern. As discussed in Section 7.1.1, these patterns are specified via the user-provided variant filter tags. In these kernels, each work-item performs a global load from each of up to 4 input arrays using the specified access pattern. Each work-item then stores the sum of the input array values it fetched in a single result array, e.g., with two load arrays, result[0] = in0[1] + in1[1]. Variant filter tags provided for these kernels specify the data type, global memory array size, work-group dimensions, number of input arrays, and thread index strides.

Second, to generate measurement kernels exercising more complex access patterns, e.g., memory accesses inside nested loops or with AFRs not equal to one, we use the work removal approach described in the previous section. We provide generators that use this tool to create microbenchmark kernels exactly matching these more complex patterns. We use memory access tags as discussed in Section 6.1.1 to identify these accesses in both the measurement kernel and the corresponding PERFLEX model feature. Variant filter tags provided for these kernels include those used to specify the original application kernel, as well as tags specifying whether to remove on-chip work and which work to remove.

Arithmetic operations: In measurement kernels designed to exercise an arithmetic operation, we first have each work-item initialize 32 local variables of the specified data type. It then performs a loop in which each iteration updates each variable using the target arithmetic operation on values from other variables. We unroll the loop by a factor of 64 and arrange the variable assignment order to achieve high throughput using the approach found in the Scalable Heterogeneous Computing (SHOC) OpenCL MaxFlops.cpp benchmark (Danalis et al. 2010). In this approach, the 32 variable updates are ordered so that no assignment depends on the most recent four instructions. After the loop completes we sum the 32 variable values and store the result in a global array according to a user-specified memory access pattern. As discussed in Section 7.1.1, we include these global stores to ensure that instructions with unused results are not dropped by an optimizing compiler.
Local memory access: In measurement kernels designed to exercise local memory access, each work-item initializes one element of a local (shared within work-groups) array to the data type specified. It then performs a loop, at each iteration moving a different element from one location in the array to another. We avoid write-races and simultaneous reads from a single memory location, and use an \( \text{ld}() \) stride of 1. After the loop completes, each work-item writes one value from the shared array to global memory. While our framework allows local memory access features to be characterized by thread index strides, we do not use these strides to differentiate local memory accesses in the demonstrations presented here. Instead, we use a single feature for all 32-bit local memory accesses occurring in measurement kernels and modeled kernels. Variant filter tags provided for this kernel include the data type, global memory array size, iteration count, and work-group dimensions, which determine the local strides for local memory access as well as the size of the local array. 

Other features: When creating the measurement kernel sets used to fit the models demonstrated in Section 8, we also generate variants of a measurement kernel that executes a variable number of local barriers, a measurement kernel similar to that described in Section 7.4 that reveals operation overlapping behavior, and a measurement kernel that launches a specified number of work-groups performing no operations. We set problem sizes to attain execution times between 1 and 1000 milliseconds, with the exception of the empty kernel generator, which produces some kernels launching as few as 16 work-groups in order to reveal the kernel launch overhead.

7.2 Computing Model Parameters

After creating a model and generating a measurement kernel set, we collect feature values for each measurement kernel and then fit the model to the data by minimizing the Euclidean norm of the residual in the nonlinear least squares problem

\[
g(p) \approx t,
\]

where the residual is defined as follows:

\[
r(p) = t - g(p), \quad \tau_k(p) = t_k - g_k(p)
\]

\[
g = g_0, \ldots, g_n, \quad p = p_0, \ldots, p_m, \quad t = t_0, \ldots, t_n
\]

Here, \( n \) is the number of measurement kernels, \( m \) is the number of model parameters, \( p_i \) is the \( i \)-th model parameter, \( g_k \) is the model function containing feature values for the \( k \)-th measurement kernel, and \( t_k \) is the output feature value for the \( k \)-th measurement kernel. Solving this problem involves creating the Jacobian:

\[
J : j_{ki} = \frac{\partial g_k}{\partial p_i}
\]

If the user is more concerned about relative prediction error than absolute prediction error, they may call `scale_features_by_output()` on the feature data before fitting, which divides each input feature value by the corresponding output feature value and sets the output feature values to 1. We perform this scaling in all examples discussed in this work.

7.3 Predicting Performance

After obtaining model parameter values using the fitting process just described, we can compute a predicted output feature (e.g., execution time) for a LOOPY kernel. This requires a dictionary of kernel arguments, i.e., problem size variable values, to compute the kernel feature values, which are used along with the parameter values to evaluate the model as demonstrated in the example in Section 2.3.

```python
model_param_values = fit_model(model, m_knl_feature_values)
exec_times = model.eval_with_kernel(model_param_values, test_knl, {"n": 1024})
```

The model evaluation time scales approximately linearly with the number of features and parameters.

7.4 Modeling Operation Overlap

As a GPU schedules subgroup execution, data movement between main memory and the processor may overlap with on-chip operations like arithmetic, and we can create nonlinear models in Perflex that model this behavior. If on-chip operations and global memory transactions overlap completely, execution time

\[
t \approx \max(c_{\text{gmem}}, c_{\text{on-chip}}),
\]

where \( c_{\text{gmem}} \) and \( c_{\text{on-chip}} \) are the time costs of global memory transactions and on-chip operations, respectively. Since Perflex models must be differentiable, we cannot use this approach directly. Instead, we use a differentiable function \( \hat{s}(x) \) approximating the step function

\[
s(x) = \begin{cases} 
0 & \text{if } x < 0, \\
1 & \text{if } x \geq 0,
\end{cases}
\]

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```python
model_param_values = fit_model(model, m_knl_feature_values)
exec_times = model.eval_with_kernel(model_param_values, test_knl, {"n": 1024})
```

The model evaluation time scales approximately linearly with the number of features and parameters.
We conclude that, at least for this kernel, on-chip-off-chip operation costs are hidden behind global memory transactions and on-chip operations as well. Figure 3 shows a comparison between $s(x)$ and $\hat{s}(x)$ with $p_{edge} = 10$.

To demonstrate the effectiveness of this technique, we create a measurement kernel in which we can vary the ratio of local to global memory accesses. In this kernel, each thread performs one 32-bit global load, followed by $m$ 32-bit local memory load-store sequences, followed by one 32-bit global store. By varying $m$, the ratio of local to global memory accesses, we control whether the execution time is dominated by global or local memory transactions.

When $m$ is small, on-chip costs may be hidden behind global memory transactions; as $m$ increases, eventually local memory transactions dominate execution time. We model this using a PERFLEX model based on Equation 5 with $c_{\text{gmem}}$ and $c_{\text{on-chip}}$ being expressions containing PERFLEX features and parameters representing the global and local memory access costs. Figure 4 displays how PERFLEX fits such a model to this data. We observe that the extent to which local memory transaction costs in this kernel are hidden behind global transaction costs varies significantly across machines. On the Nvidia Tesla K40c and Nvidia Tesla C2070 GPUs, very little, if any, of the local access cost is hidden, while on the Nvidia Titan V, Nvidia GTX Titan X, and AMD Radeon R9 Fury GPUs, the cost of anywhere from 4 to 12 local memory accesses can be hidden behind a global transaction. We conclude that, at least for this kernel, on-chip-off-chip operation overlap behavior varies across GPUs, and that a PERFLEX model based on Equation 5 can model this behavior. We will discuss results for another kernel variant where this overlap behavior varies across GPUs in Section 8.4. OpenCL version and other platform information is available in Table 2.

To obtain average execution times, we evaluate our OpenCL wall time feature, discussed in Section 6.1.4. On the AMD Radeon R9 Fury GPU, we noticed that anomalous execution times on the order of 10x higher than a variant’s usual execution time occasionally occur, seemingly randomly, and we exclude these events from our data.

We compare predicted execution times to actual execution times in Figures 6, 7, and 8 and report the geometric mean of relative error for reasons laid out by Fleming and Wallace (1986).

8.1 Models Demonstrated

In these models we categorize workload costs as

- $c_{\text{gmem}}$: global memory access,
- $c_{\text{on-chip}}$: on-chip work, i.e., local memory access and arithmetic, and
- $c_{\text{overhead}}$: barrier, kernel launch, and work-group launch costs.

We model each of these three cost components individually as a linear combination of kernel features and cost parameters, with barriers counted on a per-work-group basis via the modeling strategy described in Section 6.1.3. We demonstrate two different types of models, a linear model,

$$ t \approx c_{\text{overhead}} + c_{\text{gmem}} + c_{\text{on-chip}}, $$

and a nonlinear model that allows overlap of on-chip and off-chip operation costs,

$$ t \approx c_{\text{overhead}} + c_{\text{gmem}} \cdot \hat{s}(c_{\text{gmem}} - c_{\text{on-chip}}) + c_{\text{on-chip}} \cdot \hat{s}(c_{\text{on-chip}} - c_{\text{gmem}}). $$

In general, the extent to which on-chip operation costs are hidden behind global memory transactions varies between kernels and across architectures. To determine whether the extent of this overlap warrants the nonlinear model expressed in Equation 5, we apply multiple strategies. First, we use the work removal routine discussed in Section 7.1.1 to remove arithmetic and local memory accesses from a kernel, obtaining execution times for a version of the kernel containing only global memory traffic. We then estimate the cost of the removed on-chip operations using the costs revealed by our microbenchmark kernels. If the sum of these two separate costs is approximately equal to the total execution time for the original kernel, this suggests little to no overlap. However, if the sum of these separate costs is significantly greater than the total execution time, this

![Approximating Step Function with tanh()](image)

**Figure 3.** Approximating $s(x)$ with differentiable $\hat{s}(x)$.

| GPU (Generation) | OpenCL/Platform/Driver Info |
|------------------|----------------------------|
| Nvidia Titan V (Volta) | OCL 1.2, CUDA 10.0.246 (410.93) |
| Nvidia GTX Titan X (Maxwell) | OCL 1.2, CUDA 10.0.292 (410.104) |
| Nvidia Tesla K40 (Kepler) | OCL 1.2, CUDA 9.1.84 (390.87) |
| Nvidia Tesla C2070 (Fermi) | OCL 1.2 CUDA 9.1.84 (390.116) |
| AMD Radeon R9 Fury (GCN 3) | OpenCL/RoCm 1.2.9-20190210 |
| RoCm platform ISA runtime 1.1.9-49-g39f1a5 Kernel 4.19 |

**Table 2.** Platforms used.

To demonstrate the effectiveness of this technique, we create a measurement kernel in which we can vary the ratio of local to global memory accesses. In this kernel, each thread performs one 32-bit global load, followed by $m$ 32-bit local memory load-store sequences, followed by one 32-bit global store. By varying $m$, the ratio of local to global memory accesses, we control whether the execution time is dominated by global or local memory transactions.

When $m$ is small, on-chip costs may be hidden behind global memory transactions; as $m$ increases, eventually local memory transactions dominate execution time. We model this using a PERFLEX model based on Equation 5 with $c_{\text{gmem}}$ and $c_{\text{on-chip}}$ being expressions containing PERFLEX features and parameters representing the global and local memory access costs. Figure 4 displays how PERFLEX fits such a model to this data. We observe that the extent to which local memory transaction costs in this kernel are hidden behind global transaction costs varies significantly across machines. On the Nvidia Tesla K40c and Nvidia Tesla C2070 GPUs, very little, if any, of the local access cost is hidden, while on the Nvidia Titan V, Nvidia GTX Titan X, and AMD Radeon R9 Fury GPUs, the cost of anywhere from 4 to 12 local memory accesses can be hidden behind a global transaction. We conclude that, at least for this kernel, on-chip-off-chip operation overlap behavior varies across GPUs, and that a PERFLEX model based on Equation 5 can model this behavior. We will discuss results for another kernel variant where this overlap behavior varies across GPUs in Section 8.4. OpenCL version and other platform information is available in Table 2.

To obtain average execution times, we evaluate our OpenCL wall time feature, discussed in Section 6.1.4. On the AMD Radeon R9 Fury GPU, we noticed that anomalous execution times on the order of 10x higher than a variant’s usual execution time occasionally occur, seemingly randomly, and we exclude these events from our data.

We compare predicted execution times to actual execution times in Figures 6, 7, and 8 and report the geometric mean of relative error for reasons laid out by Fleming and Wallace (1986).

8.1 Models Demonstrated

In these models we categorize workload costs as

- $c_{\text{gmem}}$: global memory access,
- $c_{\text{on-chip}}$: on-chip work, i.e., local memory access and arithmetic, and
- $c_{\text{overhead}}$: barrier, kernel launch, and work-group launch costs.

We model each of these three cost components individually as a linear combination of kernel features and cost parameters, with barriers counted on a per-work-group basis via the modeling strategy described in Section 6.1.3. We demonstrate two different types of models, a linear model,

$$ t \approx c_{\text{overhead}} + c_{\text{gmem}} + c_{\text{on-chip}}, $$

and a nonlinear model that allows overlap of on-chip and off-chip operation costs,

$$ t \approx c_{\text{overhead}} + c_{\text{gmem}} \cdot \hat{s}(c_{\text{gmem}} - c_{\text{on-chip}}) + c_{\text{on-chip}} \cdot \hat{s}(c_{\text{on-chip}} - c_{\text{gmem}}). $$

In general, the extent to which on-chip operation costs are hidden behind global memory transactions varies between kernels and across architectures. To determine whether the extent of this overlap warrants the nonlinear model expressed in Equation 5, we apply multiple strategies. First, we use the work removal routine discussed in Section 7.1.1 to remove arithmetic and local memory accesses from a kernel, obtaining execution times for a version of the kernel containing only global memory traffic. We then estimate the cost of the removed on-chip operations using the costs revealed by our microbenchmark kernels. If the sum of these two separate costs is approximately equal to the total execution time for the original kernel, this suggests little to no overlap. However, if the sum of these separate costs is significantly greater than the total execution time, this
Figure 4. Modeling overlap of local and global memory transactions. Geometric mean of relative error displayed. Array size differs across GPUs.

serves as evidence that on-chip costs are being hidden. To become further convinced about the presence or lack of this overlap, we can attempt to model the execution time using both kinds of models and observe the results. When we use the linear model to predict execution times for a kernel exhibiting overlap of on-chip costs that are significant relative to the total kernel execution time, it over-predicts, sometimes by a significant factor as will be discussed in Section 8.2.3. We observe the opposite result when applying the nonlinear model to a kernel where the cost of on-chip work is large relative to total execution time and very little of this cost is hidden.

8.2 Measurement Kernel Sets

The measurement kernel sets used to fit these models, unlike the set used in the simple example in Section 2.3, employ a microbenchmarking approach and do not include the computation whose execution times we are predicting. Each microbenchmark kernel is designed to reveal the cost associated with a single kernel feature. The designs of the measurement kernels used here were outlined in Section 7.1.2. We use the following feature notation when referring to features, and we substitute the prefix k- for prefix f- to denote a measurement kernel exercising that particular feature.

\[ f^{-\text{mem/op type}}_{\{14 \text{ strides}\}}\{\text{data type}\}_{\{\text{AFR}\}}_{\{\text{memory access tag}\}} \]

Figure 5 shows which measurement kernels we use to fit each model. Note that an empty feature field imposes no requirements, and we may choose to omit a known feature characteristic from a feature definition if the remaining characteristics suffice to distinguish that feature from others present in the model.

8.3 Matrix Multiplication

Our first demonstration model predicts execution times for two square matrix multiplication variants. The first variant is described in Section 2.2 and prefetches tiles into local (shared) memory before performing arithmetic. The second is the same algorithm without any prefetching, and without splitting the k index. The prefetching variant achieves between 8% and 20% of peak FLOP/s rates on all five GPUs.

Both variants operate on 32-bit floating point data and use \(16 \times 16\) work-groups. Together, the two variants use five distinct global memory access patterns, as shown in Figure 5b. We model execution time using the nonlinear model expressed in Equation 8. The model features and measurement kernel set are shown in Figure 5.

Table 3 displays the model parameter values representing feature costs on the Nvidia Titan V GPU, as well as \(p_{\text{edge}}\) from Equation 8. Recall that these values

| Feature                          | Param. Value              |
|----------------------------------|---------------------------|
| f32 add                          | \(5.424 \times 10^{-12}\) |
| f32 mul                          | \(5.423 \times 10^{-12}\) |
| f32 maddd                        | \(5.010 \times 10^{-12}\) |
| f-lmem\(_{\{\text{int}\}}\{1,>1\}\{16,>16\}\) | \(9.450 \times 10^{-12}\) |
| f-gmem\(_{\{\text{mm}\}}\{\text{PF}\}\{\text{b}\}\) | \(3.471 \times 10^{-12}\) |
| f-gmem\(_{\{\text{mm}\}}\{\text{PF}\}\{\text{a}\}\) | \(4.838 \times 10^{-12}\) |
| f-gmem\(_{\{\text{mm}\}}\{\text{noPF}\}\{\text{b}\}\) | \(1.866 \times 10^{-12}\) |
| f-gmem\(_{\{\text{mm}\}}\{\text{noPF}\}\{\text{a}\}\) | \(8.578 \times 10^{-13}\) |
| local barrier                    | \(1.328 \times 10^{-13}\) |
| group overhead                   | \(1.606 \times 10^{-09}\) |
| launch overhead                  | \(7.721 \times 10^{-05}\) |
| overlap edge                     | \(1.329 \times 10^{+03}\) |

Table 3. Matrix multiplication model parameter values on the Nvidia Titan V GPU. Parameter values represent costs per unit counted according to the count granularities described in Section 5.1 with the exception of ‘overlap edge’, which is the parameter governing the sharpness of our step function approximation, \(p_{\text{edge}}\) in Equation 8.
| Models | Measurement Kernels | Features |
|--------|----------------------|----------|
| Matmul | $k\text{-gmem}_{\{1,2^{11}\} \cdot \{16,16\} \cdot 2^{11}}^{(32 \text{nau) \cdot \{16,16\}}}$ | $f\text{-gmem}_{\{1,1\} \cdot \{16,16\}}$ |
| DG     | $\text{ops (32 nau) \cdot \{16,16\}}$ | $f\text{-op-add}_{\{32\}}$ |
| FD     | $\text{ops (32 madd) \cdot \{16,16\}}$ | $f\text{-op-madd}_{\{32\}}$ |

Field: $f\text{-gmem}_{\{1,2\} \cdot \{16,16\}} \cdot \{2^{11}\} \cdot \{1\}$

Figure 5. Measurement kernels used in demonstrated models. Lighter grey lines connect a measurement kernel to features present in the kernel that are not the primary feature being targeted for measurement. Not shown: all gmem measurement kernels also contain $f\text{-launch}$, $f\text{-groups}$, and $f\text{-op-add}_{\{32\}}$ features.

Our approach aims to represent *effective* costs at maximum throughput, and that units of work whose cost we measure are determined by the count granularities discussed in Section 5.1. For example, in the non-prefetching variant, the `lid(0)` stride when reading from matrix $a$ is 0, so we count $f\text{-gmem}_{\text{mm-noPF-a}}$ once per sub-group (32 work-items) rather than once per work-item. Also recall that arithmetic operations and local memory accesses are counted once per sub-group.

In this example set of parameter values, we observe very similar costs for addition, multiplication, and multiply-add operations, as we expect, and that the local memory access cost is about twice that of the arithmetic operations. We also observe that, after compensating for the fact that $\text{mm-noPF-a}$ is only counted once per sub-group (i.e., dividing the cost by the sub-group size, 32), prefetching increases the effective cost per global memory load from these matrices by factors of about 3 and 5, which suggests the overall cost savings due to prefetching is primarily due to the reduction in total global memory accesses by a factor of the tile width, 16.

We note that the accessibility of these parameter values...
and the transparency of the costs they represent facilitate understanding of the factors affecting performance in these kernels.

Figure 6 compares modeled to actual execution times for the two variants on five GPUs, and displays the geometric mean of relative error across both variants on each individual GPU as well as the error for each individual variant-GPU combination. On all 5 GPUs, the model predicts the execution times of these variants accurately enough to determine which is faster, with less than 10% error in most cases. Across all cases the geometric mean of relative error is 4.0%.

For further exploration, we also observed the predictions that would have been made by the linear model expressed in Equation 7. Error for the non-prefetching variant would be similar, likely due to the on-chip costs being relatively small in comparison to the total execution time, but the linear model would have over-predicted execution time for the prefetching variant by between 40% and 110% on all GPUs. This suggests that the prefetching variant, which contains significantly more on-chip work, is successfully hiding the cost of local memory transactions and arithmetic operations behind global memory transactions, and that the nonlinear model is a good choice for this computation on these architectures. Results of the on-chip-cost-hiding analysis described in Section 8.3 are consistent with this conclusion.

### 8.4 DG Differentiation

Our second demonstration model predicts execution times for four variants of an element-wise differentiation of per-element polynomials used in a DG computation. The pre-transform LOOPY kernel shows the mathematical intent of these algorithms:

```python
knl = lp.make_kernel(
    "[m,i,k]: 0<=m<nmatrices and 0<=k<nelements and 0<=i<nunit_nodes",
    "res[m,k,i] = sum(j, diff_mat[m,i,j] * u[k,j])")
```

All four variants tile and parallelize the k and i loops:

```python
knl = lp.split_iname(knl, "j", lsize[0], outer_tag="g.1", inner_tag="l.1")
```

The first variant performs only these transformations and does not take advantage of local memory for data reuse.

The second variant prefetches lsize[0] \times lsize[1] (16 \times 16) tiles from u into local (shared) memory before performing arithmetic:

```python
... # (first split and tag i and k as above)
knl = lp.split_iname(knl, "j", lsize[0])
knl = lp.add_prefetch(knl, "diff_mat", ["j_in", "i_in"], lid(0))
knl = lp.realize_reduction(knl)
knl = lp.add_inames_to_insn(knl, "i_out", "j_in")
knl = lp.prioritize_loops(knl, ["m", "j_out", "j_in", "m")
```

These additional transformations tile the j loop, load parts of u into scratchpad memory, and restructure the loops to expose instruction-level parallelism.

The third variant instead prefetches lsize[0] \times lsize[1] tiles from the differentiation matrix into local memory before performing arithmetic:

```python
... # (first split and tag i and k as above)
knl = lp.split_iname(knl, "j", lsize[0])
knl = lp.add_prefetch(knl, "diff_mat", ["j_in", "i_in"], lid(0))
knl = lp.realize_reduction(knl)
knl = lp.add_inames_to_insn(knl, "i_out", "j_in")
knl = lp.prioritize_loops(knl, ["m", "j_out", "j_in", "m")
```

The fourth variant uses the same transformations as the third; however, we also transpose the memory layout of the element data:

```python
knl = lp.split_iname(knl, "j", outer_tag="g.1", inner_tag="l.1")
```

These transformations switch the inner two data axes, N0 and N1, which changes the global memory access patterns for u and res so that the stride of lid(0) is 1 instead of nunit_nodes. This significantly improves the performance of these loads. Modeling the performance of this variant might inform decision making about the data layout elsewhere within a larger application. This variant is the fastest, and achieves between 5% and 18% of peak FLOP/s rates on all five GPUs.

All four variants operate on 32-bit floating point data and use 16 \times 16 work-groups. We set matrices to 3, nunit_nodes to 64, and nelements varies as shown in Figure 6. The four variants and the measurement kernel set used to fit their model use 11 distinct global memory access patterns as shown in Figure 6.

To decide whether to use a model that allows for on-chip cost hiding, we apply the analysis described in Section 8.3 to each of the DG variants. The results suggest that on-chip work overlaps with global memory transactions, with one exception: the u-prefetching variant does not exhibit this overlap on the Nvidia Titan V, Nvidia Tesla K40c, and Nvidia Tesla C2070 GPUs. On these three GPUs, the total execution time for the u-prefetching variant is approximately the sum of the on-chip and off-chip costs. Because of this, we use the linear model expressed in Equation 7 to model the u-prefetching variant on these three GPUs, and in all other cases, we model the DG variants using the nonlinear model expressed on Equation 8. Recall that in Section 7.4 we observed that the kernel which allowed us to vary the ratio of local to global memory accesses also did not exhibit overlap on the Nvidia Tesla K40c and Nvidia Tesla C2070 GPUs.

Figure 7 compares modeled to actual execution times for the four variants on five GPUs, and displays the relative error in model predictions. Across all cases the geometric mean of relative error is 7.5%. On all four Nvidia GPUs the model predictions are sufficient to accurately rank execution times for all variants from highest to lowest. On the AMD Radeon R9 Fury GPU, while the model predictions would rank the two fastest variants in reverse order, the predicted execution times are accurate enough to narrow the space of potential variants to the two fastest options, whose execution times differ by less than 7%. Additionally, the
predictions accurately reveal the cost savings realized by the **diff_mat**-prefetching variant when operating on element data with a transposed memory layout.

### 8.5 Finite Differences

Our third demonstration model predicts execution times for two variants of a first-order 2-D finite difference stencil operation. The pre-transform **LOOPY** kernel shows the mathematical intent of these algorithms:

```python
knl = lp.make_kernel(
    "[i,j]: 0<=i,j<n",
    "res[i,j] = u[i,j+1] + u[i+1,j] - 4*u[i+1,j+1] + u[i+2,j+1] + u[i+2,j+2] + u[i+2,j+1]"
)
```

Both variants parallelize the `i` and `j` indices across threads and prefetch `lsz0[0]` x `lsz1[1]` tiles from `u` into local (shared) memory before performing arithmetic:

```python
knl = lp.split_iname(knl, "i", lsz0-2, outer_tag="g.1", inner_tag="l.1")
knl = lp.split_iname(knl, "j", lsz0-2, outer_tag="g.0", inner_tag="l.0")
knl = lp.add_prefetch(knl, "u", ["i_in", "j_in"], fetch_bounding_box=True)
knl = lp.tag_inames(knl, "u_dim:0:1.1, u_dim:1:1.0")
```

The difference between the two variants is the workgroup size, which is also the size of the tiles fetched into local memory and affects the global memory access patterns. For the first variant, we use 16 x 16 thread groups, and for the second, we use 18 x 18. With 16 x 16 work-groups, 16 x 16-element tiles are prefetched, with one fetch per thread. After this fetch, the result for each of the interior 14 x 14 elements is computed by one of 196 threads, while 68 threads remain idle, corresponding to the 68 halo elements. This strategy yields a `gid(0)` stride of 16.

Unlike the other variants we model, the global memory loads in these kernels have access-to-footprint ratios near 1. Because of this, the data throughput rate, calculated as (total global memory access count)/(execution time), is less likely to be inflated significantly by cached data reuse, and is meaningful to report. The 16 x 16 variant was slightly faster, and achieved between 40% and 82% of peak bandwidth on all 5 GPUs. FLOP/s rates were much lower, between 2% and 5% of peak.

Both variants operate on 32-bit floating point data. The model features and measurement kernel set are displayed in Figure 5. As shown in Figure 5b, the variants and the measurement kernels used to fit the model are based on 5 distinct global memory access patterns. The analysis of on-chip cost hiding that we described in Section 7.1.2 indicates that little if any such overlap occurs when executing these variants on these architectures. Because of this, we model execution time using the linear model expressed in Equation 7.

We note two potential sources of modeling error in this example. As mentioned in Section 7.1.2, the models presented here use a single feature to represent all local memory accesses. We made this decision to simplify the models and measurement kernel sets; it is not a limitation of our approach or our software, since local memory access features may include the same access pattern characteristics as global memory access. The local memory accesses in these kernels constitute a significant portion of the execution time, 10-20%, and have different access patterns. The `lid(0)` stride is 18 in the 18 x 18-tile variant, and 16 in the 16 x 16-tile variant. If these accesses differ in cost from one another, or from those in the local memory access measurement kernel, this model could not account for these differences.

Another potential source of error for this example is the affect of varying machine utilization on execution time, which our approach does not attempt to capture,
as discussed in Section 4. The amount of local memory used per work-group, as well as the number of threads per work-group, both differ between these two variants, and can affect machine utilization.

Figure 7 compares modeled to actual execution times for the two variants on five GPUs, and displays the relative error in model predictions. Note that the 256 work-item limit on the AMD GPU prevents us from executing the 18 x 18-tile variant. Despite the potential sources of error described above and the similarity in execution times between the two variants, across all cases the geometric mean of relative error is 6.8%, and the model predictions are sufficiently accurate to identify the faster variant in every case except the Nvidia Tesla C2070 GPU.

9 Related Work

Common approaches to performance prediction include analytical modeling, often based on in-depth program and hardware analysis; statistical regression and machine learning approaches; and machine and application benchmarking. Many approaches use a combination of these strategies.

Among analytical approaches to GPU performance modeling, much of the previous work yielding the most accurate predictions has focused on constructing models of instruction-level execution based on detailed hardware knowledge and instruction analysis, often for a single architecture or group of highly similar architectures. Many of these models predict well for their specific target architecture. For example, Hong and Kim (2009) present an analytical performance model for Nvidia GPU architectures that produces an execution time prediction based on estimates of memory-level and thread-level parallelism. They further extend their model for power prediction (Hong and Kim 2010). This model achieves a geometric mean error of 13.3% when predicting performance of the MERGE (Linderman et al. 2008) benchmarks on four Tesla generation Nvidia GPUs. It makes extensive use of hardware performance characteristics, such as timing delays between memory transactions, DRAM access latency, and instruction execution cycles, and it requires an analysis of PTX assembly instructions. Baghsorkhi et al. (2010) also use deep analytical knowledge of a (single) GPU architecture, and, unlike Hong and Kim (2009), model branch divergence, bank conflicts, and SIMD pipeline delays.

Other related analytical modeling works include Hammer et al. (2017), who use a partially automated analytical approach to modeling GPU loop kernel performance that allows for multiple architectures, Van Gemund (2003), who uses a partially automated symbolic analytic modeling approach to predict performance on distributed CPU machines, Pillana and Fahringer (2005), who provide a graphical user interface to aid distributed CPU model creation and employ discrete event simulation, and Unat et al. (2015), who introduce a tool employing compiler analysis to generate parameterized models with a slightly different goal, that of evaluating design trade-offs and software optimizations. All four of these approaches require a user-supplied machine model or architecture statistics.

Machine learning and statistical techniques are also used to predict performance of GPU kernels. From the perspective of optimization selection, Cavazos et al. (2006) present a probabilistic predictor of transformation selection using a non-analytical, black-box model based on an artificial neural network. Joseph et al. (2006) use techniques from machine learning to identify piecewise nonlinearities in cost metrics. Other approaches emphasize the performance of single subsystems, such as branch prediction (Emer et al. 2002). Other learning and statistical approaches include Jia et al. (2012), Kerr et al. (2012), Wu et al. (2015), Zhang et al. (2011), and Chen et al. (2018).
Some modeling approaches employ benchmarks, including Zhang and Owens (2011), who use results from microbenchmarks to derive a throughput model for instruction pipeline, shared memory, and global memory costs. They focus on identifying performance bottlenecks and guiding the optimization process rather than predicting execution time. The target kernel must be run in a simulator to gather relevant performance counters, and the binary file must be analyzed. Johnston et al. (2018) gather their set of architecture-independent program features by simulating an OpenCL device using the Oclgrind simulator and examining the LLVM intermediate representation produced. They then use these features to generate a random forest model. Konstantinidis and Cotropinis (2017) employ a microbenchmarking approach to gather GPU performance metrics, and gather information about their target kernels using Nvidia’s nvprof profiler on a reference GPU. They demonstrate results on a larger kernel set than most works we found, achieving an average error of 27%.

Two recent surveys both come to similar conclusions regarding the current GPU performance modeling landscape. In Madougou et al. (2016), researchers perform an in-depth evaluation of 12 GPGPU performance modeling tools, including 6 analytical models: Hong and Kim (2009), Kothapalli et al. (2009), Li et al. (2015), Meswani et al. (2013), Sim et al. (2012), and Song et al. (2013). The authors determine that, while the analytical models tend to be accurate for a particular hardware family or workload, they are less accurate for different hardware. They report that constructing all of these models requires significant effort and the collection or estimation of anywhere from 6 to 30 parameters characterizing the hardware or the application, which is consistent with our experience reproducing the results in Hong and Kim (2009).

Lopez-Novoa et al. (2015) come to similar conclusions after surveying over 30 models for GPU computing of various types, including 7 general-purpose execution-time-estimating models, i.e., models that are not designed for a particular application (Che and Skadron 2014; García 2013; Hong and Kim 2009; Kerr et al. 2010; Kothapalli et al. 2009; Meng et al. 2011; Nugteren and Corporaal 2012). The authors conclude that there is no accurate model valid for a wide set of architectures, and that each model they consider makes a trade-off between accuracy and breadth of hardware applicability. They also note that most models they surveyed are designed for CUDA rather than vendor-neutral OpenCL, and that Hong and Kim (2009) stands out as the model of choice for accurately predicting GPU execution times.

Figure 8. Finite difference model accuracy. The table displays the geometric mean of relative error (%).

10 Conclusions

We have demonstrated an alternative to previous GPU performance modeling approaches: a framework for constructing analytical models and fitting them to a GPU using a customized measurement kernel set. Our framework allows a developer to control the trade-offs between model accuracy, complexity, generalization, and evaluation speed, and our hardware-blind model-fitting approach allows these models to make predictions on new devices with minimal effort. We demonstrated example execution time models for three computations yielding predictions accurate enough to, e.g., allow an autotuner or human user to identify which kernel variant or subset of variants will have the shortest execution times. Across all variants of all three computations on all five GPUs, we achieved a geometric mean relative error of 6.33%. Additionally, we demonstrated how the transparency and interpretability of the model expressions, parameters, and features enables users to gain actionable insights into the factors affecting computation performance.

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