Tensor Algebra on an Optoelectronic Microchip

Sathvik Redrouthu  
Procyon Photonics  
Ashburn, Virginia  
Email: 2024sredrout@tjhsst.edu

Rishi Athavale  
Procyon Photonics  
Ashburn, Virginia  
Email: rishi.athavale1@gmail.com

Abstract—Tensor algebra lies at the core of computational science and machine learning. Due to its high usage, entire libraries exist dedicated to improving its performance. Conventional tensor algebra performance boosts focus on algorithmic optimizations, which in turn lead to incremental improvements. In this paper, we describe a method to accelerate tensor algebra a different way: by outsourcing operations to an optical microchip. We outline a numerical programming language developed to perform tensor algebra computations that is designed to leverage our optical hardware’s full potential. We introduce the language’s current grammar and go over the compiler design. We then show a new way to store sparse rank-n tensors in RAM that outperforms conventional array storage (used by C++, Java, etc.). This method is more memory-efficient than Compressed Sparse Fiber (CSF) format and is specifically tuned for our optical hardware. Finally, we show how the scalar-tensor product, rank-n Kronecker product, tensor dot product, Khatri-Rao product, face-splitting product, and vector cross product can be compiled into operations native to our optical microchip through various tensor decompositions.

Keywords—Data analytics, machine learning, optical computing, scientific computing, tensor algebra

I. INTRODUCTION

A. Tensor Algebra

Tensor algebra has numerous applications in scientific disciplines. For example, widely used multiphysics simulation software (e.g., COMSOL Multiphysics, Ansys Lumerical, etc.) must perform large-scale numerical computations to solve problems in numerous fields such as fluid dynamics, structural mechanics, heat transfer and electromagnetics [1–3]. Many of these computations are streamlined through chained tensor algebra expressions [4]. In addition, advances in machine learning (ML) due to large neural networks (e.g., DALL-E 2, GPT-3, PaLM, etc.) also make use of massive tensor algebra computations [5]. Optimizing tensor algebra becomes exceedingly important when ML models must meet time constraints (e.g., high-frequency stock trading bots) [6].

Tensors themselves can be thought of as n-dimensional numerical arrays for the purposes of this paper. Each dimension of a tensor is referred to as a mode. A tensor’s rank is the number of modes it has and therefore the number indices needed to access a specific value [7]. Rank-0 tensors, having 0 modes, require no indices to access values and thus represent a single number, or a scalar. Similarly, rank-1 tensors are simply vectors and rank-2 tensors are matrices.

Tensors of rank $n > 0$ are very useful in representing indexed data. For example, a search engine tracking page URLs, keywords, and backlinks can store collected data in a rank-3 tensor. Typically, however, not every element in this tensor is useful. It is often not the case that any given website contains each keyword and backlink ever indexed by the search engine. In the frequent scenario where a page URL does not map to a specific keyword-backlink combination, a 0 can simply be placed at tensor[URL][keyword][backlink]. This results in most of the tensor’s entries becoming 0; such a tensor is referred to as a sparse tensor [8]. We discuss efficient storage methods for sparse tensors in Sec. VI.

Of course, search giants such as Google collect much more information than described in the example. Other companies are in the same boat; in fact, according to [9], a specific rank-3 Facebook tensor has dimensions $1591 \times 63891 \times 63890$. Huge computations are performed constantly on tensors like these; such is the case for most large-scale graph applications [10]. Even after numerous algorithmic optimizations, however, such computation is far too slow to keep up with increasing demands [11]. For example, animation firms like Pixar can take up to 39 hours of computing time to render a single frame [12]. It is therefore apparent that some form of optimization sustainable throughout the future is necessary.

B. The Photonic Advantage

Many highly optimized tensor algebra libraries currently exist (e.g., Eigen, MATLAB Tensor Toolbox, and SPLATT) [13–15]. However, as Moore’s Law and Dennard Scaling reach their limits and the demand for tensor algebra increases, running tensor algebra on classical hardware will no longer be viable and these libraries must adapt [11].

An alternative to classical hardware involves optical computing (the use of photons to perform computations), which offers a significant speed increase and surmounts most of the
energy challenges posed in conventional computer engineering [16]. Moreover, its lack of dependence on the conventional transistor leads it to be independent from the decline of Moore’s Law. Recognizing this, some of us at Procyon Photonics have designed an optical microchip able to perform high-speed matrix-vector multiplication (MVM). The chip (named Tachyon 1) maintains a compact form and is inherently analog, indicating its potential in computational fields [17].

Performing tensor algebra on such a microchip would offer a significant speed increase while simultaneously sidestepping the decline of Moore’s Law. In this paper, we describe a method where this is possible.

C. Apollo

To our knowledge, no programming language has been invented that can leverage an optical microchip’s full potential and link it to fields that can be influenced by its capabilities. For these reasons, we introduce Apollo, a computing language designed specifically for Tachyon 1. Apollo supports important tensor algebra operations that are mapped onto the corresponding units on the host computer and optical chip. The language will be extended to support operations and algorithms that are not related solely to tensor algebra but still important for computationally expensive tasks, such as deep neural network (DNN) training/inference.

We begin by going through preliminary notation and definitions in Sec. II. Next, we cover the language’s grammar and supported operations in Sec. III. In Sec. IV we go over the workflow, compiler front-end, and virtual machine (VM). It is here where we introduce the most important VM instruction that Sec. VI revolves around.

Next, we illustrate a new method to store large, sparse tensors in Sec. V which we found to surpass the conventional array storage method from a memory viewpoint. In addition, we show how our method is more efficient than CSF format for our optical hardware. Finally, since Tachyon 1 is engineered to perform matrix-vector multiplication in a single instruction, we focus on decomposing complex tensor algebra expressions into sequences of matrix-vector products in Sec. VI. Efficient tensor decompositions would allow entire tensor algebra expressions to be run at an incredible speed.

II. PRELIMINARIES

A. Notation

Tensors of rank \( n > 2 \) are denoted in scripted letters (e.g., \( \mathcal{X} \)). Matrices are denoted in uppercase boldface and vectors are denoted in lowercase boldface (\( \mathbf{M} \) and \( \mathbf{v} \) respectively). The identity matrix is denoted as \( \mathbf{I} \).

B. Definitions

We use multiple tensor operations in Apollo, some of which are modifications of existing definitions. In this section, we define each operation the way it is used within the language.

Definition II.1 (Scalar-tensor product). Given a scalar \( \lambda \) and a tensor \( \mathcal{X} \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_n} \), the scalar-tensor product \( \lambda \mathcal{X} \) is given by:

\[
(\lambda \mathcal{X})_{i_1i_2\ldots i_n} = \lambda(x_{i_1i_2\ldots i_n})
\]

Definition II.2 (Rank-\( n \) Kronecker product). Given two tensors \( \mathcal{X} \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_n} \) and \( \mathcal{Y} \in \mathbb{R}^{J_1 \times J_2 \times \cdots \times J_m} \), the rank-\( n \) Kronecker product \( \mathcal{X} \otimes \mathcal{Y} \in \mathbb{R}^{I_1J_1 \times I_2J_2 \times \cdots \times I_nJ_n} \) is given by:

\[
(\mathcal{X} \otimes \mathcal{Y})_{i_1j_1\ldots i_nj_n} = (x_{i_1j_1\ldots i_nj_n})
\]

Each index \( i_1j_1\ldots i_nj_n \) is a corresponding index in a block tensor.

Definition II.3 (Tensor inner product). Given two tensors \( \mathcal{X}, \mathcal{Y} \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_n} \), the inner product \( \langle \mathcal{X}, \mathcal{Y} \rangle \in \mathbb{R} \) is given by:

\[
\langle \mathcal{X}, \mathcal{Y} \rangle = \sum_{i_1} \sum_{i_2} \cdots \sum_{i_n} x_{i_1i_2\ldots i_n} y_{i_1i_2\ldots i_n}
\]

Definition II.4 (Tensor dot product). Given two tensors \( \mathcal{X} \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_m} \) and \( \mathcal{Y} \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_{m-1} \times J_{m-1} \times \cdots \times J_n \times J_n} \), the tensor dot product \( \langle \mathcal{X}, \mathcal{Y} \rangle \in \mathbb{R}^{I_1 \times I_2 \times \cdots \times I_{m-1} \times J_1 \times J_2 \times \cdots \times J_{n-2} \times J_n \times J_n} \) is given by:

\[
\langle \mathcal{X}, \mathcal{Y} \rangle_{i_1i_2\ldots i_{m-1}j_1j_2\ldots j_nj_n} = \sum_{i_{m-1}} \sum_{j_{n-1}} x_{i_1i_2\ldots i_{m-1}j_1j_2\ldots j_{n-1}j_n} y_{i_{m-1}j_{n-1}j_1j_2\ldots j_nj_n}
\]

where \( I_m = J_{n-1} \).

Definition II.5 (Khatri-Rao product). Given two matrices \( \mathbf{A} \in \mathbb{R}^{I \times K} \) and \( \mathbf{B} \in \mathbb{R}^{J \times K} \), the Khatri-Rao product \( \mathbf{A} \odot \mathbf{B} \in \mathbb{R}^{I \times J \times K} \) is given by:

\[
\mathbf{A} \odot \mathbf{B} = [a_1 \odot b_1 \ a_2 \odot b_2 \ \cdots \ a_K \odot b_K]
\]

This can be thought of as a column-wise Kronecker product.

Definition II.6 (Face-splitting product). Given two matrices \( \mathbf{A} \in \mathbb{R}^{K \times I} \) and \( \mathbf{B} \in \mathbb{R}^{K \times J} \), the face-splitting product \( \mathbf{A} \bullet \mathbf{B} \in \mathbb{R}^{K \times I \times J} \) is given by:

\[
\mathbf{A} \bullet \mathbf{B} = \begin{bmatrix}
    a_1 \odot b_1 \\
    a_2 \odot b_2 \\
    \vdots \\
    a_K \odot b_K
\end{bmatrix}
\]

This can be thought of as a row-wise Kronecker product.

Definition II.7 (Vector cross product). Given two vectors \( \mathbf{u} \in \mathbb{R}^{3} \) and \( \mathbf{v} \in \mathbb{R}^{3} \), the vector cross product \( \mathbf{u} \times \mathbf{v} \in \mathbb{R}^{3} \) is given by:

\[
\mathbf{u} \times \mathbf{v} = \begin{bmatrix}
    e_1 \\
    e_2 \\
    e_3
\end{bmatrix}
= \begin{bmatrix}
    a_1 \ b_2 \ a_3 \\
    a_2 \ b_3 \ a_1 \\
    a_3 \ b_1 \ a_2
\end{bmatrix}
\]

We discuss how to run each of these operations on our optical hardware in Sec. VI.  

1We refer to Def II.3 in the general case to provide a complete definition, but only discuss implementation in the vector case.
IV. Compiler Design

A. Workflow

The workflow we decided on is shown in Fig. 3. Note that the Apollo compiler is 2-stage.

Fig. 2. Apollo’s grammar shown in EBNF. The base case in the recursive tensor structure is a list of comma separated integers and/or floating point values.

Fig. 3. Native Apollo code gets compiled into Apollo Virtual Machine (AVM) instructions by the compiler front-end. AVM generates standard assembly instructions for regular operations and compiles tensor algebra to t1926 instructions. Respective assemblers target the host CPU and Tachyon 1. This chosen workflow enables tensor algebra to be outsourced to Tachyon 1. Note that the scope of this paper is limited to A VM instruction generation.

B. Supported Operators

The standard PEMDAS order is supported for scalars. For tensors of rank \( n \geq 1 \), the order of operations should be defined with parenthesis. We show the operators supported in this Apollo prototype in tables I and II.

The standard assembler targets the host CPU, whereas the t1926 assembler targets Tachyon 1. Such a setup is used because Tachyon 1 is geared towards certain types of computations only.

\[
\begin{align*}
\langle lower \rangle & \Rightarrow \, ^a \cdot \, ^b \cdot \, ^c \cdot \, ^d \cdot \, ^e \cdot \, ^f \cdot \, ^g \cdot \, ^h \cdot \, ^i \cdot \\
& \, ^j \cdot \, ^k \cdot \, ^l \cdot \, ^m \cdot \, ^n \cdot \, ^o \cdot \, ^p \cdot \, ^q \cdot \, ^r \cdot \\
& \, ^s \cdot \, ^t \cdot \, ^u \cdot \, ^v \cdot \, ^w \cdot \, ^x \cdot \, ^y \cdot \, ^z \\
\langle upper \rangle & \Rightarrow \, ^A \cdot \, ^B \cdot \, ^C \cdot \, ^D \cdot \, ^E \cdot \, ^F \cdot \, ^G \cdot \, ^H \cdot \, ^I \cdot \\
& \, ^J \cdot \, ^K \cdot \, ^L \cdot \, ^M \cdot \, ^N \cdot \, ^O \cdot \, ^P \cdot \, ^Q \cdot \, ^R \cdot \\
& \, ^S \cdot \, ^T \cdot \, ^U \cdot \, ^V \cdot \, ^W \cdot \, ^X \cdot \, ^Y \cdot \, ^Z \\
\langle digit \rangle & \Rightarrow \, ^0 \cdot \, ^1 \cdot \, ^2 \cdot \, ^3 \cdot \, ^4 \cdot \, ^5 \cdot \, ^6 \cdot \, ^7 \cdot \, ^8 \cdot \\
& \, ^9 \\
\langle character \rangle & \Rightarrow \, \langle lower \rangle | \, \langle upper \rangle \\
\langle integer \rangle & \Rightarrow \, [+-]\langle digit \rangle\{\langle digit \rangle\} \\
\langle floating-point \rangle & \Rightarrow \, \{\langle integer\rangle\} \cdot \, \{\langle integer\rangle\} \\
\langle tensor \rangle & \Rightarrow \, \{\langle character \rangle\} \cdot \, \{\langle tensor \rangle\} \cdot \, \{\langle character \rangle\} \cdot \, \{\langle character \rangle\} \cdot \, \{\langle character \rangle\} \\
\langle identifier \rangle & \Rightarrow \, \langle character \rangle \, | \, \langle character \rangle \, | \, \langle character \rangle \, | \, \langle character \rangle \, | \, \{\langle character \rangle\} \cdot \, \{\langle character \rangle\} \\
\langle term \rangle & \Rightarrow \, \langle factor \rangle \, | \, \langle factor \rangle \, | \, \langle factor \rangle \, | \, \langle factor \rangle \, | \, \{\langle character \rangle\} \cdot \, \{\langle character \rangle\} \\
\langle expr \rangle & \Rightarrow \, \langle term \rangle \, | \, \langle term \rangle \, | \, \langle term \rangle \, | \, \langle term \rangle \, | \, \langle term \rangle \, | \, \{\langle character \rangle\} \cdot \, \{\langle character \rangle\} \\
\langle type \rangle & \Rightarrow \, \langle int \rangle \, | \, \langle float \rangle \, | \, \langle tensor \rangle \\
\langle statement \rangle & \Rightarrow \, \langle let \rangle \, \langle type \rangle \, \langle identifier \rangle \, \langle = \rangle \, \langle expr \rangle \, \langle ; \rangle \\
\langle program \rangle & \Rightarrow \, \{\langle statement \rangle\}
\end{align*}
\]
B. Compiler Front-end

We use a hand coded compiler front-end (lexer, parser, and code generator). This is because we have found that parser generators do not cooperate well with tensor algebra and our storage choice. We use a recursive descent parser, which works well for performance. The in-compiler tensor storage we describe in Sec. [V-B] is more easily implemented with such a parser.

It is noteworthy that there are many instances in the language where operators are overloaded. For example, consider the multiplication operator, \(*\). If \(A \times B\) is called, four cases are possible. 1) \(A\) is a scalar and \(B\) is a tensor of rank \(n > 0\), 2) \(A\) is a tensor of rank \(n > 0\) and \(B\) is a scalar, 3) \(A\) and \(B\) are both scalars, or 4) \(A\) and \(B\) are both tensors of rank \(n > 0\). The parser considers these cases and generates abstract syntax tree (AST) nodes of the correct type (e.g., variable nodes, scalar nodes, tensor nodes, etc.).

The AST is traversed in pre-order by the code generator, sequentially producing the appropriate VM instructions. Standard procedures are followed for variable handling. In the case of more exotic AST nodes (e.g., tensor nodes) the code generator calls special functions (discussed in Sec. [VI]) to generate the correct code. The VM instruction set is outlined in Sec. [IV-C].

C. Virtual Machine

Apollo’s VM is stack-based. It provides 4 memory segments (namely, the constant, global, pointer, and this segments), shown in Fig. [IV].

```
| 0 | 0 | 0 |
|---|---|---|
| 1 | 1 | 1 |
| 2 | 2 | 2 |
```

Fig. 4. The constant (abstract), global, pointer, and this virtual segments respectively.

Each one of these segments are anchored to a specific location in RAM at compile time. They are fixed in their locations, except for the this segment, which we use for tensors. Index 0 in the pointer segment contains the base address of the this segment, so if the value at index 0 changes, the this segment gets anchored to a different RAM location, similar to [18]. As the language expands, we may add additional memory segments that can dynamically change location during run-time; if we take this route, we will allocate more RAM and add more values to the pointer segment.

The constant segment is used to push and pop constants to and from the stack, as in [18]. Note that despite showing

\(^2\)The RAM referred to throughout this section is a simplified virtual abstraction. Hence, we freely interact with it using numbers in the decimal system. The actual RAM is referred to when discussing compilation to target architectures, which will be done in a future paper.

\(^3\)Exact RAM indices are not included.

| Operation | Compiles to | Description |
|-----------|-------------|-------------|
| neg       | Host ASM    | Negates the value at the top of stack. |
| add       | Host ASM    | Pops stack into \(b\). Pops stack into \(a\). Pushes \(a + b\) to stack. |
| sub       | Host ASM    | Pops stack into \(b\). Pops stack into \(a\). Pushes \(a - b\) to stack. |
| mult      | Host ASM    | Pops stack into \(b\). Pops stack into \(a\). Pushes \(ab\) to stack. |
| div       | Host ASM    | Pops stack into \(b\). Pops stack into \(a\). Pushes \(a/b\) to stack. |
| mvmul     | Host ASM    | Pops stack into \(b\). Pops stack into \(a\). Pushes \(Ab\) to stack. |

| Name | Args | Description |
|------|------|-------------|
| malloc | int size | Finds an unused RAM segment of length size, pushes pointer pointing to the first segment index to stack. |

Table III: AVM Arithmetic Instruction Set

Table IV: AVM Subroutine Instruction Set

solely integers, the segment supports integer and floating-point values. The global segment is used in conjunction with the symbol table to store variable values, which can be accessed throughout the lifetime of the program. Values in the global segment can also be references to tensors. See Sec. [V] for more information regarding tensor storage.

The memory access commands are push [segment] \(i\) and pop [segment] \(i\). The push instruction pushes the value at index \(i\) of memory segment [segment] onto the stack. The pop instruction pops the value on top of the stack onto index \(i\) of memory segment [segment] [18]. The rest of the AVM instruction set (composed of arithmetic instructions and built-in subroutines) is given in Tables [III] and [IV].

Note that each arithmetic instruction can be done in a single instruction by the corresponding processor.

Subroutines are handled with the instruction call [fname] [nArgs]. The first [nArgs] values are treated as arguments, so the virtual machine would pop the stack [nArgs] times if the call command is generated.

Since malloc has 1 argument, a possible code fragment for it looks like:

\(^4\)Apollo does not yet support user-defined subroutines, so a local segment is not required.
**push** constant 3  
**call** malloc 1

This would 1) push 3 onto the stack, 2) pop 3 off the stack and pass it into malloc, 3) find an unused RAM segment of size 3, and 4) push a pointer to the first index of that segment to the RAM. Its behavior mimics `Memory.alloc` in [18].

**V. Sparse Tensor Storage**

**A. Current Methods**

Tensor components are conventionally represented as nested arrays in standard programming languages. In C++, the components are stored as one contiguous array. To access the element at index \(ij\), the element at index \(\text{base} + i + j\) in the flattened block is indexed (where \(\text{base}\) is the base address of the array) [19]. In Java, each array of dimension \(n+1\) contains pointers to each sub-array of dimension \(n\). If \(n = 0\), the \((n+1)\)-dimensional array simply stores scalar values [20].

Since tensors are often sparse, however, these conventional methods often end up storing excess zeros, making them suboptimal. The Facebook tensor discussed in Sec. [A] has only 737,934 nonzero values and is therefore 99.999% made up of zeros. It is apparent that tensor storage optimizations must be considered. Compressed Sparse Fiber (CSF) format is a better method that stores a tensor in a tree structure, where the indices and values for only non-zero components are contained, as shown in Fig. 5. CSF performs significant better than conventional approaches for applications involved in highly sparse tensor algebra.

However, CSF requires storing pointers to each child node, likely integrated to enable fast indexing [15]. Such an optimization would typically be incredibly important; however, since our optical hardware can do an MVM in a single instruction, it is not necessary that we are able to access indices efficiently in intermediate computations. Rather, it is important that we return an entire row of indices as fast as possible. Sec. [VI] provides insight into why this is the case.

**B. Binary Sparse Tensor Tree Format**

To save memory and return sub-tensors quickly, we store the tensor in Fig. 1 as shown in Fig. 6.

**VI. Compiling Tensor Algebra Expressions**

As stated in earlier sections, the most powerful tensor algebra operation supported by Tachyon 1 that can be done in a single instruction is matrix-vector multiplication (MVM). Therefore, it is the compiler’s job to translate more complex operations into sequences of MVMs when applicable, thereby accelerating computation of the whole expression. For clarity, note that Tachyon 1 multiplies matrices and vectors in the order \(Ax = b\). Also note that decomposition into sub-tensors of who’s sizes are supported by Tachyon 1 is not covered in this paper.
A. Scalar-tensor Product

The scalar-tensor product as defined in Def. II.1 is a commutative operation that multiplies each element in a tensor $\mathbf{X}$ by a scalar $\lambda$. The product is very easy to compile; simply iterate through each vector $x_{i_1i_2\ldots i_{n-1}}$ in the tensor and generate the \texttt{mvmul} instruction to multiply it by the matrix $\lambda \mathbf{I} = \begin{bmatrix} \lambda & 0 \\ 0 & \lambda \end{bmatrix}$. Note that the compiler reorients the product to generate the matrix before the vector if the user calls it in the opposite order. In other words, it ensures that running the generated code results in a product in the order $\lambda x_{i_1i_2\ldots i_{n-1}}$.

B. Rank-$n$ Kronecker Product

The Kronecker product is useful in signal and image processing [21]. Through the Khatri-Rao product, it is useful in neural networks (through minimization of convolution and tensor sketch operations) and natural language processing [22].

Refer to Def. II.2 for the definition of the Kronecker product. For clarity, each element in the result is simply the element at $x_{i_1i_2\ldots i_n}$ multiplied by $\mathbf{Y}$ for two tensors $\mathbf{X}$ and $\mathbf{Y}$. The product can be represented compactly between two matrices as

$$
\mathbf{A} \otimes \mathbf{B} = \begin{bmatrix}
    a_{11} \mathbf{B} & a_{12} \mathbf{B} & \cdots & a_{1n} \mathbf{B} \\
    a_{21} \mathbf{B} & a_{22} \mathbf{B} & \cdots & a_{2n} \mathbf{B} \\
    \vdots & \vdots & \ddots & \vdots \\
    a_{m1} \mathbf{B} & a_{m2} \mathbf{B} & \cdots & a_{mn} \mathbf{B}
\end{bmatrix}
$$

Therefore, the compiler can compute the scalar-tensor product for each element in the resultant block tensor through the method outlined in Section VI-A.

C. Tensor Dot Product

Many fields, including machine learning and physics, demand the ability to compute the dot product efficiently [23,24]. To allow Tachyon 1 to meet this demand, we must also provide a way for the Apollo compiler to transform this operation into a sequence of MVMs. The tensor dot product is an operation between two rank-$n$ tensors, $\mathbf{A}$ and $\mathbf{B}$. Some possibly familiar tensor dot products include the rank-0, rank-1, and rank-2 dot products (scalar product, vector dot product, and matrix multiplication respectively). The compiler considers the dot product operation over the component arrays. A few cases are possible:

1) $\mathbf{A}$ and $\mathbf{B}$ are both scalars
2) Either $\mathbf{A}$ or $\mathbf{B}$ is a scalar, but not both
3) $\mathbf{A}$ is a vector/matrix, whereas $\mathbf{B}$ is a vector
4) $\mathbf{A}$ is a vector/matrix, whereas $\mathbf{B}$ is a rank-$n$ tensor with $n > 2$
5) $\mathbf{A}$ is a rank-$n$ tensor where $n > 2$, whereas $\mathbf{B}$ is a vector
6) $\mathbf{A}$ is a rank-$n$ tensor and $\mathbf{B}$ is a rank-$m$ tensor, where $n > 1$, $m > 1$, and $n \neq m$
7) $\mathbf{A}$ and $\mathbf{B}$ are both rank-$n$ tensors

Cases 1 and 2 are irrelevant since the parser maps Case 1 to the scalar product and Case 2 to the scalar-tensor product (Def. II.1 discussed in Sec. VI-A). In Case 3, $\mathbf{A}$ is always treated as a matrix and the \texttt{mvmul} command is simply generated (this accounts for Def. II.3 if $\mathbf{A}$ is a vector).

From this point on, we define a function $f_n$ that refers to Case $n$ (e.g., $f_3$ generates an MVM instruction). Continuing, in Case 4, $\mathbf{A}$ is also treated as a matrix. $\mathbf{B}$ is decomposed into a chain of vectors and a series of references to Case 3 ($f_3(\mathbf{A}, b_{i_1i_2\ldots i_{n-1}})$) are made. In Case 5, $\mathbf{A}$ is decomposed into a chain of matrices and a series of references to Case 3 ($f_3(\mathbf{A}_{i_1i_2\ldots i_{n-2}}, \mathbf{B})$) are again made.

In cases 6 and 7, we consider Def. II.4. In Case 6, the tensor of lower rank is first decomposed. Case 4 is then referenced for each matrix if $\mathbf{A}$ was decomposed (always into a matrix chain, resulting in calls to $f_3(\mathbf{A}_{i_1i_2\ldots i_{n-2}}, \mathbf{B})$) and Case 5 is referenced if $\mathbf{B}$ was decomposed (always into a vector chain, resulting in calls to $f_3(\mathbf{A}_{i_1i_2\ldots i_{n-1}}, \mathbf{B})$). Finally, in Case 7, $\mathbf{A}$ is decomposed and Case 4 is referenced ($f_4(\mathbf{A}_{i_1i_2\ldots i_{n-2}}, \mathbf{B})$).

D. Vector Cross Product

The cross product is an operation that appears frequently in computational geometry/computer graphics. A common task is to generate a third vector orthogonal to two other vectors (or a plane formed by 3 points) [25]. The cross product can also be used to calculate the distance between two lines and calculate if they are parallel. It also appears in a multitude of physics simulations.

For most applications, cross products are in $\mathbb{R}^3$ and between two vectors. We consider the cross product in a positively oriented orthonormal basis. The cross product of two vectors in $\mathbb{R}^3$ as defined in Def. II.7 is also given by the antisymmetric matrix-vector product

$$
\mathbf{a} \times \mathbf{b} = 
\begin{bmatrix}
  0 & -a_3 & a_2 \\
  a_3 & 0 & -a_1 \\
- a_2 & a_1 & 0
\end{bmatrix}
\begin{bmatrix}
  b_1 \\
  b_2 \\
  b_3
\end{bmatrix}
$$

The \texttt{mvmul} command can simply be generated from here.

E. Other Tensor Products

The Khatri-Rao product is useful in variances in statistics, multi-way models, linear matrix equations, and signal processing [26,30]. The face-splitting product is useful in convolutional layers in neural networks and digital signal processing in a digital antenna array [31,32].

The code generation method shown in Sec. VI-B can be easily extended to support the Khatri-Rao and face-splitting products given in definitions II.5 and II.6 respectively. An \texttt{mvmul} command can be generated for each index $i$ on the operands $a_i$ and $b_i$.

3 Higher rank cross products can be defined using the Levi-Civita symbol $\epsilon_{ijk}$, which we omit due to relatively few applications.
Chaining multiple operations into expressions is supported. The code generator traverses the AST with the tensor algebra operator precedence discussed in Sec. III-A and each code generation command is called sequentially as outlined in Sec. VII. As a prototype, the Apollo compiler assumes the arguments are valid and performs no expression-related error handling.

VII. DISCUSSION

There are still additions that will need to be made to the Apollo language in order to fully optimize optical computations. Most importantly, we will need to use our tensor storage algorithm only for highly sparse tensors involved in intermediate computations; we currently implement it for all tensors. We plan to also extend Apollo to generate t1926 and host instructions, integrate t1926 instructions with Tachyon 1, and develop the methodology by which Tachyon 1 would interact with the host CPU. Neural network activation functions, such as ReLU, sigmoid, and softmax, are planned to be hard-wired into the microchip; we will extend the language to support neural networks when this occurs. We also plan to add more useful tensor algebra operations based on the foundation discussed in this paper, such as the Matricized Tensor Times Khatri-Rao Product (MTTKRP). These and other extensions will help Apollo become a more powerful and efficient language.

Future research should explore tensor storage methods that will be able to more efficiently represent sparse tensors while still making them easy to index into. In order to optimize for speed, it will also be crucial to investigate how to best minimize required communication between Tachyon 1 and the host CPU, as converting between optical and electrical signals takes a significant amount of time. We plan to conduct this research ourselves, but at the same time encourage others to look into it as well.

In the future, we plan on extending the advances made in developing the Apollo language to build APIs for high-level languages (e.g., Python, Java, C++, etc.) so that they will be able to utilize Tachyon 1. This will allow users of conventional languages to be able to harness the speed of optical computing for applications such as physics simulations and ML. We specifically plan on building libraries able to integrate with the TensorFlow and PyTorch APIs so that users will be able to run ML models made with these APIs on Tachyon 1.

Our current design framework for Apollo leads the way for more powerful calculations to be performed faster on a new generation of hardware. With future advancements and optimizations, Apollo has the potential to impact numerous fields in engineering, computer science, and the natural sciences by allowing for significantly faster tensor algebra computations.

VIII. CONCLUSION

In this paper, we show how to perform tensor algebra computations on an optoelectronic microchip through Apollo, a domain specific language designed for this purpose. We then go over the language, compiler, and virtual machine designs. Next, we show a new way to store tensors that outperforms both conventional storage and CSF format from a memory viewpoint while still being compatible with our optical hardware. Finally, we go over the compilation of tensor algebra expressions into matrix-vector multiplications, which are native to our microchip. We illustrate how complex tensor algebra expressions can be run quickly and efficiently through our methods. Finally, we discuss the impact of our research, provide suggestions for future research avenues, and outline how we plan to extend the Apollo language.

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