Versatile Link PLUS transceiver development

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Abstract: The Versatile Link PLUS project targets the phase II upgrades of the ATLAS and CMS experiments. It will develop a radiation resistant optical link, operating at up to 10 Gb/s in the upstream and up to 5 Gb/s in the downstream directions with a smaller footprint and higher channel count than its predecessor. A low-profile package is being developed that allows volume production at reduced costs, but which nevertheless can be configured to suit the individual channel count needs of different detectors. This paper describes the development strategies and summarizes the status of the feasibility demonstration phase of the project.

Keywords: Front-end electronics for detector readout; Optical detector readout concepts; Radiation-hard electronics
1 Introduction

During the phase II upgrades of the ATLAS and CMS experiments at the Large Hadron Collider (LHC) several detectors and systems will be replaced to maintain or improve their physics performance despite an order of magnitude higher luminosity and level 1 trigger rate. To cope with the increasing data volume and the higher trigger rate, high-speed optical links will be deployed in large quantities as part of the upgrade programme. The tight space constraints and the high channel count of the on-detector electronics will require to develop a low-profile (20 mm x 10 mm x 2 mm target), multi-channel front-end component. During their expected lifetime these components have to withstand the on-detector radiation levels ($1 \text{ MGy total dose}$, $2 \times 10^{15} \text{n/cm}^2$ and $1 \times 10^{15} \text{hadrons/cm}^2$ total fluence) and they have to operate over a wide temperature range ($-35 \degree \text{C} - +60 \degree \text{C}$). The Versatile Link PLUS (VL+) project is developing custom front-end modules that fulfil these requirements. The front-end module will be based on radiation-hard Laser Diode Driver (LDD) and Transimpedance Amplifier (TIA) ASICs, and commercial Vertical Cavity Surface Emitting Laser (VCSEL) and PIN Photodiode (PD) components. To suit the specific needs of different detectors, such as the number of transmit and receive channels, the modules will be configurable. The proposed front-end module variants are described in section 2.

To achieve the aforementioned goals with the lowest possible risk the VL+ project is pursuing two development paths with several industrial partners. In the first case, CERN will work with commercial module manufacturers that are willing to customize their proprietary package to include the above mentioned components. To launch the discussion with various module vendors a procurement strategy has been defined. The modification steps and the procurement roadmap are detailed in section 3. In the second case, a full custom front-end module is being designed by CERN based on the same active components as in the first case and a miniaturized optical coupling block, which will be assembled by an industrial partner. To demonstrate the feasibility of the full
custom VL\(^+\) transceiver development, three prototype versions have been designed, manufactured and tested. Section 4 describes these prototypes, presents measurement results obtained during functional tests, and summarizes the experience gained during this iterative process.

2 Versatile Link PLUS transceiver

The architecture of the VL\(^+\) system shown in figure 1 is similar to the one of its predecessor, the Versatile Link [1, 2]. Close to the detector in the radiation zone, the custom VL\(^+\) transceiver (VTRx\(^+\)) interfaces between the high-speed serializer/deserializer circuits and the multi-mode optical fibre plant. In the radiation-safe zone the back-end systems can use Commercial Off-The-Shelf (COTS) components, which are the best suited for a given readout architecture. Unlike its predecessor [3], however, the VTRx\(^+\) will be asymmetric in terms of data rate and number of channels in the up-, or downstream directions.

The VTRx\(^+\) consists of the following sub-components. In the transmitter path, the laser diode driver (LDD) performs the high-speed signal conditioning to properly bias and drive a VCSEL-type laser wire-bonded directly at its output. The LDD will operate at up to 10 Gb/s. At the receiver side, the optical signal is converted to electrical using a PIN photodiode (PD). The weak electrical signal is then amplified by the transimpedance and limiting amplifier (TIA), which operates at up to 5 Gb/s. To resist tracker-grade radiation levels mentioned in section 1, radiation-hard LDD [4–6] and TIA [7] ASICs have been developed and commercial VCSEL and PIN chips have been qualified in the framework of the VL\(^+\) project. Finally, to couple light from the VCSEL to the fibre and from the fibre to the PD, the transceiver will use a miniature optical coupling block. The VTRx\(^+\) module should have an electrical and/or an optical connector interface for easier installation and maintenance.

Detectors may have different requirements depending on their readout architecture. The VL\(^+\) project addresses these needs by proposing different VTRx\(^+\) variants offering up to 1Rx and up to 4Tx channels in the same form factor, as shown in figure 2. The four transmitter channels can be implemented either using single channel LDDs or using an LDD array, however, the second option would greatly simplify the design and manufacturing. In the latter case unused transmitter channels will be disabled by configuring the LDD array.
3 Commercial module modification

During the past few years, the optical communications market has been boosted by the needs of large data center applications and miniaturized parallel optical engines became available from several vendors. These devices typically support high-speed data link applications at 10 Gb/s and beyond, and are usually available in small form-factor bi-directional (e.g. 4Tx+4Rx) or uni-directional (e.g. 12Tx or 12Rx) packages. CERN has recently launched a Market Survey to identify firms that have the know-how and technology required to customize their existing optical multi-channel transmitter and receiver modules to meet the VL⁺ requirements. Using this approach, the VL⁺ project could benefit from the vendor’s experience in the field of manufacturing and reliability. To enjoy the cost benefit from the volume production and to reduce the non-recurring engineering (NRE) cost, however, the customization should be minimized. The Market Survey includes evaluation of samples according to steps 0–3 of the modification roadmap shown in figure 3. In step 0 CERN evaluates a Commercial Off-The-Shelf (COTS) module in order to assess whether the firm masters the required technology. Step 1 is a minor customization involving the removal of the standard ASICs that are assumed not to be sufficiently radiation-hard for the final application. The step 1 module is used to assess the environmental (including radiation) resistance of the module packaging. Steps 2 and 3 are minor modification steps that re-use existing parts available from the firm to include custom radiation-hard ASICs. Step 2 uses a single-channel LDD whereas step 3 uses a quad-channel LDD, both developed in the framework of the VL⁺ project. Following on from the Market Survey, CERN will launch a Price Enquiry for the development of a custom optical module in step 4. The outcome of step 4 is a production-ready prototype that meets the VL⁺ specifications including the mechanical dimensions and connector interface. Companies having successfully completed development in step 4 (on time, in budget) will be invited to tender for full production starting in 2019.

4 Full-custom development

Although there are many benefits to working with industrial partners as described in section 3, that option may become too expensive beyond a certain level of customization due to high NRE costs. For example, this could become an important limit for meeting the target height constraint.
of 2mm in case of the VTRx+ module. The full-custom module development represents an alternative path, which allows to develop VTRx+ variants for the most exacting LHC applications. In addition, it provides a framework for building prototypes with in-house developed ASICs, for testing miniature light coupling solutions and to understand technological challenges related to optical module packaging.

To demonstrate the feasibility of this concept, three VTRx+ prototype versions have been designed by CERN and have been assembled by an industrial partner. The main components of these prototypes are summarized in table 1. The first two versions are based on the same active components: a single-channel commercial LDD, CERN’s radiation-hard Gigabit Transimpedance Amplifier (GBTIA) and commercial VCSEL and PIN photodiode chips from Philips Photonics (ULM). The 3rd prototype version uses the same receiver components, but includes the four-channel, radiation-hard Laser Driver Quad (LDQ10) and VCSEL array from Philips Photonics in its transmitter path. Two different light coupling blocks have been used on these prototypes. Version 1 and 3 use US Conec’s Mechanical Optical Interface (MOI), while Version 2 is based on a low-profile coupling block from another vendor. The MOI supports up to 12 channels (either Tx or Rx), while the low-profile coupling has 2Tx and 2Rx optimized lenses. However, the MOI mated with a PRIZM connector is twice as tall as the low-profile coupling block. The picture of the 3 assembled prototype versions is shown in figure 4. Prototype modules have been verified with functional tests detailed hereafter in sections 4.1 and 4.2.

Table 1. Table summarizing the components used in the different VTRx+ prototype versions.

| Version | Configuration | LDD   | VCSEL         | TIA   | PD    | Light Coupling Unit |
|---------|---------------|-------|---------------|-------|-------|---------------------|
| V1      | 1Tx+1Rx       | COTS  | single        | GBTIA | single| US Conec MOI        |
| V2      | 1Tx+1Rx       | COTS  | single        | GBTIA | single| Low-profile          |
| V3      | 4Tx+1Rx       | LDQ10 | quad array    | GBTIA | single| US Conec MOI        |

4.1 Transmitter characterization

To assess the performance of the transmitter, optical eye diagrams have been captured and the following parameters have been extracted from the eye diagram data for a quantitative comparison:
1. Optical Modulation Amplitude (OMA);
2. Eye Height (EH);
3. Extinction Ratio (ER);
4. Rise and fall times ($T_r$ and $T_f$);
5. Total and deterministic jitter ($T_J$ and $D_J$).

Some example eye diagrams measured at 5 Gb/s and 10 Gb/s using prototype version 1 and at 4.8 Gb/s and 10 Gb/s using prototype version 2 are shown in figure 5 and 6, respectively. Since prototype version 1 and 2 are based on the same active components, the noticeable performance difference is likely related to the different light coupling blocks. It is important to note, however, that in case of prototype version 2 the alignment between the VCSEL/PD chips and the light coupling unit might be affected due to the sub-optimal allocation of the Tx/Rx optimized lenses.

The parameters extracted from the eye diagrams measured at 5 Gb/s and 10 Gb/s using prototype version 1 and at 4.8 Gb/s and 10 Gb/s using prototype version 2 are displayed as radar plots in figure 7 and 8, respectively. These plots confirm that alignment between the VCSEL chip and the lenses of the optical coupling block is sufficiently good in both cases. However, in case of the low-profile coupling block there is more spread of OMA and EH parameters among tested devices, and there is slightly more jitter than on the prototypes built with US Conec’s MOI.
Figure 6. Transmitter eye diagrams measured on prototype version 2 using a pseudo random bit sequence (PRBS-7) running at 4.8 Gb/s and 10 Gb/s. The increased jitter is likely due to sub-optimal allocation of Tx/Rx optimized lenses of the light coupling unit.

Figure 7. Radar plots showing parameters extracted from eye diagram measured on prototype version 1 using a pseudo random bit sequence (PRBS-7) running at 5 Gb/s and 10 Gb/s.

Figure 8. Radar plots showing parameters extracted from eye diagram measured on prototype version 2 using a pseudo random bit sequence (PRBS-7) running at 4.8 Gb/s and 10 Gb/s.

Figure 9 and 10 show the eye diagrams measured on the four transmitter channels of a version 3 prototype (device 7) at 4.8 Gb/s and 10 Gb/s, respectively. The corresponding eye diagram parameters displayed on radar plots are shown in figure 11. These eye diagrams were captured...
using the default driver settings resulting in a power consumption of approx. 50 mW/ch (power consumption at maximum driver settings is approx. 70 mW/ch). One can observe some overshoot and ringing on the eye diagrams, which lead to more data-dependent jitter (ISI) at 10 Gb/s. Different LDQ10 laser driver variants are currently being characterized, with the aim of selecting the design resulting in best performance in a VTRx+ module.

4.2 Receiver characterization

Following the transmitter tests, the receiver performance was assessed by performing Bit Error Rate (BER) tests. Version 1 prototypes have been tested in optical loop-back, while Version 2 and 3 prototypes have been tested using a reference SFP+ transmitter. The measured BER curves are shown in figure 12. According to these results the receiver sensitivity is around -15 dBm, which is close to the values measured on multi-mode VTRx samples based on the similar receiver components (i.e. GBTIA and GaAs PIN photodiode). Likewise, the power consumption of the receiver portion of the prototypes remains at the level of 100 mW as it is on the current generation of VTRx.

4.3 Full-custom development summary

The different full-custom prototype versions allowed us to test and compare the performance of miniature light coupling solutions (V1 and V2) as well as to evaluate the performance of the first quad-channel laser diode driver (V3). Both the MOI and the low-profile lens array offer good optical coupling and the prototypes using them have similar transmitter and receiver performance.

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Simulations carried out by the manufacturers show that good optical coupling between VCSEL/PIN photodiode chips and fibre requires better than ±10 µm lateral alignment tolerance, which can be achieved with traditional die bonding equipments. According to the feedback received from the assembly house, the MOI has a slight advantage during pick-and-place and alignment steps, while the low-profile coupling block has larger contact surface glued to the module substrate, which may result in a more reliable assembly. Working with an industrial partner on module packaging provided insights into the assembly process, which will help to understand the technological challenges. The acquired know-how will allow us to optimize the full-custom design and to work efficiently with firms on the commercial module customization.

Figure 10. Transmitter eye diagrams measured on prototype version 3 using a pseudo random bit sequence (PRBS-7) running at 10 Gb/s.

Figure 11. Radar plots showing parameters extracted from eye diagram measured on prototype version 3 using a pseudo random bit sequence (PRBS-7) running at 4.8 Gb/s and 10 Gb/s.
Figure 12. Bit Error Rate (BER) curves measured on different prototype versions using a pseudo random bit sequence (PRBS-7).

5 Conclusion

Much progress has been made during the feasibility demonstration phase of the Versatile Link+ project. To develop radiation hard optical front-ends, two parallel development paths are being pursued. a) A procurement strategy compatible with CERN purchasing rules has been established and a Market Survey has been launched to identify firms willing to work with CERN on transceiver customization. b) To demonstrate the feasibility of the full-custom module development, three prototype version have been designed by CERN and have been manufactured by an industrial partner. The functional tests carried out in the laboratory demonstrate the good performance of these prototypes and validate the choices made. Version 3 of the prototypes is the first instance of a radiation-hard VTRX+ module with up to four transmitter channels. To achieve the 2mm module height required by the most demanding applications, however, further design iterations will be required.

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