Optical memory architectures for fast routing address look-up (AL) table operation

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Abstract

Today, the increasing demand for fast routing processes has turned the address look-up (AL) operation into one of the main critical performance operations in modern optical networks, since it conventionally relies on slow-performing AL tables. Specifically, AL memory tables are comprised of content addressable memories (CAMs) for storing a known route of the forwarding information base of the router, and random access memories (RAMs) for storing the respective output port for this route. They thus allow for a one-cycle search operation of a packet’s destination address, yet they typically operate at speeds well below 1 GHz, in contrast with the vastly increasing optical line rates. In this paper, we present our overall vision towards light-based optical AL memory functionalities that may facilitate faster router AL operations, as the means to replace slow-performing electronic counterparts. In order to achieve this, we report on the development of a novel optical RAM cell architecture that performs for the first time with a speed of up to 10 Gb s⁻¹, as well as our latest works on multi-bit 10 Gb s⁻¹ optical CAM cell architectures. Specifically, the proposed optical RAM cell exploits a semiconductor optical amplifier–Mach–Zehnder interferometer in a push-pull configuration and deep saturation regime, doubling the speed of prior optical RAM cell configurations. Error-free write/read operation is demonstrated with a peak power penalty of 6.2 dB and 0.4 dB, respectively. Next, we present the recent progress on optical CAM cell architectures, starting with an experimental demonstration of a 2-bit optical CAM match-line architecture that achieves an exact bitwise search operation of an incoming 2-bit destination address at 10 Gb s⁻¹, while the analysis is also extended to a numerical evaluation of a multi-cell 4-bit CAM-based row architecture with wavelength division multiplexed outputs for fast parallel memory operations at speeds of up to 4 × 20 Gb s⁻¹. Finally, we present a comparative study between electronic and optical RAMs and CAMs in terms of energy and speed and discuss the further challenges towards our vision.

1. Introduction

The exponential increase of internet traffic due to cloud computing and other emerging web applications has fueled the need for a higher internet access speed, thus leading to the massive installation of high-speed optical interconnects closer to the internet end user, while most emerging optical interconnect applications, e.g. high performance computing, data centers etc have also been shaped around low latency end-to-end communications [1, 2]. Owing to the growing maturity of photonic integrated technologies, 200 Gb s⁻¹ are already a commercial commodity, while optical transceivers are currently scaling optical line rates to 400 Gb s⁻¹ and up to Tb/s [3, 4]. As bandwidth and switching speeds increase, the time allotted to perform core router functions is drastically reduced. In contrast, however, the dramatic increase of mobile internet users has also significantly increased the number of addressable points and consequently the forwarding and routing table

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entries, even causing the depletion of the remaining IPv4 address space and leading to the advent of an IPv6 protocol with a quadrupled need for address look-up (AL) requirements [5]. This increasing need for faster routing functionalities, including AL, which also requires fast hardware memories to perform fast look-up of the packet’s destination address immediately upon its arrival and across the forwarding information base (FIB) of the router.

On the path to speeding up hardware memory and lower latency times when fetching data, state-of-the-art highly performing electronic static random access memory (RAM) cell technology has managed to achieve operation up to 5 GHz [6–8]. However, RAMs are inherently limited in fast AL as, owing to the address-based fetching of data, they would require multiple sequential random access to the memory and consecutive searches of the desired content. As a result, their high speed can be mainly exploited when reading data from a certain RAM location, rather than for fast searching across a FIB, while their speeds have also been shown to degrade as we move to smaller processing nodes [9]. This in turn forces the use of a specialized hardware AL memory, to enable address resolution at the wire speed upon the arrival of a packet [10, 11].

Aiming towards performing AL with only one memory access request, several hardware-based implementations have been so far proposed [12, 13] focusing on new advancements in electronic content addressable memories (CAMs) to exploit its inherent parallelism for fast search operation. To date, CAMs are used in modern routers to facilitate AL table functionalities within one clock cycle [12] as they offer content-based addressing of the stored data, as opposed to the location-based addressing of RAMs [14, 15]. However, the operational speed of CAM cells still does not exceed the barrier of a few hundreds of MHz, as they are limited by the low operational speeds and resistive-capacitive capacities of the underlying interconnect network of the multi-bit CAM match-line (ML) and AL table architecture. Indicatively, electronic CAMs fabricated at complementary metal–oxide–semiconductor (CMOS) processing technologies of 130 nm and 65 nm [16–18] have so far achieved a maximum speed of ~200 MHz [16] and ~400 MHz [17] respectively, while the latest 28 nm processing technology has delivered advancements only in terms of footprint and power consumption [18]. Despite a long history of optimization techniques for electronic mature electronic technology, state-of-the-art electronic CAMs are still scaling in terms of frequency at a slow pace, limited by the well-known electronic memory bandwidth bottleneck [19, 20] and seem incapable of keeping up with the increasing optical line rates [21]. This performance disparity is expected to continue impeding the routing system’s performance, if relying solely on slow-performing CAMs, as the increasing optical line rates will further necessitate energy-hungry, cost-expensive optoelectronic header conversions with subsequent data-rate down-conversion [22–24], to realize AL searches in MHz-only performing electronic AL tables.

Drawing from this memory bottleneck, there have been some recent advancements in photonic memories following different photonic integration approaches and architectural approaches to deliver speed, footprint, scalability and power consumption benefits [25–42]. However, the vast majority of photonic memory implementations so far reported have managed to develop only simplistic optical flip-flops (FFs) [32–41], that can only perform storing of the unitary bit. More recently, there has been an increasing research trend in combining high-bandwidth optical FFs with additional controlling circuitry, i.e. the access gate (AG) which allows for building more complex optical RAM cell layouts to support all RAM functionalities, i.e. read, write and block/grant access to the memory, to control the communication of the storage cell with the ‘outer world’ [25–31]. However, as in all these optical RAM cell demonstrations, the optical AGs have been mainly implemented as simple, unoptimized wavelength converters (WCs) [25–31], not tailored specifically for RAM operation, leaving room for further improvements in terms of high-speed operation. As a result, optical RAM cell demonstrations have so far exhibited speed capabilities only up to 5 Gb s⁻¹ [25, 27] not managing to outperform the performance of state-of-the-art electronics RAMs [43–53]. Still, in order to efficiently minimize the disparity between slow AL and continuously increasing optical transmission line rates, the development of optical CAMs is also required in order to synergize with fast optical RAM circuits towards enabling light-based AL tables with high-speed capabilities of 10 Gb s⁻¹ and beyond.

In this communication we present our vision and the latest progress on both functional elements, i.e. on optical RAM and CAM technologies, as well as on wavelength division multiplexed (WDM) multi-bit CAM architectures, suggesting a possible path towards realizing fast all-optical AL table architectures in the near future. Firstly, we initially describe the architecture of an AL table with a CAM table interconnected to a RAM table and its principle of operation; in addition, we give a short description of the prior work on optical memories at a single cell level and the integrated photonics required towards light-based AL functionalities. Then, we experimentally demonstrate a novel all-optical RAM cell utilizing an optimized differentially-biased strongly-saturated semiconductor optical amplifier–Mach–Zehnder interferometer (SOA-MZI) AG, achieving for the first time the option to exceed the 5 GHz operational speed of the state-of-the-art electronic and optical RAM cell and operate at speeds up to 10 Gb s⁻¹ [25, 27]. The proposed optical RAM cell layout is based on a monolithically integrated InP set-reset FF chip and a single hybrid integrated SOA-MZI-based AG operating in the deeply saturated SOA gain regime to control fast access to the FF memory, forming the fastest optical RAM
cell to date. Discussing the scaling from single-bit to multi-bit architectures and fully describing the vision of light-based AL functionalities, we also present our latest experimental work on a 2-bit optical CAM ML architecture for AL at 10 Gb s\(^{-1}\), the fast-performing 2-bit search operation based on content-based addressing of its stored data. The performance evaluation of the 2-bit ML is then extended with a physical layer investigation of a 4-bit all-optical CAM row architecture with ternary storing capabilities per cell to support the wildcard bit operation as well WDM-multiplexing of its four memory outputs for fast parallel comparison of the row, aiming to highlight the potential for speeds even up to 20 Gb s\(^{-1}\), in the case of fully integrated architectures [54].

Finally, we discuss the progress witnessed in the optical CAM and RAM areas and present a comparative study against electronic counterparts, so as to reveal the potential future challenges and next steps towards optical AL routing table architectures.

2. Architecture of an optical AL table

AL tables in high-end routers and packet switches consist of a two-dimensional table of CAMs for maintaining the routes of the FIB and a two-dimensional table of RAMs for storing the respective output port for this route. The most basic CAM cell, i.e. the binary CAM (B-CAM), comprises an FF that maintains one bit of the address of the stored route and an exclusive OR (XOR) comparison gate for fast exact comparison of the FF data with the incoming packet’s destination address, allowing to identify if the destination address belongs to the FIB or not. In addition, ternary CAM (T-CAM) cells also include a second FF unit to store another wildcard bit of subnet masks, i.e. the ternary X-state, whose output indicates whether we ‘care’ or ‘do not care’ for the result of the XOR comparison. Arranging multiple CAMs in one row for performing multiple XOR-based search operations allows for building an ML architecture that checks the matching of all the bits of the destination address. On the other hand, the RAM cell of the RAM table stores the output router port that the packet has to be forwarded, upon a match of its destination address. This AL memory architecture allows for the performance of a fast one-cycle search operation of a packet’s destination address across the FIB, yet it typically operates at speeds of 400 MHz and below 1 GHz, seemingly incapable of keeping pace with the vastly increasing line rates of the optical packet payload.

Our vision of light-based AL functionalities is to implement similar CAM and RAM table architectures that may facilitate faster search operations, as the means to replacing slow-performing electronic counterparts. Our proposed architecture and the main functional building blocks are conceptually illustrated in figure 1. Specifically, figure 1(a) presents an indicative example of a scheme where the routing table scheme consists of a T-CAM table interconnected to a RAM table through a proper encoding/decoding unit. The T-CAM table comprises a matrix of all-optical CAM cells following the architectural layout in figure 1(b) presented in [35] and stores all the possible destination addresses per row, while the RAM table comprises a matrix of all-optical RAM cells shown in figure 1(c) following the architectural layout presented in [25–27] and stores the respective addresses of the router output ports. In the case of an incoming packet the T-CAM table is responsible for identifying the destination address indicated by the packet header, while the encoding/decoding unit is responsible for activating the proper RAM table row that will in turn activate the proper router output port.

The operation of the optical AL memory table is described as follows. Each time, the destination address of an incoming packet is fed as the ‘search word’ into the T-CAM table, while the proper router output port to be activated emerges as the ‘retrieved word’ in the RAM table output, as shown in figure 1(a). During the AL operation the search word is broadcast to all the T-CAM rows and is bitwise compared with each one of the stored words that reside in the T-CAM table rows. In case of a proper match with a stored word in a T-CAM row, a proper ML signal is generated at the respective T-CAM row output. For example, the search word ‘1110’ matches successfully only to the world ‘1XX0’ that is stored in the second T-CAM row, where the ‘X’ state denotes that this particular bit can be matched with an input search bit of either 1 or 0. As such, the encoding/decoding circuit activates the second RAM table row, which designates that ‘port B’ is the port to direct the incoming packet in the next hop. Finally, figure 1(d) presents a CAM row architecture where a novel WDM-encoded ML scheme can be exploited to provide parallel write and comparison functionality for complete fast comparison of optical words in an optical WDM-enabled AL architecture.

Within this frame, our most recent research efforts have been aligned towards overcoming the frequency barrier set by electronic memories by realizing CAM- and RAM-based configurations completely in the optical domain [25–27, 54–59]. The first all-optical B-CAM cell demonstrations was recently reported based on a monolithically integrated SOA-MZI-based FF with speed capabilities of up to 10 Gb s\(^{-1}\) [56] achieving a large leap in the speed of memory content addressing operations; it was later followed by a series of significant achievements [54–59] also advancing the scalability [57] and architectural complexity by introducing all-optical T-CAM cell configurations [55] and realizing optical CAM ML [59] architectures. While optical CAM cells have reached 10 Gb s\(^{-1}\) operation, optical RAM cells have been limited to speeds less than 5 GHz [56]. Drawing from
this separate operational speeds demonstrated for RAM cells and CAM cells so far, we are here developing a novel RAM cell architecture that exceeds for the first time the 5 GHz barrier of electronics, achieving an operation of 10 Gb s$^{-1}$, which combined with our most recent work on 10 Gb s$^{-1}$ multi-bit optical CAM MLs [59], now holds for the first time the verified credentials for 10 Gb s$^{-1}$ AL functionalities directly in the optical domain.

3. Optical RAM architectures

In this section, we report on the key features of optical RAM cells and the proposed novel RAM cell architecture. Thus far, optical RAM cell architectures have deployed simple SOA cross-gain modulation (XGM) or SOA-MZI cross-phase modulation (XPM) switches, operating as unoptimized WCs with one control signal only [60]. As a result, their switching operation is limited by the lifetime of the carriers in the active region of the SOA, with the gain recovery from the saturated to the small signal gain being in the order of $>80$ ps [28, 61], inducing gain amplitude fluctuations that impose jitter and transient phenomena [62, 63]. In the proposed RAM cell architecture, two assist lights have been introduced in the architecture to act as holding beams to the SOA-MZI AG that deeply saturate the gain close to the transparency region and differentially biasing it, so as to circumvent the slow response of the carrier lifetime of the small signal gain and support thresholding and clipping functionalities for high-speed burst traffic [61, 64]. Moreover, the use of a push–pull scheme, with the control signal applied to both branches of the SOA-MZI AG, facilitates a symmetric configuration with more balanced and equalized signal power levels for the pulses after the switching operation of a control signal, thus significantly reducing the jitter at the final SOA-MZI signal output. This configuration facilitates shorter recovery times for the SOA gain and sharper rise and fall times in the order of 25 ps for the gated set and reset signals at the output of the SOA-MZI AG, in contrast to the 80 ps in the case of a single control signal acting as a simple WC scheme [28, 61] i.e. faster on/off switching times that allow for reducing the timing delay of the cascaded latching of the FF unit, so as to set it within the 100 ps window for a 10 Gb s$^{-1}$ write operation.

Following the rationale introduced by electronic static RAM cells [12, 25], in order to provide random-access control to a memory cell, prior to any read/write operation, an set reset (SR)-FF latching mechanism needs to always be combined with two additional AG elements to control the access of the incoming optical bit and its inverse (Bit) sequences to the memory cell. Transferring these principles into the optical domain, the optical AGs can be implemented by employing ON–OFF optical switches which are controlled by the access bit, together with an optical SR-FF which stores the logical content. To date, only a few optical RAM cells
demonstrations have been presented which also employ AG mechanisms to control communication with the ‘outer world’ yet which are based on a simplistic WC AG which supported unoptimized and moderate switching latency values [25–27, 31].

In this section we present for the first time an all-optical static RAM cell architecture which incorporates a fast AG mechanism relying on a push–pull SOA-MZI operating in the deeply saturated SOA gain regime, offering read/write functionalities at 10 Gb s\(^{-1}\). The proposed architecture utilizes a monolithically integrated InP FF chip and a hybrid integrated coupled SOA-MZI for the latching and the AG mechanism respectively, advancing the speed capabilities of optical RAMs by two times compared to previous demonstrations [25, 27]. By operating the SOA-MZI AG in a differentially-biasing mode and exploiting the gain clamping of the two SOAs, we can take advantage of the fast gain recovery dynamics of the SOAs [60], achieving fast switching times, thus enabling change of the RAM content within the 100 ps bit-slot for 10 Gb s\(^{-1}\) read/write RAM operation. Error-free operation of the proposed RAM cell is demonstrated at 10 Gb s\(^{-1}\) write/read operations with a peak power penalty of 6.2 dB and 0.4 dB, respectively at a bit error rate (BER) of 10\(^{-9}\).

### 3.1. 10 Gb s\(^{-1}\) experimental setup and results of optical RAM with a fast SOA-MZI AG

Figure 2(a) presents the logical diagram of an optical RAM cell and figure 2(b) depicts the experimental setup used to verify the proposed optical RAM cell architecture with the fast differentially-biased AG mechanism. As can be seen in figure 2(b), the AG relies on a SOA-MZI which is interconnected through an arrayed waveguide grating (AWG) to an all-optical FF memory unit based on coupled asymmetric SOA-MZIs following an already known master-slave principle [59], thus forming the optical RAM cell layout.

Two continuous wavelength (CW) auxiliary signals at a λ3 = 1548 nm wavelength generated by distributed feed-back (DFB) lasers are injected into the AG through control ports E and D. A pair of complementary Bit/\(\overline{\text{Bit}}\) data streams, after being modulated by two LiNbO3 modulators at the wavelength λ1 = 1549.5 nm and λ2 = 1550.3 nm respectively, which is driven by the complementary data outputs of a programmable pattern generator (PPG) at 10 Gb s\(^{-1}\), are coupled together through a 50/50 coupler and inserted into the AG unit through the input port G of the SOA-MZI, while their outputs emerge at the switched port C of the SOA-MZI. In contrast, the access controlling signal, also modulated at 10 Gb s\(^{-1}\) by the PPG with a pseudo-random bit sequences (PRBSs)-based Bit pattern and imprinted on λa = 1551.1 nm wavelength, is initially split through 50/50 coupler into two taps and fed to the two control branches of the SOA-MZI through ports H and A respectively, as shown in figure 2(b). By such, the AG mechanism is configured as a fast strongly-saturated push-pull SOA-MZI [60] where the two external pump lights at λ3 saturate the gains of the two SOAs of the AG leading them at a regime with faster gain recovery dynamics, mainly due to carrier heating and spectral hole burning [60] while the push–pull configuration balances out the differential phase shift between the two branches at transient gain recovery timings after a switch pulse. Following the switching operation of the Bit/\(\overline{\text{Bit}}\) signals by the AG based on the access controlling streams, the output signal is obtained at the C output port of the SOA-MZI AG, as shown in figure 2(b), amplified through an erbium-doped fiber amplifier (EDFA), to compensate for the losses of the fiber-pigtailed implementation, and demultiplexed through an AWG, to form the set and reset signals. The two set/reset signals are then bit-level synchronized through an optical delay line (ODL) before being fed at the respective set/reset branches of the FF, to control its memory switching operation. The FF unit is based on two coupled asymmetric SOA-MZI switches in a master-slave configuration [25]. More specifically, the two SOA-MZI switches are powered by two CWs at wavelengths λ4 = 1548.5 nm and λ5 = 1547.7 nm through ports A and E respectively, while the λ1-set and λ2-reset signals are transmitted through the C and D ports counter-propagating to the CW signals. As such, when an incoming set pulse arrives at the master SOA-MZI switch, it suppresses its switching operation, setting it in the slave state and allowing the

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**Figure 2.** (a) Optical RAM cell logical diagram. (b) Experimental setup of the RAM cell architecture with a fast strongly-saturated push–pull SOA-MZI AG mechanism at 10 Gb s\(^{-1}\).
opposite SOA-MZI to recover in the master condition, thus changing the data content of the FF. Due to the symmetric configuration of the FF, the roles of the master and slave are interchangeable, while the FF content during the write operation is obtained through a circulator and monitored in an oscilloscope (OSC) for evaluation purposes. During the read functionality, the overall output of the RAM cell is recorded at the input of the AG by means of an optical circulator. In the proposed layout, by taking advantage of the fast-dynamics achieved through the strongly-saturated push-pull SOA-MZI AG a switching time in the order of 20 ps is obtained at the AG part. This only adds a small jitter penalty to the latching of the FF which is in the order of 70 ps, yielding in this way to an overall latching operation of the RAM cell within the 100 ps bit-slot and finally achieving 10 Gb s\(^{-1}\) RAM operation.

Figure 3 shows the experimental results obtained during the write operation at 10 Gb s\(^{-1}\). Specifically, figure 3(a) depicts the time traces of the access signal serving as the control signal at the fast AG with the power level measured at 10 dBm, and the respective eye diagram. Figures 3(b) and (c) depict the traces of the complementary Bit/\(\overline{\text{Bit}}\) which represent the data bit stream to be written in the RAM cell, while their power levels were measured both at \(-3\) dBm, as well as their respective eye diagrams. The inverted on/off gating upon the Bit/\(\overline{\text{Bit}}\) sequences is imprinted on the set and reset signals shown in figures 3(d) and (e) with the respective eye diagrams for both signals. In figure 3(f) the FF output time trace and eye diagram are shown collected at the output port of the RAM cell, confirming the successful storage operation of the incoming values of the Bit/\(\overline{\text{Bit}}\).

As already known [25–27] storage operation takes place every time the incoming access bit equals a logical ‘0’, while, in contrast, when the access bit value turns into a logical ‘1’ a strong access pulse enters in the AG, blocking both set and reset signals while the memory content retains the latest value. The output eye diagram of RAM exhibits an extinction ratio (ER) of 6.3 dB and AM of 2.1 dB. Figure 3(g) shows the BER measurements, revealing an error-free operation for all stages of the experiment with the bit signal serving as a reference. To this end, the \(\overline{\text{Bit}}\) and access bit streams induced a 0.2 dB power penalty, while the set and reset signals have a 1.4 dB and 2.1 dB power penalty at a BER of \(10^{-9}\) respectively. Finally, for the write operation BER measurements revealed a 6.2 dB power penalty, whereas for the read operation, a 0.4 dB at a BER of \(10^{-9}\). The SOA1 and SOA2 were powered by 200 mA and 330 mA injection currents respectively, while the two gain-clamping auxiliary CWs feature optical powers of 7 dBm for \(\lambda_{\text{aux1}}\) and 3 dBm for \(\lambda_{\text{aux2}}\) respectively, so as to deeply saturate the gain of each SOA close to the gain transparency region and at the same time operate the SOA-MZI in a push-pull configuration.

4. Optical CAM and ML architectures

Following the development of a 10 Gb s\(^{-1}\) optical RAM cell, in this section we chart our latest work on a 2-bit optical CAM ML architecture which achieves exact bitwise search operation of an incoming 2-bit destination address at 10 Gb s\(^{-1}\).

4.1. Optical CAMs and ML architectures for fast AL tables

The first optical B-CAM cell was presented in 2016, successfully providing comparison and write operation at 10 Gb s\(^{-1}\) [56], thus improving the speed capabilities offered by its electronic counterparts [16–18] from a MHz to GHz regime while holding high-speed credentials to enable further speed enhancements. The demonstrated B-CAM cell was based on monolithically integrated FF for the fast storing element together with a hybrid SOA-MZI XOR-based logic gate serving for the fast comparison between the stored bit and the search bit. This configuration was later expanded into a completely optical T-CAM cell architecture extending the capabilities of the experimentally demonstrated 10 Gb s\(^{-1}\) optical B-CAM cell to the third matching state ‘X’ or ‘care/don’t care’, enabling in this way the subnet-masked operation required in modern router applications [57]. The scaling credentials of the proposed scheme were successfully evaluated through physical layer simulations in the
Recently, the first all-optical T-CAM cell was experimentally validated at 10 Gb s$^{-1}$; it comprised of two monolithically integrated InP FF and a SOA-MZI optical XOR gate. The two FFs served for storing the data bit and the ternary state '$X$', respectively, with the XOR gate used for comparison between the stored FF data bit and the search bit. The experimental results obtained from the verification indicated error-free operation at 10 Gb s$^{-1}$ for both write and ternary content addressing of the optical T-CAM cell, suggesting that the proposed architecture could in principle lead to all-optical AL memory architectures for high-end routing applications.

In this section we present our most recent results extending the previous single cells demonstrations towards the first 2-bit all-optical ML architecture, with matching or not matching information of the result of the content-based search operation in its two CAM cells being wavelength-encoded and optically multiplexed by an AWG multiplexer. The final output and matching signal is then regenerated at a cascaded SOA-based XGM WC, which collects the multi-wavelength ML signals.

4.2. Experimental setup and results of 2-bit all-optical CAM-based ML at 10 Gb s$^{-1}$

Figure 4(a) presents the logical diagram for a 2-bit optical CAM ML and figure 2(b) depicts the experimental setup employed to verify an all-optical CAM ML architecture for an indicative number of 2 CAM cells (optical CAM cell #1 and #2). Each optical CAM cell, as can be seen in the figure 4 insets, relies on the architectural layout of and is comprised of a packaged integrated FF which serves to retain the CAM content. Each FF includes two coupled SOA-MZI switches interconnected through a 5 mm-long waveguide, following in this way a master-slave configuration with a total footprint of 6 $\times$ 2 mm$^2$. The FFs have been developed within the frame of the EU-funded project PARADIGM [27]. The XOR optical gate’s operation was performed by using a hybrid silica-on-silicon SOA-MZI device. For the experimental evaluation of this scheme, two CW laser beams at $\lambda_1 = 1554.13$ nm and $\lambda_2 = 1553.81$ nm are employed, which are inserted into the respective SOA-MZIs of the FFs, while the set/reset data signals are inserted in the respective FF’s ports when a new CAM line content has to be stored through the write operation [56]. The output signals of the two FFs obtained at the $\lambda_1$ wavelength are then injected as control signals through port D to the lower branches of the respective SOA-MZIs for their use as XOR gates in CAM cell #1 and CAM cell #2, respectively. Two PPGs were employed to drive the two LiNbO3 modulators to produce two 2$^{7-1}$ PRBSs at $\lambda_3 = 1555$ nm, emulating the two search lines (SLs) which contain the 2-bit destination address of an incoming packet. Each PRBS signal is introduced into a CAM cell via port A to the upper branch of the respective XOR gate, acting as the second control signal which will be compared with the corresponding FF output. Two laser beams at $\lambda_4 = 1549.35$ nm and $\lambda_5 = 1552.60$ nm were used as the input signals for XOR1 and XOR2, respectively and were injected via port B of the corresponding SOA-MZI.

Consequently, the two XOR output signals emerge at the F ports of the SOA-MZI XOR gates with the XOR1 and XOR2 output signals being wavelength-encoded and optically multiplexed by an AWG multiplexer. The final output and matching signal is then regenerated at a cascaded SOA-based XGM WC, which collects the multi-wavelength ML signals.
XOR2 output being encoded at $\lambda_4$ and $\lambda_5$ wavelengths, respectively. These two signals are then multiplexed by means of an AWG device, producing in this way a multi-wavelength ML signal at its output, with the outcome of each search-bit operation per CAM cell being designated by a different wavelength. This multi-wavelength ML signal, acting as the control signal, is then directed into a SOA-based XGM WC which uses a CW signal at $\lambda_{ML} = 1550.16$ nm as its input signal. By filtering the output of the SOA-XGM gate through an optical bandpass filter (OBF) centered at $\lambda_{ML}$, the result of the inverted WC operation is obtained as a binary non return to zero (NRZ) ML signal imprinted on a single $\lambda_{ML}$ wavelength. The final ML signal is finally fed to an OSC and a BER tester (BERT) for signal integrity evaluation. EDFAs and polarization controllers (PCs) have been used at various stages of the experimental setup to enable proper power and polarization adjustments.

Figure 5 illustrates the results collected from the experimental evaluation of the 2-bit all-optical CAM ML at 10 Gb s$^{-1}$. Figures 5(a)–(d) depict the write operation of the set-reset FF SR-FF#1 of CAM cell#1 and figures 5(a) and (b) show the time traces of the FF#1 set and reset signals, accordingly. Figure 5(c) depicts the output signal of FF#1 while figure 5(d) shows the inverted output signal of FF#1. In figures 5(a)–(d), successful write operation can be confirmed as the FF changes its logical content and its respective FF output signal state every time a set pulse appears after a reset pulse and vice versa. Figures 5(c)–(h) show the synchronized time traces for the single-bit content addressing operation at 10 Gb s$^{-1}$, with the first and second column referring to the single-bit operation at CAM cell#1 and #2, respectively. The time trace of the FF outputs at the $\lambda_1$ wavelength for both CAM cells can be seen in figure 5(e), corresponding to a CAM line content of ‘01’ with the CAM#1 and CAM#2 cells having a logical state ‘0’ and ‘1’, respectively. Figure 5(f) shows the traces of the two SL signals before being inserted to the respective CAM cells, while the corresponding XOR output pulse traces and eye diagrams for the two CAM cells are depicted in figures 5(g) and (h), respectively. Figure 5(h) shows clear eye openings with an average ER of 8.5 dB. In the case of a match, both the stored CAM cell content and the respective SL bit are equal resulting in no light at the CAM cell output which provides a logical ‘0’ as the XOR output. On the other hand, if the stored CAM cell bit and the respective SL bit present different logical values, the XOR operation provides a logical value of ‘1’ [56, 59]. Figures 5(i)–(l) depict the 2-bit operation of the complete optical ML operation.

Figures 5(i) and (j) show again the traces of the CAM cell#1 and CAM cell#2 output signals which are equivalent to the traces of figure 5(g). These signals are then multiplexed via an AWG and a wavelength multiplexed multi-level optical signal is produced at its output, as can be seen in figure 5(k). This multi-level signal features three different power levels, with each level referring to three different cases of search misses: (a) the zero-power level stems from a ‘00’ logical value for both CAM cell output signals corresponding to an exact two-bit matching case; (b) the middle power level originates from a logical ‘1’ value at only one of the two CAM cell outputs and can be interpreted as a single-bit mismatch and finally the highest power level refers to a two-bit mismatch which occurs when both CAM cell outputs have a logical ‘1’. To this end, figure 5(l) shows the ML pulse trace imprinted at $\lambda$ at the output of the SOA-XGM gate, after the XGM wavelength conversion operation with the multi-level signal of figure 5(k). As can be seen, a logical ‘1’ appears at the SOA output only in the case of a perfect (2-bit) match between the search and stored bits, while a logical ‘0’ emerges at the SOA output in all
present a simulation analysis of an optical ML, comprising 4 T-CAM cells which perform at 20 Gb s\(^{-1}\) and investigate the scaling of the T-CAM cell concept in view of scaling the ML functionalities in terms of speed and the number of memory cells, in this section, we go combinations stored in the two CAM cells. Finally, diagrams of the multi-level multi-wavelength signal after the AWG multiplexer for all four possible state other cases. Figure 5(m) depicts the BtB eye diagrams for SL #1 and SL #2 whereas figure 5(n) shows the eye diagrams of the multi-level multi-wavelength signal after the AWG multiplexer for all four possible state combinations stored in the two CAM cells. Finally, figure 5(o) shows the respective eye diagrams of the final ML signal at the output of the SOA-XGM gate with an average ER of 6.3 dB. The BER measurements can be observed in figure 5(p) containing the SL bits, the CAM cell outputs and the final ML signals at the output of the SOA-XGM gate. Error-free operation for all four possible CAM cell content combinations is revealed, with a power penalty of 1.2 dB for the CAM cell outputs and an additional 5.9 dB for the ML output signals at a BER of 10\(^{-9}\).

5. Towards multi-cell operation

In view of scaling the ML functionalities in terms of speed and the number of memory cells, in this section, we go a step further and investigate the scaling of the T-CAM cell concept \([55, 57]\) to multiple cells. To this end, we present a simulation analysis of an optical ML, comprising 4 T-CAM cells which perform at 20 Gb s\(^{-1}\) \([36]\), while also deploying wavelength multiplexing of the four signal outputs to benefit from the inherent parallelism of the wavelength dimension introduced by integrated optics for T-CAM operation at 4 \(\times\) 20 Gb s\(^{-1}\). The logical diagram of the optical T-CAM and the setup used in the simulation analysis are respectively illustrated in figures 6(a) and (b), while its operation follows the same principle as described in previous work \([55, 57]\). The simulation analysis was conducted at 20 Gb s\(^{-1}\) using the VPIphotonics Design Suite \([63]\), relying on experimentally-validated numerical models of the SOAs, the FF and the XOR gates were \([55, 56]\).

The synchronized numerical time traces of the signals which demonstrate the proof of principle of the 4-bit optical ML are depicted in figure 7. Specifically, figures 7(a) and (b) depict the set and reset signals respectively of the XFF, which control its write operation; equivalently figures (c) and (d) show the set and reset signals of the TFF. The time traces of the stored memory content of the XFF and the TFF respectively are shown in figures 7(e) and (f), demonstrating the successful write operation to the memory, as the advent of a set pulse for the XFF in figure 7(a) or TFF in figure 7(c) results in a change of the logic memory state to a logical ‘0’ level in the XFF of figure 7(e) and TFF of figure 7(f) respectively, while a reset pulse restores the memory state back to the logical level of ‘1’. On the other hand, part of the time trace of the PRBS of the search bit at 20 Gb s\(^{-1}\) is shown in figure 7(g), which is fed to the XOR gate of the T-CAM for comparison-based search operation. The final output of the T-CAM cell 1 is shown in figure 7(h), while similar time traces have been obtained for all the remaining three T-CAM cells of the proposed architecture. The final ML signal, as defined by the wavelength multiplexing of the four T-CAM cells by the AWG, is shown in figure 7(i), resulting in a multi-level multi-wavelength signal, where each power level encodes the number of matches or misses that have been identified out of the four T-CAM cell content-comparison operations. Specifically, when there is an exact match at all four T-CAM cells, i.e. the XOR comparison operation between the search bit and the stored T-CAM content equals a zero, the final ML output power level will also correspond to a zero level. Depending on the number of T-CAM misses, the power level of the ML signal output will start increasing.

The above operation is illustrated more clearly with three descriptive examples highlighted with a gray marker in the synchronized time traces, at the time-slots #1, #9 and #27. Within time-slot #1, all four content-comparison XOR operations at the four T-CAM cells result in a match in figure 7(h), i.e. the 4-bit search.
word matches the 4-bits of the stored address, and as a result the power level of the ML signal output in figure 7(i) has a zero-power level. In contrast, for time-slot #9, when none of the four XOR comparison outputs in figure 7(h) has a logical ‘0’ level, i.e. all four bits of the search word do not match with the four bits of the stored content and there is a miss, then the signal output in figure 7(i) has a maximum power level of logical ‘1’. Time-slot #27 presents an intermediate case, where two of the T-CAM cells, specifically at the second and the fourth column of traces, feature a ‘don’t care’ state with a value of 1 at the XFF. This implies that the result of the XOR comparison will always feature a zero-power level, i.e. a matching case, regardless of the values of the incoming search bit or the stored TFF content. This happens for instance at the time-slot #27 of the 4th T-CAM cell, where the TFF features a logical ‘1’ and the search bit a logical ‘0’, yet the XOR output features an logical power level of ‘0’, verifying a successful ‘don’t care’ operation. Finally, the signal quality of the outputs of all four T-CAM cells was evaluated through eye diagrams after the numerical operation at 20 Gb s\(^{-1}\) using PRBS signals; the results are shown in figure 7(j). The plots reveal open eye diagrams for all T-CAM cells with an ER value of 13 dB.

6. Discussion and future challenges

The experimental and simulation evaluation so far presented reveals that unique benefits can be gained by exploiting optical technology to realize an all-optical WDM AL table architecture. The high-bandwidth characteristics offered by optical technology can lead to a remarkable speed increase for both write and content addressing operations in the CAMs domain. In addition, wavelength parallelism by means of WDM techniques can offer an extra degree of freedom at the system-design level allowing for sharing hardware that in turn can lead to more energy-efficient architectures where different wavelength-encoded bits are written or compared in parallel to the various cells. Going a step further, expanding wavelength parallelism to multiple MLs could in principle allow for even faster CAM table updates since more than one ML could be updated at a given time-slot.

However, aiming towards identifying future challenges to enabled light-based AL functionalities, a comparison of the developed optical RAM and CAM cells with state-of-the-art electronic counterparts in terms of speed and power consumption, is presented in tables 1 and 2 respectively, indicating their benchmarks when CMOS nodes turn to small dimensions. It is worth noting that electronic RAMs have achieved a maximum speed of up to 5.3 GHz, when built on 65 nm CMOS and optimized for high performance \[43\], showing a trend towards slowing down and giving up their fast access time at speed of 1 GHz or even below, to benefit from lower energy consumption in the order of a few fJ/bit or less \[47\]. A similar trend is also observed for electronic CAMs, where performance is typically limited in the order of 500 MHz \[51\] and reaches the 1 GHz operation only by using pattern dependent predict-and-correct schemes, while also occupying energy consumptions in the order of 1 fJ bit\(^{-1}\) \[50, 52\].

In contrast, in terms of speed for optical RAMs and CAMs, impressive progress has been witnessed over the last decade with optical CAM and RAM cells, as presented in figures 8(a) and (b) respectively. As can be seen in figure 8(a), the recent demonstration of optical CAMs presented in this manuscript outperforms electronic counterparts, achieving a close to 10 \(\times\) speed up. Equivalently for optical RAM cells, the present work is aligned with the evolutionary progress of optical RAMs and is now unlocking the architecture to exceed the speed of electronics, beyond 5 GHz. Despite the number of optical RAM cells demonstrated so far \[25–27, 31\], claiming
to reap the high-bandwidth credentials of optics, our work is the first to exceed and actually double the speed of all previous RAM cells.

However, in terms of energy efficiency, the proposed optical CAM and RAM configurations rely on bulk SOA-based modules of a generic library-based InP platform, which are however known to be rather power- and footprint-hungry components [66]. As a result, the proposed optical CAM and RAM cells consume a few hundred of pJ/bit, due to the high current required to power up the SOAs. Further improvements can certainly be achieved by replacing the SOA-based modules with alternative and more sophisticated technologies, such as photonic crystal nanocavities that can in principle yield higher integration density levels, lower-footprint routing and fJ/bit energy efficiency [40].

However, beyond memory cell optimization, additional efforts are still required towards the implementation of complete fully functional AL tables like the implementation of a WDM interconnect network for broadcasting the search words to all the MLs, and the implementation of a completely optical encoder/decoder circuit for interconnecting the CAM and RAM tables. These next steps could potentially follow similar concepts of the all-passive wavelength-based peripheral circuitry reported in the area of optical RAM and cache architectures [28, 29].

Table 1. State-of-the-art RAM cell comparison and future perspective.

| References | Technology | Energy (fJ/bit) | Freq. (GHz) | Optimization—characteristics |
|------------|------------|----------------|-------------|-----------------------------|
| [43] IBM   | 65 nm      | n.a.           | 5.3         | High speed                  |
| [44] KU Leuven | 40 nm      | 114            | 0.454       | Optimized footprint         |
| [45] MIT   | 28 nm      | 52.5           | 0.09        | Low power                   |
| [46] Intel | 22 nm      | n.a.           | 4.6         | High speed                  |
| [47] Intel | 14 nm      | 4              | 1           | Optimized power, speed      |
| [48] ASU   | 7 nm       | n.a.           | 2           | Advanced                    |
| This work (SOAs) | InP | 200 pJ | 10 | Highest speed |
| Future perspective | III–IV on Si | ~fJ | 10 | Low power (further work) |

Table 2. State-of-the-art CAM cell comparison and future perspective.

| References | Technology | Energy/search/bit (fJ/bit) | Freq. (GHz) | ML technique |
|------------|------------|----------------------------|-------------|--------------|
| [49] KAIST | 250 nm     | 17.2                       | 0.26        | Pulsed NAND-NOR |
| [50] SONY  | 130 nm     | 5.6                        | 0.2         | Charge inject ML detect |
| [51] KNU   | 65 nm      | n.a.                       | 0.5         | Selective ML |
| [50, 52] IBM | 32 nm      | 0.58                       | 1           | NOR predict correct |
| [53] UMICCH/ORACLE | 28 nm FD | 0.74                       | 0.37        | 2 single ended |
| This work (SOAs) | InP | 300 pJ/bit | 10 | High-speed look-up |
| Future perspective | III–IV on Si | ~fJ | 10 | Low power (further work) |

Figure 8. Evolution between (a) electronic and optical CAM-based memories in terms of speed in MHz and (b) electronic and optical RAM memories in terms of speed expressed in GHz over the past two decades.
7. Conclusions

A holistic overview of our recent work on optical memory architectures towards releasing a completely optical AL table has been presented. We have reported on the progress made in optical CAMs. Then we experimentally demonstrated for the first time an optical RAM cell layout for operation at 10 GHz advancing the speed capabilities by two times compared to previous state-of-the-art optical RAM cells. The proposed optical RAM implementation uses a fast AG operating in a push–pull configuration with the SOAs in the deep saturation regime. Next, we have extended our analysis from single-cell to multi-cell optical memories by presenting: (a) experimental results on a 2-bit optical CAM ML architecture for 2-bit AL at 10 Gb s$^{-1}$ and (b) a multi-cell approach with advanced functionalities and speed of an all-optical T-CAM row architecture comprising four T-CAM cells, also employing WDM-enabled ML decoding so as to allow for fast parallel comparison of complete optical words in a single row. The demonstrated T-CAM ML architecture suggests an operation speed increase of up to 20 Gb s$^{-1}$ and is verified through physical layer simulations in the VP photonic Design Suite [65]. Finally, we discussed the progress in the CAM/RAM area over the past two decades highlighting the remarkable advances witnessed by optical technology compared to electronics.

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