RAPID MAPPING OF DIGITAL INTEGRATED CIRCUIT LOGIC GATES VIA MULTI-SPECTRAL BACKSIDE IMAGING

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Abstract. Modern semiconductor integrated circuits are increasingly fabricated at untrusted third party foundries. There now exist myriad security threats of malicious tampering at the hardware level and hence a clear and pressing need for new tools that enable rapid, robust and low-cost validation of circuit layouts. Optical backside imaging offers an attractive platform, but its limited resolution and throughput cannot cope with the nanoscale sizes of modern circuitry and the need to image over a large area. We propose and demonstrate a multi-spectral imaging approach to overcome these obstacles by identifying key circuit elements on the basis of their spectral response. This obviates the need to directly image the nanoscale components that define them, thereby releasing resolution and spatial sampling requirements by 1 and 2 - 4 orders of magnitude respectively. Our results directly address critical security needs in the integrated circuit supply chain and highlight the potential of spectroscopic techniques to address fundamental resolution obstacles caused by the need to image ever shrinking feature sizes in semiconductor integrated circuits.

1. Introduction

Semiconductor integrated circuits (ICs) are pervasive and essential components in virtually all modern devices, from personal computers, to medical equipment, to varied military systems and technologies. Their functionality is defined by a massive number (∼10⁶ − 10⁹ currently) of interconnected logic gates that correspond physically to various nanoscale doped regions, polysilicon and metal (usually copper and tungsten) structures. Modern ICs are thus extraordinarily complex physical structures that are produced by equally complex processes. Validating and testing chips is becoming both increasingly important and challenging [1, 2, 3]. New techniques are essential from both a failure analysis and, in recent years, a security standpoint [4, 5, 6, 7].

Security issues have become significant as a result of the increasingly complex, fragmented and global multi-stage process by which ICs are produced. This trend has opened the door for numerous security threats including piracy, counterfeiting [3] and malicious tampering [4, 5, 6, 7]. Malicious tampering is manifest by the insertion of a few rogue gates into an IC in order to, for example, subvert firewalls, leak sensitive information or compromise device functionality [4, 5, 6, 7]. In analogy with the software threats, these are termed Hardware Trojans [3]. Unlike software vulnerabilities, Hardware Trojans require highly specialized equipment and expertise to detect and cannot simply be patched in the field. Efforts by the U.S. Defense Department to control the full process for fabricating its chips in the Trusted Foundry program [4] and the large body of research...
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on possible modifications to the chip design and fabrication \[10\] \[11\] \[12\] \[13\] \[14\] flow highlight the significance of this problem as well as the lack of appropriate testing solutions.

Current electronic testing methods fall short in testing for Hardware Trojans. Digital tests cannot exhaustively sample the massive state space which scales nonlinearly with IC complexity, and analog measurements are highly sensitive to minor fabrication variations \[13\] \[7\] \[6\]. Both can be readily designed around by an adversary \[9\] \[7\] \[6\]. There is therefore a clear and pressing need for tools that enable direct, rapid and low cost detection of IC tampering.

Any change in the functionality of an IC must map to a change in the physical structures that define its logic. A direct image of the layout therefore offers the most direct and exhaustive route to detect tampering. Measuring the physical structures as opposed to the electrical signals produced by an IC is fundamentally advantageous. Electronic measurements must consider and be designed to be robust over a wide range of complex activation and action characteristics of Hardware Trojans \[6\], in contrast to direct IC layout images that do not. Spatial mapping also has more favorable scaling rules since the measurement space varies only linearly with transistor or gate count. Traditional imaging methods, however, are fundamentally limited in their ability to handle the enormous range in length scales that are present in modern ICs. The physical features that define the transistors and their associated interconnects have dimensions below 100 nm, yet billions of them together cover an area on the order of cm\(^2\). From the standpoint of the optical resolution, these dimensions are at the limits of what can be achieved with solid immersion lenses (SILs) at the near-infrared (IR) wavelengths (1 – 3 \(\mu\)m) that are required to optically access IC circuitry through the silicon (Si) substrate \[15\] \[16\] \[17\] \[3\] \[18\]. The extremely high numerical apertures (NA) required, however, sacrifice field of view and thus present significant challenges to imaging over large areas. A similar bottleneck exists in terms of the number of spatial samples that would be required to image a full IC at a discretization commensurate with the smallest feature sizes, which are \(\sim 10 – 100\) nm. To simply record this many image points (pixels) with a conventional laser scanning confocal microscope would require at least several hours to tens of days.

In this work we propose and theoretically demonstrate the use of a multi-spectral imaging approach that takes advantage of the inherent modularity of IC design to overcome these fundamental obstacles. The basis for our method is that physical structure of a digital IC maps to a well defined series of interconnected logic gates. Each gate type is physically implemented on the chip through a series of distinct metal wire and transistor geometries that define the appropriate electronic behavior. The physical layout of a digital IC thus takes the form of a tiling of a few different types of standard cells that, significantly, have linear dimensions on the order of microns.

Imaging at the resolution commensurate with these micron scale gates, as opposed to the nanoscale wires and transistors that define them allows for dramatic reductions in spatial resolution and sampling requirements. Instead of identifying these gates on the basis of images of their detailed sub-structure, we show here that a small number (\(\sim 5\)) of measurements at different wavelengths and polarizations allow one to distinguish between gates with near 90% accuracy via a simple pattern recognition approach. This enables the possibility of mapping the type and location of every logical gate in an IC in a few minutes using a very modest 0.8 NA imaging system. The method we propose here thus directly addresses critical security issues in the IC pipeline and is highly scalable to future ITRS projections. We demonstrate our method with numerical simulations of a backside optical imaging system such as those used for IC failure analysis and a 45 nm technology node open source library \[19\] as a test case.
2. Backside Imaging of Integrated Circuits

Integrated circuits consist of a layered stack built up over a Si substrate. The bottom most layers define the active region containing the transistors and are comprised of doped regions in the Si and polysilicon. The first metal layer (M1) typically is used to connect combinations of these transistors so as to form the standard CMOS logic gates. Imaging these most basic structures would provide an ideal means with which to directly verify the faithful fabrication of a submitted chip layout at an untrusted foundry. However, achieving the required resolution and throughput is extremely challenging.

In a standard scanning confocal microscope the object is illuminated by a focused spot to produce an induced polarization, or current distribution $j(x, y, z)$, in the object. On the collection side the radiation scattered in the far-field due to this induced current is imaged onto the detector plane according to, [20]

$$ E_D(u, v) = \int \int_V G(u, v; r) j(r) \, d^3r $$
where \( r = [x, y, z] \) is the object space position, \( \mathbf{G} \) is the Green’s tensor \([20]\) for the imaging system, \( \mathbf{E}_D \) is the electric field at the detector plane \((w = 0)\).

A pixel value at position \((a, b)\) is recorded by integrating the intensity at the detector plane over an aperture, \( W \). This is general a pinhole similar in size to the point spread function at the detector plane. The resultant signal, \( S(a, b) \), can be written as,

\[
S(a, b) = \alpha \int_W \left| \mathbf{E}_D(u, v) \right|^2 du dv
\]

where \( \alpha \) is a scaling constant. The sample is raster scanned, usually by means of a scanning galvo and relay system, such that every \((\Delta_x, \Delta_y)\) a new pixel is recorded to build up the image.

Optical resolution limits are dictated by the fundamental physics described in equation 1. As an estimate, consider the paraxial limit where the dominant component of \( \mathbf{G} \) takes the form of an Airy disc whose size is approximately 0.61\( \lambda/NA \), where \( NA \) is the numerical aperture of the collection objective. The blurring of the object that results leads to the well known Abbe diffraction limit. Imaging the IC structures through the Si substrate requires using near-IR \((\lambda = 1 – 3 \mu m)\) light. This therefore severely limits resolution given that conventional air objectives have NAs below 1. For a reasonable, \( NA = 0.8 \) system, Abbe’s approximation indicates a resolution of \( \sim 750 \text{ nm} \) at \( \lambda = 1 \mu m \), significantly larger than the sizes of the relevant IC wires.

Solid immersion lenses (SILs) address these issues by placing a Si hemisphere in contact with the IC substrate backside. Central or aplanatic configurations preserve or increase, respectively, the angles of incident rays as they pass into the Si substrate enabling NAs as high as \( n_{Si} = 3.5 \) theoretically. Recent research aimed to address IC failure analysis needs has pushed the resolution limits of traditional solid immersion lens subsurface microscopy to \( \sim 100 – 150 \) nm \([17, 16, 3, 18]\).

Nevertheless, typical (minimum) line widths and separations in the M1 layer are 65 nm for the 45 nm process we use here to validate our results. These features will therefore be just at or below the impressive resolution limits of SIL systems. At leading edge, 22 nm and below, technology nodes \([1]\) the mismatch will be even worse.

Throughput limitations present an additional significant challenge. In contrast with optical resolution limits, they do not result from a fundamental physical process such as diffraction. They are due to the need to sample at rates commensurate with the smallest, nanoscale, structures to be imaged, yet map over a centimeter scale area. As a simple quantitative estimate, a reasonable sampling rate of \( \Delta = 10 – 100 \text{ nm} \), implies that \( 10^{12} – 10^{10} \) samples would be needed to cover a \( \text{cm}^2 \) area. At the MHz acquisition rates that are characteristic of conventional galvo scanning confocal systems several hours to tens of days would be required to scan a chip size area.

3. Gate-level Mapping of Integrated Circuits

The numerical simulations in Figure 2 highlight the challenges of traditional imaging methods and illustrate our proposed solution. Full details of our computational method are given in the Methods section (Appendix A1 - A3). In brief, we use a finite-difference time-domain (FDTD) solver \([21]\) to simulate the scattering of an incident beam by the nanoscale IC circuit components. The far-fields are obtained directly from these simulations via the near-to-far-field transform and then propagated through our imaging system using the angular spectrum approach and Debye approximation \([22, 23, 13]\).

We neglect refraction caused by light exiting the Si substrate for simplicity and note that this is easily avoided experimentally by commonly employed and commercially available central SIL
Figure 2. Multi-spectral backside imaging for rapid gate-level mapping of an integrated circuit. (a) Layout of a 4 x 4 tiling of integrated circuit gates (black lines and gray squares correspond to M1 lines and contacts respectively). Red dashed lines indicate gate boundaries. (b) Simulated high NA (3.4) image of the layout at a wavelength of $\lambda = 1060$ nm. The circuit is illuminated with light polarized in the $y$-direction. (c) Multi-spectral image cube of the circuit. The images are collected at low resolution (NA = 0.8 and sampled at a low rate in the spatial dimension ($\Delta = 250$ and $1400$ nm in the $x$ and $y$-directions). Each panel corresponds to an image collected at a different wavelength-polarization combination. (d) Gate map generated from the data cube in (c). Pixels are colored to indicate one of 6 possible gates. The scale bars in (a) and (b) are 1 and 2 $\mu$m respectively.

microscopes. While all calculations are therefore strictly representative of this geometry we expect that the general concepts we develop here can be utilized with a variety of different optical configurations including without a SIL.

Figure 2a shows the M1 and contacts (black and grey regions respectively) associated with a series of logic gates taken from the 45 nm Nangate library [19]. Their image produced using a 3.4 NA system [25] at a wavelength of $\lambda = 1060$ nm and 10 nm sampling rate is shown in Figure 2b. Even at such high resolution and sampling rate the detailed geometry of the metal wires cannot be
resolved. With neither adequate resolution, nor sufficient throughput, traditional imaging methods cannot offer a viable solution to IC assurance and security.

While the individual metal wires shown in Figure 2a are several 10s of nanometers in scale, the digital logic gates that they ultimately define are over an order of magnitude larger. The boundaries of these gates are outlined in red in the figure. For the particular 45 nm process we examine here their linear dimensions are on the order of 1 um. Treating the micron scale gates as opposed to the wires and transistors that define them as the smallest spatial unit to image therefore offers a route to dramatically relaxing resolution and sampling rate requirements. Optical resolution on the order of $1 \mu m$ can easily be achieved even without a SIL. Sampling at this rate such that approximately one gate maps to one pixel reduces the required pixel count by 2 - 4 orders of magnitude compared to the previous estimates. This implies the potential to image a full chip ($cm^2$ area) in 2-3 minutes considering again MHz acquisition rates.

At such low resolution and pixel count the image itself cannot be used to distinguish between the different gates. We therefore sought to instead identify the gates on the basis of their response to light incident at different wavelengths and polarizations (referred to as spectral response hereafter for brevity). Spectral scattering and absorption has been used to identify and distinguish between particulates [26, 27], tissue class in histopathology applications [28, 29] as well as characterize the sub-wavelength resonant modes present in designer metamaterials [30]. We apply similar principles here. We intentionally illuminate and image our sample with a low NA objective to match the spot size with the gate dimension (0.8NA is used here and in all the following). As a result, the individual wires that comprise each gates are excited uniformly and their collective response measured. This allows us to roughly think of each gate as an effective material that can be identified on the basis of their overall spectral response. As shown in the results in Figures 2c,d, a series of low-resolution, coarsely sampled images taken at a few (5) different spectral features can be used instead of the high resolution, finely sampled one. Applying established pattern recognition techniques [31, 28] allows us to associate each spatial pixel in the image stack with a different logic gate to form the final map in Figure 2d. In comparison with the purely spatial sampling approach, these 5 spectral measurements are dramatically more efficient than the $\sim 10^2 - 10^4$ per gate (i.e. $1 \mu m^2$ area) that would be needed to with $\Delta = 10 - 100 \text{nm}$.

Our approach represents a new and unique application of spectroscopic imaging. In addition to the first application of spectral imaging to IC backside imaging, the overarching goal and motivation is distinct from traditional applications such as those in biotechnology and remote sensing. Rather than seeking to obtain new mechanisms for contrast based on sample specific spectral bands, our aim is to overcome the need for impossibly high resolution and spatial sampling rates by more efficiently probing structure in the spectral domain.

3.1. Spectral Fingerprints of Logic Gate Geometries. In the backside imaging geometry we consider, one measures the light reflected by the metal wires and contacts that define the IC gates as well as the interface between the Si substrate and insulating oxide (SiO2) in which the IC structures are embedded. The FDTD simulations in Figure 3 illustrate the link between this particular response - the spectral reflectance - and the substructure of the different IC gates.

The results show the net reflectance of a periodic tiling each gate (see Appendix A2) under linearly polarized plane-wave illumination. Each of the six gates in our test set is defined by a distinct series of M1 wires. When illuminated, these wavelength scale wires support current oscillations that are highly dependent on the wire geometry and the illumination wavelength and polarization. From equation [1] the detected signals will therefore be highly distinct for different gates and vary strongly as a function of wavelength and polarization of the incident field. This is
Figure 3. Spectroscopy of integrated circuit ‘metamaterials’. The top row indicates the legend and shows schematics of the metal 1 (black lines) and contact (gray squares) layers of the six gates. The plots show simulated spectral response for the 6 gates under x- and -y polarized illumination. Images of the induced current along the wires in the XOR and AND gates at various wavelength (λ) and polarizations (q) are shown on the right. The (λ, q) values are (1500 nm, x), (1100 nm, y) and (2600 nm, y) from top to bottom.

Evident in the reflectance spectra, and series of near-field current distributions shown for the XOR and AND gates. An important feature that is obvious from the combination of near and far-field data shown in the figure is that although the induced current distributions and far-field spectral responses are unique fingerprints of the different gates, there is no simple one-to-one mapping between specific modes and far-field features. Instead the current modes couple to each other in a complex fashion in the near-field and produce a far-field response that is the result of the coherent interference between their scattered radiation as well as the signal reflected from the Si-SiO₂ interface. This motivates the statistical classification approach we will apply to distinguish between the different gates.

A second observation is that the majority of the current distributions excited appear to correspond to higher order modes. This is important as it implies that we can expect geometry dependent spectral features to exist over an extremely broad wavelength range and to persist in the near-IR for essentially any IC gate design even as dimensions are reduced at advanced technology nodes. We can intuitively validate this by considering a simple estimate approximating the wires as Fabry-Perot resonators for current modes in accordance with common models for dipole antennas. The lowest order (longest wavelength) mode is at \( \lambda \approx 2n_{eff}L \) (\( n_{eff} \) is the effective index and \( L \) the wire length).
length) \[32\]. The length scales of the M1 wires in the gates in Figure \[3\] range from \(\sim 100 - 1500\) nm. This indicates that a spectral response that is a strong function of the gate geometry can be observed at wavelengths between 0.4 – 9 \(\mu\)m assuming \(n_{eff} \approx 3\) as a result of proximity to the Si substrate. This extremely broad range that extends far into the infrared indicates ample room for reduction in wire length before near-IR resonant structures are no longer naturally present.

3.2. Gate Response and Variability in a Scanning Microscope. These results indicate the significant potential for the spectral reflectance of each gate to act as fingerprint that can be used to identify them. In practice our imaging system records a subset of the signals presented in Figure \[3\]. Both the limited collection cone of the objective (\(\pm 13\) deg for 0.8NA in a Si background) and the pinhole at the detector plane will reject a portion of light scattered by the IC structures. The imaging geometry also implies the need to consider the relation of each image pixel to a spatial position of the sample as it is raster scanned and the tiled logic gates that we aimed to identify.

In general, following equation \[2\] the signal at a given pixel will have the form (see Appendix A1 for derivation),

\[
S(a_i, b_j; \lambda, q)/S_0(\lambda, q) = R(x_i, y_j; \lambda, q) + \eta_{det}(\lambda, q)
\]

where \(\lambda\) and \(q\) index the wavelength and polarization state of the incident beam such that \((\lambda, q)\) defines the specific spectral feature that is measured. In equation \[3\] we have assumed that the signal has been normalized by a background, \(S_0\), that removes wavelength and polarization dependent variations that are inherent to any realistic experimental system. These include detector responsivility, source power spectral dependence and absorption in the Si substrate. This isolates the portion of the reflectance that depends solely on the spatially varying IC structure that is of interest. This reflectance, denoted \(R(x, y; \lambda, q)\), is assumed to account for the full effects of the imaging system as indicated above. It varies with the sample geometry at position \((x_i, y_i)\) and directly measured via the normalized pixel response of equation \[2\].

To link this practical measurement to the spectral reflectance of our gate objects we associate pixels \((a_c, b_c)\) that map to sample positions \((x_c, y_c)\) that coincide with the center coordinates of a specific gate \(c\) with that gate. We can therefore write,

\[
S(a_c, b_c; \lambda, q)/S_0(\lambda, q) = R(c; \lambda, q) + \eta_{det}(\lambda, q)
\]

where we have written \(R(c; \lambda, q) = R(x_c, y_c; \lambda, q)\) for short.

Equation \[4\] thus describes the measurement of the spectral reflectance of a given gate class, \(R(c; \lambda, q)\). The measurement depends not only the specific gate type centered under the microscope and the feature measured through \(R(c; \lambda, q)\), but also will inevitably include fluctuations caused by two noise sources, \(\eta_b\) and \(\eta_{det}\). System noise, \(\eta_{det}\), is independent of the actual sample position or underlying IC structure and is manifest as detector noise. The other noise term, \(\eta_b\), originates from the fact that our measurements of a given gate will likely also contain some signal from scattering off of neighboring gates.

Because of the presence of noise, \(\eta = \eta_{det} + \eta_b\), the relationship between a measurement, \(S(a_c, b_c; \lambda, q)/S_0(\lambda, q)\), and the spectral reflectance of the underlying gate class, \(R(c; \lambda, q)\), will not be deterministic. A key consideration is therefore to determine an ideal small set of features \((\lambda_i, q_i)\) to measure that will offer maximal accuracy in distinguishing between the different gate classes. This depends directly on the elements of the optical system that govern \(R\), \(\eta\) and the range of spectral features that can be accessed.
In order to address these issues formally we utilize Bayes’ theorem, which is the basis for an intuitive and established classification method. We consider a spectral reflectance measurement $M_i = S(c_0; \lambda_i, q_i)/S_0$ that we aim to use to identify the underlying class, $c_0$, via the dependence on $\mathcal{R}(c_0; \lambda_i, q_i)$. The probability that our measurement $M_i$ implies an underlying class, $c_j$, is given via Bayes’ theorem, $P(c_j|M_i) = P(M_i|c_j)P(c_j)/P(M_i)$. The distribution of measurement values, $M_i$, for each gate dictates the probability $P(M_i|c_j)$ and $P(c_j)$ scales for the prior probability of each class. The denominator, $P(M_i)$, amounts to a normalization constant. For multiple measurements, $\mathbf{M} = [M_1, M_2, \ldots, M_N]$, where the approximation made in the second line assumes statistical independence of the measurement features. This assumption is not strictly accurate, but it significantly simplifies the process of determining probability distributions and calculating the probabilities and is commonly applied. If the probability distributions that determine the right hand side of equation 5 can be characterized, each pixel can be classified as the specific gate type, $c$, that corresponds to the maximum $P(c|M)$. This amounts to dividing the $N$ dimensional measurement space into regions $R_j$ such that $\mathbf{M} \in R_j \rightarrow c = c_j$. Mis-classification errors therefore intuitively result from overlapping probability distributions.

Our ability to accurately distinguish between and identify the various gates in our set therefore depend heavily on our imaging system. Its characteristics determine the form of $\mathcal{R}$ and $\eta$ and therefore probability distributions for $P(M_i|c)$. These depend on fundamental physical constraints dictated by, for example, optical resolution as well as practical considerations that govern the availability and noise characteristics of sources and detectors.

4. Influence and Sources of Noise

For the relevant near-IR spectral region on which we focus, neither detector nor source availability should place significant constraints on the spectral features that could be used as classification measurements. Standard InGaAs detectors operate between $1 - 2.6 \mu m$ and have response times appropriate for fast imaging. Numerous sources exist that are suitable for supplying a moderate number of different input wavelengths. The primary factors governing the performance of our approach therefore are sources of error.

To assess the influence of system noise and the fundamental limits on our method, we considered (i) detector noise and; (ii) cross-talk between adjacent gates. Detector noise will always be present and sets a lower bound on measurement variation for a given measurement speed. Cross-talk between adjacent gates is directly related to both the size of the point-spread function described in equation 1 and the integration area in equation 2. It is fundamental to our approach since it is a function of the resolution and throughput trade-offs that we aim to address. In principle one can engineer around other sources of error such as experimental error due to sample alignment.

We approximated detector noise as resulting in Gaussian uncertainty distribution for a given measurement. The standard deviation (in reflectance scale), $\sigma$, can be determined from the usual definitions for detector signal-to-noise ratio $(S/N)$ via $\sigma = (S/N)^{-1} = P_{NEP}\sqrt{\Delta f}/P_S$, where $P_S$ is the power incident on the detector, $P_{NEP}$ is the noise equivalent power with respect to a $1 \text{ Hz}$ bandwidth and $\Delta f$ is the measurement bandwidth. Common InGaAs detectors have $P_{NEP} \sim 10^{-12} \text{ W}/\sqrt{\text{Hz}}$ such that on the order of $P_S \sim 0.1 - 1 \mu \text{W}$ signal power are sufficient for
Figure 4. Sources of variation in integrated circuit gates’ spectral fingerprints (a,b) Illustration of cross-talk sources in low-resolution gate spectral images. (a) Schematic of the excitation of currents in the metal lines by a ~gate-size spot. The incident beam induces currents along the wires inside the target gate (red arrows) as well as in its neighbors (blue). (b) Illustration of the signal generated via these induced currents at the detector plane. The spatially selective element, e.g. pinhole or pixel, defines a subset of these to integrate over (red dashed circle). (c,d) Variation in the spectral fingerprints of XOR and AND gates due to adjacent gates for a 0.8 NA imaging system, under $y$ polarized illumination. (e) Probability distributions for the XOR and AND gate responses at $\lambda = 1227$ nm and $y$ polarization. (f,g) Probability distributions for the two gates at all wavelengths, displayed as image plots with darker regions indicating higher probabilities. The dashed blue and red vertical lines indicate the slice corresponding to panel (e).

$\sigma < 0.01$ at MHz acquisition rates ($\Delta f = 10^6$ Hz), with the exact value depending on the wavelength, responsivity curve of the detector and thickness of the Si substrate (Appendix B.1 presents detailed calculations). The separation between the spectral reflectance curves in Figure 3b,c, is generally better than 0.05 such that noise on the order of 0.01 or below enables high classification accuracy. As a quantitative estimate we calculated the total error rate analytically via an overlap integral assuming Gaussian $p(M|c)$ centered at the reflectance values from Figure 3b and equal prior probabilities for each class. Classification accuracies above 99% are feasible for detector noise below $\sigma \leq 0.02 - 0.03$ (Figure 11 in Appendix B.2). We calculate that these $S/N$ levels can be readily achieved in a realistic confocal imaging system such as the one in [34] based on the range of powers that can be achieved with standard commercial lasers, diodes or power spectral densities offered by near-IR supercontinuum sources [35].

Cross talk between the signals coming from different gates presents a much more significant source of noise. As shown in Figures 4a,b this results from both the illumination spot driving polarizations along the wires both within and outside the gate of interest (Figure 4a) as well as,
at the detector plane, signal from the point spread functions of these current sources falling within the detection area (see, e.g. equations [1] and [2]).

To examine these effects in detail we generated a series of tiles like the one shown in Figure 2a and simulated their spectral images assuming the 0.8 NA objective. We simulated 20 images, each containing either 16 or 20 gates that were randomly selected from the Nangate library set. This yielded on average ~ 60 observations, \( S(c; \lambda, q)/S_0(\lambda, q) \), of each gate type with different surrounding gates. The fluctuations in these observations therefore is due to the error term \( \eta_\delta(c; \lambda, q) \) described in equation 4. The data for the XOR and AND gates under \( y \)-polarized illumination are shown in Figure 3c,d as examples. The series of curves follow similar paths to the net reflectance calculations presented in Figure 3 but with reduced reflectance amplitude as a consequence of the lower collection efficiency of the 0.8 NA that the image simulation accounts for. The signals from the other gates and at \( x \)-polarization yield similar results. We added a series of random Gaussian noise with \( \sigma = 0.01 \) to each of the simulated signal curves to account for detector noise, \( \eta_{det} \) and used the resulting data to build histograms describing each \( p(M_i|c_j) \). Examples for the XOR and AND gate under \( y \)-polarized illumination are shown in Figure 4c-g. The full set of data are presented in the Figure 8 in appendix A. The spreads tended to be fairly Gaussian with standard deviation of between 2 and 8 % depending on the wavelength and polarization.

**Figure 5.** Bayesian classification for identifying gate spectral fingerprints. (a) Overlaid probability maps for the XOR and AND gate probability maps at the spectral features selected. Taken with \( y \)-polarized light and an NA of 0.8. Darker shaded regions indicate higher probability of the gate. (d) Classification accuracy rates as a function of number of features, for different options for the illumination polarization (\( u \) - un-polarized, only \( x \), \( y \)-polarized or \( x/y \) - both \( x \) and \( y \) available).

5. Identifying Logic Gates

5.1. Classification Accuracies. In order to characterize the overall accuracy of our approach while accounting for these two sources of noise, we used the large number of observations we obtained to train our classifier and determine the error rates empirically. We selected (at random) 2/3 of all observations to use as a training set and reserved the other 1/3 to test the accuracy. We used the training data to re-generate the histograms describing \( p(M_i|c_j) \) as before (those in Figure 4 are based on the full set). For a given set of measurements, \( M \), these distributions can be used to calculate the corresponding \( P(M_i|c_j) \) and ultimately the probability of a given gate \( P(c|M) \) via
equation 5 using the statistical independence simplification. We used the test data to calculate the error rate for a given $M$ by classifying each test observation and checking for accuracy such that the error rate could be determined empirically simply as the fraction of incorrect predictions.

While the feature space - wavelengths between 1 and 3 $\mu$m and various polarization states - defines a large number of possible measurements, we aimed to select a small optimal subset that could readily be measured in a standard confocal microscope. We first reduced the feature space by restricting the possible polarization states that could be selected according to 4 simple regularly encountered configurations. These corresponded to unpolarized light ($q = u$), $q = x$, $q = y$ polarizations and the case where either $x$ or $y$ polarization could be selected, i.e. $q \in x,y$. The $q = u$ observations were computed as the average between the $q = x$ and $q = y$ signals. This corresponds to the incoherent sum of the two signals as is representative of unpolarized (or natural) light [36]. For each of these configurations we determined a set of 5 spectral features, $(\lambda_i, q_i)$, to use for measurements by applying a greedy algorithm that incrementally added to $M$ by choosing the feature that resulted in the minimum error at each step.

A resultant set of spectral features and their probability distributions for the XOR and AND gate are shown in Figure 5a. Two measurements, for an XOR and AND gate, are shown as the black lines and markers. Each measurement $M$ traces out a path such that the probability of it belonging to a given gate class is determined from the underlying distribution. Although the figure only shows the process for the two gates, all calculations considered the full set of 6.

We repeated the process of selecting features and calculating the overall error 10 times to cross validate our results. The resulting mean classification accuracies as a function of number of features measured are shown in Figure 5b. Error bars are included and correspond to $\pm$ one standard deviation, though are generally smaller than the markers. The small deviation in conjunction with the fact that the set of features selected varied negligibly (see Figure 7) over each of the 10 runs indicates that an adequate sized data set was used to accurately represent the distributions (see Appendix A.4). The results indicate that classification accuracies above 85% are possible with only $N = 5$ features for the variable polarization case and nearly 80% can be achieved even without polarization control. This is a significant improvement over the 16% random baseline.

5.2. Spatial sampling. The results in Figure 5 correspond to the ideal case for classification where each pixel is perfectly centered at each gate’s location. In principle this can be achieved if the gate dimensions in the $x$-direction share a common factor. This turns out to be the case for the Nangate library we used here, but this may not always be true depending on the IC library used and effects of sampling and mis-alignment are therefore important to address. In order to gain greater insight into these issues we generated a series of maps from a test image, using the previously described training data and feature set. The results for a high-sampling rate ($\Delta = 100$ nm) along $x$ are shown in Figure 6.

Figure 6b shows the spatial variation of $P(c|M)$ for each gate (darker color corresponding to higher probability). In comparison with the true gate map shown in Figure 6c: the agreement is excellent. Displaying the probabilities themselves provides greater insight into the sources of error and effects of mis-alignment. In particular, the confusion between the similar pairs of gates, such as (XOR, XNOR), anticipated based on Figure 3 is immediately confirmed, especially for both the (AND, OR) and (NAND, NOR) pairs. The correct probabilities in general tend to peak near the center of each gate and also maintain relatively high values (in comparison the the incorrect gates) over the majority of the pixels falling within the gate (Figures 6e-h). This indicates that the classification should be robust to misalignments and also enable accurate determination of the gates’ centers. The final map, with each pixel classified according to the maximally probable gate,
is shown in d. The image closely matches the true layout, with errors occurring primarily at the boundaries between two different gates as expected.

We generated a series of probability maps and gate maps for different sampling rates in the $x$ direction, ranging from 100, 250 and 500. The full results are shown together in Figure 9 in the appendix, and the gate map sampled every 250 nm is also reproduced in Figure 2. In all cases similar excellent agreement with the ground truth gate distribution was obtained. Quantitatively, in each case approximately 70% of the pixels were assigned to the correct gate and between 80 and 85% were assigned to one of the correct group (i.e. XOR or XNOR; AND or OR; NAND or NOR). Our results indicate that with minimal alignment (i.e. only in the vertical dimension) and no a-priori information about the underlying gate layout an accurate map can be obtained. The robustness of the classification to pixel alignment points to the ability to down-sample significantly without sacrificing accuracy, as long as each gate can be sampled.

6. Conclusions

Our results demonstrate that backside spectral imaging of ICs in conjunction with established pattern recognition techniques provides a powerful route towards probing their functionality. The method we propose addresses key obstacles associated with optical resolution and sampling that arise due to the nanoscale features size and massive complexity of modern ICs. These challenges fundamentally limit the ability of traditional imaging techniques to rapidly map a large fraction of a chip. The reduction in resolution requirements we achieve is particularly significant since it overcomes a fundamental physical limitation. ITRS estimates of the trends in gate sizes [1] imply that our approach can easily scale well beyond the nominal "10 nm" nodes, where any direct imaging method is completely inconceivable.
Our method has immediate applicability to the significant problem of ensuring the security of ICs. To our knowledge, no other technique offers as direct and informative a measure of the physical layout of a fabricated IC in a rapid and non-destructive fashion. The information we obtain can be used to directly verify the IC layout and spatially localize suspicious regions. We note that the accuracy in detecting actual Trojan circuits will be different, though we expect higher, than the single gate prediction accuracies we have demonstrated here. This is because mis-classifications of the type that constitute actual errors will appear as random noise dispersed throughout the layout while additional, modified circuitry will often be localized \[37\] and have structure defined by electronic functionality, routing and floor planning requirements \[5, 12\]. Combining the data we generate with other testing methods, such as those that serve to constrain easily modified dead space in the IC layout\[38\] should enable very efficient, accurate and informative testing.

Additionally, many possibilities exist for improving the single pixel accuracy from the standpoint of both computational pattern recognition as well as optical design. Alternative more advanced pattern recognition methods \[29\] in conjunction with leveraging additional a-priori information can provide significant improvements. For example, the physical dimensions of the gates are known and can be taken into account when generating the maps such as those shown in Figure 6 to avoid the isolated mis-classified pixels that are intuitively infeasible. From the standpoint of optical design, optimizing aspects such as NA and pinhole size may also offer improvements. Determining ideal parameters for a given gate size is an interesting question, since it involves a variety of trade-offs such as maximizing the diversity of the gates’ spectral response, robustness to mis-alignment and minimizing cross-talk. A particularly interesting configuration would be to illuminate at above the critical angle from the Si side, such that an evanescent wave can be used to excite the M1 layer similar to the TIRF measurements that are widely used in biological applications. This offers a means to significantly reduce signal from the metal interconnect layers above M1 that may produce additional background noise that we were not able to consider here.

We note that the concepts we have introduced here are extensible to other IC applications beyond gate substitutions in security. In general, the sensitivity of the spectral scattering response to nanoscale structure points to the opportunity to obtain more detailed information. For example, it is well known that forming conductive bridges in nanoscale metallic structures dramatically alters their antenna-like characteristics. This provides a clear route to easily detecting bridging defects which are becoming increasingly significant as a result of increased wire density \[2, 39\]. This is relevant to failure analysis where related concepts of leveraging prior information to improve spatial resolution are beginning to be explored \[40, 41\].

In general, ICs represent a compelling and ideal application of the spectral fingerprinting methods we employ here. They are inherently modular since their design paradigm is based on abstraction, hence their components fit neatly into a few well defined classes. Their physical structures are also highly uniform - an enormous amount of effort is applied to ensure this on the fabrication end in order to provide adequate yield. This implies that in physical measurements sample variations will be minimized. Both of these are dramatic departures and improvements over the situations where spectroscopic imaging techniques are often applied such as in biological systems. Access to sufficient and representative samples to use as training data is a final critical need in classification techniques that ICs offer perhaps better than any other physical system. A single IC contains typically over a million gates that are repeated and reused throughout multiple chips on multiple fabrication runs. Measurements on a small fraction of a single chip can supply training data that can be used in a classification method that will be applied to millions of chips. Spectroscopic imaging techniques therefore have the potential to satisfy critical metrology needs, in security and
also general applications, that are increasingly significant as the feature sizes and complexity in modern ICs passes beyond what can be addressed with traditional tools.

## Appendix

### Appendix A. Methods

#### A.1. Spectral Imaging in a Scanning Confocal Microscope.

The calculations and considerations we presented are representative of a scanning confocal microscope. While the general functionality and correspondence is described in the main text, we derive here all equations used and define their correspondence to a practical microscopy setup. As the central SIL configuration exactly corresponds to our computational results and is the simplest, we assume this throughout. For simplicity, we consider only the wavelength dependence of components and the sample. The extension to include polarization, $q$, is straightforward and essentially amounts to the substitution $\lambda \rightarrow \lambda, q$ for any elements that are polarization dependent.

A scanning confocal microscope illuminates the sample with a focused spot and records the reflected power that passes through a detector plane aperture. In a practical microscope, the power delivered to the focal region with the illuminating beam can be written as,

$$P_{foc}(\lambda) = [1 - A_{Si}(\lambda)] T_{Si}(\lambda) \mu_f(\lambda) P_0(\lambda)$$  \(\text{(A1)}\)

where $P_0(\lambda)$ is the source power. This equation accounts for loss in the various free space optical components, transmission through the Si-Air interface at the surface of the SIL and absorption in the Si substrate via the parameters $\mu_f$, $T_{Si}$ and $A_{Si}$ respectively. While the beam focused through the SIL is comprised of plane waves propagating at a range of angles (i.e. its angular spectrum), all are normally incident at the Si-Air interface in the central-SIL configuration (see Figure 1) thus $T_{Si}$ is solely a function of wavelength. This is also true, to good approximation, for absorption in the substrate ($A_{Si}$) since for all but the highest NA systems the difference between the path lengths of the rays associated with the minimum and maximum angles is negligible. For the 0.8NA system we focus on here the maximum angle in the Si is about 13 degrees, which leads to an about 3% increase in path length versus the 0 angle ray. Hence $A_{Si}(\lambda) = \exp(-\beta(\lambda)d)$, where $\beta(\lambda)$ is the absorption coefficient of Si and $d$ is the substrate thickness. Upon interacting with the sample a fraction of the incident power will be reflected. The total power reflected encompasses all propagating rays scattered into the substrate side,

$$P_R(x, y; \lambda) = R_S(x, y; \lambda) P_{foc}(\lambda)$$  \(\text{(A2)}\)

The quantity $R_S(x, y; \lambda)$ is the net reflectance of the sample - the fraction of the total incident power that is reflected. Generally some fraction, $f_C$, of the total reflected power is collected due to the finite cone of angles that can be captured by the collection objective.

Accounting for this fraction, and propagation back out through the Si, SIL and detection optics, the total power incident on the detector plane is,

$$P_D(x, y; \lambda) = \mu_c(\lambda) T_{Si}(\lambda) [1 - A_{Si}(\lambda)]^2 R_{S,C}(x, y; \lambda) P_{foc}(\lambda)$$  \(\text{(A3)}\)

$$= \mu_c(\lambda) [T_{Si}(\lambda)]^2 [1 - A_{Si}(\lambda)]^2 R_{S,C}(x, y; \lambda) \mu_f(\lambda) P_0(\lambda)$$  \(\text{(A4)}\)

where $R_{S,C} = f_C R_S(x, y; \lambda)$ is the fraction of the input power reflected into the collection cone of the system and $\mu_c$ describes loss due to practical collection optics.
The signal captured by the detector, described in equation 2, can therefore be written as,

\[ S(a, b) = \alpha(\lambda) f_W(x, y; \lambda) P_D(x, y; \lambda) \]

where the quantity \( f_W(x, y; \lambda) \) gives the fraction of the total power incident on the detector that is contained within the area defined by the aperture (i.e. confocal pinhole). The value depends not only on the geometry of the pinhole and the point-spread function of the imaging system, but also on the particular sample geometry. For example, even in the case of a beam reflected from a planar interface, a metallic surface will produce a tight spot at the detector plane while a high-to-low refractive index interface will produce a significantly larger spot that carries much of its power in a series of side-lobes. We associated the position independent factors with a system response, \( R_D = \alpha \mu_c T_S^2 (1 - A_{Si})^2 \mu_f \).

In a scanning confocal microscope the image is formed pixel-by-pixel by translating the sample, either physically or effectively, through the use of galvo-mirrors and a relay, and recording the signal

\[ S(a_i, b_j; \lambda) = R_D(\lambda) f_W(x_i, y_j) R_{S,C}(x_i, y_i; \lambda) P_0(\lambda) \]

assuming regular sampling intervals in the \( x \) and \( y \) directions, \( (x_i, y_j) = (x_0 + i \Delta x, y_0 + j \Delta y) \).

Non-sample dependent contributions to the signal can be removed by normalizing by a suitable background, ideally a mirror at the sample plane. In this case, the background signal is just \( S_0 = R_D f_{W,m} P_0(\lambda) \) since \( R_{S,C}(\lambda) = 1 \) for an ideal mirror. Thus,

\[ S(a_i, b_j; \lambda)/S_0 = f_W(x_i, y_j) R_{S,C}(x_i, y_i; \lambda)/f_{W,m}(\lambda) \]

(A7)

\[ = R(x_i, y_j; \lambda) \]

(A8)

where the generalized reflectance \( R(x_i, y_j; \lambda) \) is still a ratio of power out versus input, but includes also effects due to the detector plane aperture. This is commonly the response that is recorded in microspectroscopy experiments [23]. If we account for detector noise then \( S(a_i, b_j; \lambda)/S_0 = R(x_i, y_j; \lambda) + \eta_{det} \).

The reflectance of a given gate class \( c \), \( R(c; \lambda) \), is given by \( R(x_i, y_j; \lambda) \) when \( (x_i, y_j) \) correspond to the center coordinates of the gate. Therefore,

\[ S(a_i, b_j; \lambda)/S_0 = R(c; \lambda, q) + \eta_{det} + \eta_i \]

(A9)

where \( \eta_i \) is the noise due to the interference of the gates surrounding the central gate. Equation A9 gives equation 4 in the main text.

A.2. FDTD Simulations. We used a commercial FDTD solver to simulate the response of the IC M1 lines and contact layers for all calculations in the main text. All simulation geometries consisted of a semi-infinite Si substrate occupying the lower half-space and a SiO\(_2\) background in the upper-half. Both were treated as non-dispersive, loss-less materials with refractive indices of \( n_{Si} = 3.5 \) and \( n_{SiO2} = 1.45 \). The M1 layer and contacts were copper and tungsten, respectively, both treated as dispersive material with realistic relative permittivities taken from fits to the data in [42]. We neglected the active regions and polysilicon transistor gates for simplicity and due to the fact that they are expected to contribute significantly less to the gate signals in comparison with the metal structures. The M1 layer and contacts were copper and tungsten, respectively, and embedded in a homogeneous SiO\(_2\) \((n = 1.45)\) dielectric background, with the M1 situated a height
of 100 nm above the Si substrate. The height of the M1 layer was 130 nm. All lateral dimensions were taken from the Nangate library standard cells \[19\].

The calculations in Figure 3 of the main text assume illumination with a uniform, linearly polarized, normally incident plane wave. The boundary conditions are periodic in the lateral plane and absorbing (PMLs) in the \(z\) direction. Each gate simulated defined the unit cell such that the results correspond to an infinite tiling in the lateral plane. The power transmitted through a plane in the Si lower half-space, behind the source, was calculated and normalized to the source power to determine the net reflectance.

A.3. FDTD Simulated Microscopy Images. We simulated the images of the IC gate components by calculating the far-field angular spectrum, \(\tilde{E}_\infty(s_x, s_y)\), from the FDTD simulations. The near-fields recorded on a plane behind the source in the Si substrate were used to compute the far-fields via the near-to-far-field transform \[21\]. The Si - SiO\(_2\) interface is automatically accounted for since it lies within the simulation domain.

The angular spectrum represents the far-field as a series of plane-waves defined by the direction cosines \(s_x = \sin \theta \cos \phi\) and \(s_y = \sin \theta \sin \phi\), where \(\theta\) and \(\phi\) are the usual spherical coordinates (see Figure 1). The far-fields computed from the simulations are those inside the Si substrate, and must be propagated through it, and the imaging system consisting of the collection objective and tube-lens. Neglecting refraction at the Si-Air interface (as with, e.g. a central-SIL), the relative weighting of the plane wave components stays constant despite overall reductions in amplitude due to absorption in the Si substrate and reflection at the interface. We account for the reduction in overall power incident at the detector and its implications for S/N in the relevant calculations (see Appendix A1 and Appendix B1). Therefore, the image at the detector plane can be formed via,

\[
E_D(u, v, w) = \frac{jn_1 \sqrt{n_1}}{\lambda M} \int_{0}^{\text{NA}} \tilde{E}_\infty(s_x, s_y)e^{j k_0 n_1 (s_x u/M + s_y v/M)} d\Omega \tag{A10}
\]

where the integral is over the collection cone of the objective NA \[22, 23, 43\].

Equation (A10) can be used directly to compute the image formed by a confocal imaging system where the object is illuminated by a finite sized beam (in principle with the same NA as the collection objective) and the object is simulated as isolated via standard PML boundary conditions.

Because the full confocal simulation approach requires a focused beam excitation source a fairly large computational domain is required and each wavelength point requires a separate simulation. The latter requirement is due to the fact that the source is modeled as a sum of plane-waves that are defined by a fixed \(k\) vector such that the angle of incidence changes with wavelength \[44\]. In order to reduce the computational burden when simulating the large number of IC gate images over a broad spectral bandwidth that was required to train and test our classifier we performed a simplified calculation based on two approximations: (i) simulating the object as periodic \[43\] and; (ii) exciting the simulation with a normally incident uniform plane-wave. In terms of the far-field, the resultant angular spectrum is a discrete series corresponding to the diffraction orders,

\[
E_D(u, v, w_0) = \frac{1}{M} \sum_{k,l \in \text{NA}} s_{k,l} e^{jkG_x u/M + jG_y v/M} \tag{A11}
\]

where \(G_x = 2\pi/(p_x)\), \(G_y = 2\pi/(p_y)\) are the grating wavevector magnitudes with \(p_x\) and \(p_y\) corresponding to the \(x\) and \(y\) dimensions of the unit cell. The weightings \(s_{k,l}\) are normalized such that \(|s_{k,l}|^2\) give the relative fraction of the incident power in each grating order \[21\] and \(|E_D|^2\)
from equation A11 gives the power for unit area. Because the source has infinite extent over the full simulation domain, to calculate the reflectance of each pixel in the multi-gate simulations we normalized the integrated intensity over the integration window \( W \) to the power delivered to the same area in the object space.

This approach dramatically reduces the required number of simulations. It enabled us to simulate a large unit cell, which corresponded to a 4x4 or 5x4 tiling of gates, at once and record all wavelengths with a single simulation. Hence we were able to generate the over 350 total gate observations each of which contained 50 wavelength points with 20 FDTD simulations. In contrast, without the approximation one simulation is required per gate observation per wavelength point such that 17,500 simulations would have been required.

The cost of the approximations used are that they neglect any illumination side effects or spatial selectivity and therefore over-emphasize cross-talk between adjacent objects that are approximately a point-spread-function distance apart. This is because all objects are excited coherently and uniformly. In the case of illumination by a focused beam, only objects within the illuminating spot are excited. For objects that are much closer together than the size of the focused spot, the approximation is not significant since they will be excited coherently with the same amplitude in both cases. Objects that are much further apart than the point-spread-function of the collection objective, will be incorrectly excited coherently, but the spots they produce on the detector plane will not overlap. The 0.8 NA with which we performed all calculations yields a spot size on the order of \( 1 - 2\mu m \) in the near-IR, which is roughly on the order of the gate size. The wires in the gate are therefore driven uniformly, but neighboring gates are excited to a lesser degree.

A.4. Gate Identification. We empirically calculated the error rate of our classifier by segmenting our data into a train and test set and using the latter to determine the rate of mis-classifications. If insufficient data is present neither the train nor test data sets will accurately represent the true statistical behavior of the observations. As a result the features selected and error rates will depend strongly on the test and train data. If sufficient data are present, not matter how the observations are divvied up, the statistical distributions they describe will be the same. Therefore both the error rate and features selected should be consistent irregardless of exactly which observations are put into the test or train set.

To verify that this was the case here, we randomly segmented our data into test and train sets and determined features and error rates. We repeated this process 10 times. As shown in Figure 5b in the main text, the error rate varied negligibly Figure 7 shows the features chosen to classify the gates for each of the four polarization cases. The features selected are also extremely consistent across all 10 runs. Features selected earlier were highly consistent. This is expected since they are the most useful in discriminating between the different gates. Features selected later tend to be less consistent as they offer less improvement. This is reflected in the slopes of the accuracy curves in Figure 5 of the main text.

A.5. Integrated Circuits and Simulated Training Samples. All integrated circuit gate layouts are taken from the Nangate 45 nm open source library [19]. The library specifies the planar geometries of the various layers - diffusion, polysilicon, contact, metal 1 - present in each gate. Throughout, for simplicity, we limited our analysis to the metal 1 and contact layers and Si substrate. Due to the lower refractive index contrast the diffusion and polysilicon layers will contribute to the signal to a significantly smaller degree.

The specific gates we selected for our test set were the six smallest 2-input fundamental gates in the library. These are denoted, in full, ‘XOR2_X1’, ‘XNOR2_X1’, ‘AND2_X1’ and so on for the
Figure 7. Feature selection over multiple runs. The features selected during the empirical feature selection and error calculation process are shown for each of the four polarization cases (a - u), (b - x), (c - y) and (d - x, y). Each row in the panels represents one of the 10 runs. The different markers indicate the order the features were selected in, the first, 1, being the most important and last, 5th, being the least.

Other gates. All gates in the set, and in the entire library, are consistently dimensioned at 1.14 µm in the vertical direction. This is due to the fact that in an IC the source voltage and ground rails are arranged on a regular 1D grid and the gates tiled in between them (see e.g. Figure 2). The horizontal dimensions are $d_i = 1.14$ µm for the (XOR, XNOR), $d_j = 0.76$ µm for (AND, OR) and $d_k = 0.57$ µm for (NAND, NOR).

Figure 8. Spectral probability maps for the six fundamental logic gates imaged using a 0.8NA collection objective. The maps are shown for unpolarized (left) $x$ (middle) and $y$ (right) polarized illumination. The type of each logic gate is indicated. The apparent 'jumps' in some of the spectra are due to diffraction orders and are artifacts of the periodic simulation.
To generate the various spectral responses and histograms shown in Figure 4 in the main text and Figure 8, we generated a series of random tilings of these gates and simulated their images. The gates are arranged on a rectangular grid in the $y$ direction in a series of rows as illustrated in Figure 2 of the main text. The gates are placed randomly, subject to the constraint that all the rows must have a fixed length in $x$ to be compatible with the periodic unit cell of our simulation approach. We chose a unit cell size that corresponded to 4 rows and 4 gates per row with one of each pair type plus an addition gate of the middle size (total length $d_i + 2d_j + d_k$). Because the gates’ horizontal dimensions share a common factor, this unit cell could also be solved for with 5 gates per row (2 of type $j$ and 3 of type $k$). For each new simulation, one of the two possible solutions was selected at random (equal probability). For each row in the tilings, gate order and the exact gate for each type (i.e., XOR or XNOR) was again selected randomly for maximum diversity. In all we generated 20 different tilings which yielded a total of 22 observations each for the XOR and XNOR gates (the least frequent gates) and over 75 for each of the remaining gates in the set. The resultant probability distributions for all gates and polarizations are shown in Figure 8. We additionally generated a new image, not used in any of the feature selection or error calculations, to generate the results in Figures 6 and 9. Our spatial classification example described in Figure 6 of the main text is shown for 3 different $x$ direction sampling rates in Figure 9.

![Figure 9](image_url)

**Figure 9.** Influence of spatial sampling on the acquired probability map. Spatial gate and probability maps are generated as described in the main text. The spatial sampling interval in the $x$ direction is 100, 250 and 500 nm from the first to bottom row. The first column shows the gate level map with each pixel assigned to a gate class via the Bayes’ decision rule used throughout.

**Appendix B. System and Detector Noise Effects**
B.1. Signal-to-noise ration estimates. In order to estimate the influence of detector noise we used the usual definition of signal-to-noise ratio \( S/N \),

\[
S/N = \frac{i_S}{i_N} = \frac{R(\lambda) P_S}{\sqrt{\Delta f R(\lambda_p) P_{NEP}}}
\]

where \( i_N \) is the standard deviation in the detected signal, \( R(\lambda) \) is the detector responsivity and \( \lambda_p \) denotes the peak responsivity wavelength. The signal power, \( P_S \), depends on the sample reflectance via \( P_S = R \beta P_0 \), where \( P_0 \) is the source power and \( \beta \) scales for loss in the measurements system. Converting to a reflectance scale amounts to dividing all signals by \( P_S(R=1) \) such that the standard deviation in reflectance is given by \( \sigma = (S/N)^{-1} = P_{NEP}/\sqrt{\Delta f}/P_S \) as in the main text, where we have assumed \( P_S \) is measured for a perfectly reflecting sample at the peak responsivity. Assuming the noise is purely additive, this \( \sigma \), can be used for all the probability distributions when approximated as Gaussian.

Commercially available extended InGaAs detectors have a \( P_{NEP} \sim 10^{-12} \text{W}/\sqrt{\text{Hz}} \) and a high responsivity between \( \lambda = 1 - 2.6 \mu\text{m} \) \[45\]. From equation B1, the required signal power to achieve a given \( S/N \) is given by,

\[
P_{S,\text{det}}(S/N, \lambda, \Delta f) = (S/N) \sqrt{\Delta f R(\lambda_p) P_{NEP}/R(\lambda)}
\]

Figure 10 gives a sense of the required powers to produce a \( S/N \) of 100 at MHz imaging rates (i.e. \( \Delta f = 1 \text{MHz} \)) for a typical commercial InGaAs detector, calculated according to eq. B2 where the responsivity curve is extracted from the data sheet in \[45\]. As stated in the main text, power levels on the order of 0.1 – 1 \( \mu\text{W} \) should be sufficient to achieve \( S/N > 100 \) therefore \( \sigma \sim 0.01 \).

To estimate the required input power to generate the desired signal levels at the detector we need to account for the sources of loss in the optical system as outlined in Appendix A1. Assuming \( \mu = \mu_c \approx \mu_f \), and that the detector plane aperture is not excessively small, \( P_D = [\mu T_{Si}(1-A_{Si})]/P_0 \). For a system like the one in \[34\], we estimate conservatively \( \mu \approx 0.2 \) where the majority of the loss is due to a non-polarizing beam splitter and a near-IR objective lens. For normally incident light and a Si refractive index of \( n = 3.5 \) \( T_{Si} \approx 0.7 \). Figure 10 describes these sources of loss and the implied required source power to yield a low detector noise of \( \sigma = 0.01 \). Our estimate for \( \beta \) was taken from Figure 1 in \[46\] is shown in Figure 10a and corresponds to a heavily doped Intel substrate. The required source powers assuming the same extended InGaAs detector as in Figure 10 and three different thickness substrates are shown in panel d. Milliwatt level source powers are clearly sufficient.

B.2. Gaussian Noise Approximation Estimates. To initially estimate the error in classification as a function of detector noise, we modeled the probability distribution at each wavelength as a Gaussian with a fixed standard deviation, \( \sigma \), and mean \( \mu \) given by the reflectance at a given feature,

\[
p(M|c) = \frac{1}{\sqrt{2\pi}\sigma} e^{-(M_i-\mu_{ij})^2/(2\sigma^2)}
\]

where \( \mu_{ij} = R(\lambda_i, q_i, c_j) \) using the spectra in Figure 3. Since the decision rule is \( M \in R_j \rightarrow c = c_j \), the error in classification can be calculated analytically as the overlap integral,
Figure 10. Required power for $S/N = 100$ measurements at $\Delta f = 1$ MHz and influence of optical system loss. (a) Responsivity of a Thorlabs extended InGaAs biased detector. The detector’s $P_{NEP} = 1 \times 10^{-12}$. (b) Power required for different values of $P_{NEP}$ ($10^{-11}$, $10^{-12}$ and $10^{-13}$ as indicated assuming the InGaAs responsively curve in (a). (c) Absorption coefficient for a heavily doped Si substrate. Extracted from Fig. 1 of [46]. (d) Transmission (single pass) through 50, 100 and 200 $\mu$m thick substrates. (e) Fraction of input power received at the detector for three different thickness Si substrates. Same legend as in (d). (f) Required input power from the source accounting for all sources of loss and detector responsivity.

Figure 11. Influence of Gaussian noise on gate classification accuracy. (a) Classification accuracy as a function of number of features used for a standard deviation of $\sigma = 0.05$. (b) Error rate ($1 - \text{Accuracy}$) as a function of noise ($\sigma$) in percent. The inset shows the low noise rates on a log scale.

\begin{equation}
K_{ij} = \int_{R_i} p(M|c_i)P(c_i) \, dM
\end{equation}
which gives the probability of incorrectly classifying gate type $c_i$ as $c_j$. The total error is the sum over all possible combinations of incorrect classifications. In order to compute the integral in equation [34], the quantity $p(M|c_i)$ still needs to be calculated just as was necessary to form the classification probability $P(c_i|M)$. Since we again used the assumption of independence the error rate calculated in this way is an approximation of the true error rate. We used equation [17] to determine the error in classification and selected classification features using the greedy approach described for a standard deviation of $\sigma = 0.05$. Figure [1] shows the accuracy increase as features are added for the four polarization configurations. We then fixed our feature vector $M$ and calculated the error rate as the noise level was varied. The results are shown in Figure [1b] and indicate that for $\sigma < 0.03$ accuracies of more than 99% (error below $10^{-2}$) are possible.

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