A Leakage-Tolerant 16–Bit Comparator using Lector Technique Based Footless Domino Logic Circuit

Sapna Rani Ghimiray, Preetisudha Meher, Manish Kumar
1Dept. of Electronics & Comm. Engg., NERIST, Arunachal Pradesh, India
2Dept. of Electronics & Computer Engg., NIT, Yupia, Arunachal Pradesh, India
3Department of ECE, Madan Mohan Malaviya University of Technology, Uttar Pradesh

Abstract: The continuous scaling has resulted in increased sub-threshold leakage current due to decreased threshold voltage. LECTOR is a technique to decrease the problem of leakage in CMOS circuits, it includes a p-type and n-type leakage controlled transistors (LCTs), which are self-controlled, between supply to ground which offers the extra resistance which will reduce the problem of leakage current in the CMOS circuits. In this paper 16-bit Lector based standard foot-less domino (SFLD) comparator is introduced, which provides 74% efficient reduction in leakage and is also efficient in terms of performance compared to basic 16-bit SFLD comparator. Simulations are performed in gpdk_90 nm CMOS technology using cadence virtuoso tool.

Keywords: Comparator, Domino Logic, Lector, SFLD.

1. INTRODUCTION

High–performance microprocessors, communication systems, and many other systems widely employ high fan-in dynamic comparators [1]. As superscalar microprocessors make enormous use of associative matching logic and dynamic comparators in support of virtual memory mechanisms and out-of-order executions, a power efficient as well as faster comparator is desirable. For high – speed and low power chip performed domino circuits are extensively used and can be classified broadly into footed and footless domino [2-3]. The footer transistor isolates the pull-down network (PDN) from ground preventing the state change of dynamic node by PDN during the pre-charge phase making it better with respect to timing characteristics. On the other hand, if the footer transistor is omitted from the circuit, the footless domino reduces both the power dissipation and the circuit evaluation delay. Due to different characteristics, the footed and footless domino based circuits both are extensively employed in leakage tolerant, high-performance processors [3].
Power consumption is an important factor in the design of CMOS VLSI circuits and high leakage current in nanometer region is becoming a significant contributor in power consumption of CMOS circuits with technology scaling. Consequently, the identification and modeling of different leakage components is mandatory for reduction of leakage power in low-power applications [4]. Gate length and oxide thickness are responsible for leakage power and it varies exponentially with threshold voltage and other parameters. Leakage current mechanism includes the following:

Sub-threshold leakage current ($I_{\text{sub}}$), in MOS transistors, which occurs when the gate voltage is lesser than the threshold voltage and consists of diffusion current, Refer to “(1),”.

$$I_{\text{sub}} = \mu_0 \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot V^2 \cdot e^{\frac{V_t - V_g}{nV}}$$

(1)

where, $\mu_0$ is the zero bias mobility, $C_{ox}$ is the gate oxide capacitance; $(W/L)$ is aspect ratio. The variable $V$ is the thermal voltage constant, $V_{gs}$ represent gate to source voltage, and the parameter $\nu$ is the sub-threshold swing coefficient. Fig. 1 shows the sources of leakage current.

Gate oxide tunnelling current ($I_G$), in which tunnelling of electrons results in leakage current due to high electric field across a thin gate oxide layer[5].

Reverse-biased junction leakage current ($I_{\text{REV}}$), the leakage at the junction occurs from the drain or source to the substrate through the reverse biased diodes when a transistor is OFF.

Junction leakage, which results from minority carrier diffusion and drift near the edge of the depletion regions, and also from recombination of electron–hole pairs in the depletion regions of reverse–bias junctions.

Hot–carrier injection, typically results in short–channel transistors. Due to a strong electric field near the silicon oxide interface, electrons or holes gain enough energy to overcome the interface and enter the oxide layers.

Gate–induced drain leakage ($I_{\text{GIDL}}$), is caused by high field effect in the drain junction of MOS transistors. Higher the supply voltage and thinner the oxide leads to increased GIDL.

Punch through leakage, results due to the decreased separation between depletion regions at the drain substrate and source-substrate junction. It occurs mainly in short-channel devices, where thus separation is very small.

The remaining paper is organized as follows. The Leakage current analysis in footless domino logic circuit and footless domino logic comparator is explained in section 2. In section 3.
Lector technique and proposed comparator logic is explained. Simulation results and analysis are explained in section 4. Finally, conclusion is enclosed in section 5.

2. LEAKAGE CURRENT ANALYSIS IN FOOTELESS DOMINOLOGIC CIRCUIT

2.1 Leakage Current Characteristics of PMOS and NMOS Devices

![Figure 2: NMOS and PMOS transistors (a) Maximum gate oxide leakage current state, (b) Maximum sub-threshold leakage current state.]

NMOS and PMOS transistors maximum gate oxide leakage and Sub-threshold leakage current is shown in Fig. 2. In Fig. 2(a) four components of $I_{\text{gate}}$ are shown: Gate –to– drain tunneling current ($I_{\text{gd}}$), gate – to – body tunneling current ($I_{\text{gb}}$), gate – to – channel tunneling current ($I_{\text{gc}}$) and gate – to – source tunneling current ($I_{\text{gs}}$) [6]. $I_{\text{gd}}$ and $I_{\text{gs}}$ are the tunneling edge currents from gate to drain and source terminals respectively, through the gate-to-drain and gate-to-source overlap areas. $I_{\text{gc}}$ is shared among source and drain terminals [7], whereas, $I_{\text{gb}}$ is smaller than the other three components of leakage gate current.

Transistor turning ON along with maximum potential difference between the gate-to-source and gate-to-drain terminal results in maximum gate oxide leakage current as shown in Fig. 2(a). Also, transistor turning OFF along with maximum potential difference between the gate to source and gate-to-drain terminal results in maximum sub-threshold leakage current as shown in Fig. 2(b).

The probability of electron tunneling is much greater than the probability of hole tunneling through the silicon dioxide which is used as a gate oxide in bulk CMOS technology. $I_{\text{gate}}$ on a PMOS device is much lower than the $I_{\text{gate}}$ of NMOS device with similar physical dimensions; width, length and $\text{tox}$ in deep submicron technology and at the same voltage difference across the insulator gate. The difference in gate leakage current ($I_{\text{gate}}$), between PMOS and NMOS transistor typically increases with increase in the supply voltage.

2.2 A 16-Bit Standard Footless Domino Comparator Circuit

The schematic design of a 16-bit input domino comparator with standard footless domino has been shown in Fig. 3. During pre-charge phase, clock is ‘0’, and all inputs become zero. Hence, at this time, dynamic node gets pre-charged through the $M_{\text{Pre}}$ transistor, as a result: the output of the comparator becomes ‘0’. During evaluation phase, when the clock is ‘1’, $M_{\text{Pre}}$ transistor goes OFF and the pull-down network becomes active and conducts based upon the logic levels of the applied inputs [8].

If all the bits of input A and input B are equal and matching, no discharge path exists between dynamic node and GND. But, if applied level logic of input A and input B vary asingle bit position, a conducting path is established between dynamic node and GND, resulting in discharging of the dynamic node. This leads to output node of comparator to become 1, along with giving way for a worst case scenario for the delay. The major problem in comparator...
design using basic domino logic is that; it fails to operate correctly for smaller size of the keeper transistor, M_K, because of high leakage current. Also, it dissipates enormous amount of energy on both: full match of input bits and mismatch of input bits.

Figure 3: Basic 16-bit Footless Domino Logic Comparator.

Figure 4: Generalized structure of Leakage Controlled Logic Gates
3. LECTOR TECHNIQUE

The purpose of this circuit technique is to effectively enhance the reduction of the gate oxide leakage current and the sub-threshold leakage current simultaneously. Fig. 4 shows the generalized structure of LECTOR technique. The concept behind this approach for the reduction of leakage power is the use of effective stacking of transistors between the path i.e., from VDD to GND. The observation based on [9] depicts that 'a state containing more than single transistor OFF in a path between supply voltage to ground is much less leaky than a state containing only a single transistor OFF in a path from VDD to GND.'

In this approach, two leakage control transistors LCTP (PMOS) and LCTN (NMOS) are introduced in between the pull-up and pull-down network and the gate of these two transistors are controlled by the source terminal of each other. Here, transistor LCTP and LCTN's switching depends on the potential difference at node Np and Nn, respectively. Hence, for any combination of applied input one of the lector transistors will operate near cut-off region, increasing the resistance between supply and ground rails leading to shrinking of the leakage current. The advantage of this approach is no need for external circuitry, since, LCT's are self-controlled.

The proposed 16-bit Lector based Footless domino comparator is shown in Fig. 5. The working of the proposed comparator is similar to standard footless domino comparator, except the dynamic node is changed in the proposed comparator. The drain node of LCTP and LCTN are connected together to form the input of the static CMOS inverter. This new input line is the dynamic node in the proposed comparator, whereas the evaluation network

![Figure 5: Proposed 16-bit Lector based Footless domino Comparator.](image-url)
is connected to node $N_N$. The explanation for leakage reduction of the proposed domino comparator circuit is as follows: During pre-charge phase, when the clock is low the dynamic node is charged to $V_{DD}$ through transistors, $M_{PS}$ and $LCTP$. The pre-charging of dynamic node is almost independent of the input states, hence, if all the inputs are low before the clock is set to low then the node $N_N$ will be at low voltage and transistor $LCTP$ offers the less resistance path for charging dynamic node. If all the applied inputs are high, then the potential difference at node $N_N$ is insufficient for turning OFF $LCTP$ completely i.e., $LCTP$ is operating near its cut-off region. Therefore, resistance due to $LCTP$ will be much lesser than the completely OFF state resistance leading to high charging of the dynamic node. In this case, only the leakage current is dependent on the applied inputs whereas, the comparator output is independent of these inputs.

Now, during evaluation phase, when the clock is high, dynamic node gets discharged or charged depending upon the applied input vectors. If all the inputs are matching, the dynamic node will not be discharged by the pull-down network and the output of the comparator is low and it turns ON keeper transistor, $M_K$. The voltage potential at node $N_P$ will turn ON the transistor $LCTN$, but potential at node $N_N$ will not allow the transistor $LCTP$ to completely cut-off making it operate near cut-off region leading to high resistance path between supply and ground shrinking the sub-threshold and gate leakage current. Here, if all the inputs are low, the $LCTP$ will operate near cut-off region and if all the applied inputs are high, the $LCTN$ will operate near cut-off region. Hence, by employing LCTs, the resistance between the supply and GND is increased which in turn reduces leakage current and simultaneously increases propagation delay of the domino comparator circuit. The proper sizing of the lector transistors, $LCTP$ and $LCTN$, helps in controlling the propagation delay of the circuit.

4. SIMULATION RESULTS AND ANALYSIS

A 16-bit basic standard footless domino comparator and the proposed 16-bit lector based footless domino comparator circuits were designed and simulated using Cadence Virtuoso 90nm technology in all process corners, at 110°C. The supply voltage used in the simulation is 0.9 V and the circuit operates in 500 MHz clock frequency.

4.1 Power Dissipation

The average power consumption in case of 16-bit standard footless domino comparator is about 126.4 uW. Whereas, the average power dissipation in case of proposed 16-bit lector based footless domino comparator is found to be 33.12 uW. The comparison has been done for both comparators and is shown in Fig. 6. The comparison clearly indicates the fact that the proposed comparator has the lowest power dissipation which indicates reduced leakage current.

4.2 Delay

Even though the delay is not much higher in proposed domino comparator due to proper sizing of the lector transistors used in the design, simulation has clearly indicated the fact that standard footless domino comparator is faster than lector based footless domino comparator. The delay comparison for all comparators has been done and shown in Fig. 7. The delay for the 16-bit standard footless domino and lector based proposed comparators are found to be 30.34
psand 37.77 ps, respectively. The delay has been calculated for\textit{th}, 209.951 mV and 0.9 V supply voltage.

\textbf{4.3 Power-Delay Product}

For domino logic circuits there exists a trade-off between the power and delay. With reduced leakage power, propagation delay increases. Hence, for better performance the designed circuit must have the lower Power-Delay Product (PDP). Therefore, Power-Delay Product has also been calculated and compared for both the comparator circuits. Fig.8 shows PDP comparison. The PDP for the 16-bit standard footless domino comparator and proposed 16-bit lector based footless domino comparators are 3.834E-15 s, and 1.25E-15 s, respectively.

Table I: Power dissipation, Delay and PDP used for both 16-bit comparator circuits

| Parameters for analysis | Circuits                                      |
|-------------------------|-----------------------------------------------|
|                         | Standard Footless Domino Comparator | LECTOR based Footless Domino Comparator |
| Power Dissipation       | 126.4 uW                                    | 33.12 uW                                 |
| Normalized Power        | 1                                            | 0.26                                      |
| Delay                   | 30.34 ps                                     | 37.77 ps                                 |
| Normalized Delay        | 1                                            | 1.24                                      |
| PDP                     | 3.834 fs                                     | 1.25 fs                                  |
| Normalized PDP          | 1                                            | 0.37                                      |

Figure 6: Power dissipation comparison for both comparators

Figure 7: Propagation delay comparison for both comparators

Figure 8: Power-Delay-Product comparison for both comparators
The Performance analysis of designed 16-bit standard footless domino comparator and 16-bit lector based footless domino comparator with respect to power dissipation, delay and PDP is summed up in the form of Table I. All the parameters are normalized with respect to standard footless domino logic comparator.

Here the simulation proves that the proposed lector based footless domino logic comparator is more efficient in terms of leakage current, power-delay-product at the expense of increased propagation delay. The amount of increased in delay is within tolerance range for the high performance required circuit application and can be further reduced by proper sizing of lector transistors.

5 CONCLUSION

Basic standard footless domino and Lector based footless domino 16-bit comparator circuits have been designed, simulated and compared with respect to Power consumption, delay and power-delay-product. Comparison reveals that the proposed comparators more efficient in terms of power consumption and PDP. The simulation results show proposed 16-bit lector based comparator is 74% more efficient in terms of power dissipation. The PDP of the proposed comparator is lowest and 67.39% efficient than the standard footless domino comparator and hence it proves progress in leakagereduction and acceptable speed for high-speed applications. We can further work towards noise improvement. The proposed leakage tolerant footless domino technique can be used in Wide fan-in OR gate and comparators which are required in high performance microprocessors and signal processing.

ACKNOWLEDGMENT

The authors wish to thank NIT Arunachal Pradesh, YUPIA for providing the simulation environment.

REFERENCES

[1] Menendez ER, Maduike DK, Garg R, Khatri SP, “CMOS comparators for high-speed and low-power applications”, International conference on computer design, ICCD’06, pp. 76–81, 2006.
[2] V. Kursun and E. G. Friedman, “Domino Logic with Variable Threshold Voltage Keeper,” IEEE Transactions on Very Large Scale Integration(VLSI) Systems, Vol. 11, pp. 1080-1093, 2003.
[3] H. Mahmoodi-Meimand and K. Roy, “A Leakage-Tolerant High Fan-in Dynamic Circuit Style,” IEEE International Systems-on-Chip Conference, pp. 117-120, 2003.
[4] A. Dutta, S. R. Ghimiray, M. Kumar, "Performance comparison of 3 bit ECRL ADC with conventional logic style,"International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT’2016), pp. 444-448, 2016.
[5] K. Roy, H. Mahmoodi, S. Mukhopadhyay, “Leakage control for Deep Submicron Circuits”, International Symposium on Microtechnologies for the New Millennium, vol. 5117, pp. 135-146, 2003
[6] Z. Liu and V. Kursun, “Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies,” Transactions on Circuits and Systems Part II—Express Briefs, Vol. 53, No. 8, pp. 692-696,2006.
[7] H. Sasaki, M. Ono, T. Ohguro, S. Nakamura, M. Satio and Iwai, “1.5 nm Direct-Tuneling Gate Oxide Si MOS- FETs,” IEEE Transactions on Electron Devices, Vol. 43, No. 8, pp. 1233-1242, 1996.
[8] Ergin, O., Ghose, K., Kucuk, G., Ponomarev, “A Circuit–Level Implementation of Fast, Energy Efficient CMOS Comparators for High–Performance Microprocessors”, in Proc. Of ICCD, pp.118–121, 2002.
[9] M. C. Johnson, D. Somasekhar, L. Y. Chiou and K. Roy, “Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS,” IEEE Transactions on VLSI Systems, Vol. 10, pp. 1-5, 2002.
[10] Preetisudha Meher and K. K. Mahapatra, “Modifications in CMOS Dynamic Logic Style: A Review Paper”, Journal of the Institution of Engineers – Springer “Series-B”, Vol. 96, pp. 391–399, 2013.

Sapna Rani Ghimiray received the B.Tech degree in Electronics and Communication Engineering from the North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India, in 2012 and the M.Tech degree in VLSI Design from Manipal University, India, in 2014. She is currently working towards the Ph.D. degree in the Department of Electronics and Communication Engineering from the North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India. Her current research interests include leakage-tolerant circuit design and low-power VLSI design.

Dr. Preetisudha Meher is now working as an assistant professor at National Institute of Technology, Arunachal Pradesh, India. She has done Ph.D from National Institute of Technology, Rourkela, India. Her area of interest is VLSI and Embedded systems. She had passed her M.Tech from National Institute of Science and Technology, India in the year 2008. She had done her B. Tech from Biju Pattnaik University of Technology, India. She is a researcher having many IEEE and other journal and conference papers.

Dr. Manish Kumar is now working as an associate professor at Madan Mohan Malaviya University Of Technology, Uttar Pradesh, India. He has done Ph.D from ISM Dhanbad, India, in the year 2014. He had done B.Tech and M.Tech from North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India, in the year 2002 and 2010, respectively. His area of interest is low power VLSI design and digital electronics.