G4LTL-ST: Automatic Generation of PLC Programs

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Abstract. G4LTL-ST automatically synthesizes control code for industrial Programmable Logic Controllers (PLC) from timed behavioral specifications of input-output signals. These specifications are expressed in a linear temporal logic (LTL) extended with non-linear arithmetic constraints and timing constraints on signals. G4LTL-ST generates code in IEC 61131-3-compatible Structured Text, which is compiled into executable code for a large number of industrial field-level devices. The synthesis algorithm of G4LTL-ST implements pseudo-Boolean abstraction of data constraints and the compilation of timing constraints into LTL, together with a counterstrategy-guided abstraction-refinement synthesis loop. Since temporal logic specifications are notoriously difficult to use in practice, G4LTL-ST supports engineers in specifying realizable control problems by suggesting suitable restrictions on the behavior of the control environment from failed synthesis attempts.

Key words: industrial automation, LTL synthesis, theory combination, assumption generation

1 Overview

Programmable Logic Controllers (PLC) are ubiquitous in the manufacturing and processing industries for realizing real-time controls with stringent dependability and safety requirements. A PLC is designed to read digital and analog inputs from various sensors and other PLCs, execute a user-defined program, and write the resulting digital and analog output values to various output elements including hydraulic and pneumatic actuators or indication lamps. The time it takes to complete such a scan cycle typically ranges in the milliseconds.

The languages defined in the IEC 61131-3 norm are the industry standard for programming PLCs [1]. Programming in these rather low-level languages can be very inefficient, and yields inflexible controls which are difficult to maintain and arduous to port. Moreover, industry is increasingly moving towards more flexible and modular production systems, where the control software is required to adapt to frequent specification changes [2].

With this motivation in mind, we developed the synthesis engine G4LTL-ST for generating IEC 61131-3-compatible Structured Text programs from behavioral specifications. Specifications of industrial control problems are expressed in a suitable extension of linear temporal logic (LTL) [16]. The well-known LTL operators $\mathcal{G}$, $\mathcal{F}$, $\mathcal{U}$, and $\mathcal{X}$ denote “always”, “eventually”, “(strong) until”, and “next”’s relations over linear execution traces. In addition to vanilla LTL, specifications in G4LTL-ST may also include
Input: $x, y \in [0, 4] \cap \mathbb{R}$, err $\in \mathbb{B}$, Output: grant1, grant2, light $\in \mathbb{B}$, Period: 50ms

$$\begin{align*}
1 & \text{G}(x + y > 3 \rightarrow X\text{grant1}) \\
2 & \text{G}(x^2 + y^2 < \frac{7}{2} \rightarrow X\text{grant2}) \\
3 & \text{G}(\neg(\text{grant1} \land \text{grant2})) \\
4 & \text{G}(\text{err} \rightarrow 10\text{sec}(\text{light})) \\
5 & \text{G}((\text{G}\neg\text{err}) \rightarrow (\text{FG}\neg\text{light}))
\end{align*}$$

Fig. 1. Linear temporal logic specification with arithmetic constraints and a timer.

- non-linear arithmetic constraints for specifying non-linear constraints on real-valued inputs;
- timing constraints based on timer constructs specified in IEC 61131-3.

A timing constraint of the form $10\text{sec}(\text{light})$, for example, specifies that the light signal is on for 10 seconds. Moreover, the semantics of temporal specifications in G4LTL-ST is slightly different from the standard semantics as used in model checking, since the execution model of PLCs is based on the concept of Mealy machines. Initial values for output signals are therefore undefined, and the synthesis engine of G4LTL-ST assumes that the environment of the controller makes the first move by setting the inputs.

Consider, for example, the PLC specification in Figure 1 with a specified scan cycle time of $50\text{ms}$ (line 1). The input variables $x, y, \text{err}$ store bounded input and sensor values, and output values are available at the end of each scan cycle at $\text{grant1}, \text{grant2}$, and $\text{light}$ (line 1). According to the specification in line 6, the output $\text{light}$ must be on for at least 10 seconds whenever an error occurs, that is, input signal $\text{err}$ is raised. Line 7 requires that if $\text{err}$ no longer appears, then eventually the $\text{light}$ signal is always off.

The transition-style LTL specifications 3 and 4 in Figure 1 require setting $\text{grant1}$ (resp. $\text{grant2}$) to true in the next cycle whenever the condition $x + y > 3$ (resp. $x^2 + y^2 < \frac{7}{2}$) holds. Finally, $\text{grant1}$ and $\text{grant2}$ are supposed to be mutually exclusive (line 5).

The synthesis engine of G4LTL-ST builds on top of traditional LTL synthesis techniques [15, 11, 17, 4] which view the synthesis problem as a game between the (sensor) environment and the controller. The moves of the environment in these games are determined by setting the input variables, and the controller reacts by setting output variables accordingly. The controller wins if the resulting input-output traces satisfy the given specification. Notably, arithmetic constraints and timers are viewed as theories and thus abstracted into a pseudo-Boolean LTL formula. This enables G4LTL-ST to utilize CEGAR-like [8, 14, 12] techniques for successively constraining the capabilities of the control environment.

Since specifications in linear temporal logic are often notoriously difficult to use in practice, G4LTL-ST diagnoses unrealizable specifications and suggests additional assumptions for making the controller synthesis problem realizable. The key hypothesis underlying this approach is that this kind of feedback is more useful for the engineer compared to, say, counter strategies. The assumption generation of G4LTL-ST uses built-in templates and heuristics for estimating the importance and for ordering the generated assumptions accordingly.

\[4\] Appendix C provides the detailed formulation and implemented algorithm for LTL synthesis.
Whenever $a$, then $b$ for $t$ seconds

$G(a \rightarrow (t1.start \land b \land X(b U t1.expire)))$

Whenever $a$ continues for more than $t$ seconds, then $b$

$(a \leftrightarrow t1.start) \land G(\neg(a \land X a) \leftrightarrow X t1.start) \land G(t1.expire \rightarrow b)$

Whenever $a$, then $b$, until $c$ for more than $t$ seconds

$G(a \leftrightarrow t1.start) \land G(\neg(c \land X c) \leftrightarrow X t1.start) \land G(a \rightarrow (b \land X((b U t1.expire)) \lor G(\neg t1.expire)))$

Table 1. Real-time specification patterns and their encodings.

Synthesis of control software, in particular, has been recognized as a key Industrie 4.0 technology for realizing flexible and modular controls (see, for example, [3], RE-2 on page 44). The synthesis engine G4LTL-ST is planned to be an integral part of a complete development tool chain towards meeting these challenges. G4LTL-ST is written in Java and is available (under the GPLv3 open source license) at

http://www.sourceforge.net/projects/g4ltl/files/beta

In the following we provide an overview of the main features of G4LTL-ST including Pseudo-Boolean abstractions of timing constraints, the abstraction-refinement synthesis loop underlying G4LTL-ST and its implementation, and, finally, the template-based generation for suggesting new constraints of the behavior of the environment for making the control synthesis problem realizable. These features of G4LTL-ST are usually only illustrated by means of examples, but the initiated reader should be able to fill in missing technical details.

2 Timing Abstractions

The timing constraint in Figure 1 with its 10 seconds time-out may be encoded in LTL by associating each discrete step with a 50ms time delay. Notice, however, that up to 200 consecutive X operators are needed for encoding this simple example.

Instead we propose a more efficient translation, based on standard IEC 61131-3 timing constructs, for realizing timing specifications. Consider, for example, the timed specification $G(err \rightarrow 10sec(light))$. In a first step, fresh variables $t1.start$ and $t1.expire$ are introduced, where $t1$ is a timer variable of type TON in IEC 61131-3. The additional output variable $t1.start$ starts the timer $t1$, and the additional input variable $t1.expire$ receives a time-out signal from $t1$ ten seconds after this timer has been started. Now, the timing specification $G(err \rightarrow 10sec(light))$ is rewritten as an LTL specification for a function block in the context of a timer.

$G(t1.start \rightarrow XFt1.expire) \rightarrow G(err \rightarrow (t1.start \land light \land X(light U t1.expire)))$

The antecedent formula ensures that the expire signal is eventually provided by the timing block of the environment. Since no provision is being made that there is a time-out exactly after 10 seconds, however, the precise expected behavior of the time-out environment is over-approximated.

It is straightforward to generate PLC code using timing function blocks from winning strategies of the controller. Whenever $t1.start$ is set to true the instruction $t1(IN:=0,
3 Abstraction-Refinement Synthesis Loop

The input to the synthesis engine of G4LTL-ST are LTL formulas with non-linear arithmetic constraints with bounded real (or rational) variables, and the workflow of this engine is depicted in Figure 2. Notice, however, that the abstraction-refinement loop in Figure 2 is more general in that it works for any decidable theory $\text{Th}$.

In a preliminary step $\text{Abstract}$ simply replaces arithmetic constraints on the inputs with fresh Boolean input variables. The resulting specification therefore is (like the timer abstraction in Section 2) an over-approximation of the behavior of the environment. In our running example in Figure 1 (ignoring line 6, 7), $\text{Abstract}$ creates two fresh Boolean variables, say $\text{req1}$ and $\text{req2}$, for the two input constraints $x + y > 3$ and $x^2 + y^2 < \frac{1}{2}$ to obtain the pseudo-Boolean specification

$$G(\text{req1} \rightarrow \text{X grant1}) \land G(\text{req2} \rightarrow \text{X grant2}) \land G(\neg(\text{grant1} \land \text{grant2}))$$

Fig. 2. Abstraction-refinement synthesis loop.
Clearly, this pseudo-Boolean specification with input variables \( \text{req1} \) and \( \text{req2} \) over-approximates the behavior of the environment, since it does not account for inter-relationships of the arithmetic input constraints.

In the next step, LTL controller synthesis checks whether or not the pseudo-Boolean LTL formula generated by Abstract is realizable. If the engine is able to realize a winning strategy for the control, say \( M_{ctrl} \), then a controller is synthesized from this strategy. Otherwise, a candidate counter-strategy, say \( M_{env} \), for defeating the controller’s purpose is generated.

The pseudo-Boolean specification (1), for example, is unrealizable. A candidate counter-strategy for the environment is given by only using the input \((\text{true}, \text{true})\), since, in violation of the mutual exclusion condition (1), the controller is forced to subsequently set both \( \text{grant1} \) and \( \text{grant2} \).

The Extract module extracts candidate counter-strategies with fewer pseudo-Boolean input valuations (via a greedy-based method) whose validity are not proven at the theory level. Consequently, the Extract module generates a candidate counter-strategy that only uses \((\text{req1}, \text{req2}) = (\text{true}, \text{true})\) and the input valuations \( S = \{ (\text{true}, \text{true}) \} \) are passed to the Theory Checker.

A candidate counter-strategy is a genuine counter-strategy only if all pseudo-Boolean input patterns are satisfiable at the theory level; in these cases the environment wins and Theory Checker reports the unrealizability of the control problem. In our running example, however, the input \((\text{true}, \text{true})\) is not satisfiable at the theory level, since the conjunction of the input constraints \( x + y > 3 \) and \( x^2 + y^2 < \frac{7}{2} \) is unsatisfiable for \( x, y \in [0, 4] \). G4LTL-ST uses the \( \text{JBernstein} \) [6] verification engine for discharging quantifier-free verification conditions involving non-linear real arithmetic. In order to avoid repeated processing at the theory level, all satisfiable inputs are memorized.

Unsatisfiable input combinations \( s_{in} \) are excluded by Refine. In our running example, the formula \( G(\neg(\text{req1} \land \text{req2})) \) is added as a new assumption on the environment, since the input pair \((\text{true}, \text{true})\) has been shown to be unsatisfiable.

\[
G(\neg(\text{req1} \land \text{req2})) \rightarrow (1) \quad (2)
\]

In this way, Refine successively refines the over-approximation of the behavior of the environment. Running the LTL synthesis engine on the refined specification 2 yields a controller: if one of \( \text{req1} \) \( (x + y > 3) \) and \( \text{req2} \) \( (x^2 + y^2 < \frac{7}{2}) \) holds, the controller may grant the corresponding client in the next round, since \( \text{req1} \) and \( \text{req2} \) do not hold simultaneously.

**Refinement of Timer Environments.** The refinement of over-approximations of environmental behavior also works for the abstracted timer environments. Recall from Section 2 that the initial abstraction is given by \( G(\texttt{t1.start} \rightarrow \texttt{X F t1.expire}) \). Assuming, for example, that \( \texttt{t1.expire} \) appears two iterations after \( \texttt{t1.start} \) in a candidate counter-strategy, one might strengthen this initial assumption with \( G(\texttt{t1.start} \rightarrow ((\texttt{X} \neg \texttt{t1.expire}) \land (\texttt{XX} \neg \texttt{t1.expire}) \land (\texttt{XXX} \texttt{F t1.expire}))) \).

**Synthesized Code.** The synthesized PLC for the complete control specification in Figure 1 is listed in the Appendix A. This synthesized function block can readily be passed
to industry-standard PLC development tools for connecting function blocks with concrete field device signals inside the main program to demonstrate desired behavior. Notice that the synthesized code in Appendix A is separated into two independent state machines. This separation is based on a simple analysis of G4LTL-ST for partitioning the specification into blocks with mutually independent output variables. In particular, in Figure 1, the formulas in line 3 to 5 do not consider err and light, and the formulas in lines 6 and 7 do not consider x, y, grant1, grant2. Therefore, code for these two blocks can be synthesized independently.

Constraints over input and output variables. Even though the current implementation of G4LTL-ST is restricted to specifications with arithmetic constraints on inputs only, the abstraction-refinement synthesis loop in Figure 2 works more generally for arithmetic constraints over input and output variables. Consider, for example, the specification $G(x > y \rightarrow X(z > x))$ with input variables $x, y \in [1, 2] \cap \mathbb{R}$ and output variable $z \in [0, 5] \cap \mathbb{R}$. Abstraction yields a pseudo-Boolean specification $G(in \rightarrow out)$ with in, out fresh input variables for the constraints $x > y$ and $z > x$, respectively. Now, pseudo-Boolean LTL synthesis generates a candidate winning strategy $M_{ctrl}$ for the controller, which simply sets the output out to be always true. The candidate controller $M_{ctrl}$ is realizable if every pseudo-Boolean output assignment of $M_{ctrl}$ is indeed satisfiable on the theory level. This condition amounts to demonstrating validity of the quantified formula $(\forall x \in [1, 2] \cap \mathbb{R}) (\exists z \in [0, 5] \cap \mathbb{R}) z > x$. Using the witness, say, 3 for the existentially quantified output variable $z$, a winning strategy for the controller is to always set the output $z$ to 3, and the control synthesis problem therefore is realizable.

Otherwise, the candidate controller strategy is not realizable at the theory level, and, for pseudo-Boolean outputs, refinement due to un-realizability of the control synthesis problem is achieved by adding new constraints as guarantees to the pseudo-Boolean specification. For example the constraint $G(\neg(grant1 \land grant2))$ is added to the pseudo-Boolean specification, if pseudo-Boolean outputs grant1 and grant2 are mutually exclusive at the theory level.

In this way, the abstraction-refinement synthesis loop in Figure 2 may handle arbitrary theory constraints on input and output variables as long as corresponding verification conditions in a first-order theory with one quantifier-alternation can be decided. The implementation of G4LTL-ST could easily be extended in this direction by using, for examples the verification procedure for the exists-forall fragment of non-linear arithmetic as described in [7]. So far we have not yet encountered the need for this extensions, since the PLC case studies currently available to us are restricted to Boolean outputs.

4 Assumption Generation

An unrealizable control synthesis problem can often be made realizable by restricting the capabilities of the input environment in a suitable way. In our case studies from the manufacturing domain, for example, suitable restrictions on the arrival rate of workpieces were often helpful. G4LTL-ST supports the generation of these assumptions from a set of given templates. For example, instantiations of the template $G(\forall a \rightarrow (X(\neg a U b)))$, where $a$ and $b$ are meta-variables for inputs, disallows
| Example |
|---------|
| Timer(T)/Data(d) | Lines of spec | Synthesis Time | Lines of ST |
| Ex1       | T, D         | 9             | 1.598s (comp)  | 110        |
| Ex2       | T            | 13            | 0.691s         | 148        |
| Ex3       | T            | 9             | 0.303s         | 80         |
| Ex4       | T            | 13            | 0.678s (comp)  | 210        |
| Ex5       | T            | 11            | 0.446s         | 41         |
| Ex6       | -            | 7             | 0.397s (comp)  | 165        |
| Ex7       | D            | 8             | 17s            | 43         |
| Ex8       | T            | 8             | 0.397s (comp)  | 653        |
| Ex9       | abstract D,T | 3 + model (< 200 loc) | 1.55s | 550 |
| Ex10      | abstract D,T | 3 + model (< 200 loc) | 3.344s | 229 |
| Ex11      | abstract D,T | 3 + model (< 200 loc) | 0.075s | 105 |

Table 2. Experimental result based on the predefined unroll depth (3) of G4LTL-ST. Execution time annotated with “(comp)” denotes that the value is reported by the compositional synthesis engine.

successive arrivals of an input signal $\textbf{?a}$. For a pre-specified set of templates, G4LTL-ST performs a heuristic match of the meta-variables with input variables by analyzing possible ways of the environment to defeat the control specification.

The underlying LTL synthesis engine performs bounded unroll [17] of the negated property to safety games. Therefore, whenever the controller cannot win the safety game, there exists an environment strategy which can be expanded as a finite tree, whose leaves are matched with the risk states of the game. Then, the following three steps are performed successively:

- **Extract** a longest path from the source to the leaf. Intuitively, this path represents a scenario where the controller endeavors to resist losing the game (without intentionally losing the game). For example, assume for such a longest path, that the environment uses $\textbf{a} \wedge \neg \textbf{a} \wedge \neg \textbf{a} \wedge \neg \textbf{a}$ to win the safety game.
- **Generalize** the longest path. Select from the set of templates one candidate which can fit the path in terms of generalization. For example, the path above may be generalized as $\textbf{FG}\neg \textbf{a}$. For every such template, the current implementation of G4LTL-ST defines a unique generalization function.
- **Resynthesize** the controller based on the newly introduced template. For example, given $\phi$ as the original specification, the new specification will be $(\neg \textbf{FG}\neg \textbf{a}) \rightarrow \phi$, which is equivalent to $(\textbf{GF}\textbf{a}) \rightarrow \phi$. Therefore, the path is generalized as an assumption stating that $\textbf{a}$ should appear infinitely often.

If this process fails to synthesize a controller, then new assumptions are added to further constrain the environment behavior. When the number of total assumptions reaches a
pre-defined threshold but no controller is generated, the engine stops and reports its inability to decide the given controller synthesis problem.

5 Outlook

The synthesis engine of G4LTL-ST has been evaluated on a number of simple automation examples extracted both from public sources and from ABB internal projects. The evaluation results in Table 2 demonstrate that, despite the underlying complexity of the LTL synthesis, G4LTL-ST can still provide a practical alternative to the prevailing low-level encodings of PLC programs\(^5\), whose block size are (commonly) within 1000 LOC. This is due to the fact that many modules are decomposed to only process a small amount of I/Os. For small sized I/Os, the abstraction of timers and data in G4LTL-ST together with counter-strategy-based lazy refinement are particularly effective in fighting the state explosion problem, since unnecessary unrolling (for timing) and bit-blasting (for data) are avoided. Data analysis is also effective when no precise (or imprecise) environment model is provided, as is commonly the case in industrial automation scenarios.

Mechanisms such as assumption generation are essential for the wide-spread deployment of G4LTL-ST in industry, since they provide feedback to the designer in the language of the problem domain. Extensive field tests, however, are needed for calibrating assumption generation in practice. Moreover, a targeted front-end language for high-level temporal specification of typical control problems for (networks of) PLCs needs to be developed [13].

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\(^5\) Short descriptions of the case studies have been added to the appendix.
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A Synthesized Function Block

Structured Text generated by G4LTL-ST for the synthesis control problem in Figure 1.

FUNCTION_BLOCK FB_G4LTL

VAR_INPUT
  x: REAL; y: REAL;
  error: BOOL;
END_VAR

VAR_OUTPUT
  grant1: BOOL; grant2: BOOL;
  light: BOOL;
END_VAR

VAR
  cstate1 : INT := 0; cstate2 : INT := 0;
  p0 : BOOL; p1 : BOOL;
  t1: TON;
END_VAR

VAR CONST T1_VALUE : TIME := TIME#10s; END_VAR

p0 := (x)+(y)>3; p1 := (x*x)+(y*y)<3.5; ( * Update the predicate based on sensor values * )

CASE cstate1 OF ( * State machines * )
  0: IF ((p0 = TRUE) AND (p1 = FALSE)) THEN cstate1 := 9; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = FALSE) AND (p1 = FALSE)) THEN cstate1 := 0; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = FALSE) AND (p1 = TRUE)) THEN cstate1 := 7; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = TRUE) AND (p1 = TRUE)) THEN cstate1 := 11; grant1 := TRUE; grant2 := FALSE;
     END_IF;
  7: IF ((p0 = TRUE) AND (p1 = FALSE)) THEN cstate1 := 9; grant1 := FALSE; grant2 := TRUE;
     ELSIF ((p0 = FALSE) AND (p1 = FALSE)) THEN cstate1 := 0; grant1 := FALSE; grant2 := TRUE;
     ELSIF ((p0 = FALSE) AND (p1 = TRUE)) THEN cstate1 := 7; grant1 := FALSE; grant2 := TRUE;
     ELSIF ((p0 = TRUE) AND (p1 = TRUE)) THEN cstate1 := 11; grant1 := TRUE; grant2 := FALSE;
     END_IF;
  9: IF ((p0 = TRUE) AND (p1 = FALSE)) THEN cstate1 := 9; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = FALSE) AND (p1 = FALSE)) THEN cstate1 := 0; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = FALSE) AND (p1 = TRUE)) THEN cstate1 := 7; grant1 := TRUE; grant2 := FALSE;
     ELSIF ((p0 = TRUE) AND (p1 = TRUE)) THEN cstate1 := 11; grant1 := TRUE; grant2 := FALSE;
     END_IF;
  11: IF ( (true ) ) THEN cstate1 := 11; grant1 := TRUE; grant2 := FALSE; END_IF;
END_CASE;

CASE cstate2 OF
  0: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (true)) THEN cstate2 := 6; light := FALSE; END_IF;
  43: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (true)) THEN cstate2 := 43; light := FALSE; END_IF;
  6: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (true)) THEN cstate2 := 6; light := FALSE; END_IF;
  396: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (t1.Q = FALSE)) THEN cstate2 := 396; light := TRUE;
     ELSIF ( (error = FALSE) AND (t1.Q = TRUE)) THEN cstate2 := 43; light := FALSE; END_IF;
  381: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (t1.Q = FALSE)) THEN cstate2 := 396; light := TRUE;
     ELSIF ( (error = FALSE) AND (t1.Q = TRUE)) THEN cstate2 := 43; light := FALSE; END_IF;
  12: IF ( (error = TRUE) AND (true)) THEN cstate2 := 12; light := TRUE; t1(IN:=0, PT:=T1_VALUE);
     ELSIF ( (error = FALSE) AND (t1.Q = FALSE)) THEN cstate2 := 396; light := TRUE;
     ELSIF ( (error = FALSE) AND (t1.Q = TRUE)) THEN cstate2 := 43; light := FALSE; END_IF;
END_CASE;
END_FUNCTION_BLOCK
B Evaluation

In this section, we outline specifications for each problem under analysis.

- **Ex1** Original example listed in Figure 1.
- **Ex2** Simplified specification for *equivalence with discrepancy time monitoring*: The discrepancy time is the maximum period during which both inputs may have different states without the function block detecting an error. The block should signal error when two input valuation differ in their values for more than time $T$.
- **Ex3** Simplified specification for *safety request*: It monitors the response time between the safety function request ($\text{s.opmode}$ set to $\text{FALSE}$) and the actuator acknowledgment ($\text{s.ack}$ switches to $\text{TRUE}$). Whenever the time exceeds the user-specified threshold $T$, signal error and propose again request to the actuator.
- **Ex4** Simplified specification for *sequential muting*. Sequential muting is a standard mechanism to monitor the entry of workpieces into critical region using 4 sensors; it is used when transporting the material into the danger zone without causing the machine to stop. The mechanism should signal the entry and leave of objects, and if the object does not leave the critical region within a user-specified time interval $T$, error should be reported.
- **Ex5** Control for conveyor belt. Transfer an object when light barrier detects it. If another object appears before the current output leaves, signal light and make alarm sound for $T$ seconds. Resume when the $\text{reset}$ button is pressed. Also retain silence when no object arrives.
- **Ex6** Example specification from the paper *"Formal Specification and Verification of Industrial Control Logic Components"* [13].
- **Ex7** Control synthesis for simple *nonlinear systems*, where the underlying dynamics is captured by a predicate transition system, which can be considered as the result of timed relational abstraction [20]. To successfully control the system, one needs to perform numerical reasoning also on the theory level, as the specification and the environment model use different predicates.
- **Ex8** Low-level *device function synthesis*. Our previous work MGSyn [5] synthesizes high-level orchestration code (in C++) to control each cell via OPC DA communication[6]. Nevertheless, it assumes that each station (cell) should provide a set of pre-specified functions (as a library) to control low-level devices. As an experiment, we use G4LTL-ST to synthesize some these basic functions for the Pick&Place module of the FESTO modular production system[7]. The combination of MGSyn and G4LTL-ST therefore completes the whole picture of automatic synthesis.
- **Ex9** The *DC-DC boost converter* circuit example [18]. The goal is to synthesize a PLC controller which opens or closes switches appropriately such that the behavior of the underlying linear hybrid system is always constrained under a certain threshold. The environment model (as a transition system) is generated from timed

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[6] http://en.wikipedia.org/wiki/OPC_Data_Access

[7] http://didacticonline.de/int-en/learning-systems/mps-the-modular-production-system/stations/pick-place-station-small-is-beautiful.htm
relational abstraction [20] extended with predicates. Two additional models are provided.

- **Ex10** Control of inverted pendulum with a physical model processed under timed-relational abstraction.
- **Ex11** Control of track system with a physical model processed under timed-relational abstraction.
- **Ex12** ABB Corporate Research in-house example (wind turbine yaw controller; details restricted).
- **Ex13** ABB Corporate Research in-house example (tide gate controller; details restricted).

- **Assumption generation.** We use commonly seen examples (e.g., from Lily [11]) to demonstrate the use of assumption generation. G4LTL-ST fails to synthesize controllers for these examples under the unroll depth 3 (some problems are realizable when increasing the unroll depth), but under this feature G4LTL-ST simple continues the synthesis process and discovers appropriate assumptions.

### C LTL Synthesis Engine

In this section, we formulate required definitions the implemented algorithms for LTL synthesis.

**Linear Temporal Logic (LTL)** Given two disjoint set of atomic propositions $V_{in} = \{i_1, \ldots, i_m\}$ and $V_{out} = \{o_1, \ldots, o_n\}$, the LTL formulas over $V_{in} \cup V_{out}$ are defined inductively:

- $v \in V_{in} \cup V_{out}$ is an LTL formula.
- If $\phi_1, \phi_2$ are LTL-formulas, then so are $\neg \phi_1, \neg \phi_2, \phi_1 \lor \phi_2, \phi_1 \land \phi_2, \phi_1 \to \phi_2$.
- If $\phi_1, \phi_2$ are LTL-formulas, then so are $G \phi_1, F \phi_1, X \phi_1, \phi_1 U \phi_2$.

Given an $\omega$-word $\sigma \in \omega \to 2^{V_{in} \cup V_{out}}$ and a natural number $i \in \omega$, the semantics of LTL is defined as follows.

- $\sigma, i \models v$ iff $v \in \sigma(i)$.
- $\sigma, i \not\models \neg \phi$ iff not $\sigma, i \models \phi$. Similar definitions follow for other logic operators $\lor, \land,$ and $\to$. We use interchangeably $\neg$ and $!$.
- $\sigma, i \models G \phi$ iff for all $j \geq i$: $\sigma, j \models \phi$.
- $\sigma, i \models F \phi$ iff for some $j \geq i$: $\sigma, j \models \phi$.
- $\sigma, i \models X \phi$ iff $\sigma, i + 1 \models \phi$.
- $\sigma, i \models \phi_1 U \phi_2$ iff for some $j \geq i$: $\sigma, j \models \phi_2$, and for all $k = i, \ldots, j - 1$: $\sigma, k \models \phi_1$.

**$\omega$-automaton.** A nondeterministic B"uchi word (NBW) automaton over $\Sigma = 2^{V_{in} \cup V_{out}}$ is a finite automaton $A = (Q, \Sigma, q_0, \Delta, F)$, where $Q$ is the set of states, $q_0$ is the initial state, $F \subseteq Q$ is the set of final states, and $\Delta \subseteq Q \times \Sigma \times Q$ is the transition relation. A

\footnote{NOTICE: For this model, a special input format is used to read the result of relational abstraction and product it with the translated game, rather than viewing them as environmental assumptions (when doing so, the environmental assumption contains around 200 lines) and bring all assumptions into the process of generating B"uchi automaton and perform bounded unroll.}
run on an input word $\sigma = \sigma_1 \sigma_2 \ldots$, where $\sigma \in \Sigma^\omega$, is a sequence $\rho = q_0 q_1 \ldots$ over states in $A$ such that (1) $q_0 = q_0$ and (2) for all $i \geq 0$: $(q_i, q_{i+1}) \in \Delta$. $A$ accepts $\sigma$ if there exists a run $\rho$ such that $q_i \in F$ for infinitely many $i$. A universal co-B"uchi word (UCW) automaton follows the above notation, but only accepts $\sigma$ if for every run $\rho$, $q_i \in F$ for only finitely many $i$.

From LTL to $\omega$-automaton It is known that for every LTL formula $\phi$, there exists an equivalent Buchi automaton representation $A_{\phi}$, such that a word $\sigma \in \Sigma^\omega$ satisfies $\phi$ iff there exists an accepting run in $A_{\phi}$ on $\sigma$ (algorithms can be found in, e.g., [9, 10]). Figure 3 shows some simple LTL formulas and the corresponding Buchi automata. Final states are with double circles. For the ease of understanding, in the graphical representation we fold many edges having the same source and destination into one, and represent these edges as a logic formula on the edge label. E.g., $\text{req} \leftrightarrow \text{grant}$ in Figure 3 actually represents the set $\{\langle \text{req}, \text{grant} \rangle, \langle \text{req}, \text{grant} \rangle, \langle \text{req}, \text{grant} \rangle, \langle \text{req}, \text{grant} \rangle\}$.

Edge-labeled game A labeled-game arena has the form $G = (Q, Q_0, E, q_0, \Sigma_{in}, \Sigma_{out}, L)$, where $Q$ is the set of locations, $Q_0 \subseteq Q$ is the set of control locations, $E \subseteq Q \times Q$ is the transition relation, $q_0$ is the initial location, $L$ is a labeling function mapping from each transition with source in $Q_0$ to $\Sigma_{out}$, and each transition with source in $Q \setminus Q_0$ to $\Sigma_{in}$. Such a graph is partitioned into two areas $Q_0$ and $Q_1 = Q \setminus Q_0$ (environment locations). A play is a sequence $\rho = r_0 r_1 \ldots$ with $(r_i, r_{i+1}) \in E$ which is built up based on player selections: if $r_i \in Q_0$ then control (player-0) decides the next location, and if $r_i \in Q_1$ then environment (player-1) decides the next location.

A strategy for control is a function $f : Q^+ \rightarrow Q$ which allocates a play prefix $r_0 \ldots r_k$, $r_k \in Q_0$ a set $Q' \subseteq Q$ of vertices such that $(r_k, r_{k+1}) \in E$, for all $r_{k+1} \in Q'$. A strategy $f$ is winning for control at location $q_0$, if any play $\rho$ starting from $q_0$ following $f$ satisfies the winning condition. In this paper we only use safety condition:

- Safety condition: a play is safety winning if $\text{occ}(\rho) \cap F = \emptyset$, where $F \subseteq Q$ is the set of risk states, and $\text{occ}(\rho)$ refers to the set of locations that appears in $\rho$. 

![Fig. 3. Some LTL formulas and their corresponding Buchi automaton, where $V_{in} = \{\text{req}\}$, $V_{out} = \{\text{grant}\}$, and $\Sigma = \{\langle \text{req,grant} \rangle, \langle \text{req,grant} \rangle, \langle \text{req,grant} \rangle, \langle \text{req,grant} \rangle\}$](image-url)
C.1 LTL Synthesis

Given a set of input and output variables $V_{in} = \{i_1, \ldots, i_m\}$ and $V_{out} = \{o_1, \ldots, o_n\}$, together with an LTL formula $\phi$ on $V_{in}$ and $V_{out}$. Let $A_\phi$ be the corresponding Büchi automaton of $\phi$. The LTL synthesis problem (where the environment takes the first move) asks the existence of a controller $f_{LTL} : (2^{V_{in}} \times 2^{V_{out}})^* \times 2^{V_{in}} \to 2^{V_{out}}$ such that, for every input sequence $a = a_1 a_2 \ldots$, where $a_i \in 2^{V_{in}}$:

- Given the prefix $a_1$ produce $b_1$.
- Given the prefix $a_1 b_1 \ldots a_k b_k a_{k+1}$, produce $b_{k+1}$.
- The produced output sequence $b = b_1 b_2 \ldots$ ensures that the word $\sigma = \sigma_1 \sigma_2 \ldots$, where $\sigma_i = a_i b_i \in 2^{V_{in} \cup V_{out}}$, creates an accepting run of $A_\phi$.

Equivalently, we can adapt the same definition by applying it to UCW, i.e., given $\phi$, the controller should only allow the all runs created by produced word to visit the $A_{\neg \phi}$ its final states only finitely often. Such a definition will be used later in bounded synthesis via safety games.

(Example) Consider the specification $\phi = \text{req} \leftrightarrow \text{grant}$. Based on our definition, any controller which outputs the same value as input in the first input-output cycle is considered to be a feasible solution.

C.2 LTL Synthesis via UCW and Bounded-unroll Safety Games

Given the LTL specification $\phi$, the roadmap of our method is to first construct the Büchi word automaton $A_{\neg \phi}$, and view it as an UCW, i.e., if an $\omega$-word $\sigma$ can visit final states of $A_{\neg \phi}$ only finitely often on every run, $\sigma$ is an $\omega$-word of $\phi$. Again assume that the construction of $A_{\neg \phi}$ is provided.

Creating Game-like Representations The first step, after creating $A_{\neg \phi}$, is to apply Algorithm 1 to create a game representation $G_{\neg \phi}$. Consider again the synthesis process of $\phi = G(\text{req} \rightarrow F\text{grant})$. Figure 4 (a) and (b) show the corresponding $A_{\neg \phi}$ and the translated game. A controller will, for every input sequence, produce the corresponding output sequence to ensure that all paths in the generated game will visit final states in $G_{\neg \phi}$ only finitely often. Not difficulty, we can observe a solution highlighted at Figure 4 (b), which outputs $\text{grant}$ at $s_1[1]$ (i.e., when input equals $\text{req}$) and outputs $\text{grant}$ or $!\text{grant}$ at $s_1[0]$ (i.e., when input equals $!\text{req}$). Outputting $\text{grant}$ at $s_1[1]$ ensures that $s_2$ is never visited from the initial state.

Bounded Unroll into Safety Games Once when the game representation $G_{\neg \phi}$ of $A_{\neg \phi}$ is generated, we then perform a $k$-bounded unroll by exploring all finite words of size $k/2$ defined in $A_{\neg \phi}$ to create a safety game. For all vertices whose descendants are not fully expanded, we consider them to be risk states. We define equivalence relation which enables to treat the two different vertices as the same one. By doing so, the unfolding in general does not create an arena with a tree structure but rather an arena with loops.

Given $G_{\neg \phi} = (Q, Q_0, E, q_0, \Sigma_{ins}, \Sigma_{out}, L)$ with final states $F_{\neg \phi} = \{f_1, \ldots, f_n\}$ provided by Algorithm 1, a node (i.e., an equivalence class) in the translated safety
The Büchi automaton for $\neg \phi = \neg (G \text{ (req } \rightarrow \text{ Fgrant)})$ (a). The translated arena $G$ (b). The generated safety game (with equivalence class folding) using unroll of depth 2 (c), where the pink vertex is considered as a risk state.

The game uses a set $\{q(v_1, \ldots, v_n)\}$ as its identifier, where $q \in Q$ is the last visited vertex and $v_i \in \mathbb{N}_0$ is the number of visited times for final state $f_i$, for a finite word whose corresponding state sequence ends at $q$. Algorithm 2 shows a worklist algorithm which performs $k$-bounded unroll to create a new safety game.

The worklist algorithm first pushes the initial state into the list (line 1,2). Then it continuously removes elements in the list to perform the expansion. As each state is associated with a number when it is placed in the worklist (line 2,5,9) and will not produce new elements to the list when the value exceeds $k$, the algorithm guarantees termination. If the element taken from the list is an environment vertex, then new vertices are created based on all possible input values (line 4). Otherwise, the algorithm considers, given an output valuation $\text{out}$, what are all possible successor states (line 6, 7). In line 7, for the ease of understanding, we use the following functions.

- **update**($q(v_1, \ldots, v_n)$, list($F$)) updates $v_i$ by $v_i + 1$, if in the list representation of $F$, the index of $q$ equals $i$. It is also used in line 1, i.e., if the initial state is a final state, then the value should start with 1 rather than 0.
• Given \( q = \{ q_1(v_1, \ldots, v_{1n}), \ldots, q_k(v_k, \ldots, v_{kn}) \} \), the operation \( q \triangleright q_i(v'_1, \ldots, v'_{in}) \) replaces \( q_i(v_1, \ldots, v_{in}) \) in \( q \) by \( q_i(\max(v_1, v'_1), \ldots, \max(v_{in}, v'_{in})) \). For example \( \{ q_1(1, 0), q_2(2, 3) \} \triangleright q(0, 1) \) we derive \( \{ q_1(1, 1), q_2(2, 3) \} \). Originally, having two elements \( q_1(1, 0) \) and \( q_1(0, 1) \) means that to visit \( v_1 \), there exists two runs where the first traverses the first final state and the other traverses the second final state. We do not maintain two separate information but rather use an overapproximation. It is the reason why our method is called merge-over-all-paths, as such a technique is borrowed from static analysis in program verification.

Therefore, in line 7, when the state is updated from \( q_i \) to \( q_i' \), at first the algorithm produces \( q_i'(v_1, \ldots, v_{in}) \). Then it uses function \( \text{update}() \) to update the number of visited final states considering \( q_i' \). Then it uses \( \triangleright \) to merge the result of newly computed \( q_i' \) to existing results. Line 8 checks if there exists a vertex in \( Q_s \) which has the same value of \( \text{succ} \) (using \( Q_s, \text{getEquiv} (\text{succ}) \)). If such a vertex exists, then connect all outgoing edges to the existed vertex rather than \( \text{succ} \).

(Example) Consider the following specification: \( \phi_{TG} : G(\text{req} \rightarrow (\text{grant} \lor \text{Xgrant})) \land G(\text{grant} \rightarrow \text{Xgrant}) \), which specifies that when a request arrives, a grant should be issued \text{true} immediately or with at most one unit delay. However, it is disallowed to issue to consecutive grants. Figure 5 shows the Büchi automaton of the complement specification \( \neg \phi_{TG} \). Two paths (1) \( s_1 \rightarrow s_2 \rightarrow s_4 \) and (2) \( s_1 \rightarrow s_3 \rightarrow s_4 \) reflect the erroneous scenario where in (1) a request is not granted in time, and in (2) there are two consecutive grants. Let \( \text{list}(F) = \{ s_2, s_3, s_4 \} \). Figure 6 shows the result of unrolled safety game. \( G_{\neg \phi_{TG}} \) starts with initial state \( s_1 \), and it has not visited any final state. Therefore the algorithm creates vertex \( \{ s_1(0, 0, 0) \} \) and add to the worklist (line 1). Then the algorithm creates \( \{ s_1(0, 0, 0), s_1(0, 0, 0) \} \) reflecting different input values (line 4). \( s_1 \) can move to \( \{ s_1, s_3 \} \) via \text{grant} when receiving input \text{req}. Therefore, we link \( \{ s_1(0, 0, 0) \} \) to a new environment vertex \( \{ s_1(0, 0, 0), s_3(0, 1, 0) \} \), where \( s_3(0, 1, 0) \) denotes that final state \( s_3 \) has been reached once (recall that \( s_3 \) is the second element in \( \text{list}(F) \), so \( s_3(0, 1, 0) \) changes to \( s_3(0, 1, 0) \) after \( \text{update}() \)). For \( s_1 \) and \( s_3 \), given any input, if output equals \( !\text{grant} \), \( s_3 \) cannot proceed while \( s_1 \) can move to \( s_1 \) or \( s_2 \). Therefore, by responding \( !\text{grant} \), \( \{ s_1(0, 0, 0), s_3(0, 0, 0) \} \) and \( \{ s_1(1)(0, 0, 0), s_3(1)(0, 1, 0) \} \) will move to \( \{ s_1(0, 0, 0), s_2(1, 0, 0) \} \). In this example, an unroll of depth 5 is sufficient to create a controller.
\[\neg (G (\text{req} \rightarrow (\text{grant} \lor X\text{grant})) \land G(\text{grant} \rightarrow X!\text{grant}))\]

**Fig. 5.** The Büchi automaton \(A_{\neg \phi_{TG}}\) for \(\neg \phi_{TG}\) (left) and the translated arena \(G_{\neg \phi_{TG}}\) (right).

**Fig. 6.** The generated safety game (with equivalence class folding) from \(G_{\neg \phi_{TG}}\) using unroll of depth 3.
Algorithm 1: Translating an automaton into a game

input : $A_\phi = (Q_\phi, \Sigma = \Sigma_{in} \times \Sigma_{out}, q_0, \Delta_\phi, F_\phi)$
output: $G_\phi = (Q, Q_0, E, q_0, \Sigma_{in}, \Sigma_{out}, L), F$ as accepting states

begin
   let $Q = Q_0 = E = L = \emptyset$
   /* Create environment locations in $G_\phi$ */
   \[ Q := Q \cup Q_\phi \]
   /* Create control locations in $G_\phi$ */
   for $q \in Q_\phi$ do
      for $in \in \Sigma_{in}$ do
         $Q := Q \cup \{ q[in] \}$
         $Q_0 := Q_0 \cup \{ q[in] \}$
   /* Create deadlock state in $G_\phi$ */
   $Q := Q \cup \{ q_{dead} \}$
   for $in \in \Sigma_{in}$ do
      $Q := Q \cup \{ q_{dead}[in] \}$
      $Q_0 := Q_0 \cup \{ q_{dead}[in] \}$
   /* Create environment edges and labeling in $G_\phi$ */
   for $q \in Q \setminus Q_0$ do
      for $q[in] \in Q_\phi$ do
         $E := E \cup \{ (q, q[in]) \}$
         $L(q, q[in]) := L(q, q[in]) \cup \{ in \}$
   /* Create control edges and labeling in $G_\phi$ */
   for $(q_1, in, out, q_2) \in \Delta_\phi$ do
      $E := E \cup \{ (q_1[in], q_2) \}$
      $L(q_1, q_2) := L(q_1, q_2) \cup \{ out \}$
   /* Create missing control edges $G_\phi$ */
   for $q[in] \in Q_0$ do
      for $out \in \Sigma_{out}$ do
         if $\exists q' \in Q \setminus Q_0$ such that $out \in L(q[in], q')$ then
            $E := E \cup \{ (q[in], q_{dead}) \}$
            $L(q[in], q_{dead}) := L(q_1[in], q_{dead}) \cup \{ out \}$
   let $q_0 = q_0_{\phi}$, and $\Sigma_{in}, \Sigma_{out}$ reuses contents in $A_\phi$
return $(G_\phi, F_\phi)$
Algorithm 2: Depth-$k$ unroll to safety games

**Input:** $G = (Q, Q_0, E, q_0, \Sigma_{in}, \Sigma_{out}, L, F : \{f_1, \ldots, f_n\}, k \in \mathbb{N}$

**Output:** $G_s = (Q_s, Q_{s0}, E_s, q_{s0}, \Sigma_{in}, \Sigma_{out}, L_s, s_{risk}) \in Q_s$

**Begin**

1. let $Q_s := \emptyset; E_s := \emptyset$
   
   /* Create worklist with initial element */

2. let worklist := \emptyset

3. let $q_{s0} := \{\text{update}(q_0(0, \ldots, 0), \text{list}(F))\}$

4. worklist.add($q_{s0}, 1$)

5. $Q_s := Q \cup \{q_{s0}, q_{risk}\}$

6. while worklist \neq \emptyset do

7. let $q = (\{q_1(v_1, \ldots, v_{1n}), \ldots, q_k(v_{k1}, \ldots, v_{kn})\}, i)$ := worklist.removeFirst()

8. if $i \leq k$ then

9. /* create edges for environment vertex */

10. for $in \in \Sigma_{in}$ do

11. let $\text{succ} := \{q_1[\text{in}](v_1, \ldots, v_{1n}), \ldots, q_k[\text{in}](v_{k1}, \ldots, v_{kn})\}$

12. $Q_s := Q \cup \{\text{succ}\}, Q_{s0} := Q_{s0} \cup \{\text{succ}\}; E_s := E_s \cup (q, \text{succ});$

13. $L(q, \text{succ}) := \{\text{in}\}$

14. worklist.add($\text{succ}, i + 1$)

15. else /* create edges for control vertex*/

16. for $out \in \Sigma_{out}$ do

17. let $\text{succ} := \emptyset$

18. for $q_i(v_i, \ldots, v_{in}) \in q$ do

19. /* $L(q_i, q_i') \in L(q_i, q_i') \in \text{list}(F))\}^

20. $\text{succ} := \text{succ} \cup \text{update}(q_i'(v_1, \ldots, v_{in}), \text{list}(F))\}$

21. /* Check if a vertex of same equivalence class has appeared */

22. if $Q_s.getEquiv(\text{succ}) \neq \text{null}$ then

23. $E_s := E_s \cup (q, Q_s.getEquiv(\text{succ}));$

24. $L(q, Q_s.getEquiv(\text{succ})) := \{\text{out}\}$

25. else

26. $E_s := E_s \cup (q, \text{succ}); L(q, \text{succ}) := \{\text{out}\}$

27. $Q_s := Q_s \cup \{\text{succ}\}$

28. worklist.add($\text{succ}, i + 1$)

29. else

30. $E_s := E_s \cup (q(v_1, \ldots, v_n), q_{risk})$

31. return $(Q_s, Q_{s0}, E_s, q_{s0}, \Sigma_{in}, \Sigma_{out}, L_s, q_{risk})$