High Efficiency Mechanism Analysis of Resonant Switched-Capacitor Converter

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ABSTRACT The switched-capacitor (SC) converters are gaining popularity in some practical use. Its resonant counterpart, with a small inductor as current shaper in the architecture, has the advantage of smoother charging current, smaller voltage and current variation ratio and so on. This paper presents a generic and thorough analysis of the efficiency mechanism of the resonant switched-capacitor converter (RSCC). It decomposes any RSCC into three basic sub-circuits of SRLC circuit, CRLC circuit and SRLC circuit, which are analyzed and compared with corresponding sub-circuits of SCC, respectively. Then the overall efficiency of a RSCC could be derived. Furthermore, a new calculation method of output impedance is developed in another perspective to reveal the high efficiency mechanism of RSCC. On this basis, the high efficiency operation condition for RSCC could be obtained. Finally, a resonant bridge modular switched-capacitor converter (RBMSCC) is proposed and built for example of extended implementation of RSCC to achieve high efficiency operation. Some useful comments for designing resonant switched-capacitor converters are suggested.

INDEX TERMS DC-DC power conversion, resonant converter, output impedance, switched-capacitor.

I. INTRODUCTION

The traditional power converters predominantly use magnetic components (inductors and transformers) as energy storage elements. Due to the bulky size and relatively high cost of the magnetic components, it features low power density and poor integration. Therefore, the inductance-less switched-capacitor converters (SCC) [1]–[4] are gaining popularity recent years because of their significant benefit of lightweight, small size, high power density and convenience to integrate, making it the prime candidate to replace traditional inductor-based converters and preferable in some applications [5]–[8]. However, there are some pending issues such as discontinuous input current, high peak current, and large voltage and current variation rate with associated electromagnetic interference (EMI) problems [9]–[11]. To make up for the weakness, a small series inductor can be introduced into the SCC to reduce high current peak and achieve zero current switching (ZCS) [12], [13]. The corresponding developed topologies are called resonant switched-capacitor converters (RSCC). Some complicated and useful topologies of RSCC with multiple control strategy have been proposed and developed [11], [14], [15].

Previous works have analyzed the efficiency problem and loss mechanism of SCC [16]–[20]. In [16], a basic charging circuit in SCC consisting of a series connection of a source, an ideal switch and a capacitor is considered. It is revealed that an inevitable and fixed charge-up loss will always accompany the charging process, which is determined by the step change of the capacitor voltage. Reference [17] comprehensively analyzes the efficiency mechanism of the equivalent circuits to form a SCC. However, for more complicated SC topologies, case when a capacitor is charged through a flying capacitor is not considered. Moreover, the resonant-operation is not under consideration. In [18], simple 1:1 SCC with its resonant counterpart is taken for example to derive the unified model of SCC, which is similarly, lack of universality. Reference [20] analyzes the intrinsic energy loss caused by the voltage gap between capacitors and proposes a soft-operation scheme to eliminate the current transient during the switching instance of a Dickson SCC, therefore avoiding charge-up...
the efficiency analysis of each sub-circuit respectively and build a basic method for efficiency improvement, the efficiency mechanism of RSCC is systematically analyzed, from a whole system. Meanwhile a new and more generalized method on output impedance of SC type converter have been derived [21]–[28]. A SC type converter can be equivalent to a generic model as Fig.2. The ideal transformer exports ideal output voltage and total conduction loss of the converter is equivalent to the loss generated by output current flowing through the output impedance \( R_e \). With larger \( R_e \), the converter would perform lower efficiency. Some calculation methods on output impedance of SC type converter have been derived [23]–[27]. In [23] and [24], the output impedance of 1:1 SCC is derived by denoting the voltage difference of \( V_{in} \) and \( V_{out} \) with the voltage gap of the flying capacitor and the output impedance can be found by \( (V_{in} - V_{out})/i_{out} \). This method is not generalized and not accurate when limited output capacitor is considered. In [25], the charge distribution vector of two-phase SCC is analyzed, which also reflects the current relationship. The expressions of output impedance under low frequency region (SSL) and high frequency region (FSL) are calculated separately. For SSL, the SCC works in Full-Charging (FC) mode while for FSL, the SCC work in nearly No-Charging (NC) mode. Since this method treats the capacitors and switches as independent elements, it’s not suitable for modeling RSCCs. In [26], a more generalized method based on average-current conduction loss is proposed. The advantage of this calculation method is that it is not only suitable for two-phase SCC, but also applicable for multi-phase converters and their resonant-operation type. But this method may be inaccurate when large output voltage ripple occurs.

To present a generic and comprehensive analysis of RSCC and build a basic method for efficiency improvement, the efficiency mechanism of RSCC is systematically analyzed, from the efficiency analysis of each sub-circuit respectively and then to a whole system. Meanwhile a new and more generalized calculation method for output impedance relying on the capacitor voltages for SC type converter is derived.

The rest of the paper is organized as follow: In Section II, the efficiency analysis of each sub-circuit for RSCC is conducted, and efficiency of sub-circuits between SCC and RSCC is compared. In Section III, efficiency insight between unit gain SCC and RSCC is discussed based on output impedance. In Section IV, the resonant bridge modular switched-capacitor converter is proposed for example of extended implementation of RSCC. Experimental results are given in Section VI. Then the conclusion is drawn in Section VII.

II. EFFICIENCY ANALYSIS AND COMPARISON OF BASIC SUB-CIRCUITS OF RSCC

A. EFFICIENCY OF SRLC CIRCUIT

Considering the charging phase of RSCC, the conduction path usually contains switch devices, input voltage source, resonant inductor, flying capacitors and a resistor which denotes the total equivalent resistance of entire circuit path, including the equivalent series resistance (ESR) of capacitors, the on-state resistance of power MOSFETs \( R_{on} \), the equivalent resistance of inductor and other stray resistance. Therefore, the charging path of an RSCC can be usually represented as a SRLC circuit, as is shown in Fig.1 (a).

Typical voltage and current waveforms of SRLC circuit are shown in Fig. 3. As SRLC circuit is underdamped circuit, time domain analytical solution of the voltages and current can be derived as:

\[
\begin{align*}
V_C(t) &= \frac{(V_{C\min} - V_{in})\omega_L}{\omega} e^{-\delta t} \sin(\omega t + \beta) + V_{in} \\
I(t) &= \frac{V_{in} - V_{C\min}}{\omega L} e^{-\delta t} \sin \omega t \\
\delta &= R/2L, \quad \omega = \sqrt{1/LC - (R/2L)^2}, \\
\omega_0 &= \sqrt{\delta^2 + \omega^2}, \quad \cos \beta = \delta/\omega_0
\end{align*}
\]

where \( \omega \) is the \( Q \)-adjusted resonant frequency for the SRLC circuit, assuming a quality factor, \( Q = (L/C)^{0.5}/R \). \( V_{C\min} \) denotes the initial voltage of capacitor.

It is assumed that maximum charging time period is \( T_d \), where \( T_d = \pi/\delta \) in which case the energy is not flowing back and zero-current switching is realized. The charging time is denoted by \( T_c \). By the classification of \( T_c \), charging process can be classified into two categories: partial charging (PC) at \( T_c < T_d \) and full charging (FC) at \( T_c = T_d \).

During charging time \( T_c \), the initial voltage and terminal voltage are denoted by \( V_{C\min} \) and \( V_{C\max} \), respectively. The
In basic analysis, the charging efficiency refers to the energy that capacitor receives from the energy releaser. Therefore, the PC efficiency of this process can be derived as:

$$\eta_{SRLC\text{-}full} = \frac{\Delta E_C}{\Delta E_{in}} = \frac{1}{2} \frac{V_{C_{\max}} + V_{C_{\min}}}{V_{in}} \approx \frac{\bar{V}_C}{V_{in}}$$

(3)

The full-charging situation occurs when the charging time equals to $T_c$. Substituting $T_d$ to (3), the FC efficiency of SRLC sub-circuit can be derived as:

$$\eta_{SRLC\text{-}partial} = \frac{\Delta E_C}{\Delta E_{in}} = \frac{1}{2} \frac{V_{C_{\max}} + V_{C_{\min}}}{V_{in}} \approx \frac{\bar{V}_C}{V_{in}}$$

(4)

$\alpha_1$ is the amplitude attenuation coefficient, which yields $\alpha_1 = e^{-\delta T_c}$. Under ideal condition, $\alpha_1$ equals to 1, in which case the FC efficiency of SRLC circuit reaches 100%. It is indicated that reducing the total resistance of charging and discharging path of RSCC is effective to improve the transfer efficiency, unlike the case of SCC.

Equations (3) and (4) both indicate that the charging efficiency is independent of the circuit inductor and resistance. Once the terminal voltage $V_{C_{\max}}$ is fixed, the sum of energy consumed by the resistor and energy stored in the inductor maintains a fixed value. The energy stored in the inductor can be expressed as:

$$\Delta E_L = (V_{C_{\min}} - V_{in})^2 e^{-2\delta T_c} \sin^2 \omega T_c / (2 \omega^2 L)$$

(5)

Equation (5) is a decreasing function as $R$ increases, thus with a smaller equivalent resistance, more energy will be stored in the inductor and less energy will be consumed by the resistor.

The charging process starts with two possible initial conditions: zero initial state with $V_{C_{\min}} = 0$ and nonzero initial state with $V_{C_{\min}} > 0$, as depicted in Fig.4.

Through analyzing, some conclusions on SRLC yields:

1) Under zero initial state, the charging efficiency is decided by $V_{C_{\max}}$ and increases with an increasing $V_{C_{\max}}$. Differ from the non-resonant case, the capacitor can be charged up to more than $V_{in}$ and up to $V_{in} (1 + \alpha)$ (up to 2 $V_{in}$ under ideal condition). In PC, if $V_{C_{\max}} < V_{in}$, the charging efficiency will be less than 50%; if $V_{C_{\max}} > V_{in}$, it will be greater than 50%. In FC, it will reach $(1 + \alpha_1)/2$, which is 100% under ideal condition.

2) Under nonzero initial state, the amplitude of both voltage and current waveforms will drop and peak voltage of capacitor goes down. The charging efficiency is decided by the sum of critical voltages. In FC process under ideal condition, terminal voltage can only reach $(2 V_{in} - V_{C_{\min}})$ but the charging efficiency is still 100%.

3) The charging efficiency of SRLC charging process is independent of the totality of $R$ and $L$. To reach same terminal voltage, increasing of $R$ will lead to slightly increased charging duration $T_c$ and reduced peak value of charging current. Instantaneous current and voltage waveforms of SRLC charging circuits with different $R$ are shown in Fig.5 (a) and Fig.5 (b), respectively.

**B. EFFICIENCY OF CRLC CIRCUIT**

The second kind of equivalent circuit is denoted by CRLC circuit shown in Fig.1 (b). The energy releaser is usually replaced from a bulk capacitor by a relatively small resonant capacitor. Assumes that the voltages across both $C_o$ and $C$ are close enough, as is the practical case. Typical voltage and current waveforms are shown in Fig.6(a). Replacing the series $C$ and $C_o$ by $C_E$,

$$C_E = \frac{C C_O}{C + C_O} = \left(\frac{1}{1 + m}\right) C$$

where, $m$ is the ratio between $C$ and $C_o$ ($C_o = mC$). As shown in Fig.6(b), the CRLC circuit becomes second-order circuit. Suppose that the initial voltages on $C$ and $C_o$ are $V_{C_{\max}}$ and $V_{O_{\min}}$, respectively. This basic sub-circuit can be solved:

$$\begin{align*}
V_{C_i}(t) &= \left(\frac{V_{C_{\max}} - V_{O_{\min}}}{\omega L}\right) e^{-\delta t} \sin(\omega t + \beta) \\
I(t) &= \frac{V_{C_{\max}} - V_{O_{\max}}}{\omega L} e^{-\delta t} \sin(\omega t) \\
\delta &= R/2L,
\end{align*}$$

(7)

Applying the basic voltage-current relationship of a capacitor, it yields:

$$\begin{align*}
V_{C_i}(t) &= \frac{V_{C_{\max}} - V_{O_{\min}}}{\omega L} e^{-\delta t} \sin(\omega t + \beta) \\
V_{O_i}(t) &= C (V_{C_{\max}} - V_{C_{\min}}) e^{-\delta t} \sin(\omega t + \beta) \\
\omega_o &= \sqrt{\delta^2 + \omega^2}, \cos \beta = \delta / \omega_o
\end{align*}$$

(8)

Assuming that after a charging time $T_c$, the voltage on $C$ goes down to $V_{C_{\min}}$ and $C_o$ is charged from $V_{O_{\min}}$ to $V_{O_{\max}}$. According to charge balance, the relationship between critical voltages is:

$$V_{C_{\min}} = V_{C_{\max}} - m(V_{O_{\max}} - V_{O_{\min}})$$

(9)
In this case, the amplitude attenuation coefficient is:
\[
\alpha_2 = e^{-(R/2L)\pi/\sqrt{1/(LC)}} \approx \frac{1}{\sqrt{1/(LC)}}
\]

From formulas (12) and (14), the charging efficiency of CRLC circuit is independent of the totality of L and R. The energy loss on resistor will decrease and energy stored in the inductor will increase with decrease of equivalent resistance. However, it is indicated from the efficiency expressions that efficiency is in connection with \(\Delta V_C\) and \(\Delta V_O\). To get high discharging efficiency, both \(\Delta V_C\) and \(\Delta V_O\) should be controlled small.

\(\Delta V_C\) and \(\Delta V_O\) is in connection with the ratio of \(C\) and \(C_o\), denoted as \(m\). Take zero initial state for simplicity, the efficiency expression of CRLC circuit can be rewritten as

\[
\eta_{CRLC} = \frac{V_{O_{max}}}{2V_{C_{max}} - mV_{O_{max}}}
\]

(16)

Charging \(C_o\) to specific voltage, smaller \(m\) value will lead to higher charging efficiency. The FC terminal voltage expression of \(C_o\) can be rewritten as:

\[
V_{O_{max}} = \frac{2V_{C_{max}}}{1 + m}
\]

(17)

Increasing of \(m\) value will lead to decrease of the FC terminal voltage on \(C_o\), which may cause the desired voltage to be unreachable. So \(m\) value should be carefully selected in practical application.

### C. Efficiency of SRLC\(^2\) Circuit

For practical RSCC, it’s a common switching phase where voltage source and pre-charged flying-capacitor deliver energy to the output capacitor. The corresponding equivalent sub-circuit is shown in Fig.1 (c), denoted as SRLC\(^2\) circuit. For more complicated typology, more than one flying capacitor may be employed but can be equivalent to one. Typical voltage and current waveforms of SRLC\(^2\) circuit are shown in Fig.7. The instantaneous voltage on each capacitor can be derived:

\[
V_C(t) = \frac{C_D(V_{in} + V_{C_{max}} - V_{O_{min}})e^{-\delta t} \sin(\omega t + \beta)}{CV_{C_{max}} + CV_{O_{min}} + C_DV_{in}} + \frac{(C + C_D)e^{-\delta t} \sin(\omega t + \beta)}{C + C_D}
\]

\[
V_O(t) = \frac{C_D(V_{O_{min}} - V_{C_{max}} - V_{O_{min}})e^{-\delta t} \sin(\omega t + \beta)}{CV_{C_{max}} + CV_{O_{min}} + C_DV_{in}}
\]

(18)
In FC case, the terminal voltages on capacitors are:

\[
\begin{align*}
V_{C_{\text{min}}} &= C_O(V_{O_{\text{min}}} - V_{C_{\text{max}}} - V_{in})/\alpha_2 \\
&+ CV_{C_{\text{max}}} + C_OV_{O_{\text{min}}} - C_OV_{in} \\
V_{O_{\text{max}}} &= C(V_{in} + V_{C_{\text{max}}} - V_{O_{\text{min}}})/\alpha_2 \\
&+ CV_{C_{\text{max}}} + C_OV_{O_{\text{min}}} + CV_{in} \\
&+ CV_{O_{\text{max}}} + CV_{C_{\text{max}}} - CV_{O_{\text{min}}} \\
&/C + C_O
\end{align*}
\]

The energy profile can be found:

\[
\begin{align*}
\Delta E_{in} &= \int_0^{T_d} V_{in} \cdot I_C(t) \, dt \\
&= C_EV_{in}(V_{in} + V_{C_{\text{max}}} - V_{O_{\text{min}}})(\alpha_2 + 1) \\
\Delta E_C &= \int_0^{T_d} V_C(t) \cdot I_C(t) \, dt \\
&= \frac{1}{2} C(V_{C_{\text{max}}}^2 - V_{C_{\min}}^2) \\
\Delta E_{C_{O}} &= \int_0^{T_d} V_{O_{t}} \cdot I_{C_{t}}(t) \, dt \\
&= \frac{1}{2} C_O(V_{O_{\text{max}}}^2 - V_{O_{\text{min}}}^2)
\end{align*}
\]

Then, the charging efficiency of SRLC\textsuperscript{2} circuit is derived as (21), as shown at the bottom of the page.

From (21), it is suggested that the efficiency of SRLC\textsuperscript{2} circuit is affected by the initial voltage gap between the flying capacitor and output capacitor, and the respective voltage gap between initial and terminal on each capacitor. Specifically, to get high charging efficiency, the initial voltage gap on different capacitors and the voltage gap between critical voltages on each capacitor should all be controlled small.

To sum up, the efficiency expressions of the typical sub-circuits are listed in Table 1.

**D. EFFICIENCY COMPARISON OF SUB-CIRCUITS FOR SCC AND RSCC**

Detailed and complete analysis of SCC has been represented in previous works [16]–[20]. With the same assumption of the critical voltages on each capacitor, the mathematical conclusion on efficiency of the sub-circuits form SCC is summarized in Table 1 as well.

\[
\eta_{\text{SRLC}\textsuperscript{2}} = \frac{C_O(V_{O_{\text{max}}}^2 - V_{O_{\text{min}}}^2)}{2C_EV_{in}(V_{in} + V_{C_{\text{max}}} - V_{O_{\text{min}}})(\alpha_2 + 1) + C(V_{C_{\text{max}}}^2 - V_{C_{\min}}^2)} \\
= \frac{2CV_{O_{\text{min}}} + C^2(V_{in} + V_{C_{\text{max}}} - V_{O_{\text{min}}})(\alpha_2 + 1)}{CC_O(C + C_O)V_{in} + 2C_OV_{C_{\text{max}}} - C_O^2(V_{in} + V_{C_{\text{max}}} - V_{O_{\text{min}}})(\alpha_2 + 1)}
\]

Comparing the efficiency expression of each sub-circuit from RSCC with their counterpart from SCC, some conclusion can be drawn:

1) The efficiency expression of SRLC circuit is the same as that of SRC circuit. Likewise, the efficiency expression of CRLC circuit is the same as that of non-resonant situation.

2) When a capacitor is linked to a voltage source or another capacitor, the charging efficiency is determined by the critical voltages of the capacitors and power source, regardless of the intermediate components.

3) The intermediate components function to affect the shape and duration of charging current. When there ideally doesn’t exist any intermediate components, the charging current is infinite impulse with zero conduction time. The presence of resistance makes the current exponential with high peak value. Then introducing an inductor makes the current sinusoidal. The current peak is greatly reduced but the time duration is longer.

**III. EFFICIENCY INSIGHT BETWEEN UNIT GAIN SCC AND RSCC BASED ON OUTPUT IMPEDANCE**

Considering the generality, SCC and RSCC with unit gain is represented to make comparison for efficiency insight. For unit gain SCC, a simplest two-phase complete converter consists of a SRC sub-circuit and a CRC sub-circuit. And for unit gain RSCC, the simplest case consists of a SRLC sub-circuit and a CRLC sub-circuit, as is depicted in Fig.8.

A two-phase RSCC may work in different mode with the change of switching frequency. There is a critical frequency \(f_c\) for each phase. With previous assumption, the critical frequency of each operation phase equals to the resonant frequency and the two critical frequencies equal to each other approximately, which yields:

\[f_{c1} = f_{c2} = \frac{\omega}{2\pi}\]

The inductor current under three different switching frequencies are shown in Fig.9: a) \(f_{sw} < f_c\), b) \(f_{sw} = f_c\) and c) \(f_{sw} > f_c\). When \(f_{sw}\) is larger than \(f_c\), the converter works at continuous current mode (CCM), and there is current back-flow to the voltage input source in this situation, which naturally leads to unnecessary additional power loss. When \(f_{sw}\) and \(f_c\) are identical, it’s resonant operation. When \(f_{sw}\) is smaller than \(f_c\), the converter works at discontinuous current mode (DCM). The DCM corresponds to the process where the capacitor is fully charged.

The efficiency change of a SCC or RSCC with the change of the switching frequency is usually reflected by the output impedance modeling [21]. The SC type converter in
TABLE 1. Efficiency expression of each sub-circuit from RSCC and SCC.

| Sub-circuit | Partial-charging (PC) Typical Expression | Full-charging (FC) Typical Expression | Max. |
|-------------|------------------------------------------|--------------------------------------|------|
| RSCC        | \( \frac{V_{\text{PC}} + V_{\text{FC}}}{2V_o} \) | \( \frac{1}{2} \left( \frac{V_o - V_{\text{PC}}}{{\alpha}_1} + \left( \frac{V_o + V_{\text{PC}}}{2} \right) \right) \) | 100% @FC,R=0 |
| CRLC        | \( \frac{V_{\text{PC}} + V_{\text{FC}}}{V_{\text{PC}} + V_{\text{FC}}} \) | \( \frac{(1-\alpha_1)\frac{V_{\text{PC}} + V_{\text{FC}}}{m + 2}}{2m + 1 + \alpha_1} \) | 100% @FC,R=0 |
| SRLC^2      | \( \frac{m(1 + m)(V_{\text{PC}}^2 - V_{\text{FC}}^2)}{2mV_o(V_o + V_{\text{PC}} - V_{\text{FC}})(e^{-2\tau_{\text{PC}}} + 1) + (1 + m)(V_{\text{PC}}^2 - V_{\text{FC}}^2)} \) | \( \frac{2CV_{\text{PC}} - C^2(V_{\text{PC}} + V_{\text{FC}} - V_{\text{DO}})(\tau_{\text{PC}} + 1)}{CC_o(C + C_{\text{DO}})V_o + 2C_oV_{\text{PC}} - C_{\text{DO}}(V_{\text{PC}} + V_{\text{FC}} - V_{\text{DO}})(\alpha_1 + 1)} \) | 100% @FC,R=0 |
| SRC         | \( \frac{V_{\text{PC}} + V_{\text{FC}}}{2V_o} \) | \( \frac{V_o + V_{\text{FC}}}{2V_o} \) | <100% @any R |
| CRC         | \( \frac{V_{\text{PC}} + V_{\text{FC}}}{V_{\text{PC}} + V_{\text{FC}}} \) | \( \frac{V_{\text{FC}} + (m + 1)V_{\text{DO}}}{(m + 2)V_{\text{FC}} + mV_{\text{DO}}} \) | <100% @any R |
| SRLC^2      | \( \frac{m(1 + m)(V_{\text{PC}}^2 - V_{\text{FC}}^2)}{2mV_o(V_o + V_{\text{PC}} - V_{\text{FC}})(1 - e^{-2\tau_{\text{PC}}} + 1) + (1 + m)(V_{\text{PC}}^2 - V_{\text{FC}}^2)} \) | \( \frac{2CV_{\text{PC}} - C^2(V_{\text{PC}} + V_{\text{FC}} - V_{\text{DO}})}{CC_o(C + C_{\text{DO}})V_o + 2C_oV_{\text{PC}} - C_{\text{DO}}(V_{\text{PC}} + V_{\text{FC}} - V_{\text{DO}})^2} \) | <100% @any R |

open loop can be represented as the equivalent circuit shown in Fig.2. The transformer exports the ideal output voltage, the total loss of the converter is equivalent to the loss generated by average output current flowing through the output impedance, denoted as \( R_e \).

A new output impedance calculation method is derived in this paper using the critical voltages of flying capacitor and output capacitor. Assumption is made that the converters are operated under FC mode (namely DCM). The time diagram and current waveforms in a switching period are depicted in Fig.10 (a).

For RSCC, since the power loss can be expressed as:

\[
P_{\text{loss}} = f_{\text{sw}}[CV_{\text{in}}(V_{C_{\text{max}}} - V_{C_{\text{min}}}) - \frac{1}{2}C_{\text{O}}(V_{O_{\text{max}}}^2 - V_{O_{\text{min}}}^2) - \frac{2V_{O}^2}{R_L}T_d] \tag{23}
\]

The average output current is expressed as:

\[
I_{\text{out}} = f_{\text{sw}} C(V_{C_{\text{max}}} - V_{C_{\text{min}}}) \tag{24}
\]

Applying the critical voltages on capacitors, the output impedance can be derived as:

\[
R_{\text{RSCC}} = \frac{V_{N} - V_{D}}{f_{\text{sw}} C(V_{C_{\text{max}}} - V_{C_{\text{min}}})} = \frac{1}{f_{\text{sw}} C} \frac{1 - \alpha_2}{1 + \alpha_2} \tag{25}
\]

For SCC, applying the energy profile, the output impedance can be described as (26), as shown at the bottom of the next page.

Comparing (26) with (25), the only difference between the output impedance expression of RSCC and that of SCC is the charging time. Utilizing the relationship of the critical voltages on capacitors, the output impedance can be further derived:

\[
R_{\text{SCC}} = \frac{1}{f_{\text{sw}} C} \frac{1 + e^{-2f_{\text{sw}}\tau}}{1 - e^{-2f_{\text{sw}}\tau}} \tag{27}
\]

where, \( \tau \) is the time constant of each sub-circuit from SCC. The relationship between output impedance and switching frequency for RSCC is shown in Fig.10 (b) with blue solid
line for theoretical result and blue dashed line for experimental result, where the experimental result is tested based on the employed components in Table 2. The relationship between output impedance and switching frequency for SCC is shown in Fig. 10 (b) with red solid line for theoretical result and red dashed line for experimental result.

Some conclusion could be drawn from the analysis:

1) With larger output impedance, the converter conducts lower transfer efficiency. When the two-phase converter operates in DCM mode, also known as in SSL region, to get highest efficiency, the switching frequency should be set to be equal to the critical efficiency of the converter.

2) When the two types of converters operate at same switching frequency, the current of common branch path of charging and discharging circuit for both converters, denoted as $I_{RSCC}$ and $I_{SCC}$, respectively, are shown in Fig. 10 (a). SCC suffers a higher current stress due to a much smaller charging time in each phase while the current in RSCC is smoother but the charging process takes a longer time.

3) Under FC, the sub-circuits of SCC have fixed conduction loss, the high current peak can be brought down by introducing a resistor into each sub-circuit while the total transfer efficiency keeps unchanged. For RSCC, increasing of resistance has rarely influence on current waveform but will highly increase the energy loss. Therefore, for RSCC, with more reduced equivalent path resistance, the transfer efficiency will be higher. In essence, larger path resistance will kill the degree of sinusoidal and the current RMS value will rise due to its increasing waveform coefficient.

4) With smaller switching frequency, the output impedance of SCC gets larger and therefore the transfer efficiency gets lower. RSCC has smaller output impedance compared to the native SCC operating at same switching frequency. The plots reflect that to get same transfer efficiency, RSCC can be operated at a frequency that is lower than its counterpart.

### IV. EXTENDED ANALYSIS OF RSCC BASED ON BMSCC

In this paper, a 4X boost resonant bridge modular switched-capacitor converter (RBMSCC) is proposed as the extended implementation of RSCC. The topology is shown in Fig. 11 (a), including an H-bridge, which consists of switches $S_1 - S_4$, a resonant inductor $L$, two flying capacitors $C_{1a}$ and $C_{1b}$ and two output capacitors $C_{2a}$ and $C_{2b}$. The flying capacitors $C_{1a}$ and $C_{1b}$ are resonant with the inductor and their values are relatively small, denoted by $C$. The output capacitors $C_{2a}$ and $C_{2b}$ with large values are represented by $C_o$.

The driving diagram is represented in Fig. 11 (b). Switches $S_1$, $S_2$ and $S_3$, $S_4$ are driven by gate signals $V_{g1}$ and $V_{g2}$, respectively and $V_{g1}$ and $V_{g2}$ are complementary signals with duty cycle of 50%.

To realize zero current switching (ZCS), the switching frequency $f_s$ is set to be lower than resonant frequency $f_r$ and $f_r$ is calculated by

$$f_r = \frac{1}{2\pi \sqrt{LC}}$$

Typical waveforms of resonant inductor and the capacitors are shown in Fig. 11 (b) below the gate signals. There are two operation phases in a switching period as shown in Fig. 12. In phase I, $S_1$, $S_4$ are turned-on and $S_2$, $S_3$ are turned-off. There are two operation circuits as depicted in Fig. 12 (a). One loop is comprised of $V_{in}$, $C_{1a}$ and $L$, which corresponds to a SRLC circuit considering the stray resistance of circuit path; the other loop is comprised of $V_{in}$, $C_{1b}$, $C_{2b}$ and $L$, which corresponds to a SRLC circuit considering the stray resistance. In phase II, $S_2$, $S_3$ are turned-on and $S_1$, $S_4$ are turned-off. There are also two operation circuits as shown in Fig. 12 (b). One consists of $V_{in}$, $C_{1b}$ and $L$, corresponding to a SRLC circuit considering the stray resistance. The other loop consists of $V_{in}$, $C_{1a}$, $C_{2a}$ and $L$, corresponding to a SRLC circuit considering the stray resistance. The two operation phases have approximately identical processing time $T_d$, which is consistent with half of the circuit resonant period.

Due to symmetry of the operation, the capacitors can be divided into two groups: one consists of $C_{1a}$ and $C_{2a}$ and the other consists of $C_{1b}$ and $C_{2b}$. Each group of capacitors are operated as the combination of two basic sub-circuits: SRLC.

### TABLE 2. Specifications of the unite gain SCC and RSCC.

| Comp. | Parameters | Comp. | Parameters |
|-------|------------|-------|------------|
| Q1-Q2 | KIA3510A/9m Ω | C | MIPP2055J2310916L/C/2uF/14mΩ |
| $L_r$ | 3.5uH | $C_o$ | SHJL-500-40/4-40/40nF |
| $V_{in}$ | 25V | $R_L$ | 5Ω |

### FIGURE 11. RBSCC. (a) Topology (RBSCC). (b) Typical waveforms.
circuit and SRLC circuit. Group of capacitors $C_{1a}$ and $C_{2a}$ is taken as a representative to derive the efficiency of RBMSCC. The equivalent sub-circuits for this group corresponding to the phase analysis are shown in Fig 13. Since the inductor is utilized for both groups of capacitors, the equivalent inductance in the sub-circuits is $2L$. It is supposed that the output capacitor $C_{2a}$ is much larger compared to the flying capacitor $C_{1a}$. The equivalent stray resistance of two operation phases are denoted by $R_1$ and $R_2$, respectively.

According to analysis of the basic sub-circuits, the energy variation of each component during a switching period is summarized in Table 3.

In phase I, the circuit loop containing $C_{1a}$ and $C_{2a}$ is equivalent to a SRLC circuit, the energy loss in this phase is denoted by $\Delta E_{loss1}$ and can be derived according the analysis in part II:

$$\Delta E_{loss1} = CV_{in}(V_{C_{max}} - V_{C_{min}}) - \frac{1}{2}C(V_{C_{max}}^2 - V_{C_{min}}^2).$$  \hspace{1cm} (29)

In phase II, the energy loss is denoted by $\Delta E_{loss2}$:

$$\Delta E_{loss2} = C_EV_{in}(V_{in} + V_{C_{max}} - V_{C_{min}})(\alpha_2 + 1) + C(V_{C_{max}}^2 - V_{C_{min}}^2)/2 - C_O(V_{O_{max}}^2 - V_{O_{min}}^2)/2$$
$$-\frac{T_d}{4R_L}(V_{O_{max}} + V_{O_{min}})^2.$$  \hspace{1cm} (30)

Then the overall efficiency of the whole converter can be derived (31), as shown at the bottom of the page.

It is seen from formula (31) that the overall efficiency of a RBMSCC is expressed by the critical voltages of the capacitors. Other kinds of RSCC topology may consist of different sub-circuits but can be solved with the given result for each sub-circuit and the same efficiency derivation method for the whole converter. This is instructive for practical application of RSCC since a practical method is given to reveal and predict the efficiency of RSCC by calculating the critical voltages of the capacitors using the circuit parameters.

The output impedance of proposed RBMSCC can be derived utilizing the presented critical voltage calculation method. Since power loss of RBMSCC can be expressed using the energy profile:

$$P_{loss} = f_{sw}[CV_{in}(V_{C_{max}} - V_{C_{min}}) + C_EV_{in}(V_{in} + V_{C_{max}} - V_{O_{min}})(\alpha_2 + 1)$$
$$+ \frac{1}{2}C(V_{C_{max}}^2 - V_{C_{min}}^2) - \frac{1}{2}C_O(V_{O_{max}}^2 - V_{O_{min}}^2) - \frac{V_{O_{max}}}{R_L} \cdot T_d]$$  \hspace{1cm} (32)

The average output current is expressed as:

$$I_{out} = f_{sw}[C(V_{C_{max}} - V_{C_{min}}) + C_E(V_{in} + V_{C_{max}} - V_{O_{min}})(\alpha_2 + 1)].$$  \hspace{1cm} (33)

In this structure, the charge balance is expressed as:

$$C(V_{C_{max}} - V_{C_{min}}) + C_E(\Delta V_{O} + \Delta V_{C})$$
$$= C_O(V_{O_{max}} - V_{O_{min}}) + I_L \cdot T_d.$$  \hspace{1cm} (34)

Consequently, the output impedance can be derived as (35), as shown at the bottom of the next page.

Applying the critical voltages on capacitors, the output impedance can be further derived as

$$R_{RBMSCC} = \frac{1}{f_{sw}C} \frac{m}{2m(\alpha_2 + 1)}$$  \hspace{1cm} (36)

From the analysis of RBMSCC, the time-domain solution for a specific RSCC topology is completely derived, using the basic conclusion of sub-circuits, more complicated topology could be resolved.

Some suggestions on parameter design for efficiency improvement are concluded as follow:

1) There is no fixed charge-up loss as in SCC for RSCC. Therefore, to improve the efficiency, the equivalent resistance in circuit path is as smaller as better.

2) The resonant inductor functions to eliminate the current spike and takes a proportion of delivered energy. With

$$\eta_{RBMSCC} = \frac{(C + C_O)[2C_O R_L (V_{O_{max}}^2 - V_{O_{min}}^2) + (V_{O_{min}} + V_{O_{max}})^2] + T_d]}{2(C + C_O)CR_L V_{in}(V_{C_{max}} - V_{C_{min}}) + 2C_O V_{in}(V_{in} + V_{C_{max}} - V_{C_{min}})(\alpha_2 + 1)}.$$  \hspace{1cm} (31)

| Table 3. Energy variation of each component. |
|---------------------------------------------|
| Component | Phase I | Phase II |
| Source $(\text{E}_{1a})$ | $C V_{n}(V_{C_{max}} - V_{C_{min}})/2$ | $C V_{n}(V_{O_{max}} - V_{O_{min}})(\alpha_2 + 1)$ |
| $C_{1a}$ | $C V_{n}(V_{C_{max}} - V_{C_{min}})/2$ | $C V_{n}(V_{O_{max}} - V_{O_{min}})/2$ |
| $C_{2a}$ | $-(V_{O_{max}} - V_{O_{min}})^2T_d/8R_L$ | $C_O(V_{C_{max}}^2 - V_{C_{min}}^2)/2$ |
| Load $(\text{E}_{2a})$ | $(V_{O_{max}} + V_{O_{min}})^2T_d/8R_L$ | $(V_{O_{max}} + V_{O_{min}})^2T_d/4R_L$ |
larger inductance, more energy will be stored in the inductor and less energy will be consumed by the resistor and efficiency is increased. However, it will kill the power transfer capacity.

3) The parameter selection of capacitors is reflected by the flying capacitor-output capacitor correlation ratio \( m \). With decreasing of \( m \), the output impedance of RSCC decreases and hence the efficiency is improved. Nevertheless, smaller \( m \) value makes more rapid voltage vibration on output capacitor, which introduces unfavored high output voltage ripple. So \( m \) value should be properly designed to meet the requirement of high efficiency and low output ripple.

V. SIMULATION AND EXPERIMENTAL VERIFICATIONS

Hardware prototype has been implemented for proposed RBMSCC and Fig.14 provides the photograph. Full component listing and design specification is provided in Table 4. Excellent agreement between simulation and the experimental results is achieved and given in Fig.15.

Total equivalent path resistance for the prototype is found to be 60m\( \Omega \) (summation of on-state resistance of switches, ESR of the capacitors and stray resistance). Additional resistor can be inserted in both charging and discharging circuit to change the path resistance. Fig.16 (a) shows the efficiency of RBMSCC with different path resistance.

The converter switching frequency is slightly lower than the critical resonant frequency (42kHz) of the circuit. In steady-state, measured output voltage and power is 96.45V and 186.05W, input current is 7.72A. The critical voltages of flying capacitor are found to be \( V_{C_{\text{min}}} = 12.22V \) and \( V_{C_{\text{max}}} = 36.33V \), the critical voltages of output capacitor are \( V_{O_{\text{min}}} = 47.89V \) and \( V_{O_{\text{max}}} = 48.57V \). The prototype operation is consistent with the model derivation results. Measured transfer efficiency \( \eta_{\text{RBMSCC}} \) and output impedance \( R_{\text{RBMSCC}} \) are 96.44% and 1.87\( \Omega \), respectively, which is also in close proximity with the model derivation results (96.1% and 2.03\( \Omega \)).

The plot of RBMSCC efficiency against \( m \) value is shown in Fig.16 (b). The \( m \) value is changed by varying flying capacitance while keeping the output capacitance unchanged. Fig.16 (c) depicts the efficiency of RBMSCC against switching frequency (ranging 0-150kHz) and in comparison with its non-resonant type BMSCC. For BMSCC, the resonant inductor is removed from the prototype. With the switching frequency increase into FSL region, two efficiency will converge

\[
R_{\text{RBMSCC}} = \frac{V_{in} - \bar{V}_O}{f_{sw}[C(V_{C_{\text{max}}}-V_{C_{\text{min}}})+C_E(V_{in}+V_{C_{\text{max}}} - V_{O_{\text{min}}})(\alpha^2 + 1)]}
\]  

TABLE 4. Component listing and specifications of the prototype.

| Component | Parameters |
|-----------|------------|
| \( S_1-S_4 \) | KIA3510A/9m \( \Omega \) |
| \( f_{sw} \) | 40kHz |
| \( V_{in} \) | 25V |
| \( P_{out} \) | 200W |
| Nominal Conversion Ratio | 1:4 |

FIGURE 14. Photograph of prototype in test platform.

FIGURE 15. Voltage/current waveforms of RBMSCC. (a) Simulation. (b) Test.

FIGURE 16. Experimental results of RBMSCC. (a) efficiency against path resistance. (b) efficiency against \( m \) value. (c) efficiency against switching frequency for RBMSCC and BMSCC.
to a fixed value, independent of switching frequency. The results are in agreement with the analytic conclusions well.

VI. CONCLUSION
A generic and comprehensive analysis on the basic subcircuits and overall efficiency of RSCC has been presented in this paper. The charging efficiency of each sub-circuit and overall efficiency can be expressed with the critical voltages of capacitors. According to efficiency expression of each sub-circuit, the key point to improve charging efficiency is to increase the average voltage of the capacitors, $V_C$ and $V_O$.

A new calculation method of output impedance is derived, revealing the efficiency mechanism in a different perspective. The output impedance of RSCC decreases with an increasing of switching frequency, implying higher transfer efficiency.

To realize high-efficiency operation, in a practical converter, a relatively high switching frequency should be used, and relatively high ratio of inductance and equivalent resistance should be set. Comparing RSCC with SCC, reducing the equivalent path resistance is no use to improve transfer efficiency for SCC but is useful for RSCC at FC mode operation. The output impedance curve of SCC lies above that of RSCC, which means RSCC conduct a higher efficiency than SCC at the same switching frequency.

The efficiency mechanism analysis provides guidance for complex RSCCs with multiple sub-circuits to obtain high efficiency operation and RBMSS is implemented to validated the analysis.

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