Static Non-linearity in Graphene Field Effect Transistors

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Abstract—The static linearity performance metrics of the GFET transconductor are studied and modeled. Closed expressions are proposed for second and third order harmonic distortion ($H_2$, $H_3$), second and third order intermodulation distortion ($\Delta I M_2$, $\Delta I M_3$), and second and third order intercept points ($A_{I I P2}$, $A_{I I P3}$). The expressions are validated through large-signal simulations using a GFET VerilogA analytical model and a commercial circuit simulator. The proposed expressions can be used during circuit design in order to predict the GFET biasing conditions at which linearity requirements are met.

Index Terms—GFET, non-linearity, RF circuit.

I. INTRODUCTION

GRAPHENE based field effect transistors (GFETs) are nowadays considered as a technology option for future high-speed RF circuits and systems. Performance metrics such as high intrinsic transit frequency $f_T$ and transconductance gain $g_m$ have shown very competitive performance when compared to similarly sized devices of other technologies [1], [2], [3]. Another key performance metric that is important in RF systems and that must be carefully characterized in GFETs is the linearity.

RF circuits must process weak signals in the presence of strong interference; therefore, they must exhibit high linearity performance. Non-linearities in the RF circuits are the source of several undesirable effects such as harmonic distortion, gain compression, intermodulation, cross-modulation, AM/PM conversion, DC offsets, etc. [4]. Therefore, it is of paramount importance to study and characterize the intrinsic non-linearities of the GFET devices. Initial measurements of linearity of GFETs have shown that is possible to achieve good linearity performance [5]. However, an analytic study that allows to identify the GFET linearity under different design parameters and biasing conditions is required.

Fig. 1 shows the small-signal representation of the GFET. The small-signal representation assumes that the components are linear. However, the capacitances $C_{gs}$, $C_{gd}$, transconductance $g_m$, and output resistance $r_o$ are in fact non-linear components. The capacitors are storage elements which exhibit memory effects. Their non-linearity is dynamic and as can be expected, its effect is more visible at high frequencies. The parameters $g_m$ and $r_o$ have a memoryless behavior and therefore their non-linearities are static. The effect of the non-linearity of $r_o$ depends mainly on the loading conditions at the drain of the device. In most common cases, there are impedances smaller than $r_o$ loading the drain. Therefore, the impact of the non-linearities of $r_o$ is generally reduced. The non-linearity of $g_m$, on the other hand, can not be reduced unless negative feedback is intentionally applied at the expense of noise and gain degradation. The non-linearity of $g_m$, in fact, places a fundamental limit on the total non-linearity of the device. This paper introduces closed expressions for the second and third order static non-linearity of $g_m$ which are the main concerns in RF applications.

II. TRANSCONDUCTANCE NON-LINEARITY

The static non-linearity at the drain current can be approximated by using a Taylor expansion polynomial:

$$I_D = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + \ldots + a_n v_{in}^n(t) \quad (1)$$

where $I_D$ is the drain current, and $v_{in}$ is an input voltage signal at the gate. The first three coefficients $(a_1, a_2, a_3)$ generally dominate the non-linearities for small signals. Higher order terms appear when the input signals are large enough so that the device leaves the saturation region and stops acting as an amplifier. This condition is known as clipping and can be avoided by ensuring proper signal levels at the input. The first terms can be found by differentiating (1) and solving for the unknown coefficients:

$$a_1 = \frac{\delta I_D}{\delta v_{in}} \bigg|_{v_{in}=0}, \quad a_2 = \frac{1}{2} \frac{\delta^2 I_D}{\delta v_{in}^2} \bigg|_{v_{in}=0}, \quad a_3 = \frac{1}{6} \frac{\delta^3 I_D}{\delta v_{in}^3} \bigg|_{v_{in}=0} \quad (2)$$

The drain current in GFETs can be expressed as [6]:

$$I_D = \mu WC_{TOP} \left( V_{eff} - V_{DS1}/2 \right)$$

$$L/V_{DS1} + \frac{\mu}{2} \sqrt{\pi C_{TOP}/e} \sqrt{V_{eff} - V_{DS1}/2} \quad (3)$$

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where \( \mu \) is the mobility, \( W \) the transistor width, \( L \) the transistor length, \( C_{TOP} \) is the top oxide capacitance density, \( e \) the elementary charge, \( \omega \) is obtained from the surface phonon energy of the substrate \( h\omega \), and \( V_{eff} = V_{GSI} + V_{TH,0} \). The zero bias threshold voltage \( V_{TH,0} = eN_f/C_{TOP} \) accounts for the shift in the Dirac point due to the doping level \( N_f \). Equation (3) is valid for the first triode and saturation/negative resistance regions when \( V_{eff} > V_{DSi}/2 \) and \( \Delta^2/\pi^2 e_f^2 \ll \pi|Q\eta_{AV}|/e \). By performing several substitutions, (3) can be expressed as:

\[
I_D = \frac{A x}{L/V_{DSi} + B \sqrt{x}}
\]

where \( A = \mu W C_{TOP} \), \( B = \frac{\mu}{2} \sqrt{\pi C_{TOP}/e} \), and \( x = V_{eff} - V_{DSi}/2 \). The coefficients \( a_1 \) to \( a_3 \) are found by taking derivatives of (4) with respect to the variable \( x \) (\( \delta x = \delta V_{eff} = \delta V_{GSI} \), and replacing the results in (2). Accordingly, the polynomial coefficients are:

\[
a_1 = \frac{AV_{DSi} (2L + BV_{DSi} \sqrt{x})}{2 (L + BV_{DSi} \sqrt{x})^2}
\]

\[
a_2 = -\frac{AV_{DSi} (B^2V_{DSi} x + 3BLV_{DSi} \sqrt{x})}{8x (L + BV_{DSi} \sqrt{x})^3}
\]

\[
a_3 = \frac{AV_{DSi} (L^2 + BL^2 + BV_{DSi} x + 4BLV_{DSi} \sqrt{x})}{16x^{3/2} (L + BV_{DSi} \sqrt{x})^4}
\]

Once (5), (6), and (7) are substituted in (1), the resulting polynomial depends only on technology parameters and biasing voltages, and can be used to calculate the harmonic and intermodulation distortion of GFET devices.

### A. Second and Third Harmonic Distortion

The second and third order harmonic distortion levels \( (HD_2 \) and \( HD_3 \)) produced by a single input tone \( v_m \cos (\omega_1 t) \) are found by calculating the ratio of the output currents at the harmonics frequencies \( (2\omega_1, 3\omega_1) \) to the output current at the fundamental frequency \( \omega_1 \). The second harmonic distortion is given by:

\[
HD_2 = \left| \frac{a_2}{a_1} \right| v_m
\]

\[
HD_2 = \frac{v_m L^2}{4x (L + BV_{DSi} \sqrt{x}) (2L + BV_{DSi} \sqrt{x})} - \frac{v_m}{8x}
\]

The third harmonic distortion is:

\[
HD_3 = \left| \frac{a_3}{a_1} \right| v_m^2
\]

\[
HD_3 = \left( \frac{BV_{DSi} (x^2V_{DSi}^3 + L^2)}{32x^{3/2}} + \frac{B^2LV_{DSi}^2}{8x} \right) \left[ (L + BV_{DSi} \sqrt{x})^2 (2L + BV_{DSi} \sqrt{x}) \times v_m^2 \right]
\]

### B. Intermodulation Distortion

The second order intermodulation distortion \( (\Delta IM_2) \) produced by two input tones \( v_m \cos (\omega_1 t) \) and \( v_m \cos (\omega_2 t) \) is found by calculating the ratio of the output intermodulation product at \( \omega_1 \pm \omega_2 \) to the output at any of the fundamental frequencies \( (\omega_1, \omega_2) \):

\[
\Delta IM_2 = \left| \frac{a_2}{a_1} \right| v_m
\]

\[
\Delta IM_2 = \frac{v_m L^2}{2x (L + BV_{DSi} \sqrt{x}) (2L + BV_{DSi} \sqrt{x})} - \frac{v_m}{4x}
\]

The third order intermodulation distortion \( (\Delta IM_3) \) produced by two input tones \( v_m \cos (\omega_1 t) \) and \( v_m \cos (\omega_2 t) \) is found by calculating the ratio of the output intermodulation product at \( (2\omega_1 - \omega_2, 2\omega_2 - \omega_1) \) to the output at any of the fundamental frequencies \( (\omega_1, \omega_2) \):

\[
\Delta IM_3 = 3 \left| \frac{a_3}{a_1} \right| v_m^2
\]

\[
\Delta IM_3 = \left( \frac{BV_{DSi} (x^2V_{DSi}^3 + L^2)}{32x^{3/2}} + \frac{B^2LV_{DSi}^2}{8x} \right) \left[ (L + BV_{DSi} \sqrt{x})^2 (2L + BV_{DSi} \sqrt{x}) \times v_m^2 \right]
\]

### C. Second and Third Order Intercept Points

While the \( HD_2, HD_3, \) \( \Delta IM_2, \) and \( \Delta IM_3 \) allow quick estimations of the distortion levels for a given input voltage \( v_m \), they are not suitable as figures of merit for comparing the linearity performance. These comparisons are normally done using the so-called second and third order intercept points \( (A_{IIP2}, A_{IIP3}) \). The \( A_{IIP2} \) is defined as:

\[
A_{IIP2} = \left| \frac{a_1}{a_2} \right|
\]

\[
A_{IIP2} = 4x + \frac{8L^2 \sqrt{x}}{BV_{DSi} (3L + BV_{DSi} \sqrt{x})}
\]

The \( A_{IIP3} \) is defined as:

\[
A_{IIP3} = \sqrt{\frac{4 \left| a_1 \right|}{3 \left| a_3 \right|}}
\]

\[
A_{IIP3} = \sqrt{\frac{32x^{3/2} (L + BV_{DSi} \sqrt{x})^2 (2L + BV_{DSi} \sqrt{x})}{3BV_{DSi} (L^2 + B^2V_{DSi}^2 x + 4BLV_{DSi} \sqrt{x})}}
\]
D. Validation of Linearity Expressions

The best way to validate the proposed linearity expressions is to compare the linearity metrics calculated by using these expressions with linearity measurements on GFET devices. When such measurements are unavailable, an alternative approach is to estimate these linearity metrics by performing large-signal time-domain transient simulations using transistor models. A caveat of this approach is that the accuracy of these estimations depends on how accurate the transistor model is. In this work, linearity metrics are estimated by performing large-signal simulation using a commercial circuit simulator (Cadence Spectre) and the GFET Verilog-A model from [7]. This model has been successfully used and verified by using measurements of differently sized GFETs fabricated by different groups. The test device is a 440 nm length, 1 µm width GFET from [8]. The model parameters are \( N_T \approx 0 \) (\( V_{TH,0} \approx 0 \) V), \( \varepsilon_r = 3.5 \), \( T_{OX} = 8.5 \) nm (\( C_{TOP} = 3.6 \times 10^{-3} \text{F/m}^2 \)), \( \mu = 7000 \) cm\(^2\)V\(^{-1}\)s\(^{-1} \), \( \Delta = 66.8 \) meV, and \( h\omega = 56 \) meV. The GFET is biased at \( V_{DS} = 0.4 \) V and \( V_{GS} = 1.5 \) V. Single and two-tone periodic-state simulations are performed in order to obtain the harmonic content of the drain current. The amplitude of the input signals \( v_m \) is set at 20 mV. The frequency of the input signal for the single-tone test is 1 kHz while the frequencies for the two-tone test are 10 kHz and 11 kHz.

Fig. 2 and Fig. 3 show the simulated spectrum content of the drain current for the single-tone and two-tone tests, and the simulated and calculated distortion levels. It can be seen that the calculated values of \( HD_2 \), \( HD_3 \), \( \Delta IM_2 \), and \( \Delta IM_3 \) predict very accurately the simulated distortion levels. The simulated second and third order intercept points are found by using the expressions \( A_{IIP2,\text{sim}}(dBV) = 20\log_{10}(v_m) + |M_{2,\text{sim}}(dB)| \), and \( A_{IIP3,\text{sim}}(dBV) = 20\log_{10}(v_m) + |M_{3,\text{sim}}|/2(dB) \). Table I shows a summary of the calculated and simulated linearity metrics. In addition, the table shows simulated linearity metrics for an equally sized NMOS device (440 nm length, 1 µm width) which was biased at the same \( V_{DS} \) and \( V_{GS} \) voltages as the test GFET. The NMOS device belongs to a 0.15 µm CMOS commercial process and these metrics were extracted using the same large-signal simulations in Cadence Spectre. It can be appreciated that the GFET device outperforms the MOS device under similar conditions. This is a very encouraging result that shows the potential of GFET devices for highly-linear RF circuits.

| Technology | Calculated | Simulated | Simulated |
|------------|------------|-----------|-----------|
| HD\(_2\)   | -55.6 dB   | -57 dB    | -45.7 dB  |
| HD\(_3\)   | -105 dB    | -108 dB   | -96.7 dB  |
| \( \Delta IM_2 \) | -49.6 dB | -51 dB    | -39.7 dB  |
| \( \Delta IM_3 \) | -95.5 dB  | -96.1 dB  | -87.2 dB  |
| \( A_{IIP2} \) | 15.7 dBV  | 17 dBV    | 5.7 dBV   |
| \( A_{IIP3} \) | 13.8 dBV  | 14 dBV    | 9.6 dBV   |

III. Conclusions

This paper has presented analytical expressions for the GFET transconductance non-linearity, which is the main source of distortion. The proposed expressions can be efficiently used to predict the linearity performance metrics of GFETs under different technology parameter values and biasing conditions. These expressions enable to perform comparisons of linearity performance of GFETs with other transistor technologies. As an example, a linearity comparison between a GFET and a CMOS device was performed. The comparison shows that the GFET outperforms its similarly sized CMOS counterpart. Therefore, GFET devices can potentially be used to design highly-linear RF circuits.

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