Transient Stability Assessment for Current Constrained and Unconstrained Fault Ride-Through in Virtual Oscillator Controlled Converters

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Abstract—Unified virtual oscillator controller (uVOC) inherits the rigorous analytical foundation offered by oscillator based grid-forming (GFM) controllers and enables fast over-current limiting and fault ride-through (FRT). Control design for effective FRT requires transient stability analysis. Existing transient stability analysis methods and studies are limited in either considering only current unconstrained scenarios or neglecting the simultaneous power angle and voltage dynamics. Under current-constrained faults, the voltage and power angle dynamics are strongly coupled and both play critical roles in determining transient stability. Therefore, decoupled analysis of the two, typically used in transient stability studies, does not offer comprehensive insight into the system dynamics. In this work, the overall FRT method for uVOC is presented and a comprehensive modeling and analysis method for transient stability is developed under both current-saturated and unsaturated symmetrical AC faults. We utilize phase-plane analysis of the overall system in a single graphical representation to obtain holistic insights into the coupled voltage and power angle dynamics. The FRT controller and the analysis method have been validated through simulations and hardware experiments. The results demonstrate that uVOC is not constrained by a critical clearing angle unlike droop and virtual synchronous machine (VSM) type second order controllers.

Index Terms—Transient stability, unified virtual oscillator control (uVOC), virtual oscillator control (VOC), grid forming converter, fault ride-through, critical clearing angle, current saturation

I. INTRODUCTION

Unified virtual oscillator control (uVOC) provides a unified analysis, design, and control implementation framework for both grid-forming (GFM) and grid-following (GFL) converters [1]. The GFM operation of uVOC leverages the rigorous analytical foundation developed for dispatchable virtual oscillator control (dVOC) [2]-[5]. In GFL applications, bidirectional power flow control and DC bus voltage regulation is achieved. In all modes of operation, no phase-locked-loop (PLL) is required which enables to circumvent the synchronization issues associated with PLLs under weak grid conditions. Moreover, fast over-current limiting and fault ride-through (FRT) is obtained without the need for switching to a back-up controller during fault.

Implementation of over-current limiting control in GFM converters remains an open research problem till date [6]. In GFM control structures employing cascaded voltage and current tracking loops, explicit current limiters on the current references offer the most intuitive solution; however, such limiters lead to saturation and eventual instability in the outer synchronization loops such as the active and reactive power control loops [7]. Instead of imposing explicit current limits, virtual impedance for current limiting has been proposed [8]. As an alternative, droop controller considering current limits were proposed in [9], [10]. Explicit current limiters along with a dynamic virtual resistance was proposed in [11]. Contrarily, uVOC is a nonlinear time-domain controller which does not employ inner voltage and current tracking loops. Unlike droop based methods, uVOC includes current reference generation in the synchronizing oscillator, which facilitates imposing explicit current limiters without saturating the synchronization loop [1]. However, transient stability analysis is required for control design to achieve effective FRT.

Transient stability is defined as the ability of converters to maintain synchronism with the utility grid when subjected to a major grid disturbance [12]. For instance, a voltage source converter may experience a sudden large voltage sag due to an upstream AC fault. Extensive research on transient stability for PLL based GFL converters were reported in [13], [14]. Transient stability of droop and/or virtual synchronous machine (VSM) based grid forming converters were reported in [15]-[18]. For ease of analysis and modelling most transient stability studies ignore the converter current limit imposed by hardware capability [15]-[17]. In [19], transient stability of dVOC is studied ignoring converter current limits. Critical clearing angle (CCA) defines a characteristic limitation of second order controllers emulating virtual inertia such as droop controllers and VSM [15]; synchronization stability is lost if a fault without an equilibrium is not cleared before the power angle exceeds the CCA. Due to its first order nature, dVOC was shown to be unconstrained by such a CCA under current unsaturated faults [19]. However, most severe fault events cause current saturation which leads to significantly distinctive dynamic response from that under current-saturated conditions. Moreover, power angle (δ) dynamics and voltage (V) dynamics are typically studied separately; for instance, δ − δ plots are used in most transient stability studies [15]-[19]. In addition, separate V − δ curves are used, where the voltage dynamics V is implicit. Consequently, such analyses does not provide comprehensive insight into the overall system dynamics. Evidently, the state-of-the-art lacks effective analysis method for transient stability assessment of...
oscillator based controllers.

The key contributions of this work are twofold: Introduction of a convenient phase-plane analysis based graphical method using $\dot{x} - x$ surfaces which incorporates both $V$ and $\delta$ dynamics in a single three-dimensional figure; and development of a comprehensive modelling and analysis methodology for assessing transient stability of uVOC based converters under both current-constrained and unconstrained fault conditions by leveraging the $\dot{x} - x$ surfaces. The rest of the paper is organized as follows: First, uVOC structure with FRT features is presented. Second, illustrative examples of current-saturated and unsaturated faults are presented and subsequently dynamic models are developed for both conditions. Third, the $\dot{x} - x$ surfaces are introduced. Fourth, experimental results are presented to validate the modelling, methodology, and analysis.

Figure 1. A uVOC based VSC under an upstream AC fault.

II. CONVERTER AND CONTROL STRUCTURE

A VSC equipped with an LCL filter employing uVOC is depicted in Fig. 1 whereas the uVOC structure is shown in Fig. 2. The identical uVOC controller structure is used for FRT as well. Although uVOC can be configured to operate in both grid-forming and grid-following modes under normal conditions, in this work only the grid-forming operation with real power vs. frequency and reactive power vs. voltage droop is considered for brevity. Additionally, only symmetrical faults are considered. The transient response of the system under extreme grid events such as an upstream fault is of interest for proper design of the controller to achieve effective FRT. To emulate such faults of varying severity while looking into the point of coupling (PoC), the electrical network is modelled with a fault through an impedance $Z_f$ (see Fig. 1). Any such fault leads to a fast and proportionate voltage drop at the PoC leading to a large-signal response by the VSC. Prior to delving into the transient stability assessment, the controller structure is briefly outlined in the following subsection.

A. Controller (uVOC) Structure

uVOC is a nonlinear time-domain controller implemented in the stationary $\alpha\beta$ reference frame. In the analysis that follows, boldface notation is used to indicate space vectors in $\alpha\beta$ frame; complex vector and column vector notations such as $\mathbf{i} = [i_1 \ i_2]^T \leftrightarrow [i_1 \ i_2 \ i_3]^T$, are used interchangeably. As shown in Fig. 2, uVOC is the first order controller and the controller state $\mathbf{v}$ is updated following the control law given as

$$\dot{\mathbf{v}} = j\omega_0 \mathbf{v} + j\eta(\mathbf{i}_{0,\text{sat}} - \mathbf{i}) + \mu(V_0^2 - \|\mathbf{v}\|^2)\mathbf{v},$$

where $j = \sqrt{-1}$ denotes the imaginary unit and $\|\mathbf{v}\| = \sqrt{v_1^2 + v_2^2}$ denotes Euclidean norm; $\omega_0$ and $V_0$ denote the nominal set-points for system frequency and the L-N peak voltage, respectively. Note that $V_0 = \sqrt{2}V_g$, where $V_g$ denotes the corresponding L-N root-mean-square (RMS) value and such notation is followed for other variables throughout the rest of the paper. The voltage magnitude correction gain and synchronization gains are denoted as $\mu$ and $\eta$, respectively. The converter-side current $i_1 = [i_{1,a} \ i_{1,b} \ i_{1,c}]^T$ or the grid-side current $i_2 = [i_{2,a} \ i_{2,b} \ i_{2,c}]^T$ can be used as the converter output current feedback $\mathbf{i}$ for uVOC implementation. Following the instantaneous power theory, the current reference $\mathbf{i}_0$ is generated as

$$\mathbf{i}_0 = \frac{2(P_0 - jQ_0)\mathbf{v}}{N\|\mathbf{v}\|^2},$$

where $P_0$ and $Q_0$ denote the references/set-points for real and reactive power, respectively and $N = 1$ or $N = 3$ is used for single-phase and three-phase applications, respectively.

B. Current-Constrained Operation

The VSC enters current-constrained operation once the converter output current $\|\mathbf{i}\|$ exceeds an over-current threshold

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Figure 2. uVOC structure - (a) controller implementation, (b) fault management sub-system generates two signals $x_f$ and $x_r$ which are used for transitioning between normal and current-constrained modes of operation.
\(\hat{I}_T\), which may be caused by a fault or severe voltage-sag on the grid side. The current-limiting subsystem, shown in Fig. 2(b), generates and latches a control signal \(x_f\) once such an over-current event is detected. Once the terminal voltage magnitude \(|\nu_{PoC}|\) returns above the under-voltage threshold \(V_T\), \(x_f\) is cleared and the controller resumes normal operation. Another control signal \(x_r\) is generated following \(x_f\); \(x_r\) is ramped down over the duration of \(t_F\) to facilitate smooth transition from current-constrained to normal operation.

For effective FRT under current-constrained condition, two key objectives must be achieved:

1) **Fast Over-Current Limiting:** The converter output current must be limited without saturating/destabilizing the synchronizing loop. The oscillator dynamics given by (1) achieves power synchronization though an instantaneous droop response (1), which must be unaffected by the current limiting operation. Fortunately, uVOC uses explicit current references in its synchronization structure. Therefore, a circular saturation/limiter can be directly incorporated in the synchronization controller as

\[
i_{0,\text{sat}} = \begin{cases} i_0, & |i_0| \leq \hat{I}_m \\ i_0 \times (\hat{I}_m/|i_0|), & \text{otherwise} \end{cases}
\]

where \(\hat{I}_m\) denotes the maximum allowable current constrained by the converter hardware. In Section IV-B, the circular limiter is shown to enable retention of the instantaneous droop response under current constrained operation. However, the oscillator dynamics is not typically fast enough to enable fast current limiting; an active resistance \(R_0\) is used on the current error \((i_{0,\text{sat}} - i)\) for faster current limiting response. As can be seen in Fig. 2, the synchronization gain \(\eta\) serves as a complex integral gain on the current error and the integral action can be augmented by raising the gain as \(\eta = \eta_0(1+x_r/\tau_f)\), where smaller \(\tau_f\) leads to faster settling time.

2) **Feasibility Constraint:** The voltage magnitude correction term in (1), tends to restore the nominal voltage magnitude which may not be feasible in case of severe grid faults/voltage sags under current constrained operation. The feasibility constrain can be explained using a simplified system model. For clarity and ease of analysis, the system shown in Fig. 1 can be simplified into an equivalent representation shown in Fig. 3. In the frequency range of interest for transient stability assessment, the control-computation delay, effect of the PWM, and the filter capacitor \(C_f\) can be ignored [1], [15], [20]. The converter-side and grid-side inductors and the corresponding parasitic resistances are combined into \(Z_{12} = s(L_1 + L_2) + R_1 + R_2\). The grid/rest of the network can be modelled by a Thevenin equivalent. The grid impedance \(Z_{g1}\) and \(Z_{g2}\), location of the fault, and the impedance \(Z_f\) (see Fig. 1) result in the equivalent source \(v_{TH}\) and equivalent impedance \(Z_{TH}\), seen by the VSC while looking into the PoC. By varying the equivalent source and impedance, faults of varying severity can be emulated in the analysis and during experiments.

To illustrate the feasibility constraint, we consider a grid fault with \(v_{TH} = 0.5\) p.u. and \(Z_{TH} = 0.1\) p.u.; the converter terminal voltage cannot be regulated to larger than \(0.62\) p.u. if the output current is constrained at \(1.2\) p.u. during the fault.

Such physical limits must be respected during FRT. Therefore, the voltage magnitude correction gain is parameterized as \(\mu = (1-x_r)\mu_0\), which disables the magnitude correction term under current constrained operation. Unlike droop control or VSM, no inner voltage or current reference tracking loops are used in uVOC; the uVOC output \(v_r\), given as

\[v_r = v + R_0(i_{0,\text{sat}} - i) - Z_v(s)i,\]

is used directly by the pulse-width-modulator (PWM). The virtual impedance \(Z_v(s)\) is used for stabilization of the oscillator [1] and harmonic voltage/current compensation [21], [22].

### III. Faults Under Current-Constrained and Unconstrained Conditions

Potential fault events can be classified into two categories - faults under unsaturated current conditions and those under saturated current conditions. To illustrate how a fault may occur without exceeding the converter current limit, first, we briefly review the droop characteristic of uVOC given as

\[
\dot{V} = 2\mu V(V_0^2 - V^2) + \frac{\eta}{\sqrt{\omega}}(Q_0 - Q),
\]

\[
\omega = \omega_0 + \frac{\eta}{\sqrt{\omega}}(P_0 - P),
\]

where \(V = \sqrt{2}/\omega V^2\) and \(P\) and \(Q\) denote the real and reactive power output, respectively. The detail derivation can be found in (5). Evidently, the controller exhibits \(V - Q\) and \(P - \omega\) droop response. In an event of a voltage sag caused by an upstream fault, the controller increases its reactive power output to reduce the voltage deviation from the nominal set-point \(V_0\). Based on the severity of the fault and other operating conditions such as grid frequency and power set-points \(P_0\) and \(Q_0\), the converter may reach steady-state without reaching the over-current limit. In such cases, the converter does not enter the current-constrained operation marked by \(x_f = x_r = 1\). However, in case of more severe faults, the converter may enter current-constrained operation. To illustrate the effect of such fault events, we consider a system described in Appendix A.

Examples of two types of faults are described in the following subsections.

#### A. Case I: Current-Unconstrained Fault

A simulated grid fault under current unconstrained condition for a three-phase VSC is shown in Fig. 4; the simulation is performed using detailed switching model in PLECS Stan- dalone platform. The equivalent grid impedance is taken as \(Z_{TH} \approx 0.52\) p.u. with a reactance-to-resistance \((X/R)\) ratio of 20 which gives a short-circuit ratio (SCR) of \(\approx 1.9\). The power references are set as \(P_0 = 0.38\) p.u. and \(Q_0 = 0\); a fault is emulated by introducing a step voltage sag from \(v_{TH} = 1\) p.u. to \(v_{TH} = 0.6\) p.u. (see Fig. 5). Due to
its grid-forming nature, the converter increases its reactive power output which is reflected in the output current, i.e., \( i_2 \) increases to 0.63 p.u.; consequently, the PoC voltage is raised to 0.92 p.u.. The converter output current \( i_2 \) does not exceed the current limit \( I_m \) = 1.2 p.u. during the initial overshoot as well as when steady-state is reached.

**B. Case II : Current-Constrained Fault**

To model a more severe fault, grid impedance of \( Z_{TH} = 0.1 \) p.u. is considered. The current-limiting subsystem, shown in Fig. 2(b), is disabled and the circular limiter, shown in Fig. 2(a), is excluded to illustrate how the converter would respond without any current-limit constrains. The power references are set as \( P_0 = 0.27 \) p.u. and \( Q_0 = 0 \). Now the fault is emulated by a step change from \( v_{TH} = 1 \) p.u. to \( v_{TH} = 0.5 \) p.u.; although the PoC voltage is raised to 0.7 p.u., the output current goes through a large transient exceeding the maximum limit \( I_m \) and settles at \( i_2 \approx 2 \) p.u. > \( I_m \). Evidently, the current-limit is exceeded by the initial overshoot. Without an effective current-limiting and FRT controller, the VSC must disconnect from the grid/electrical network under such fault conditions to protect the hardware. Therefore, an appropriate FRT controller needs to be implemented and comprehensive transient stability analysis is required for the design of the FRT controller. The current-limiting subsystem and the circular limiter block are responsible for clamping the output current at \( I_m \), once such an over-current is detected.

The converter and the control system exhibit distinctly different dynamic responses for the two different cases. Effective FRT requires proper analysis and design for transient stability of the system in both cases. In the following section, dynamic models are developed for such analyses.

**IV. Dynamic Model**

Without loss of generality, the dynamic model is developed in a synchronous reference frame rotating at the grid frequency \( \omega_g \) and aligned with the equivalent grid voltage \( v_{TH} = \sqrt{2}V_{TH}e^{j\omega_g} \).

**A. Current-Unconstrained Operation**

During current-unconstrained operation, the active resistance is disabled and \( \mu \neq 0 \), and \( i_{0,\text{sat}} = i_0 \). The voltage magnitude and angle dynamics, given by (5), can be obtained in the synchronous reference frame as

\[
\begin{align*}
\dot{V} & = 2\mu V(V_0^2 - V^2) + \eta \frac{V}{N}(Q_0 - Q), \\
\dot{\delta} & = \omega_g - \frac{V}{N^2} (P_0 - P),
\end{align*}
\]

(6)

where \( \int \omega dt = \omega_g t + \delta \). Note that \( \delta \) is termed as the so-called power angle. The dynamics of the converter output current \( i_{d0} = i_d + ji_q \leftrightarrow \sqrt{2}(I_d + jI_q) \) in the synchronous frame can be derived as

\[
\begin{bmatrix}
\dot{I}_d \\
\dot{I}_q
\end{bmatrix} = 
\begin{bmatrix}
\frac{-B_e}{L_e} & \omega_g \\
-\omega_g & \frac{-B_q}{L_q}
\end{bmatrix}
\begin{bmatrix}
I_d \\
I_q
\end{bmatrix} + \frac{1}{L_e} \begin{bmatrix}
V \cos(\delta) - V_{th} \\
V \sin(\delta)
\end{bmatrix}.
\]

(7)

Here, the equivalent resistance \( R_e = R_a + R_1 + R_2 + R_{TH} \) and the equivalent inductance \( L_e = L_a + L_1 + L_2 + L_{TH} \), whereas the virtual impedance \( Z_v(s) \) (see Fig. 2) is implemented as

\[
Z_v(s) = \frac{R_{e0}}{s/\omega_b + 1} + x_r \frac{8L_{e0}}{s/\omega_b + 1}.
\]

(8)

The bandwidth \( \omega_b \) is selected so as to avoid amplification of high-frequency noise. Due to the limited bandwidth \( \omega_b \), the effective virtual impedances differ from \( L_{e0} \) and \( R_{e0} \) and can be determined as \( L_e \approx \text{Im}\{Z_v(j\omega_0)\} \) and \( R_e \approx \text{Re}\{Z_v(j\omega_0)\} \). Note that the virtual inductor is not typically required during normal operation but rather used for limiting the current overshoot during the initial fault instants and fault-clearing.

The first-order filter corresponding to the virtual inductance in (5) is updated by the digital controller irrespective of mode of operation but the filter output is used with the scaling of \( x_r \). Setting \( \dot{I}_d = 0, \dot{I}_q = 0 \) and taking \( X_e = \omega_b L_e \), the output current components are obtained and the real and reactive power outputs are derived as

\[
\begin{align*}
P &= N[V^2 R_e - VV_{TH} (R_e \cos(\delta) - X_e \sin(\delta))] \\
Q &= N[V^2 X_e - VV_{TH} (X_e \cos(\delta) + R_e \sin(\delta))].
\end{align*}
\]

(9)
Evidently, the power synchronization mechanism is retained and angle dynamics can be derived as
\[ \dot{\delta} = \omega_0 - \omega_\gamma + \frac{\eta}{NV^2} \left( \frac{NVIm}{S_0}Q_0 - Q \right) \] (11)

The real and reactive power outputs are obtained as
\[ P = \frac{N}{R_e^2 + X_e^2} \left[ V^2R_e - VVR_T \{ R_e \cos(\delta) - X_e \sin(\delta) \} \right] \]
\[ + (VVR_0I_m/S_0) \{ R_eP_0 - X_eQ_0 \} \]
\[ Q = \frac{N}{R_e^2 + X_e^2} \left[ V^2X_e - VVR_T \{ X_e \cos(\delta) + R_e \sin(\delta) \} \right] \]
\[ + (VVR_0I_m/S_0) \{ X_eP_0 + R_eQ_0 \} \] (15)

V. TRANSIENT STABILITY ASSESSMENT

In [15], for transient stability analysis of droop based converters \( \delta - P \) and \( V - \delta \) curves are used where the voltage dynamics \( \dot{V} \) is implicit and the system equilibrium points over \( V - \delta \) distribution cannot be determined through the graphical analysis. uVOC also exhibits dynamic behavior in both the power angle \( \delta \) and the voltage magnitude \( V \), as shown by (6) and (11). Consequently, \( \dot{\delta} - \delta \) and/or \( V - \delta \) curves do not show a holistic response of the system and hence are not sufficient for transient stability assessment of uVOC. Therefore, for a comprehensive analysis we adopt superimposed three-dimensional plots of \( \dot{\delta} \) and \( \dot{V} \) over the distribution of \( V \) and \( \delta \), denoted as \( \dot{x} \) and \( \delta \) surfaces henceforth.

A. Case I : Current-Unconstrained Fault

First, we consider the current-unconstrained fault described in Section III-A. The \( \dot{x} \) surfaces at pre-fault condition are shown in Fig. 6. The \( \dot{x} \) surfaces are generated evaluating the time-derivatives \( \dot{\delta} \) and \( \dot{V} \) using (6) over the two-dimensional distribution of \( \delta \) and \( V \). For a clear graphical representation, the derivative values are normalized by their respective absolute maximum values over the whole \( \delta - V \) distribution. Evidently, a unique equilibrium point, marked as \( a \), is found at the intersection of \( \dot{\delta} = 0 \) and \( \dot{V} = 0 \).
curves. The small signal-stability of the equilibrium point $a \equiv (\delta_a, V_a)$ can be readily evaluated graphically through inserting small perturbation; for instance, while the operating point is perturbed slightly to some power angle $\delta < \delta_a$, the derivative of power angle becomes positive, i.e., $\dot{\delta} > 0$ and consequently the operating point moves back towards $a$. Conversely, small increase in the power angle as $\delta > \delta_a$, makes the power angle derivative $\dot{\delta} < 0$ which eventually forces the operating point to move back towards $a$. Similarly, the small signal stability along the $V$-axis can be verified.

Next, when a sudden voltage sag is introduced in the equivalent grid source from $v_{TH} = 1$ p.u. to $v_{TH} = 0.6$ p.u., as described in Section III-A, the resulting $\dot{x} - x$ surfaces are depicted in Fig. 7(a). The corresponding zoomed-in view of the system trajectory, i.e., the movement of the system operating point, is shown in Fig. 7(b). The system trajectory is obtained through time-domain numerical solution of the system model given by (6) and (13); the ode45 solver [23], based on the Dormand-Prince (4,5) pair [24], was used in MATLAB to obtain the system trajectory.

At the instant of the fault, the power angle $\delta$ and the voltage $V$ remain at the pre-fault equilibrium $(\delta_a, V_a)$, but the derivatives move to their respective $\delta$ and $V$ surfaces arriving at $b$ and $c$, respectively. The derivatives move along their respective surfaces and eventually reach a new equilibrium $\delta$. The movement of the system trajectory and the equilibrium points at pre-fault and fault conditions match identically with simulated results shown in Fig. 4. Similar analysis can be performed for the transient response during fault-clearing which has been excluded in the interest of space.

B. Case II : Current-Constrained Fault

The $\dot{x} - x$ surfaces at the pre-fault condition for Case II described in Section III-B are depicted in Fig. 8(a); a stable and unique equilibrium $a \equiv (\delta_a, V_a)$ is observed. The corresponding simulated response is shown in Fig. 8(b).

Next, a step change from $v_{TH} = 1$ p.u. to $v_{TH} = 0.5$ p.u. causes a fault condition which leads to over-current beyond $I_m$. However, unlike Section III-B the full controller shown in Fig. 2(a) and (b) including the circular current limiter and the fault-management subsystem is employed. Furthermore, once a fault is detected, the reactive power set-point is increased as $Q_0 = \sqrt{S_1^2 - P_1^2}$ to leverage the remaining current capability of the converter to raise the terminal voltage. The corresponding $\dot{x} - x$ surfaces and the zoomed-in view of the system trajectory are shown in Fig. 8(c). Immediately at the fault instant, the system operating point stays at the pre-fault equilibrium $a \equiv (\delta_a, V_a)$. Subsequently, the derivatives $\dot{\delta}$ and

![Figure 8. Phase-plane analysis and simulated response for current-constrained fault (Case II) - (a) normalized $\dot{x} - x$ surfaces at pre-fault condition, (b) simulated current-constrained fault with $v_{TH} = 0.5$ p.u. and $Z_{TH} \approx 0.1$ p.u. with current-limiting sub-system and circular limiter enabled, (c) normalized $\dot{x} - x$ surfaces and movement of operating point from pre-fault equilibrium $a$ to equilibrium $\delta$ under fault condition.](image-url)
\[ \hat{V} \] reaches the new equilibrium \( d \) following \( a - b - d \) and \( a - c - d \) trajectories on their respective surfaces. Evidently, the system reaches steady state quickly (see Fig. 8(b)) as predicted by the trajectory analysis and the output current is clamped at the maximum allowable value \( I_m \).

Another class of fault response is resulted if no equilibrium can be reached under fault condition, i.e., no feasible power flow for given real and reactive power set-points and grid condition. Such a case is described in the following subsection.

C. Case III: Fault With No-Equilibrium Point

If no feasible equilibrium exists during fault, the system exhibits a limit-cycle behavior. To illustrate such a response, during pre-fault condition we consider \( v_{TH} = 1 \) p.u., \( Z_{TH} = 0.52 \) p.u.; power references are set as \( P_0 = 0.8 \) p.u. and \( Q_0 = 0 \). The \( \dot{x} - x \) surfaces corresponding to the pre-fault condition are depicted in Fig. 9(a): two equilibrium points, i.e., intersection points of \( \dot{\delta} = 0 \) and \( \dot{V} = 0 \) curves, are observed which include a stable equilibrium \( a_s \) and an unstable equilibrium \( a_u \). The stability property of each point can be verified graphically following the same procedure described in Section V-A. Therefore, the system operates at \( a_s \) during pre-fault condition. At fault condition triggered by a step change in the grid voltage from a step change from \( v_{TH} = 1 \) p.u. to \( v_{TH} = 0.5 \) p.u. leads to the \( \dot{x} - x \) surfaces shown in Fig. 9(b). Evidently, no equilibrium point exists, i.e., no intersection between \( \dot{\delta} = 0 \) and \( \dot{V} = 0 \) curves. Consequently, starting from the pre-fault equilibrium \( a_s \), the system moves into a limit-cycle behavior. From the trajectory analysis, the period of the limit-cycle is determined as \( \approx 393 \) ms.

The advantages of the proposed phase-plane analysis using \( \dot{x} - x \) surfaces over the conventional approach using \( \dot{\delta} - \delta \) and \( V - \delta \) curves become evident in the analysis for Case III. In the conventional method, \( \dot{\delta} - \delta \) curve shows existence of equilibrium points (\( \delta = 0 \)); however, the \( V - \delta \) plot shows a limit-cycle behavior. Although, the conventional method indicates a limit-cycle behavior, it fails to explain why and how such oscillatory behavior occurs. Contrarily, the proposed \( \dot{x} - x \) surfaces immediately reveals that although \( \delta = 0 \) and \( V = 0 \) cannot be reached which leads to the limit-cycle response.

The first-order dynamics of uVOC has a large-signal stability advantage over second-order controllers such as droop control or VSM. Second order controllers are constrained by

Figure 9. Phase-plane analysis and simulated response for fault without an equilibrium (Case III) - (a) normalized \( \dot{x} - x \) surfaces at pre-fault condition, (b) normalized \( \dot{x} - x \) surfaces at fault condition, when no equilibrium exists and the system trajectory follows a limit-cycle, (c) system trajectory after fault clears at different points on the limit-cycle; all trajectories reach the post-fault equilibrium, (d) simulated fault response when no equilibrium exists during fault.
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VI. EXPERIMENTAL RESULTS

The experiments are performed using a single-phase system with identical passive components and control parameters as those used for analysis and simulation of the three-phase system in the preceding sections; the power ratings are scaled to 33% to obtain an equivalent system. The detail system parameters are listed in Appendix A.

A. Case I

The first set of experiments are performed for the system and grid conditions identical to those in Section V-A. The converter response is shown in Fig. 10(a). As predicted by the analysis and simulation, in response to the grid voltage sag to $v_{TH} = 0.6$ p.u. the converter output current does not exceed the current limit $I_m$ (see Fig. 10(b)) and the reactive current injection raises the converter terminal voltage to $v_{poc} \approx 0.94$. Once the grid voltage returns to the nominal value, normal operation is retained. The transients when the fault occurs and during the fault-clearing are shown in Fig. 10(b) and 10(c), respectively.

B. Case II

The next set of experiments are performed at identical conditions as described in Section V-B. In response to the grid voltage sag to $v_{TH} = 0.5$ p.u., an over-current fault is detected once the converter current exceeds $I_m$ (see Fig. 11(b)); the controller increases its reactive power output while clamping the output current at $I_m$ which raises the converter terminal voltage to 0.64 p.u. Once the fault is cleared, the converter returns to normal operation (see Fig. 11(a) and (c)).

C. Case III

For the system and grid conditions described in Section V-C the test results are shown in Fig. 12. In response to the fault, the converter output current reaches $I_m$ and enters current
saturated operation. As predicted by the analysis, a limit-cycle response with a period of \(\approx 400\text{ms}\) is observed (see Fig. [2] (a)). Note that the output current is limited to \(I_m\) during the fault. Once the fault is cleared, the converter returns to normal operation quickly (see Fig. [2] (b)).

**VII. CONCLUSION**

A comprehensive modeling and analysis method has been developed for transient stability assessment of uVOC based grid-forming converters under both current constrained and unconstrained symmetrical faults. The proposed phase-plane analysis provides holistic insight into both voltage and power angle dynamics through a single graphical representation. Due to its first order nature, uVOC is not constrained by a critical clearing angle unlike second order droop based controllers; such property of uVOC is retained under current-constrained faults as well. The large signal nonlinear analysis demonstrates that uVOC with its fast response and built-in fault ride-through parameters exhibits strong stability characteristics. The modelling and analysis method has been validated through simulation and hardware experiments.

**APPENDIX A**

**SIMULATION AND EXPERIMENTAL SETUP**

The simulations and experiments are performed using a three-phase and an equivalent single phase VSC, respectively, with identical LCL filter and control parameters. The power ratings of the three-phase system is chosen as \(\times 3\) of those for the single-phase system. The system parameters are listed in Table [I]. Note that two interleaved sub-phases are used in each phase and hence an effective switching frequency of 75 kHz is achieved which reduces the LCL filter requirements [25]. The control parameters are listed in Table [II]. All parameters are listed using \(P_{\text{rated}}\) and \(V_0\) as base quantities.

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**Table I**

| Symbol | Parameter | For \(3\phi\) (for 1\phi) |
|--------|-----------|--------------------------|
| \(S_{\text{rated}}\) | Rated power | 9 kVA (3 kVA) |
| \(P_{\text{rated}}\) | Rated real power | 7.5 kW (2.5 kW) |
| \(Q_{\text{rated}}\) | Rated reactive power | 5 kVAR (1.67 kVAR) |
| \(V_0\) | Nom. (L-N RMS) voltage | 120 V |
| \(\omega_0\) | Nom. frequency | \(2\pi(60)\) rad/s |
| \(f_{sw}\) | Switching frequency | 37.5 kHz |
| \(f_s\) | Sampling frequency | 37.5 kHz |
| \(L_a\) | Converter-side inductor | \(\approx 0.04\) pu \(\times 2\) interleaved |
| \(L_f\) | Network-side inductor | \(\approx 0.005\) pu |
| \(C_f\) | Filter capacitor | \(\approx 0.004\) pu |

**Table II**

| \(\eta\) | \(19.95\) | \(\mu\) | \(7.1 \times 10^{-4}\) |
| \(\tau_f\) | 0.11 | \(R_0\) | 0.43 p.u. |
| \(L_{v0}\) | 0.29 p.u. | \(R_{v0}\) | 0.04 p.u. |
| \(\omega_0\) | \(2\pi(600)\) rad/s | \(I_m\) | 1.2 p.u. |
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