A SINGLE STAGE 1 KW ISOLATED SINGLE SWITCH ACTIVE POWER FACTOR CORRECTED SOFT SWITCHING AC-DC CONVERTER

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Abstract

Active Power factor corrected AC-DC converters in the power range of 500 watts and above are mostly accomplished in a two-stage process. The front end is non-isolated boost regulator working in CCM and the second stage is a DC-DC converter with isolation. This process is less efficient, complex and consumes more area. The front end PFC in CCM is a major source of EMI requiring heavy line filters to meet the international interface specifications.

A novel single-stage AC-DC converter for the output power of 1KW is proposed here, which has many advantages such as Single active switch, completely soft switched and isolated. The new configuration is fabricated and tested for all the parameters. A near unity PF is achieved and the worst case efficiency is recorded to be 94%. All the test data are presented.

Key Words: Power factor correction, soft switching, CCM, BCM control, Resonant reset, High power

I. Introduction

Electrical utility grid supplies AC voltage to the end users while most of the electrical/electronic appliances connected to the grid require a stable, galvanically isolated DC voltage for their operation. Therefore AC to DC converter is mandatory in all such appliances. These converters, in the present times, are invariably switched mode power converters operating at the 100’s of KHz frequency [VIII].

Switch Mode Power Converters, SMPCs contain nonlinear circuit elements such as diodes, Mosfet switches and /or IGBTs in addition to linear circuit elements. These elements give rise to non-sinusoidal currents being drawn from the grid and hence the current wave shape is heavily distorted. Distorted current contains large harmonic content and this leads to poor utilization of the grid. Harmonic currents other than the fundamental component lead to unwanted heat generation in the distribution lines and transformers [II]. Moreover, the distorted current waveform exhibits a very poor power factor.
Therefore International agencies have drawn stringent interface specifications for all appliances connected to the grid [3]. Power factor is one such specification and the standard IEC61000-3-2 [III] clearly specifies the permissible current harmonics, power factor, and the Total Harmonic Distortion THD.

Adhering to the above-referred standards for a switch mode AC DC converter demands an active power factor correction technique. Active power factor correction PFC involves usage of control algorithms, special integrated circuits, MOSFET switches, and extra hardware. PFC first corrects the distorted current wave shape to near sinusoidal wave and then its phase to be the same as that of the supply voltage [IV].

Input current shape in an AC DC converter without any PF correction is very spiky and it is drawn from the mains supply only for a short duration in a one-half cycle of the mains voltage. Therefore, to make the input current continuous throughout one mains cycle, boost regulators are employed in the front end of AC-DC converters. Since the output of a boost converter is always greater than the input voltage, the input current is continuous. This makes the boost configuration very adaptable for PFC applications [XII]. A typical boost regulator is shown below:

![Figure 1 Conventional Boost Converter](image)

Boost regulators can operate in two distinct modes, depending on the boost inductor current level. If the current in $L_b$ falls down and/or remains at zero value, within the switch SW1 OFF time then the boost regulator is said to be working in Boundary conduction mode (BCM) control or discontinuous conduction mode (DCM) control mode. If the current in $L_b$ does not reach zero value during the end of OFF time of SW1, then the mode is termed as Continuous conduction mode (CCM) control. Both schemes have merits and disadvantages [V].

For high power, AC-DC converters in excess of 500 watts, only CCM control of boost regulators are employed [VII]. In PFC applications, Boost regulator in CCM control accepts the rectified mains voltage as the input and generates a regulated high voltage of the order of 400V DC output. Variety of control ICs are available for commercial applications, which can be used to build the boost regulator, achieving the PF correction and generating the high voltage at the output. The output voltage in the range of 400V DC is not galvanically isolated from the input. Therefore, to generate the user required low voltage DC voltage with isolation, a second stage DC-DC converter is installed, which works on the high voltage DC bus output of the PFC boost regulator and generates a stable low DC output voltage which is galvanically isolated from the input side. Thus, to derive the low voltage, isolated stable DC
voltage from the input AC mains and also have the unity power factor, a two-stage approach is adopted by the industry.

Switch mode converters came in to replace the linear counterparts to mitigate two factors, 1) The efficiency, 2) Size. These two are achieved because the main switch in SMPC is non-dissipating in theory and it operates at very high frequency. Present day industry is demanding more power to be packaged in smaller areas. This can happen only when the switching frequency can be raised to higher levels. But, the effect of switching at a higher frequency is that the losses in the main switch would increase as the switches are non-ideal and dissipate power during every switching transition. Therefore, to mitigate the switching losses at higher frequencies, “soft switching” is adapted which significantly reduces the switching loss.

Soft switching is an industry-accepted technique in most of the power converters. The details of soft switching are well reported in the literature. The soft switching is attracting the interest of researchers’ continuously. A recent review of soft switching techniques, their merits and limitations are reported in [I].

II. Problem Statement

It has been substantiated above that Power Factor correction is an essential element in all nonlinear loads connected to AC Grid. Also, it is established that PFC and obtaining isolated DC voltage for the end user is a two-stage process. The front end Boost stage for high power output is essentially a CCM boost regulator which contributes to high Electromagnetic Interference EMI, dissipates considerable power and is a source of very high INRUSH current. Therefore the current research has been set with the following goals. The focus is on high power, say greater than 750 Watts output AC-DC converters.

1. Propose a new configuration for AC-DC converter with single stage conversion.
2. Achieve total soft switching for power components to improve efficiency and reduce EMI.
3. Avoid any additional active switch to achieve soft switching.
4. The AC-DC converter shall not have INRUSH current during power ON.
5. The input power factor shall be near to unity and should meet the IEC standard 61000-3-2
6. Input and output have galvanic isolation.

III. CONTRIBUTION OF THE PRESENT WORK

A novel and unique configuration is proposed which is a single stage, single switch, soft switched, Isolated AC-DC converter with PF correction which has no Inrush current. The uniqueness of the proposed scheme is highlighted as follows:

Active power factor correction circuits can be broadly classified into two categories i.e.; a) Low power up to 200 watts and b) high power above 200 watts. Low power PFC converters employ BCM flyback/boost configuration and these cannot be extended beyond 250 watts. All high power PFC converters are CCM boost configured. Many control ICs are commercially available for both such applications. However, in the proposed configuration, a BCM controller PFC IC is utilized to control a CCM boost regulator to achieve very good PF and also soft switching. A
practical converter with such a BCM control is designed, fabricated and tested for up to 1KW. The novelty of the scheme is in employing BCM control for CCM boost which exploits the advantages of both the schemes. The goal set for the present research is to design and validate a novel single stage single switch soft switching AC-DC converter with power factor correction and input-output galvanic isolation. Further, it is also mandated that any new configuration conceived shall have the least efficiency of 94% at full load and minimum input voltage. This is so, because, in a two-stage AC-DC converter, the best case efficiency can only be about 93%, assuming 97% for PFC and 96% for the DC-DC converter. Soft switching BCM controlled CCM PFC is combined with the capacitive coupled and transformer isolated version. The final configuration arrived is shown in figure 2.

![Figure 2 The Final Configuration](image)

Incoming AC voltage is rectified with a high power rectifier and the time-varying DC voltage \( V_{IN} \) is connected to a boost inductor \( L_B \). Boost inductor is designed to operate in the CCM for the most part of the load conditions. Main MOSFET switch drives a resonant transformer \( T_R \) and boost inductor \( L_B \). The junction of \( L_B \) and \( T_R \) primary is connected to an isolation transformer \( T_{IS} \) through a coupling capacitor \( C_{CIN} \). Secondary of the \( T_{IS} \) has a DC restoration circuit delivering the isolated DC output voltage \( V_O \). Secondary of \( T_R \) is also connected to the output through diode \( D_{S2} \). All the diodes are normal fast recovery diodes as against the high voltage Schottky silicon carbide diodes. In an otherwise high-frequency CCM boost converter always the silicon carbide diodes are used for reducing power dissipation in the MOSFET switch. \( T_R \) is a flyback transformer operating in BCM. A BCM PFC control IC FAN7527 Fairchild make is utilized in the present context to achieve the PF and also soft switching. BCM controller senses the complete energy transfer phase of \( T_R \) and initiates the turn-ON of the MOSFET switch with a predetermined delay [XI]. Turn OFF of the switch is determined by the closed loop controller signal depending on the load and line conditions and maintaining the output voltage. Clearly, the proposed configuration has a single switch which is soft switched, PF corrected, isolated and regulated DC output and single stage control.

The operating principle for realizing soft switching is explained in the sequence given below.

**Stage 1:** The controller signals to turn OFF the Switch. SW1 goes OFF and \( V_D \) continues at zero value because of \( C_R \). Then \( V_D \) starts increasing as \( C_R \) gets charged by \( I_{INP} \). When \( V_D \) equals the value of \( V_{XOFF} \), the current in the boost inductor gets diverted to the output.

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Stage 2: During this period, $L_R$ and $C_R$ start resonating and as a result, $V_D$ continues increasing. $V_D$ attains a maximum value when the stored energy in $L_R$ becomes zero. The peak value of $V_D$ is calculated using

$$I_{INP} \cdot \sqrt{\frac{L_R}{C_R}} + V_{XOFF}$$

The design criterion ensures that $V_D$ reaches $2V_{XOFF}$, the diode $D_S$ cuts in and clamps $V_D$ to $2V_{XOFF}$.

Stage 3: At this time, all the stored energy in $L_R$ is delivered to the load and ZCD signal in the sense winding goes to LOW (this is a part of BCM control IC). This period is $T_{RESET}$. In a regular BCM controller, the drive signal is switched ON at the instant ZCD goes to LOW.

Stage 4: The proposed scheme introduces a delay $t_D$ in ZCD reaching the controller IC. The reason to set a delay is, to allow a second resonance between $L_R$ and $C_R$. $V_D$ starts reducing sinusoidally as the energy in $C_R$ starts getting transferred to $L_R$. When $V_D$ reduces to $V_{XOFF}$, $L_R$ discharges $C_R$ further. $V_D$ reaches zero value within exactly the half resonant time period of $L_R$ and $C_R$. The delay time $t_D$ is set to this half resonant time so that the controller switches ON SW1 at Zero voltage.

It can further be noted that at turn ON of SW1, the presence of $L_R$ with zero current ensures zero current turn ON. Thus, ZV turn OFF, ZVS and ZCS turn ON are achieved with a BCM control while the main boost inductor $L_B$ is still in CCM.

**IV. OPERATING PRINCIPLE**

$C_{CIN}$ and $C_{CO}$ are the coupling capacitors which are considered as voltage sources and act as key elements in deriving isolated output voltage. Voltage $V_X$ adjusts itself to an adequate value to deliver the required output voltage due to closed-loop feedback for varying line and load conditions. The voltage across $C_{CO}$ represents the contribution of the input voltage component to the output voltage as it is the case with any boost converter. Due to the circuit configuration, it can be seen that the voltage across $C_{CIN}$ is always equal to the input DC voltage itself. Voltage $V_X$ swings between two values, $V_{XON}$ and $V_{XOFF}$ within a switching cycle during ON and OFF times of the MOSFET switch respectively.

Assuming the turns ratio of isolation transformer $T_{IS}$ as 1:1, the output voltage is defined by

$$V_O = (V_{IN} - V_{XON}) + (V_{XOFF} - V_{IN}) = V_{XOFF} - V_{XON}$$

Further, by balancing the volt-seconds across boost inductor $L_B$,

$$(V_{IN} - V_{XON}) \cdot T_{ON} = (V_{XOFF} - V_{IN}) \cdot T_{OFF}$$

The duty cycle $D = \frac{(V_{XOFF} - V_{IN})}{(V_{XOFF} - V_{XON})}$

$V_{XOFF}$ value cannot be lower than the peak of the highest input AC voltage, which in the present case works out to be $(264 \times 1.414)$, say 380V DC. The upper limit of $V_{XOFF}$ is dictated by the absolute maximum breakdown voltage $V_{DSM}$ of the MOSFET switch and the turns-ratio of $T_R$.

$$V_{XOFF} \text{ max} = \frac{(0.7 \times V_{DSM})}{2}$$. This gives a safety margin of 30% on the breakdown voltage rating of the MOSFET switch.
Turns ratio of $T_R$ is selected to reflect $V_{XOFF}$ max across its primary when MOSFET is OFF and $D_{s2}$ is conducting. This is a mandatory condition to achieve ZVS at turn ON for MOSFET switch [IX]. The turns-ratio of 1:1 for isolation transformer is just quoted as a reference. In practice, it depends on the output voltage requirement. In the present prototype unit, it was selected to be 2.0 for an output voltage of 150 V DC. Selection of turns-ratio for $T_{IS}$ is based on the limiting values of $V_{XON}$ and $V_{XOFF}$. Likewise, the turns-ratio for $T_R$ was selected to be 2.8 to reflect around 420 VDC on to the primary at 150 V DC output. With this, MOSFET will exhibit ZVS at Turn ON, up to 420 V at $V_{XOFF}$. For any value beyond, the ZVS at Turn ON ceases. As discussed and referred in [VI,X,XIII,XIV,XV], Transformer $T_R$ was fabricated as two parts, with primaries connected in series and the secondaries in parallel. This reduced the stress in secondary and improved efficiency. Each transformer turns ratio was 1.4 adding up to 2.8.

$V_{XON}$ settles down to a value depending on the load condition and input voltage. In fact, both $V_{XOFF}$ and $V_{XON}$ vary with line and load. $V_{XON}$ can be equated as follows:

For a CCM condition wherein the current in the inductor, $L_B$ is continuous, $L_B$ can be treated as a constant current source with the current $I_{IN}$, neglecting the inductor ripple current. However, in the practical case, the boost inductor in CCM is designed to have a $\Delta I$ of 40% of $I_{IN}$ where $I_{IN}$ is the input DC current for a given input voltage and output load.

$C_{CIN}$ and $C_{CO}$ are considered to be voltage sources within one switching cycle. $C_{CIN}$ is always charged to the input voltage $V_{IN}$. Writing the equations at the end of switch ON time $T_{ON}$,

$$I_{INP} = (V_{XON}/L_R)T_{ON} + ((V_{XON} - V_{DS})/L_M)T_{ON}$$

$I_{INP}$ is the peak of input current including the ripple current equal to 1.2$I_{IN}$. $L_M$ is the magnetizing inductance of the isolation transformer $T_{IS}$ and $L_R$ is the primary inductance of $T_R$. $I_{IN}$ is given by

$$(V_{O}*I_{O})/V_{IN}*\eta,$$ where $\eta$ is the efficiency of the converter. For a condition where the boost inductor $L_B$ goes into BCM/DCM, the $V_{XON}$ is given by

$$V_{IN} - V_{XON} = V_{XON}/L_R + (V_{XON} - V_{IN})/L_M$$

Thus, $V_{XON}$ is clearly dependent on Switch ON time, input voltage and output load current.

V. Component Selection

As can be seen from the above equations, all the parameters are interdependent and, to arrive at component values, a set of nonlinear equations need to be solved. Alternatively, the iterative process can be adapted. However, for the practical practicing engineers, it is best to propose an easier and approximate approach by which quick selection of components is possible. Following sequence is elaborated to arrive at components in a practical environment.
I. The starting point can be the worst case condition of the lowest input voltage and full power, which is 190V DC and 1000W output power. Under such conditions, input current \( I_{IN} = \frac{1000}{0.94} \times 190 = 5.6\)Amps, say 6.0A. Fix the switching frequency to around 100 KHz for this operating point. Output voltage \( V_o \) is selected to be 150V DC.

II. Next step shall be to select the resonant capacitor \( C_R \). From the data sheets of the MOSFET switch selected, 40 nS is the turn OFF time \( t_F \). So to achieve ZVS during turn OFF, while turning OFF say 6.0Amps of current, a capacitor value of 2.0Kpf is needed.

III. MOSFET switch has the maximum breakdown voltage of 1200V. Keeping a margin of 30%, \( V_{XOFF} \) is fixed as \( 0.7 \times 1200/2 = 420\) V DC.

IV. Turns-ratio of \( T_R \), \( N \) is arrived as \( \frac{V_{XOFF}}{V_O} = \frac{420}{150} = 2.8\) For a normal boost regulator, at 190V DC and 420DC output, the duty cycle is 0.55. Since, in this case, the \( V_{XON} \) is not zero and has a finite value, choose \( D = 0.7 \).

V. For a duty factor of 0.7 and 100KHz switching frequency, the OFF time \( T_{OFF} \) is equal to 3.0 microseconds and \( T_{ON} = 7.0 \) microseconds.

VI. So from equation 3, \( V_{XON} = 92\) V DC, say 100 V.

VII. From equation 1, for \( V_O \) of 150V DC, the turns-ratio of \( T_{IS} \) selected as 2.0 which would be able to derive up to 160V DC for the given \( V_{XOFF} \) and \( V_{XON} \) values.

VIII. Selection of \( L_R \) is as per the sequence denoted in chapter5, however, for clarity sake, it is revisited here.

IX. The turn OFF duration of the MOSFET switch is the complete energy transfer time \( T_{RESET} \) of \( T_R \) plus the delay time equal to \( \pi \sqrt{L_R * C_R} \) which is

\[
T_{OFF} = T_{RESET} + \pi \sqrt{L_R * C_R}
\]  

(6)

The \( T_{RESET} \) is calculated by \( V_O = L_S * (I_{INP} * N) / T_{RESET} \) where \( L_S \) is the secondary inductance of \( T_R \) given by \( L_R / N^2 \). Therefore

\[
T_{RESET} = \frac{(L_R/N^2) * I_{INP} * N}{V_O}, \text{ where } I_{INP} \text{ is the primary peak current. Hence}
\]

\[
T_{RESET} = \frac{K * I_{INP}}{N * V_O}, \quad (7)
\]

Define \( I_{INP}/ (N * V_O) \) as \( K \) for computational simplicity. Thus

\[
T_{RESET} = K * L_R
\]  

(8)

There by

\[
T_{OFF} = K * L_R + \pi \sqrt{L_R * C_R}
\]  

(9)

\[
\pi \sqrt{L_R * C_R} = T_{OFF} - K * L_R
\]

Squaring on both sides

\[
\pi^2 (L_R * C_R) = (T_{OFF} - K * L_R)^2
\]

\[
\pi^2 (L_R * C_R) = T_{OFF}^2 - 2 * T_{OFF} * K * L_R + K^2 * L_R^2
\]

\[
K^2 * L_R^2 - (\pi^2 C_R + 2 * T_{OFF} * K) * L_R + T_{OFF}^2 = 0
\]

Solving the quadratic equation, the value of \( L_R \) is given by

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\[ L_R = \left\{ (\pi^2 C_R + 2 T_{OFF} K) + \sqrt{(\pi^2 C_R + 2 T_{OFF} K)^2 - 4 K^2 T_{OFF}^2} \right\} / (2 K^2) \quad (10) \]

Substituting the values for \( I_{INP}, N, V_{O}, C_R \) and \( T_{OFF} \) the value of \( L_R \) can be computed.

X. Therefore solving for \( L_R \) we get \( L_R = 92.5 \mu H. \)

XI. \( L_B \) is computed to keep the converter in the CCM mode. Therefore allowing a \( \Delta I \) of 40% of 6.0Amps at the maximum ON time of 7.0\( \mu S, \)

\[ L_B = (190-100) \times 7.0 \times 10^{-6} / 2.4 = 262.5 \mu H. \]

The actual working model had the following values for the critical components:

\( L_B = 250 \mu H \)

\( L_R = 100 \mu H \)

\( T_{IS} \) had a turn’s ratio of 2.0, step down with primary 20 turns and secondary 10 turns.

\( L_M \) was 1.5 \( \mu H \)

MOSFET Switch: 1200V, 280m\( \Omega \) Silicon Carbide. Part Number: SCT2280KE, ROHM make

\( C_{CIN} \) and \( C_{CO} = 2.2 \mu F \)

\( C_R = 2.2 \text{ KpF} \)

All the magnetic components were EE25/13/7 Ferrite core with N87 grade and double stacked.

To cross verify the computations, we can substitute the values of \( L_R, V_{XON}, \) and \( T_{ON} \) in equation 4, to compute the value of \( I_{INP}. \)

\[ I_{INP} = 7 \times 10^{6} \times (100/100 \times 10^{-6} - 90/1.5 \times 10^{-3}) = 7 \times 0.42 = 6.58 \text{ Amps which is a very close to the expected value of 5.6 \times 1.2 = 6.72 Amps.} \]

VI. Test Results and Discussion

A working model of 1KW AC-DC converter as per the above configuration was fabricated. The proto unit is shown in Figure 3. Also to have a benchmark reference for the proposed converter, a two-stage hard switched AC-DC converter with PFC was fabricated and evaluated for all the results. The two-stage version is shown in fig 4.

Figure 3. The prototype unit
Detailed tests were carried out on both the proposed single stage version and the standard two-stage version. The test data are extensively tabulated. Following tests/sequence was followed:

I. Firstly, the unit was tested for its load capability and its capacity to deliver 1KW was established. The output voltage was set to 150V DC.

II. Inrush current: Input current during power ON with the unit loaded to full load and nominal AC input voltage was monitored on a storage oscilloscope. As expected, at turn ON, no inrush current was noticed. As the bulk capacitor is absent in the input section, and the controller FAN7527 has an under voltage lockout feature, no inrush current is possible.

III. Efficiency evaluation: One important parameter to be evaluated is the efficiency of the converter. Therefore, to accurately evaluate the efficiency figures, the converter was fed with a stable DC source instead of AC and output was connected to a variable load. Both input and output currents were continuously monitored. The input voltage was varied from 190V DC to 325V DC and so also the load was varied from 300Watts to 1000Watts. Obtained results, including the switching frequency, was noted and tabulated. Switching frequency varied from the highest of 275 KHz to the lowest level of 95Khz. The highest frequency occurs and minimum load and the highest input voltage. This is so because, for this condition, the input current is at its minimum and hence the complete energy transfer time, $T_{\text{RESET}}$ in $T_R$ is the lowest giving rise to minimum OFF time. For the entire range of 300 Watts to 1000 Watts, the efficiency figure remained within the limits of 94.4 to 95.6%. In contrast, the two-stage converter efficiency varied from as low as 89.36% to a maximum of 94.38%. Speaking in terms of loss improvement, the two-stage had a loss of 68.76 watts at 1000 watts output and 220V DC input, whereas the single stage had a loss of only 57.3 watts. Around 12 watts of power saving is noticed in a single stage version. One other interesting observation is at lower power levels. At 300 watts of output, the two-stage version reported a loss of around 36 watts in the input range of 190V to 325V, leading to an efficiency of about 89.5%. However, the single stage version scores extremely well here by reporting a loss of only 18 watts which is 50% lower compared to two-stage, and efficiency is more than 94.5%. Another observation to be highlighted is the fact that the single stage losses remained...
almost constant at 18 watts, though the switching frequency varied by a factor of 1.6 clearly depicting soft switching. Same is the case even for 500 watts of output power. The two-stage has a loss of around 43 watts whereas the single stage has only about 23 watts. Highest efficiency reported in a two-stage converter was for the highest input voltage of 325V DC. This is so because at 325V DC the boost regulator has the highest efficiency to generate 385V DC. Losses registered at this voltage were 59 watts at 1000 watts power. In comparison, the single stage version had only 49 watts loss for these conditions. The highest efficiency recorded for a single stage version is 95.9%, say 96 % for an output of 750 watts and 325V DC input.

![Table 1 Efficiency of a Single Stage Converter](image)

| IN PUT VOLTAGE | 300W | 500W | 750W | 1000W |
|----------------|------|------|------|-------|
| 190            | 94.4%| 94.9%| 94.6%| 94.8% |
| 220            | 94.5%| 95.2%| 95.2%| 94.6% |
| 275            | 94.7%| 95.6%| 95.7%| 95.2% |
| 300            | 94.5%| 95.6%| 95.8%| 95.1% |
| 325            | 94.5%| 95.3%| 95.9%| 95.2% |

Table 1 Efficiency of a Single Stage Converter

![Figure 5 Efficiency of a Single Stage Converter](image)

Table 2 Losses in a Single Stage Converter

![Table 2 Losses in a Single Stage Converter](image)

| IN PUT VOLTAGE | 300W | 500W | 750W | 1000W |
|----------------|------|------|------|-------|
| 190            | 17.9 | 26.9 | 42.8 | 64.2  |
| 220            | 17.4 | 24.7 | 37.9 | 57.4  |
| 275            | 16.8 | 23.1 | 33.4 | 50.0  |
| 300            | 17.4 | 23.0 | 32.8 | 51.9  |
| 325            | 17.5 | 24.7 | 32.3 | 50.0  |
IV. To depict the soft switching characteristic of the converter, drain, and gate switching waveforms of the MOSFET have to be captured. Therefore, to clearly demonstrate the soft switching, the unit was again powered with the DC input voltage. A two-channel digital storage oscilloscope was connected to gate and Drain of the MOSFET switch. The switching waveforms were captured for two extreme conditions, such as 300 watts output power at 325 V DC input (figure 7) and Full load of 1000 watts at minimum input voltage (figure 8). ZVS switch ON and OFF can clearly be seen, wherein the gate voltage crosses the threshold turning ON the switch, only after the drain voltage has reached zero value. Likewise, the drain voltage starts rising, only after the gate voltage has fallen below the threshold. ZVS at turn ON and turn OFF are very distinctly identified in the oscilloscope waveforms. Likewise, the waveform at V_X (figure 9) is captured with respect to drain waveform to set an idea of the working unit.

Figure 6: Losses in a Single Stage Converter

Figure 7 Gate and drain Waveforms of Single Stage Converter

Figure 8 Gate and drain Waveforms of Single Stage Converter
The same waveforms were captured for a two-stage AC-DC converter. In both the PFC MOSFET and the DC-DC converter MOSFET it was very clearly seen that the drain voltage is still at high value when the gate signal crosses the threshold depicting a hard switched situation.

POWER FACTOR and THD: Subsequent to the efficiency and soft switching evaluation, the AC-DC converter was taken up for AC measurements such as PF, THD, and current harmonic recordings. For this, the test equipment used was WT210, Power Analyzer, manufactured by YOKOGAWA. It can measure all the required parameters. The single stage AC-DC converter was powered with a variable AC source through the WT210 analyzer. Power factor and THD were recorded for three different input voltages and three different output powers. The input was varied from 180V AC to 264V AC and load was also for four different levels of 300W, 500W, 750W and 1000W. Observations are shown in Table 3.

| INPUT VOLTAGE VAC | OUTPUT POWER W |
|-------------------|----------------|
| 300W              | 0.988          |
| 500W              | 0.996          |
| 750W              | 0.999          |
| 1000W             | 0.999          |

Table 3 Power Factor of a Single Stage Converter

![Power Factor Single Stage](image)
Like any other active power factor correcting converter, the PF was poor at high line and low power output. Excepting at 300W, and 264V AC where the PF was 0.946, all other conditions exhibited a very good PF. For 750W and 1000W, the PF was better than 0.995 under all the line conditions. Similarly, THD also was poor for high line and lowest power of 300 W. For all other conditions, THD was less than 12%. In fact for the power level of 750W; THD was less than 10% for all line conditions. For 1KW, though the PF was excellent, THD was little more than 10%. It is to be put on record here, that the single stage AC DC converter did not have any line filter at the input side while making the above measurements. Excepting two 1.0μF box capacitors across Line and Neutral, no other filter was provided. This is to measure the PF and THD parameters under the worst case scenario. When the same parameters are compared with that of the two-stage converter, the PF readings were slightly poor compared to a single stage, whereas the THD readings were excellent. All through, the THD was well below 5%, the reason that can be attributed to Lower PF but better THD in two stage is that the two-stage version was a well-established industry model with an elaborate line filter in the Π configuration and high-value Box capacitors across Line and Neutral.

CURRENT HARMONIC MEASUREMENT. In addition to the THD, IEC specification dictates the individual recording of harmonic RMS currents. The instrument WT210 has this facility too and hence the current harmonics are recorded for full load condition and nominal AC input voltage. The findings are depicted in table.05 and also bar graph figure .10. The measurements meet the
specification. As anticipated all the even harmonics are absent. Except the 3rd harmonic which has 0.5 amperes, while the fundamental was 4.25 amperes, rest all the odd harmonics were negligible. Up to 20th harmonic readings are established. Here too, the two-stage version scores better, in the sense that the third harmonic is as low as 0.05 amperes while the fundamental was at 4.22 amperes.

![Figure 12 Harmonics of a Single Stage Converter](image)

**Table 5 Harmonics of a Single Stage Converter**

| Harmonics | Value   |
|-----------|---------|
| Harmonics 1 | 4.25    |
| Harmonics 2 | 0       |
| Harmonics 3 | 0.5     |
| Harmonics 4 | 0       |
| Harmonics 5 | 0.04    |
| Harmonics 6 | 0       |
| Harmonics 7 | 0.028   |
| Harmonics 8 | 0       |
| Harmonics 9 | 0.02    |
| Harmonics 10 | 0      |
| Harmonics 11 | 0.008  |
| Harmonics 12 | 0       |
| Harmonics 13 | 0.01    |
| Harmonics 14 | 0       |
| Harmonics 15 | 0.02    |
| Harmonics 16 | 0       |
| Harmonics 17 | 0.018  |
| Harmonics 18 | 0       |
| Harmonics 19 | 0.028   |
| Harmonics 20 | 0       |

**IX. INPUT CURRENT WAVESHAPE:** Though, the PF and THD are measured and recorded, for ease of understanding and to give the first level feel of the converter operation, input current wave shape is also captured on the oscilloscope and put on record. Two channels of the oscilloscope depict the input voltage and simultaneously the input current. Input current was measured, as the voltage drop across a 0.1 ohm power resistor connected in series with the neutral line of the AC input supply. Pictorially, the input current waveform obtained was near sinusoidal and in phase with the input voltage. When compared, even the two-stage converter also exhibited a similar current waveform.
X. OUTPUT RIPPLE: output voltage ripple was recorded at full load and nominal AC input voltage. The recorded value was 3.0Volts on 150VDC, amounting to about 2%. The ripple content was that of the 100Hz component. Similarly, load regulation is also about 2%. It is as per the understanding because the loop response/bandwidth of the converter has to be very low to get a better PF. whereas the two-stage converter had the ripple below150 mV, amounting to less than 0.1%. The line frequency component is also negligible. Similarly, the two-stage converter has excellent load regulation, better than 0.1%.

XI. However, the single stage converters are generally used as an intermediate bus voltage on which high power Point of Load (POL) converters work to deliver high current supply to target load. For such an operating scenario, slightly higher ripple and poorer response is not an issue. Likewise, the application areas such as Battery chargers do not absolutely demand lower ripple and good response. So for all the advantages a single stage, the drawback of higher ripple or poor response can easily be traded in the real-life industry applications.

VII. COMPARISON OF SINGLE AND TWO-STAGE CONVERTERS

The following graphs indicate the direct comparison of the performance of the two-stage version and the proposed single stage version at one shot. Efficiency, losses and PF and are compared. The test data depict the clear advantage of single stage AC-DC converter over the two-stage version.
VIII. Conclusions

Single stage power factor corrected AC DC converters in the range of 500 watts and more are gaining prominence due to their advantages. These have been explained above and an attempt is made in this research to propose and develop a new configuration for a single stage, single switch, and soft switching AC DC converter with power factor correction. A Practical working model has been built to deliver 1Kw of power which is ideally suited for battery charging applications and isolated intermediate Bus voltage for point of load converters. All the test results are published and compared with a standard two-stage AC DC converter. Clearly, the proposed scheme exhibits an edge over the two-stage version. The unique feature of the scheme is in adapting BCM control for a CCM boost configuration.

Any high power two-stage AC-DC converter would have a minimum of three active switches. One switch for CCM PFC boost converter and at least two switches for the
following DC-DC converter. Many times the high power DC-DC converter can be a full bridge version, demanding four switches. Therefore the proposed version of single switch scores well. Likewise, the soft switching nature of the proposed scheme brings in the advantage of minimizing the power loss in the active switch, thus improving the reliability. It is envisaged that the proposed converter with soft switching would exhibit lower EMI and hence lesser filtering requirements.

The price paid for achieving the advantages in the proposed scheme is the fact that the switching frequency varies widely with Line and load conditions.

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