Effect of Interface State Trap Density on the Performance of Scaled Surface Channel In$_{0.3}$Ga$_{0.7}$As MOSFETs

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Abstract. The effect of interface state trap density, $D_{it}$, on the $I_D$-$V_G$ characteristics of scaled surface channel MOSFETs based on In$_{0.3}$Ga$_{0.7}$As channel has been investigated using drift-diffusion simulations. We have developed a methodology to include arbitrary energy distributions of interface states into the input simulation decks and analysed their impact on subthreshold characteristics and drive current when these devices are scaled from a gate length of 65 nm to 35 nm, 25 nm and 18 nm. The distributions of interface states having high density tails that extend into the conduction band can significantly impact the subthreshold performance of the larger gate length device. Furthermore, the same distributions have smaller impact on the performance of shorter channel devices which were designed with smaller high-$\kappa$ thickness.

1. Introduction

MOSFETs based on III-V semiconductors are currently the most promising devices for the near-end of the ITRS [1]. High electron mobility and low effective mass resulting in a very high injection velocity and low backscattering promise very high device performance [2]. The development of a suitable $\text{Ga}_2\text{O}_3$/GdGaO (GGO) gate stacks for GaAs with low interface state density ($\sim 1 \times 10^{11}$/cm$^2$) have been already reported resulting in an unpinned oxide/semiconductor interface [3][4]. This is an essential step enabling the realisation of III-V transistors in future CMOS circuits and systems. However, the introduction of such novel III-V materials into MOSFETs, requires transistor architectures that can take a full advantage of the high mobility and high injection velocity in the channels [2]. The presence of interface state density distributions in these material systems can still impact the overall performance of the scaled transistors. Herein, we investigate the potential device performance and the impact of interface states ($D_{it}$) on the output characteristics of scaled surface channel (SC) In$_{0.3}$Ga$_{0.7}$As MOSFETs using a commercially available Drift-Diffusion (DD) TCAD tool [5].

2. Surface Channel In$_{0.3}$Ga$_{0.7}$As MOSFET architecture

We have simulated scaled SC In$_{0.3}$Ga$_{0.7}$As MOSFETs from a gate length of 65 nm to 35 nm, 25 nm and 18 nm. A cross section of the investigated SC devices is illustrated in Fig. 1. This design is based on a traditional bulk MOSFET device structure with In$_{0.3}$Ga$_{0.7}$As channel
growth on p-type doped GaAs buffer substrate. On top of this sits a high-κ GGO layer (κ = 20) separating the In$_{0.3}$Ga$_{0.7}$As channel from the metal gate that is modelled using an assumed work function of 4.25 eV. Highly doped implanted n-type regions are simulated using a Gaussian-type distribution with a peak doping dose reported in table of Fig. 1. The lateral extensions are similarly defined and self-aligned to the gate.

| Thickness [nm] | Gate length [nm] |
|---------------|-----------------|
| 65            | 35              |
| 35            | 25              |
| 25            | 18              |

| Source-to-gate spacer (L$_{SG}$) | 80 | 37 | 26 | 20 |
| Gate-to-drain spacer (L$_{GD}$) | 80 | 37 | 26 | 20 |
| High-κ GGO (T$_D$) | 10 | 5.1 | 4.6 | 3.6 |
| In$_{0.3}$Ga$_{0.7}$As channel (T$_C$) | 10 | 10 | 7 | 5 |
| GaAs buffer (T$_B$) | 300 | 300 | 300 | 300 |
| HDD depth (L$_{HDD}$) | 70 | 35 | 26 | 18 |
| Extension depth (T$_{Ext}$) | 22 | 20 | 14 | 10 |
| EOT | 1.95 | 1.0 | 0.9 | 0.7 |
| Doping concentrations [×10$^{17}$/cm$^3$] | 65 | 35 | 25 | 18 |
| Peak S/D n-type | 100 | 100 | 200 | 400 |
| Uniform p-type | 10 | 5 | 10 | 24 |

Figure 1. Cross-section of scaled SC In$_{0.3}$Ga$_{0.7}$As transistors and the corresponding dimensions, doping concentrations and effective oxide thickness (EOT).

3. Results and discussion

The layer structures of the scaled SC transistors as well as dimensions and doping concentrations are summarised in Fig. 1. The high-κ gate oxide is assumed to be GGO with a dielectric constant of 20. The dimensions and doping profiles are optimised using a DD simulations and account for limitations of doping concentrations in III-V materials. The simulated $I_D$-$V_G$ characteristics at low and high drain voltages for each SC gate length MOSFET are plotted in Fig. 2. A proper scaling of critical dimensions and doping profiles is made following the ITRS prescriptions and in order to minimise subthreshold slope and DIBL deterioration (Fig. 3). The effect that the D$_{it}$ has on the performance characteristics is then studied by developing a methodology to include an arbitrary D$_{it}$ distributions into the device simulation procedure. Due to the use of the drift-diffusion approach, the simulations are restrained only in the subthreshold region at low drain voltage aiming mainly to illustrate the impact of the D$_{it}$ on subthreshold slope and mobile charge control in the channel.

The measured and used D$_{it}$ distributions in the device simulations are plotted in Fig. 4. In each case, zero corresponds to the position of the conduction band edge (E$_C$). The measured distribution in Fig. 4(A) was recently reported in [6] and is that for a GdGaO/Ga$_2$O$_3$ dielectric stack on heterostructure with an In$_{0.3}$Ga$_{0.7}$As channel. The D$_{it}$ distribution plotted in Fig. 4(B) is the same as that shown in Fig. 4(A) but includes an extrapolated extension of the D$_{it}$ distribution into the conduction band. The D$_{it}$ of Fig. 4(C) is 2.5 times higher than the measured one. In the device simulations, only acceptor states in the upper half of the conduction band are considered. Furthermore, each one of the plotted distributions in Fig. 4 is then aligned to the conduction band edge of In$_{0.3}$Ga$_{0.7}$As which is immediately below the high-κ layer. We assume that the experimentally determined D$_{it}$ distributions will not dramatically change when the devices are scaled down.

The simulated $I_D$-$V_G$ characteristics at low drain bias ($V_{DS}$=50 mV) for 65 nm gate length In$_{0.3}$Ga$_{0.7}$ SC MOSFET excluding and including D$_{it}$ from Fig. 4(A) are plotted in Fig. 5. The interface density of states which has a large tail density at the conduction band will not affect significantly the deep subthreshold region of the In$_{0.3}$Ga$_{0.7}$As SC MOSFET. The subthreshold
Figure 2. $I_D$-$V_G$ characteristics at low ($V_D=50$ mV) and high ($V_D=1$ V) drain voltages of scaled SC In0.3Ga0.7As device.

Figure 3. Subthreshold slope (SS) and DIBL versus gate length of the scaled SC MOSFETs at low drain voltage (squares); at high drain voltage (circles) and DIBL (triangles).

Figure 4. Measured and modified GGO/GaAs $D_{it}$ distributions used in simulations of the scaled SC device.

Figure 5. $I_D$-$V_G$ characteristics at $V_D=50$ mV of 65 nm gate length SC MOSFET, with $D_{it}$ (triangles) and without $D_{it}$ (squares).

slope (SS) deteriorates close to the threshold voltage and will cause its shift. The on-current is lowered by nearly 40% just above the threshold but will recover at the large gate bias overdrive.

The simulated $I_D$-$V_G$ characteristics at low drain bias of ($V_{DS}=50$ mV) for the scaled 35 nm, 25 nm and 18 nm gate length devices are plotted in Fig. 6. The inclusion of the measured GGO/GaAs $D_{it}$ distribution from Fig. 4(A) into the simulation has little affect on the deep subthreshold behaviour for each of the scaled device structures. This is because the Fermi level sweeps through a relatively low $D_{it}$ ($\sim 2\times10^{11}/\text{cm}^2\cdot\text{eV}$) until approximately 0.2 eV below the conduction band edge as shown in Fig. 4 and demonstrated in Figs. 5 and 6. Above this energy $D_{it}$ dramatically increases to approximately $4\times10^{12}/\text{cm}^2\cdot\text{eV}$ resulting in significant deterioration of the subthreshold slope and a shift in $V_T$. Due to the scaling process, the high-$\kappa$ oxide thickness is reduced as well as channel thickness which both affect the electrostatic integrity. Therefore, the drive current increases for each shorter channel SC MOSFET. The same $D_{it}$ in each case affects the drain current with a different ratio due to the increasing
values of current for each scaled gate length device. The resulting degradation in the SS due to the measured $D_{it}$ distributions is less significant for shorter channel length devices. Fig. 6(C) for example shows a smaller degradation in the SS and corresponding smaller shift in the $V_T$ when compared with the results in Fig. 6(A). However, the possible extension of the $D_{it}$ in the conduction band (Fig. 4(B)) or larger magnitude of $D_{it}$ (Fig. 4(C)) due to different fabrication processes for smaller device (below 65 nm gate length) can affect the SS and reduces the mobile charge in the channel above threshold (Fig. 6).

Figure 6. $I_D-V_G$ characteristics of scaled In$_{0.3}$Ga$_{0.7}$As SC MOSFET with gate length of (A) 35 nm, (B) 25 nm and (C) 18 nm at $V_D=50$ mV. The impact of GGO/GaAs $D_{it}$ from Fig. 4 is also shown. Current is plotted on both log (left) and linear scales (right) in each case.

4. Conclusion
The effect of $D_{it}$ on the subthreshold characteristics and performance of scaled In$_{0.3}$Ga$_{0.7}$As surface channel has been investigated. Numerical investigations demonstrate that specific distributions of interface states can significantly affect the subthreshold performance of these device. Surface channel designs are more sensitive to interface states in the upper half of the bandgap. This is due to the manner in which the Fermi level sweeps through this particular energy region during device operation.

The results herein show that smaller gate length devices are less affected by the interface state density distributions. For smaller device lengths, the high-$\kappa$ oxide thickness is reduced as well as the channel thickness which both affect the electrostatic integrity. Therefore, the drive current is increased for the shorter channel SC MOSFET and the applied $D_{it}$ affects the drain current with different ratios due to the larger values of the drive current for smaller gate length devices. The larger magnitude of $D_{it}$, possibly due to different fabrication processes for smaller devices, can affect both the subthreshold characteristics and $I_{on}$ current. This limits the range of distribution of interface states that can contribute to the trapping of charge and results in performance degradation. We would like to point out that the simulation results herein are strictly for low drain bias assuming a constant mobility in the channel. A more accurate study at a high drain voltage will require drift-diffusion simulations calibrated to the results obtained from ensemble Monte Carlo simulations [2][7] in order to accurately adjust both the low field mobilities and saturation velocities in each case.

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