Low Power Ultra-Wideband VCRO in 130nm CMOS Technology

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Abstract. The development of a voltage-controlled oscillator (VCO) that can operate at high performance within the ultra-wideband (UWB) frequency while consuming low power is useful for future device implementation in communication systems. This paper presents a design of a low power ultra-wideband ring-oscillator (VCRO) in 130nm complementary metal-oxide-semiconductor (CMOS) technology with a single-ended differential pair architecture for UWB application. The aim of this project is to optimize the VCRO with low power technique to ensure it consumes less power and able to operate within the UWB frequency. All design architecture, schematic and layout and simulation and analysis are implemented using Cadence Tool in 130nm CMOS technology. Through simulation and analysis process, this VCRO achieved a wider frequency from 7.186 GHz to 9.651 GHz with lowest power consumption of 0.78 mW. This VCRO has tuning range of 25.54%. The output noise and figure of merit (FOM) at 1 MHz offset frequency is -153.1 dBc/Hz and -234.83 dBc/Hz while at a 10 MHz offset frequency, the output noise and FOM is -162.0 dBc/Hz and -223.73 dBc/Hz respectively. Through overall analysis, it can be concluded that this VCRO has better performance compared to previous work in terms of power consumption, output noise and frequency tuning range.

1. Introduction

In the rapidly growing field of wireless communication, the device that capable to operate in high performance along with the long lifetime is very demanding. Thus, the development of voltage-controlled oscillator (VCO) with ultra-wideband (UWB) and at the same time consumed low power could be useful for the future devices implementation [1].

The UWB technology had widely been developed in designation of wireless system. The UWB technology capable to transmit information within wide bandwidth over 3.1GHz to 10.6GHz [1], [2]. It also consumed low power within short-range data transmission and does not interfere with different wireless technology. These characteristic assure the UWB technology is suitable for short-distance application such as wireless personal area network (WPAN) and wireless body area network (WBAN) systems [2], [3].
The UWB technology has very wide tuning range, it is a challenge to build a VCO with ultra-wideband frequency along with the low power consumption. Since many wireless devices are battery-powered, it is very important to minimize the power consumption.

In this modern world, it is high demand of portable device which is not only capable to be handle and easily remove, but also able to operate with high performance and long-lifetime. The high performance means it could able to operate effectively within short time. In terms of UWB application, the devices should be able to transfer the data with high speed and high bit rates within a short time.

Motivated by this demand, the design of VCO with ultra-wideband frequency and consume low power could help to amplify the performance in phase-locked loop (PLL) application for example. The existence of high performance of PLL will further the development of wireless application and make better future.

The VCOs have been designed in various method. Two common types that been used for design VCO are LC-based oscillator and ring-based oscillator [4]. LC-based has narrow tuning range of frequency but much better in term of temperature, noise frequency stability and power supply compared to ring-based. Alternatively, the narrow tuning range can be overcome by adding the switched inductor, switched capacitors and variable active inductors [5]. These alternatives may extend the tuning range but it will increase the complexity of circuit which can affect the high power consumption. While, ring-based oscillator gives wider tuning range and usually used in monolithic IC due to small chip area occupied. Thus, it is more cost effective compared to LC-based [4], [6]. VCO is the important part in communication system and mainly used in designing the frequency synthesizer using phase locked loop (PLL) [1]. PLL frequency synthesizer offer very high level of stability and accuracy in communication system. In order to get these offers, a VCO with high performance is needed and implemented into that system. Thus, it is necessary to design the VCO with wider tuning range but simplicity and ease of integration [1].

2. Single-Ended Differential Pair of VCRO architecture

The proposed VCRO architecture implemented using CMOS three-stages single-ended differential pair configuration of ring oscillator. Figure 1 shows the circuit of the proposed VCRO with three delay stages.

![Figure 1. Proposed VCRO circuit architecture](image)

The transistor level circuit of the proposed VCRO consists of eight transistors which the upper part of circuit consists of four PMOSs while the lower part of circuit consists of four NMOSs as shown in Figure 2 implemented using Cadence tool in 130 nm CMOS technology. The control part of the PMOS and NMOS are set with length/width of 0.13 μm/1 μm and 0.13 μm/3 μm. On the other hand, the three stages of delay cell that combined together become ring oscillator are set with length/width of 0.13 μm/2 μm for PMOS and 0.13 μm/3 μm for NMOS. The simulation was carried out with a 1.3V supply.
voltage and voltage control varying between 0.5V to 2.5V with the load capacitance of 0.01pF. The frequency of 6 GHz with 1V of amplitude was applied for initial sinusoidal wave.

Figure 2. Proposed VCRO circuit implementation

3. Results and discussion

The setting of simulation was done by using Virtuoso Analog Design Environment with WaveScan Waveform Tool. The output waveform were evaluated and analysed by using WaveScan Waveform Tool. Figure 3 indicates the input of VCRO with power supply of 1.3V and voltage control of 2.5V at the initial sinusoidal frequency of 6 GHz and 1V amplitude. The simulation setting of transient analysis at the stop time of 20 ns. Figure 4 demonstrates the output of VCRO. Based on the output waveform, the oscillation frequency is calculated through WaveScan Calculator. The result shows the highest oscillation frequency is 9.651 GHz. Since the VCRO contains three stages of delay cell, the input pulse will be invert three times and gives the output with same shape but smaller voltage. Via manually calculation, the frequency also can be calculated using Equation 1

\[ f_{osc} = \frac{1}{T} \]  

where T indicate the period of waveform.
The result of transient analysis and DC operating point at various control voltage between 0.5 V to 2.5 V with initial frequency and amplitude of 6 GHz and 1 V, respectively was shown on Table 1. The static power and dynamic power are be calculated by using Equation 2 and Equation 3, respectively.

\[ P_{\text{static}} = I_{\text{total}} \times V_{DD} \]  

(2)

where \( I_{\text{total}} \) indicate the total current of overall current and \( V_{DD} \) is the voltage of power supply.

\[ P_{\text{dynamic}} = \text{Capacitor} \times V_{DD}^2 \times \text{Frequency} \]  

(3)

Thus, the total power can be measured with addition of static power and dynamic power, as shown on Equation 4.

\[ P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} \]  

(4)

Figure 3. Input waveform of VCRO

Figure 4. Output waveform of VCRO
Through investigation on Table 1, it was clearly that $V_{ctrl}$ is the variable that changes through the analysis and producing result in term of oscillation frequency and overall current. When the $V_{ctrl}$ is varied to 0.5 V, the overall current shows the lowest value which is 0.507 mA. Total power consumption by the circuit is the lowest which is 0.78 mW. In contrast, by setting the $V_{ctrl}$ to 2.5 V, the overall current reached 1.489 mA. This overall current affects and increases the power consumption through the circuit to 2.099 mW. In terms of oscillation frequency, minimum and maximum frequency can be achieved when the $V_{ctrl}$ is varied to 0.5 V and 2.5 V. From these values, the tuning range percentage and centre frequency can be determined through Equation (5) and (6). Based on the desired output oscillation frequency, tuning range can be measured using Equation.

$$\text{TR} \% = \left( \frac{f_{\text{max}} - f_{\text{min}}}{f_{\text{max}}} \right) \times 100\% \quad (5)$$

where $f_{\text{max}}$ indicate maximum frequency and $f_{\text{min}}$ indicate minimum frequency of desired oscillation.

$$f_{\text{centre}} = \left( \frac{f_{\text{max}} - f_{\text{min}}}{2} \right) + f_{\text{min}} \quad (6)$$

where $f_{\text{centre}}$ referred to centre frequency of oscillation

Based on Equation 5, the tuning range of this VCRO is:

TR (%) = \left( \frac{9.651 - 7.186}{9.651} \right) \times 100\%

TR (%) = 25.54 \%

Regarding to Equation 6, the centre frequency of oscillation is:

$$f_{\text{centre}} = \left( \frac{9.651 - 7.186}{2} \right) + 7.186 \text{ GHz}$$

$$f_{\text{centre}} = 8.42 \text{ GHz}$$

The VCRO tuning range is 25.54% while $f_{\text{centre}}$ is 8.42 GHz as shown in Table 1, offer better tuning range to allow the VCRO to operate at variety of frequencies. On the other hand, the value of $f_{\text{centre}}$ is used to find the figure of merit (FOM).

| $V_{ctrl}$ (V) | Frequency (GHz) | $I_{\text{total}}$ (mA) | $P_{\text{static}}$ (mW) | $P_{\text{dynamic}}$ (mW) | $P_{\text{total}}$ (mW) |
|----------------|-----------------|-------------------------|--------------------------|---------------------------|------------------------|
| 0.5            | 7.186           | 0.507                   | 0.659                    | 0.121                     | 0.780                  |
| 1.0            | 8.179           | 1.456                   | 1.893                    | 0.138                     | 2.031                  |
| 1.5            | 9.283           | 1.482                   | 1.927                    | 0.157                     | 2.084                  |
| 2.0            | 9.632           | 1.488                   | 1.934                    | 0.163                     | 2.097                  |
| 2.5            | 9.651           | 1.489                   | 1.936                    | 0.163                     | 2.099                  |

Figure 5 demonstrates the output noise of the VCRO. The simulation setting was set with noise analysis. It can be investigated that the overall output noise of the VCRO is -153.1 dBc/ Hz at a 1MHz offset frequency and -162.0 dB/ Hz at a 10 MHz offset frequency.
Figure 5. Output noise of VCRO

Through overall analysis, the FOM can be determined. FOM is used to estimate the performance of VCRO [1] and can be calculated using Equation 7.

\[
FOM = P_{\text{noise}} - 20 \log \left( \frac{f_{\text{centre}}}{f_{\text{off}}} \right) - 10 \log \left( \frac{P_{\text{diss}}}{1\,\text{mW}} \right)
\]  

(7)

where \( P_{\text{noise}} \) indicates the output noise with an offset frequency, \( f_{\text{centre}} \) is centre frequency and \( f_{\text{off}} \) is offset frequency, and \( P_{\text{diss}} \) is the dissipated power by VCRO.

By using Equation (7), at a 1 MHz offset frequency, the FOM of the VCRO can be calculated as:

\[
FOM = P_{\text{noise}} - 20 \log \left( \frac{f_{\text{centre}}}{f_{\text{off}}} \right) - 10 \log \left( \frac{P_{\text{diss}}}{1\,\text{mW}} \right) 
\]

\[
FOM = -153.1 \, \text{dBc/Hz} - 20 \log \left( \frac{0.42\,\text{GHz}}{1\,\text{MHz}} \right) - 10 \log \left( \frac{0.99\,\text{mW}}{1\,\text{mW}} \right) 
\]

\[
FOM = -234.83 \, \text{dBc/Hz} 
\]

Hence, by putting the entire variables in Equation (7), the FOM of this VCRO can be determined. At a 1 MHz offset frequency, the FOM is -234.83 dBc/Hz and at a 10 MHz offset frequency, the FOM is -223.73 dBc/Hz. The values of FOM is depends on the output noise The low value of FOM offers better performance of the VCRO. The results of the overall analysis are encapsulate in Table 2.
Table 2. Result summary of VCRO at different parameters

| Result of Analysis                                      | This Work |
|---------------------------------------------------------|-----------|
| Frequency Maximum                                       | 9.651 GHz |
| Frequency Minimum                                       | 7.186 GHz |
| Maximum Power Dissipation                               | 2.099 mW |
| Minimum Power Dissipation                               | 0.778 mW |
| Tuning Range                                            | 25.54%    |
| Centre Frequency                                        | 8.42 GHz  |
| Output Noise @ 1MHz                                     | -153.1 dBc/ Hz |
| Output Noise @ 10MHz                                     | -162.0 dBc/ Hz |
| FOM @ 1MHz                                              | -234.83 dBc/ Hz |
| FOM @ 10MHz                                             | -223.73 dBc/ Hz |

Based on Table 3, this work is the third lowest power consumption when compared to [2] and [14] but achieved higher tuning range with 3.32% increases. Comparing to research in [1], even though it has the widest tuning range, but this proposed work has better power consumption. In terms of output noise, this proposed work have better noise performance compared to other previous work with using the same technology with increasing of 80.54% from research in [1].

Table 3. Comparison of VCRO at different parameters with same technology

| No. | Year | Technology (nm) | Power (μW) | Frequency (GHz) | Tuning Range (%) | Output noise (dBc/ Hz) |
|-----|------|-----------------|------------|-----------------|------------------|------------------------|
| This work | 2017 | 130             | 778        | 7.186-9.651     | 25.54            | -153.1 @ 1MHz          |
| [6]  | 2016 | 130             | 835        | 3.328-4.606     | 27.75            | -74.5 @ 1MHz           |
| [14] | 2015 | 130             | 750        | 3.500-4.500     | 22.22            | -79 @ 1MHz             |
| [5]  | 2013 | 130             | 50         | 3.500-4.500     | 22.22            | -79 @ 1MHz             |
| [1]  | 2008 | 130             | 7020       | 3.400-7.630     | 55.43            | -84.8 @ 1MHz           |

Figure 6 shows the layout circuit of three-stage VCRO with single-ended differential pair configuration. The three-stage ring oscillator of PMOS and NMOS were set with width of 2μm and 3μm respectively. Meanwhile, the control PMOS and NMOS were having width of 1μm and 3μm, respectively. The total layout area size of yield VCRO without the bonding pad is 11.80 μm X 9.9 μm (116.82 μm²)
Figure 6. Layout circuit of three-stage VCRO

This VCRO has successfully passed DRC and ERC verification without any error occurred as the design followed all the rules and can be proceeding to next physical verification. The LVS was also done and pass successfully.

4. Conclusion

The proposed three stage of voltage-controlled ring-oscillator (VCRO) with single –ended differential pair architecture have been designed that able to operate in the range of frequencies of 7.186 to 9.651GHz at power supply of 1.3V implemented in 130nm CMOS technology. It has wide tuning range which is 25.54% with the power consumption of 0.78mW.

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