Circuit-aware Device Modeling of Energy-efficient Monolayer WS$_2$ Trench-FinFETs

Tarun Agarwal, Yoseung Lee, and Mathieu Luisier

Abstract—The continuous scaling of semiconductor technology has pushed the footprint of logic devices below 50 nm. Currently, logic standard cells with one single fin are being investigated to increase the integration density, although such options could severely limit the performance of individual devices. In this letter, we present a novel Trench (T-) FinFET device, composed of a monolayer two-dimensional (2D) channel material. The device characteristics of a monolayer WS$_2$-based T-FinFET are studied by combining the first-principles calculations and quantum transport (QT) simulations. These results serve as inputs to a predictive analytical model. The latter allows to benchmark the T-FinFET with strained (s)-Si FinFETs in both quasi-ballistic and diffusive transport regimes. The circuit-level evaluation highlights that WS$_2$ T-FinFETs exhibit a competitive energy-delay performance compared to s-Si FinFET and WS$_2$ double-gate transistors, assuming the same mobility and contact resistivity at small footprints.

Index Terms—2D materials, monolayer WS$_2$ FinFET, multi-scale modeling, benchmarking, strained-Si FinFETs.

I. INTRODUCTION

The technology scaling has necessitated the downsizing of contacted gate pitch (CGP) and minimum footprint ($W_{foot}$) of contemporary FinFETs to achieve Power-Performance-Area (PPA) requirement of sub-10 nm technology nodes [1]. As the next technology option, one-fin device might be considered for their potential to reduce the footprint. In such configurations, only few process parameters can control the performance of FinFETs, for example: the fin height ($H_{fin}$). Alternatively, a different channel material with better transport properties than silicon could be used [2].

Recently, two-dimensional (2D) materials have emerged as promising candidates to build the next-generation high-performance transistors thanks to their attractive electrical and mechanical properties [3]. Among them, monolayer WS$_2$, a so-called transition-metal-dichalcogenide (TMD), has attracted considerable attention from the semiconductor community. Indeed, WS$_2$-based transistors promise high ON-state currents owing to the low transport effective mass, high intrinsic carrier mobility [4], [5], and excellent electrostatics associated with the 2D channel. Hence, monolayer WS$_2$ shows great prospects for future sub-10 nm gate length transistors [6].

In this letter, we investigate the potential of an alternative 2D material device, the WS$_2$ Trench (T-) FinFET, at a device footprint of 24 nm. Its electrical behavior is evaluated through first-principles and quantum transport (QT) calculations combined with circuit-level simulations, as explained in Section II. The electronic properties of the fin-shaped monolayer WS$_2$ are first obtained from density functional theory [7] and then passed to a ballistic QT solver [8] to calculate the current vs. voltage and capacitance vs. voltage characteristics. In Section III, we benchmark the energy efficiency of the WS$_2$ T-FinFET with the WS$_2$ double-gate FET and strained (s)-Si FinFET studied in our previous work [9]. The WS$_2$ T-FinFET shows lower energy consumption and delay than s-Si FinFET for the same channel mobility.

Fig. 1. Methodology a) Creation of a bent atomic monolayer WS$_2$ structure mimicking its deposition on a SiO$_2$ fin, b) Electronic band-structure calculation of the atomic cell with and without bending using first-principles calculations, c) Simulation of the monolayer WS$_2$-based T-FinFET over one fin pitch with a ballistic QT solver, d) Extraction of effective gate capacitance ($C_{G}$), sub-threshold slope (SS) and drain-induced barrier lowering ($\delta$), from QT calculations and insertion of them into a predictive analytical model [11] to obtain the “I-V” characteristics of the T-FinFET, e) Ring-oscillator simulation with the analytical model of [12] and derivation of relevant circuit-level metrics such as delay and energy-consumption.
| $\alpha_{\text{bend}}$ ($^\circ$) | $w_{\text{fin}}$ (Å) | $h_{\text{fin}}$ (Å) | $m^*_v$ (Valley) ($^*\mu_0$) | $m^*_h$ (Valley) ($^*\mu_0$) | $E_G$ (eV) |
|---|---|---|---|---|---|
| 0 | 285 | – | 0.33 (K) | 0.5 (K) | 1.75 |
| 48 | 261 | 62 | 0.32 (K) | 2.0 (Γ) | 1.22 |
| 60 | 241 | 74 | 0.32 (K) | 2.0 (Γ) | 1.27 |
| 72 | 219 | 84 | 0.32 (K) | 2.0 (Γ) | 1.26 |
| 72 | 424 | 160 | 0.32 (K) | 2.0 (Γ) | 1.09 |

**II. METHODOLOGY**

Our circuit-aware device modeling methodology is outlined in Fig. 1. First, the monolayer WS$_2$ is bent with an angle ($\alpha_{\text{bend}}$) to generate the required T-Fin shape, which resembles the conventional Fin shape (Fig. 1(a)). The electronic structure of the bent monolayers is then computed from the first-principles VASP simulator [7] and the generalized gradient approximation (GGA) of Perdew, Burke, and Ernzerhof (PBE) [10]. Table I summarizes the width and height of the considered fin-shaped WS$_2$ monolayers ($w_{\text{fin}}$ and $h_{\text{fin}}$), and the corresponding electron/hole effective masses ($m^*_v/m^*_h$) and bandgap ($E_G$) for different $\alpha_{\text{bend}}$ values. It is worth noting that the band curvature or $m^*_h$ at the conduction band minimum (CBM) remains unchanged, regardless of the bending angle, while the location of the valence band maximum (VBM) changes from K-valley to Γ-valley resulting in a change in $E_G$, as shown in Fig. 1(b). This finding allows us to safely resort to the effective mass approximation to perform quantum transport simulations within the non-equilibrium Green’s function (NEGF) formalism, thus making the investigation of realistic device structures possible.

Fig. 1(c) shows the schematic of the WS$_2$ T-FinFET with a fin pitch (FP) = 24 nm and $W_{\text{fin}} = 5$ nm. Here, the device simulation domain in the width direction is set to one FP. The quasi-ballistic/diffusive device characteristics are then calculated by combining the ballistic QT simulations and the predictive analytical model, shown in Fig. 1(d), to account for the scattering in the WS$_2$ channel. In this approach, the key device parameters are first extracted from ballistic QT, e.g., the effective gate capacitance ($C_G$), sub-threshold slope (SS), and drain-induced barrier lowering ($\delta$). The extracted parameters are then injected into the predictive analytical model to calculate the effective drain currents. Fig. 1(d) also compares the ballistic and quasi-ballistic transfer characteristics of monolayer WS$_2$ T-FinFET that are obtained from QT simulations and from the predictive analytical model, respectively. The ratio of effective ON current ($I_{\text{ONeff}}$) and ballistic ON current ($I_{\text{ONball}}$) is indicated to be 0.39 at $V_{GS}=0.7$ V. Interestingly, as indicated in Fig. 1(c), WS$_2$ T-FinFET comprises of two additional planar monolayer WS$_2$ FETs in the trench. It then shows more effective device width ($W_{\text{dev}} = 2*(W_{\text{ext}}+H_{\text{fin}})+W_{\text{fin}}$) within one FP than s-Si FinFETs ($2*H_{\text{fin}}+W_{\text{fin}}$). For a FP of 24 nm, the maximum width of these planar FETs is 6.8 nm, taking into account the 0.7 nm thickness of monolayer WS$_2$, 0.5 nm of the SiO$_2$ interfacial layer, and 1.5 nm of the HfO$_2$ dielectric layer.

Finally, to assess the circuit-level metrics, we perform the ring-oscillator (RO) simulations including the device and interconnect parasitics, using Cadence Spectre Simulation Platform [13]. The parasitic capacitances ($C_{\text{par}}$) depend on the FET architectures and are calculated using the analytical expressions proposed in [14], [15]. The wire capacitance ($C_w = 0.27$ fF/μm) and resistances ($R_w = 317 \Omega/\mu\text{m}$) are included between each RO stage in the circuit-level simulation, with a wire length of 50 CGP, as shown in Fig. 1(e). The contact resistivity ($\rho_{\text{C}}$) is chosen to be $10^{-8}$ Ω·cm$^2$, which corresponds to a contact resistance of 100 $\Omega$·μm for a contact length of 10 nm. We also assume balanced nFET and pFET performance in the RO simulation. Hence, the circuit evaluation primarily benchmarks the n-channel devices. To show the energy-efficiency of different device options, the energy-delay product (EDP) is chosen as the central figure-of-merit in this letter.

**III. RESULTS AND DISCUSSION**

Fig. 1(d) shows the transfer characteristics of WS$_2$ T-FinFET for a fixed FP = 24 nm and $H_{\text{fin}} = 15$ nm, with an intrinsic phonon-limited electron mobility $\mu = 360$ cm$^2$/V·s [5]. The effective device width can be controlled by changing either the fin height ($H_{\text{fin}}$) or the extensions of the channel width ($W_{\text{ext}}$). Only a change in $W_{\text{ext}}$ affects the FinFET footprint ($W_{\text{foot}} = FP$) while $H_{\text{fin}}$ does not. Fig. 1(a) exhibits that the $I_{\text{ONball}}$ obtained from QT framework scales linearly with $W_{\text{dev}}$, i.e., with both $H_{\text{fin}}$ and $W_{\text{ext}}$. This is due to the rather uniform distribution of the charge density across the fin-shaped WS$_2$ channel, as highlighted in Fig. 2(b).

**Device characteristics**, a) Ballistic ON current with effective device width ($W_{\text{dev}}$) for different $H_{\text{fin}}$ and $W_{\text{ext}}$, b) Charge density in the WS$_2$ channel distributed across the T-FinFET width (y) and height (z) at $V_{GS}=0.61$ V and $V_{DS}=10$ mV, c) Comparison of the effective ON current of a WS$_2$-based T-FinFET and double-gate (DG) FET as a function of the device footprint ($W_{\text{foot}}$). Here, $I_{\text{OFF}}$ is set to 100 nA/μm (2.4 nA for FP=24 nm), d) Comparison of the $I_{\text{OFF}}$ characteristics of a WS$_2$-based T-FinFET and DG-FET as well as s-Si FinFET at $V_{PD}=0.61$ V. The source and drain extension lengths are set to 15 nm for all cases.

Fig. 2(c) compares the $I_{\text{ONeff}}$ of WS$_2$-based T-FinFETs with different fin heights to that of double-gate (DG) FET for device footprints ($W_{\text{foot}}$) ranging between 15 and 40 nm. It appears that the DG FETs are only beneficial at footprints...
larger than 30 nm. By increasing $H_{fin}$, the T-FinFET can always outperform the DG FET, demonstrating the advantage of the proposed architecture. Next, we compare the transfer characteristics of the WS$_2$-based T-FinFET and DG FET to those of a conventional s-Si FinFET in Fig. 2(d), using $C_G$, SS and $\delta$ values listed in Table II. Thanks to their atomic layer thickness, the T-FinFET and DG-FET show a better gate controllability than the s-Si FinFET. However, the performance of these device architectures need to be compared at the circuit-level by combining the device characteristics with parasitic capacitances and resistances.

Fig. 3 shows the “EDP vs delay” between WS$_2$ T-FinFET, DG FET, and s-Si FinFET for different $H_{fin}$, supply voltage ($V_{DD}$), and contact resistivity ($\rho_C$). In this study, the bottom-left corner of each plot represents the sweet spot corresponding to those of a conventional s-Si FinFET in Fig. 2(b), using characteristics of the WS$_2$ of the proposed architecture. Next, we compare the transfer parasitic capacitances and resistances.

In Fig. 3(a), we see that the WS$_2$ T-FinFET promises better circuit-level energy-efficiency (i.e. lower EDP) at higher mobility values, e.g. 40 cm$^2$/Vs, which is the result of charged impurity scattering in WS$_2$ with an impurity concentration $N_{imp}=1.35 \times 10^{12}$ cm$^{-2}$ [5], the EDP of the WS$_2$ T-FinFET is 26% lower than that of the s-Si FinFET for the same delay. The advantage of T-FinFET is about the same (28% lower EDP) at higher mobility values, i.e. 600 cm$^2$/Vs.

The effect of $\rho_C$ on the EDP is highlighted in Fig. 3(c) at different $H_{fin}$. The insets show a larger EDP increase at high $H_{fin}$ for the s-Si FinFET than the WS$_2$ T-FinFET due to its higher total capacitance. Also, $\rho_C$ values below $1 \times 10^{-9}$ $\Omega$.cm$^2$ do not have any significant impact on the EDP, while a change in $\rho_C$ from $1 \times 10^{-8}$ to $1 \times 10^{-9}$ $\Omega$.cm$^2$ results in 18 and 23% lower EDPs for the WS$_2$ T-FinFET and s-Si FinFET, respectively.

IV. CONCLUSION

The electron/hole effective masses and bandgaps of fin-shaped monolayer WS$_2$ have been computed using the first-principles. It is found that the $m_e^*$ does not change with the bending angle. For the benchmarking, the energy-delay product of the WS$_2$ T-FinFET has been compared to the WS$_2$ DG-FET as well as the s-Si FinFET through a circuit-aware device modeling framework. It has been shown that the WS$_2$ T-FinFET can outperform the s-Si FinFET with the same channel mobility and contact resistivity. For supply voltages above 0.5 V, the WS$_2$ T-FinFET promises better circuit-level performance than the WS$_2$ DG-FET.

TABLE II

| Device       | $L_G$ (nm) | $C_G$ ($\mu$F/$\mu$m$^2$) | SS (mV/dec) | $\delta$ (V/V) |
|--------------|-----------|---------------------------|-------------|----------------|
| WS$_2$ DG    | 12        | 360                       | 60.76       | 0.05           |
| WS$_2$ T-FinFET | 12        | 360                       | 2.9         | 0.075          |
| s-Si FinFET  | 12        | 680                       | 75.28       | 0.1            |

REFERENCES

[1] D. Yakimets, M. Garcia Bardon, D. Jang, P. Schuddinck, Y. Sherazi, P. Weckx, K. Miyaguchi, B. Parvais, P. Raghavan, A. Spesot, D. Verkest, and A. Mocuta, “Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology,” in IEDM Tech. Dig., San Francisco, CA, USA, pp. 20.4.1-20.4.4, Dec. 2017. DOI: 10.1109/IEDM.2017.8268429

[2] M.L. Chen, X. Sun, H. Liu, H. Wang, Q. Zhu, S. Wang, H. Du, B. Dong, J. Zhang, Y. Sun, and S. Qiu, “A FinFET with one atomic layer channel,” Nat. Commun., vol. 11, no. 1205, pp. 1-7, Mar. 2020. DOI:10.1038/s41467-020-15956-0

[3] S. Wachter, D.K. Poluyashkin, O. Bethge, and T. Mueller, “A microprocessor based on a two-dimensional semiconductor,” Nat. Commun., vol. 8, no. 14948, pp. 1-7, Apr. 2017. DOI:10.1038/ncomms14948

[4] Z. Jin, X. Li, J. T. Mullen, and K. W. Kim, “Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides,” Phys. Rev. B, vol. 90, no. 4, pp. 045422(1)-045422(7), July 2014. DOI:10.1103/PhysRevB.90.045422

[5] Y. Lee, S. Fiore and M. Laisier, “Ab initio mobility of single-layer MoS$_2$ and WS$_2$: comparison to experiments and impact on the device characteristics,” in IEDM Tech. Dig., San Francisco, CA, USA, pp. 24.4.1-24.4.4, Dec. 2019. DOI:10.1109/IEDM195773.2019.8993477

[6] T. K. Agarwal, B. Soare, I. Radu, P. Raghavan, G. Iannaccone, G. Fiori, W. Dehaene, and M. Heyns, “Material-Device-Circuit Co-optimization of 2D Material based FETs for Ultra-Scaled Technology Nodes,” Scientific reports, vol. 7, no. 5016, pp. 1-7, July 2017. DOI:10.1038/s41598-017-04553-3

[7] G. Kresse and J. Furthmüller, “Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set,” Phys. Rev. B, vol. 54, no. 16, pp. 11169-11186, Oct. 1996. DOI:10.1103/PhysRevB.54.11169

Fig. 3. Circuit-level benchmarking of WS$_2$ T-FinFET, DG FET, and s-Si FinFET for C$_{GS}$= 42 nm, a spacer length of 10 nm and permittivity of 3.9. The Energy-Delay Product (EDP) vs. delay is shown as a function of (a) $V_{DD}$ for different $H_{fin}$ at $\mu_{s,WS_2}=360$ (680) cm$^2$/Vs and $\rho_C=1 \times 10^{-8}$ $\Omega$.cm$^2$, (b) $V_{DD}$ for different mobility values at $H_{fin}=60$ nm and $\rho_C=1 \times 10^{-8}$ $\Omega$.cm$^2$, and (c) $H_{fin}$ for different contact resistivity values at $\mu_s=600$ cm$^2$/Vs and $V_{DD}=0.7$ V.

Going one step further, to understand the role of the channel mobility ($\mu$), we compare the WS$_2$ T-FinFET and s-Si FinFET in the quasi-ballistic (high $\mu$) and diffusive (low $\mu$) regimes, as shown in Fig. 3(b). The WS$_2$ T-FinFET appears as a better device option than the s-Si FinFET at constant channel mobility and contact resistance. At small mobility values, e.g. 40 cm$^2$/Vs, which is the result of charged impurity scattering in WS$_2$ with an impurity concentration $N_{imp}=1.35 \times 10^{12}$ cm$^{-2}$ [5], the EDP of the WS$_2$ T-FinFET is 26% lower than that of the s-Si FinFET for the same delay. The advantage of T-FinFET is about the same (28% lower EDP) at higher mobility values, i.e. 600 cm$^2$/Vs.
[8] M. Luisier and A. Schenk, “Two-Dimensional Tunneling Effects on the Leakage Current of MOSFETs With Single Dielectric and High-κ Gate Stacks,” in *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1494-1501, June 2008. DOI: 10.1109/TED.2008.922493.

[9] T. K. Agarwal, M. Rau, I. Radu, M. Luisier, W. Dehaene and M. Heyns, “Performance Comparison of s-Si, In$_{0.53}$Ga$_{0.47}$As, Monolayer BP, and WS$_2$-Based n-MOSFETs for Future Technology Nodes-Part I: Device-Level Comparison,” in *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3608-3613, Aug. 2019. DOI:10.1109/TED.2019.2912005.

[10] J. P. Perdew, K. Burke, and M. Ernzerhof, “Generalized Gradient Approximation Made Simple,” *Phys. Rev. Lett.*, vol. 77, no. 18, pp. 3865-3868, Oct. 1996. DOI:10.1103/PhysRevLett.77.3865.

[11] T. Agarwal, A. Szabo, M.G. Bardon, B. Soree, I. Radu, P. Raghavan, M. Luisier, W. Dehaene, and M. Heyns, “Benchmarking of monolithic 3D integrated MX$_2$ FETs with Si FinFETs,” in *IEDM Tech. Dig.*, San Francisco, CA, USA, pp. 5.7.1-5.7.4, Dec. 2017. DOI:10.1109/IEDM.2017.8268336.

[12] S. Rakheja and D. Antoniadis, “MVS Nanotransistor Model (Silicon),” *nanoHUB* (Version 1.1.1), 2015. DOI:10.4231/D3RR1PN6M.

[13] Cadence Spectre Simulator. Accessed: 2021. [Online]. Available: http://www.cadence.com/products/cic/spectrecircuit/pages/default.aspx.

[14] J. Lacord, G. Ghibaudo and F. Boeuf, “Comprehensive and Accurate Parasitic Capacitance Models for Two- and Three-Dimensional CMOS Device Structures,” in *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1332-1344, May 2012. DOI: 10.1109/TED.2012.2187454.

[15] T. K. Agarwal, M. Rau, I. Radu, M. Luisier, W. Dehaene and M. Heyns, “Performance Comparison of s-Si, In$_{0.53}$Ga$_{0.47}$As, Monolayer BP, and WS$_2$-Based n-MOSFETs for Future Technology Nodes-Part II: Circuit-Level Comparison,” in *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3614-3619, Aug. 2019. DOI: 10.1109/TED.2019.2923820.