FPGA-based low-cost synchronized fiber network for experimental setups in space

T. Oberschulte, a, T. Wendrich b and H. Blume a

a Institute of Microelectronic Systems, Leibniz Universität Hannover, Appelstraße 4, 30167 Hannover, Germany
b Institute of Quantum Optics, Leibniz Universität Hannover, Welfengarten 1, 30167 Hannover, Germany

E-mail: tim.oberschulte@ims.uni-hannover.de

ABSTRACT: Custom experiment setups in physics often require control electronics to execute actions and measurements on a small time scale. When further constraints limit the experiment’s environment, for example when the experiment is inside a sounding rocket, conventional network systems will not suffice those constraints because of weight, heat or budget limitations. This paper proposes a network architecture with a time resolution of less than 1 ns over a pair of plastic fibers while using low-cost commercial hardware. The plastic fibers in comparison to copper fibers have a low weight and additionally can isolate parts of the setup galvanically. Data rates of 40 Mbit s⁻¹ enable the network to transfer large amounts of measurements and configuration data over the network. Proof-of-concept implementations of network endpoints and switches on small FPGAs are analyzed in terms of synchronicity, data rate and resource usage. Using commercial parts the resolution of 1 ns is reached with a standard deviation of less than 100 ps. Compared to a copper wire implementation the weight is reduced by about one order of magnitude. With its low weight at a low cost, the network is useful in space or laboratory setups which require high time resolution.

KEYWORDS: Trigger concepts and systems (hardware and software); Space instrumentation; VLSI circuits

ArXiv ePrint: 2109.11638

*Corresponding author.
1 Introduction

Complex control electronics are often required for modern physics experiments. In bigger setups, those electronic components may even be located far away from each other but need to communicate and execute commands with precise isochronous timing. When experimenting in limiting surroundings, like aboard a sounding rocket or in orbital flight in space, additional constraints will come along, e.g. weight limits or system heat dissipation limitations. Two missions where such limitations apply are discussed here.

In 2017 the first Bose-Einstein condensate (BEC) has been created on board a sounding rocket in MAIUS-A [1]. In two follow-up missions, the MAIUS-B [2] and Bose-Einstein Condensate Cold Atom Laboratory (BECCAL) [3] projects, two different atomic species will be used for creating BECs aboard a rocket and on the International Space Station (ISS). For those two new projects several new requirements arose in terms of weight, routing complexity, isolation, synchronicity, data rates and financial budget.

As an additional laser system and other new parts will increase the volume and mass of the design, several parts have to become smaller and lighter to fit into the rocket and not exceed its take-off weight. The approach to improve the communication system’s weight is a reduction of cables and connectors: the MAIUS-A apparatus had many meters of separate copper wires for clock, data, address selection and trigger signals. The goal is to replace most of those cables by a single connection, which is easy to route through the setup.

Especially in the BECCAL project, which occupies three separately powered lockers on ISS, but also in lab-setups, the electrical ground potential of different electronic experiment parts may not be the same. Thus, a galvanic isolation in the communication system is useful to prevent ground level shifting. This can be achieved by using optical fibers instead of copper cables.
For the BEC experiments a central trigger impulse is needed, which arrives at all endpoints in deterministic time. For repeatability those trigger signals require a jitter performance in the nanosecond scale and have to keep the same offsets even when power-cycling the experiment.

All reconfigurable electronic parts of BECCAL should be programmable while in orbit for flexibility and for the possibility of error mitigation. Therefore, the network must be capable of sending bitstreams or device images of multiple megabytes in size quickly, to reduce the experiment’s downtime.

Finally, the system is limited on using hardware which is low on power, thermal dissipation and fits the small budget. In this case only commercial off-the-shelf (COTS) and small form factor hardware may be used. As the endpoints will interface with highly specialized custom sensors and actuators at a high speed, Field Programmable Gate Arrays (FPGAs) are used, which will provide the performance needed for the communication stack while staying in the mentioned budgets.

Possible candidates for the communication system are real-time Ethernet (e.g. Profinet or Ethernet POWERLINK), SpaceWire or SpaceFibre [4–6]. Profinet does not suffice the required timing constraints, does not prevent ground level shifts and a typical interface implementation is too large for smaller COTS FPGAs [7, 8]. Another Ethernet-based candidate presented by Födisch et al. in 2016 has a resolution of 8 ns but again is too large and is not isolated [9]. While SpaceWire is also based on electrical connection, which does not fulfill the galvanic isolation requirement, its successor SpaceFibre seems promising. But as for real-time Ethernet, a typical interface implementation is also too large for smaller FPGAs, especially when switches with multiple ports in the network are needed. Key points of those technologies are shown in table 2 in section 4.

In section 2 a proposed communication system which fulfills the requirements listed above will be described. The design choices to implement high synchronicity while maintaining a low complexity are explained in sections 2.1 and 2.2. Afterwards, the evaluation of the system’s main goals is described and the results are discussed in section 3.

2 System design

The proposed communication system has a tree topology and consists of a single host as the tree root, multiple switches for branching and endpoints as tree leaves. The communication between two hops of the network is realized via plastic optical fibers, one for each transmission direction: the fiber transmitting data and timing information from a master port to the slave port is called Tx fiber, the receiving one is called Rx fiber. The host is the master of the whole network. Only master ports are implemented here, which supply a clock to the connected slave ports. There may be multiple hosts in a network for failover. Switches have master and slave ports, which forward communication requests originating from a connected device. Multiple slave ports may be configured at a switch for redundancy. An endpoint only has slave ports and is the termination point of communication in the network. Transported user data payloads will be processed there.

Figure 1 exemplarily shows the planned network for the BECCAL project divided into the control electronics, the physics package and the laser system. The endpoints are electronic boards with a stackable PC/104-like connector. They drive sensors and actuators on boards stacked onto them by executing commands from the network, for example the laser phase-lock in the laser system.
or the electromagnets of magneto-optical traps in the physics system. The BEC experiments are controlled by a computer which is connected to the host by Ethernet.

Figure 1. Planned network topology for the BECCAL apparatus. Plastic optical fiber connections (in pairs of Tx and Rx fibers) run between the host, the switches and the endpoint cards. The network is controlled by a computer connected via Ethernet.

The use of a single plastic optical fiber pair instead of multiple wires reduces the weight and routing complexity and also provides galvanic isolation. In sections 2.1 and 2.2 the design decisions are described to implement synchronization and maintaining a high data rate while using fewer resources.

2.1 Network synchronicity

One main goal of the network is to provide a method for precise deterministic global timing. The network should keep the same communication delays and behavior even if it is restarted. Therefore, deterministic synchronization of transmitted bits and symbols is needed.

Bit synchronization of the network is performed by using a protocol which encapsulates data in a timing-recoverable signal for the Tx fiber. The used base clock is three times faster than the bit rate: every data bit transmission takes three cycles, starting with a logical 1 (high) followed by the actual data bit and a logical 0 (low) for one cycle each. Thus, every third clock cycle a rising edge occurs, on which a phase-locked loop (PLL) at a following slave port deterministically can lock onto. The slave can sample the data bits on the falling edges of that recovered clock. Figure 2 shows an example of the Tx fiber protocol.
Figure 2. Block and timing diagram of the Tx fiber bit level protocol for a transmission from a master to a slave. The slave’s PLL locks onto the rising edges of the Tx fiber signal (first marked orange). The transmitted data bit sequence is 101, each actual data bit is marked by a circle and sampled on the falling edge of the recovered slave clock.

The Rx fiber protocol does not contain information for timing recovery. The data bits are transferred “as-is” on a base clock with a third of the frequency of the Tx fiber base clock. They can be decoded at the receiver by oversampling.

Symbol synchronization is done by encoding every byte with the 8b/10b line code described by Widmer and Franaszek which adds a running disparity and multiple in-band signaling and synchronization words [10]. It redundantly encodes every data byte as 10 bit symbols on the line. Some symbols not used for data bytes are used as control words. In the beginning and when a point-to-point connection does not transmit data, an idle symbol is transmitted. The special 8b/10b comma symbols’ sequences of bits, K.28.1 and K.28.5, cannot occur as a part of another valid 8b/10b symbol stream (they are prefix-free) and thus can be used for synchronization by detecting the start of a valid symbol in the bitstream.

Using the bit and symbol synchronization methods, a slave device can deterministically lock its clock and symbol processing onto a master device. At this point a trigger symbol can be inserted, which can be used for synchronous triggering at the endpoints: the trigger symbol is a special 8b/10b control symbol which can be sent at any time. When the host sends a trigger symbol, all switches will immediately forward it to their connected devices. As all point-to-point connections deterministically are bit and symbol synchronous with a constant phase shift and the trigger symbol is forwarded with a constant delay at switches, the latencies of a trigger symbol distributed from the host to all endpoints is constant, too. Those latencies can be measured beforehand and can be used to synchronize the trigger execution at endpoints by using high frequency counters.
2.2 Implementation complexity and transfer speeds

To provide high throughput and low resource usage in the implemented system, a simple data structure and addressing scheme should be defined which does not need complex routing structures or address tables. The user data is embedded in packets which contain the destination address by which they are routed to their destination. A packet begins with the transmission of a Start of Packet (SOP) 8b/10b control symbol, followed by a packet header which contains fields for the destination and source address. Afterwards the payload is transferred and the packet finished with sending the 8b/10b control symbol End of Packet (EOP). By design the packets are not limited in size. Figure 3 shows the fields of a data packet.

**Figure 3.** Transport layer data packet fields from bit 7 (MSB) down to bit 0. Start and end are indicated by 8b/10b control words apart the data stream.

The destination address nibble (4 bit) fields are simply the port numbers at the host or switches to which the packet should be forwarded. Every switch will forward the packet to the port in \( \text{Dst.Addr}[0] \) with the destination fields shifted to the right by one nibble, removing the used part and adding four zero bits at \( \text{Dst.Addr}[3] \). When a packet arrives with a 0 for \( \text{Dst.Addr}[0] \) its destination has been reached and the device can process the contents. Every device in the network of up to 4 hops and with up to 14 slave devices (one address is the master port, and address 0 is the local device) can be addressed that way. Simultaneously the source address fields at every hop are filled with the port where the packet arrived to provide a reply address for the packet. The shifting is shown in figure 4.

With this addressing scheme any intermediate device only needs a buffer of 2 Bytes for the destination address fields to initially determine the target port and shift the address. After adding the source port to the shifted source address all other data just can be forwarded. No address tables are needed, which reduces the need of complex logic constructs. Only the host needs to know the network’s topology for sending packets as the reply address of a packet is generated on the fly when traversing the network. Because the packets do not need to be buffered at every hop and can be passed through after 2 Bytes, low delays and high data rates are possible.
Figure 4. Address part modification at an intermediate device. The packet is coming in on port $P$. The destination addresses are shifted to the right by one entry, the incoming port number is added to the source address on the right.

For flow control two different 8b/10b idle symbols can be sent: one to signal the availability of buffer capacity (ready to receive) and another to signal that the buffer is running full (not ready to receive). Those idle symbols propagate back through the network to momentary stop transmission of new data. A hysteresis on the buffer levels can be used to block or unblock the connection. The buffer should only be used to temporarily store data while the network is throttled down automatically by flow control and usually data should be forwarded immediately. Therefore, only several bytes need to be added as buffers at intermediate devices.

3 Measurement and evaluation

The system described in section 2 was implemented using Intel MAX10 and Microchip SmartFusion2 FPGAs. The circuit boards for a host device, a switch and an endpoint were designed and the FPGA firmware for each was implemented. The hardware is shown in figure 5.

The host device uses a Microchip SmartFusion2 System on a Chip (SoC) and functions as a bridge from Ethernet into the fiber network. Its ARM Cortex-M3 hard processing system is used for Ethernet and TCP operations and packet processing. The FPGA fabric is used for the fiber protocol’s transport layer encoding and hardware interface access. It generates the main clock signal for the network and can send global triggers. It is based on an evaluation board for prototyping purposes.

The switch is implemented on an Intel MAX10 FPGA and is configured to have one upstream (slave) port, where it recovers its clock from, and seven downstream (master) ports where other switches or endpoints can be connected. The internal configuration of the switch can be accessed by a virtual interface at port 0 (the local device address) which makes the switch usable like an endpoint. It also contains an SMA connector trigger output for debugging.

The endpoint implementation is also implemented on an Intel MAX10 FPGA. This endpoint has a configurable trigger unit for precisely triggering cards stacked onto it via the two PC/104-like connectors which contain 10 separate trigger lines.

3.1 Weight and complexity reduction

The former interconnect used in the MAIUS-A mission contained one Ethernet cable for data, 10 copper cables for trigger lanes, and one coaxial cable for the clock signal per endpoint. All of those will be replaced by the presented network system with only one pair of plastic fibers for each hop. In addition to the reduced routing complexity inside the experiment it also has an impact onto the weight: the 10 formerly used No. 28 AWG copper wires in a ribbon cable with a
Figure 5. Photograph of the setup with a host A, switch B and an endpoint C. The host is connected with the control computer via Ethernet and powered via USB. Its fiber master port is connected to the upstream (slave) port of the switch. The switch is powered via the cable on its top right and connects over the rightmost fiber master port to the endpoint.

cross-sectional area of 0.0804 mm$^2$ had a weight of 3 g m$^{-1}$, the RG-174 coaxial cable a weight of 12 g m$^{-1}$ and the CAT6 Ethernet cable added 46 g m$^{-1}$. The total interconnection mass with copper wires calculates as

$$10 \times 3 \text{ g m}^{-1} + 12 \text{ g m}^{-1} + 46 \text{ g m}^{-1} = 88 \text{ g m}^{-1}.$$  

Using two plastic optical fibers, with a mass of 3.8 g m$^{-1}$ each, the total interconnection mass will be 7.6 g m$^{-1}$, a reduction by more than a factor of 10.

For the BECCAL mission with a total interconnect length of approximately 23 m this means a reduction by

$$23 \text{ m} \times 88 \text{ g m}^{-1} - 23 \text{ m} \times 7.6 \text{ g m}^{-1} = 2.024 \text{ kg} - 0.1748 \text{ kg} = 1.85 \text{ kg}$$

when using the proposed fiber network instead of the copper wires.

3.2 Trigger delay variance

The deterministic synchronization of the system, especially of the trigger signal, is of capital importance. Therefore, the jitters of the clock and the trigger delays were measured.

First, the constancy of the locking onto the clock signal by a slave with the same delay was evaluated. In case of the host and the switch, the rising edges of the host’s oscillator and the slave’s recovered clock from the Tx line are 7.58 ns apart with a standard deviation of 46 ps. This also holds when power-cycling any of the devices, i.e. resynchronizing them. As the host’s oscillator
already jitters with a standard deviation of 36 ps, this variance could be reduced drastically by using a more stable oscillator at the host.

To measure the board-to-board trigger jitter, the global trigger signal sent by the host is outputted on an SMA connector at the switch and at the endpoints. Thus, the variances of the delays of the trigger signals between the cards were measured and analyzed as depicted in figure 6. The trigger has been sent from the host into the network 5000 times and each one has been recorded by an oscilloscope at a sample rate of 5 GHz. As reference points for the measurement the beginning of the 8b/10b trigger symbol and rising edges (50% low to high) of the trigger outputs at the switch and endpoint were used. An exemplary measurement is shown in figure 7. \( \Delta_{HS}, \Delta_{HE}, \text{ and } \Delta_{SE} \) denote the evaluated delays from host to switch, from host to endpoint, and from switch to endpoint, respectively.

![Figure 6. Setup of the trigger delay measurement. The fiber ports are depicted as squares, the trigger outputs as triangles. The devices are connected via the Tx and Rx plastic fiber pairs. On the oscilloscope the triggers of switch and endpoint are connected directly whilst the host’s Tx fiber signal is captured to detect the trigger symbol. The trigger is started by a special Ethernet frame.](image)

Table 1 shows that the trigger arrival times in the test network are distributed with a standard deviation of maximum 248.2 ps and in a range of 1.63 ns. Despite those high variances of the two segments \( \Delta_{HS} \) and \( \Delta_{SE} \), when looking at the measures for the chained Host to Endpoint delay \( \Delta_{HE} \), its variance counterintuitively is smaller with a standard deviation of 99.6 ps in a range of 0.73 ns. That is most likely due to the switch trigger output having a higher jitter because the cable is longer, affecting the measures from and to the switch. However, this output discrepancy does not affect the full chain variance. The same results were achieved when power cycling the network between the trigger transmissions.

![Table 1. Measured variances of the trigger occurrences as shown in figure 7. SD is the standard deviation.](table)

| Delay           | Mean (ns) | Min (ns) | Max (ns) | SD (ps) |
|-----------------|-----------|----------|----------|---------|
| Host to Switch  | \( \Delta_{HS} \) | 319.46   | 318.72   | 320.32  | 248.2   |
| Switch to Endpoint | \( \Delta_{SE} \) | 581.26   | 580.45   | 582.08  | 239.2   |
| Host to Endpoint | \( \Delta_{HE} \) | 900.72   | 900.30   | 901.03  | 99.6    |
Figure 7. Exemplary delay measurement of one trigger distribution. The bottom graph shows the 8b/10bTx signal of the host encoded as explained in figure 2, including the 8b/10b trigger signal and multiple idle signals. The middle graph displays the measured trigger output of the switch, the top one shows the trigger outputted by the endpoint.

3.3 Network data rates

The theoretical data rate of the channel is limited by the clock frequency and the number of data bits transferred at a time. The used Tx base clock is 150 MHz, but only every third bit is a data bit, resulting in one bit of the 8b/10b code with a rate of 50 MHz. In this code 8 bit of data are encoded as 10 bit on the channel, limiting the data rate to 40 Mbit/s.

To measure the achievable data rate, packets of multiple sizes were transferred over the channel. At the switch and the endpoint parts or multiples of an existing 256 Byte firmware ROM were read via a custom application layer protocol for the data transfers. All data in the payload of the transport layer packets as shown in figure 3 is counted as user data for the measurements, i.e. the address and start/end symbols are excluded.

Figure 8 shows the results of the measurements for the data rates from the host directly to the endpoint, to the switch and to the endpoint routed through the switch. For smaller packets the data rate is lower because the overhead of control data sent with every packet is bigger than the user data itself. When increasing the packet sizes, the data rate increases up to a maximum of 39.92 Mbit s⁻¹ at a packet size of about 918 kB. The small discontinuities in the mid-range of the diagram are caused by reaching the maximum buffer sizes in the host and resulting waiting cycles.

The switches data rate is a bit lower than the one of the endpoint, because the implementations slightly differ. The switch has two more queues in the switching fabric which delay a packet by multiple hundred nanoseconds. Furthermore the chain of switch and endpoint has the highest delivery time and therefore the rise in data rate at higher packet sizes compared to the other two.
Figure 8. Median data rate measured when reading data directly from an endpoint, a switch and an endpoint via a switch over the proposed network for multiple packet user data sizes (displayed on a logarithmic scale). The dashed line marks the maximum rate of 39.92 Mbit s$^{-1}$ reached with the biggest packets.

A higher data rate may be reached when increasing the clock frequencies. This is limited by the capabilities of the ports of the FPGAs and the fiber port switching capabilities.

3.4 Resource usage

All used FPGAs have a low power footprint with limited fabric capabilities of only 8 kLEs (Logic Elements) to 10 kLEs. The FPGA firmware was implemented in VHDL without using vendor specific components (with exception of the PLLs) and is portable to FPGAs of other manufacturers. Each fiber interface, including the bit-level and 8b/10b-level encoding and decoding units, uses about 590 Logic Elements (LEs) (LUT-4) and 2 memory blocks. This is less then one-tenth of the size of the SpaceFibre interface implementation [11]. The 8 port switch additionally uses units for packet arbitration, identification and monitoring, resulting in 6438 LEs for the whole FPGA design and fits the Intel MAX10 10M08 FPGA.

Table 2. Comparison of existing network technology in terms of connection type, timing resolution, typical interface implementation size on FPGAs in number of Logic Elements (LEs) and data rate.

| Name                  | Connection | Resolution | Size    | Data rate     |
|-----------------------|------------|------------|---------|---------------|
| Profinet [7, 8]       | Electrical | 1 ms       | 7 kLEs  | 100 Mbit s$^{-1}$ |
| SpaceWire [11–13]     | Electrical | 7 $\mu$s   | 0.52 kLEs | 200 Mbit s$^{-1}$ |
| SpaceFibre [11, 14]   | Optical    | 58 ns      | 7.2 kLEs | 2000 Mbit s$^{-1}$ |
| Ethernet Födsch et al. [9] | Electrical | 8 ns      | 3.4 kLEs | 1000 Mbit s$^{-1}$ |
| proposed network      | Optical    | < 1 ns     | 0.59 kLEs | 40 Mbit s$^{-1}$ |
4 Summary

It is shown that it is possible to build a low-cost, deterministic low-jitter isochronous and galvanically isolated network with a simple protocol and a data rate of almost 40 Mbit s\(^{-1}\) for experimental setups and realize a proof-of-concept implementation. Deterministic global network synchronicity precision of under 1 ns with a standard deviation of less than 100 ps is possible when only using commercial parts. Table 2 shows the proposed network in comparison to some existing technologies.

Furthermore, the goal of reducing the weight and complexity of the network used in the MAIUS-A and BECCAL missions is reached by sending clock, trigger and data signals over a single plastic fiber. This reduces the weight by more than a factor of 10 and cuts down the number of cables from 3 to 1 for every connection.

Aside from the space missions this network can also be used for custom laboratory setups where high synchronicity at a low cost is needed. Its galvanic isolation and fiber lengths of up to 50 m also makes it usable when spanning multiple rooms with different electrical grids.

Acronyms

- **BEC** Bose-Einstein condensate
- **BECCAL** Bose-Einstein Condensate Cold Atom Laboratory
- **COTS** commercial off-the-shelf
- **EOP** End of Packet
- **FPGA** Field Programmable Gate Array
- **ISS** International Space Station
- **LE** Logic Element
- **PLL** phase-locked loop
- **SoC** System on a Chip
- **SOP** Start of Packet

References

[1] D. Becker et al., *Space-borne bose–einstein condensation for precision interferometry*, *Nature* **562** (2018) 391.

[2] J. Grosse et al., *The maius sounding rocket missions — recent results, lessons learned and future activities*, in *Proceedings of the International Astronautical Congress, IAC*, Adelaide Australia (2017).

[3] K. Frye et al., *The Bose-Einstein condensate and cold atom laboratory*, *EPJ Quantum Technol.* **8** (2021) 1.

[4] J. Feld, *PROFINET — scalable factory communication for all applications*, in *Proceedings of IEEE International Workshop on Factory Communication Systems*, Vienna Austria (2004), pg. 33.
[5] S. Parkes and P. Armbruster, *Spacewire: a spacecraft onboard network for real-time communications*, in *14th IEEE-NPSS Real Time Conference*, Stockholm Sweden (2005), pg. 6.

[6] S. Parkes, C. McClements and M. Suess, *Spacefibre*, in *International SpaceWire Conference*, Saint Petersburg Russia (2010), pg. 41.

[7] M.K. Ishak, G. Herrmann and M. Pearson, *Reducing delay and jitter for real-time control communication in ethernet*, in *2013 15th International Conference on Advanced Communications Technology (ICACT)*, Phoenix Park South Korea (2013), pg. 162.

[8] E. Germanos and W. Seiss, *Synchronizing mechatronic systems in real time using fpgas and industrial ethernet communications*, White Paper WP-01249-1.0 (2015).

[9] P. Födisch, B. Lange, J. Sandmann, A. Büchner, W. Enghardt and P. Kaever, *A synchronous Gigabit Ethernet protocol stack for high-throughput UDP/IP applications*, *2016 JINST* 11 P01010 [arXiv:1510.01384].

[10] A.X. Widmer and P.A. Franaszek, *A dc-balanced, partitioned-block, 8b/10b transmission code*, *IBM J. Res. Devel.* 27 (1983) 440.

[11] S. Parkes et al., *SpaceWire and SpaceFibre on the Microsemi RTG4 FPGA*, in *2016 IEEE Aerospace Conference*, Big Sky U.S.A. (2016), pg. 1.

[12] B.P. Van Leeuwen, J.M. Eldridge and J.E. Leemaster, *Spacewire network simulation of system time precision*, Technical Report, Sandia National Lab.(SNL-NM), Albuquerque U.S.A. (2011).

[13] C. McClements, S. Parkes and A. Leon, *The spacewire codec*, in *International SpaceWire Seminar*, ESTEC Noordwijk The Netherlands (2003).

[14] L. Chen, S. Liu and H. Jiang, *Scheduling methods of spacewire fiber-optic bus and verification*, in *Signal and Information Processing, Networking and Computers*, Y. Wang, M. Fu, L. Xu and J. Zou, eds., Springer, Singapore (2020), pg. 304.