High performance reconciliation for practical quantum key distribution systems

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Abstract

Quantum key distribution (QKD) is a promising technique for secure communication based on quantum mechanical principles. To improve the secure key rate of a QKD system, most studies on reconciliation primarily focused on improving the efficiency. With the increasing performance of QKD systems, the research priority has shifted to the improvement of both throughput and efficiency. In this paper, we propose a high performance solution of Cascade reconciliation,
including a high-throughput-oriented framework and an integrated-optimization-oriented scheme. Benefiting from the fully utilizing computation and storage resources, effectively dealing with communication delays, the integrated-optimization-oriented parameters setting, etc., an excellent overall performance was achieved. Experimental results showed that, the throughput of up to 570Mbps with an efficiency of 1.038 was achieved, which, to our knowledge, was more than four times faster than any throughput previously demonstrated. Furthermore, throughputs on real data sets were capable of reaching up to 86Mbps even on embedded platforms. Additionally, our solution offers good adaptability to the fluctuating communication delay and quantum bit error rate (QBER). Based on our study, low performance (i.e. low power-consumption and cost-effective) CPU platforms will be sufficient for reconciliation in the existing and near-term QKD systems.

Keywords: Quantum key distribution, Information reconciliation, Cascade, High speed, High efficiency

1 Introduction

Quantum key distribution (QKD) is a promising technique for distributing unconditionally secure keys between remote parties in real time [1]. Although QKD systems can theoretically contribute towards enhancing the security of the communication systems, their practical applications are constricted due to their low secure key rates and high costs [2, 3]. To address this issue, most research focused on the optimizations of the two major QKD layers, i.e., the so-called photonic layer and post-processing layer [2]. The photonic layer has in the past been considered the biggest impediment to improving the secure key rate. However, with the recent advances in single-photon detector technologies [4], photonic integrated circuits [5] and other key technologies [6, 7], the performance bottleneck is gradually shifting to the post-processing layer [2, 8]. Thus, as the major performance-limiting module in the post-processing layer, reconciliation has attracted extensive attentions [9–12]. In practice, the reconciliation module has two main performance metrics: efficiency (i.e. the ratio of actual transmitted information to the necessary amount of information) and throughput (i.e. the amount of data that can be processed per second) [13]. In the early stage of development, most reconciliation studies focused solely on efficiency because the efficiency is the dominant factor for the secure key rate and the requirement for throughput is easy to meet due to the limited performance of the photonic layer. With the increasing performance of the photonic layer, the requirement for the throughput of reconciliation increases sequentially. Therefore, in high-speed QKD systems, not only efficiency but also throughput should be taken into consideration [2, 9, 14]. Unfortunately, the above two metrics are often inversely correlated [15, 16], which makes it challenging to simultaneously improve throughput and efficiency. Consequently,
this study focusses on the integrated optimization of efficiency and throughput of the reconciliation module in discrete-variable (DV) QKD systems which are more widely deployed.

In general, the reconciliation protocols in DV-QKD systems can be divided into two categories: interactive and non-interactive [17]. The most widely used interactive reconciliation protocol was Cascade [18]. In this protocol, the correlated sequences belonging to the two remote parties were first shuffled and divided into blocks. Then, the errors were detected and corrected by comparing the parity bits of these blocks and performing binary search operations, respectively. The aforementioned operations had to be performed iteratively for a number of passes to correct further errors. In addition, the Cascade protocol utilized the relationships among passes to correct more errors by involving backtracking operations. Although a number of communication rounds were required in the Cascade protocol, the advantages of simplicity and relatively high efficiency were obvious [19]. For further improvement of efficiency, some later efforts concentrated on the modifications and optimizations of the original Cascade protocol [20–22]. However, nearly all these protocols suffered from high communication overhead, potentially limiting their applications in practical QKD systems [9]. Accordingly, the non-interactive reconciliation protocols based on forward error correction methods, such as low density parity check (LDPC) [23–27] or polar codes [28–30], were proposed. Due to the much less of communication rounds, the non-interactive protocols showed good performance even when the communication delay was high.

Although research of non-interactive protocols have received much attention, this study is devoted to the high-performance Cascade reconciliation based on the following considerations. On one hand, the high communication overhead, which was considered to be the main drawback of Cascade protocols, has relatively low impact on the reconciliation performance required by most realistic deployments of QKD. For instance, in a most common fiber-based QKD system, a low latency communication channel is available by either multiplexing quantum and classical channels, or just by using a different fiber in the same fiber bundle. Therefore, the total end-to-end latency is close to only about 1ms [13]. Under such a realistic condition, an implementation of the original Cascade protocol on two Intel i7 processors achieved a throughput of up to 82Mbps with an efficiency of 1.125 [13]. The above results validated the potential of Cascade protocols to reach high throughput despite the adverse effects caused by high communication overhead. Moreover, the increase in authentication cost of a practical QKD system is usually negligible, even though multiple communication rounds are required in Cascade reconciliation. This is because the remote parties do not need to check the authenticity of communications over the classical channel per round. Instead, the authenticity is usually checked by an exchange of hash values of the whole incoming traffic after the privacy amplification (PA) stage [3, 31]. Meanwhile, on the other end, in addition to the inherent advantages of Cascade, such as simplicity and high efficiency, Cascade also has several other advantages over non-interactive
protocols. First, the rateless feature of Cascade [20] results in better adaption to the QBER variations. Second, the QBER range, within which Cascade protocols perform well, is just the focus of most DV-QKD systems [5]. Third, the characteristic of low computation complexity makes Cascade well suited to work together with a PA module which requires significant computation resources [32]. Therefore, put all together, we believe that Cascade reconciliation will be a better choice for most real-world scenarios than non-interactive protocols.

Consequently, this study is primarily aimed at improving both the throughput and efficiency via a high performance solution for Cascade reconciliation. In this regard, the main contributions of our work are as follows. First, a high-throughput-oriented framework is proposed to increase utilization of computation resources and effectively deal with communication delay. Second, on the basis of the framework, we propose an integrated-optimization-oriented scheme, including the optimizations of core parameters, storage scheme and backtracking process. Results of experiments reported show that a throughput of 570Mbps with efficiency of 1.038 is achieved at 1% QBER by using two i7-6700HQ CPUs connected by a 50 km long optical fiber. This is more than four times the throughput of the fastest reconciliation protocol known to us.

The rest of this paper is organized as follows. Section 2 introduces several measures for reconciliation efficiency and a brief description of a highly efficient improved Cascade protocol available in the literature. Section 3 presents the details of our proposed high performance solution, while its throughput and efficiency results are reported and analyzed in Section 4.

2 Reconciliation Efficiency

Assuming random variables $A$ and $B$ represent Alice’s and Bob’s sequences of length $n$, respectively. Then according to the noiseless coding theorem, the minimum amount of exchanged information for successful reconciliation is given by the conditional entropy $H(A | B)$ [20]. In a DV-QKD system, the discrepancies between $A$ and $B$ can be assumed to the consequence of a transmission over a binary systematic channel (BSC) with crossover probability $\varepsilon$ which is usually referred to as QBER. Therefore, $H(A | B)$ can be written as $nh(\varepsilon)$, where the binary Shannon entropy $h(\varepsilon) = -\varepsilon \log_2(\varepsilon) - (1 - \varepsilon) \log_2(1 - \varepsilon)$. Let $m$ be the length of the leaked information, the reconciliation efficiency $f$ can be defined as:

$$f = \frac{m}{nh(\varepsilon)} \quad (1)$$

Since $nh(\varepsilon)$ is the minimum length of exchanged information, a smaller $f$ means a better reconciliation and $f = 1$ stands for the perfect reconciliation. Let $R$ denotes the ratio of transmitted information to the code length, such that $R = 1 - m/n$. Then, the efficiency $f$ can be rewritten as:
Following the information theory, one transmitted bit can reveal at most one bit information. Therefore, in Cascade reconciliation, the norm is to use the number of transmitted bits in one direction $m^*$ as an upper bound for $m$, since $m^*$ may be linearly correlated and linear combinations of bits do not leak information.

In practice, the frame error rate (FER), which is the probability that reconciliation fails for a given frame, should also be taken into consideration. For non-interactive protocols, the FER may be caused by non-convergence or converging to an inappropriate frame. In the case of Cascade protocols, some sub-blocks may contain positive numbers of undetected errors after implementing reconciliation procedure, which leads to an unsuccessful reconciliation. We note that the error frame can be detected by an additional step called verification [19] and have to be discarded. It is also remarkable that, in practice, higher $f$ may not imply better reconciliation due to the presence of FER. Generally, the value of FER is adjusted downwards by $10^{-3}$ to avoid its negative effect. In some Cascade studies [20, 33], a modified efficiency $f_{FER}$ was used by taking into account the FER. The $f_{FER}$ can be calculated as follows:

$$f_{FER} = \frac{(1 - FER)(1 - R) + FER}{h(\varepsilon)}$$

3 High Performance Solution of Cascade Reconciliation

In this section, we propose a high performance solution of Cascade reconciliation, including a high-throughput-oriented framework and an integrated-optimization-oriented scheme. The proposed implementation framework effectively inhibits the throughput degradation caused by high communication delay. In addition, the optimizations of frame processing are also considered to meet the needs of high-performance parallel implementation. On the basis of this framework, we propose an implementation scheme that optimizes core parameters, storage scheme and backtracking process.

3.1 High-Throughput-Oriented Framework

Our framework, which is similar to the blockchain technology, is an optimized integration of the existing techniques that is timely and pivotal for practical applications. The framework is schematically illustrated in Processing Flowchart 1. To maximize the overall throughput performance, different levels presented in the proposed framework have to attain high levels of performance. The first level, located among multiple processor cores, is where several sequences are simultaneously reconciled. The main problem of this level centers on the provision of an efficient parallel processing approach. The second
level is located inside the processor core and an efficient pipeline scheduling of threads is designed to minimize adverse effects of communication delay. The third level is located inside each thread and it is primarily concerned with ensuring that, wherever possible, the functional modules are in working state rather than waiting state. Detailed implementations of the three levels are presented in the remainder of the section. We note that although our framework is designed for the specific improved Cascade protocol in [22], it can be adapted to other variations of Cascade protocols with relatively minor modifications.

### Processing Flowchart 1 Implementation Framework

1: **Level 1: Parallel Processing**
2: 
3: **for** each core **par** - **do**
4: 
5: **Level 2: Multi Pipeline**
6: 
7: **for** stage = 1 → STAGE\textsubscript{max} **do**
8: 
9: **Level 3: Cascade Reconciliation**
10: 
11: **for** round = 1 → ROUND\textsubscript{max} **do**
12: 
13: **end for**
14: 
15: **end for**

### 3.1.1 Parallel Processing

In theory, the parallel implementation can significantly improve the throughput performance. However, the actual performance gain, by taking advantage of the parallel implementation, is affected by many factors. For instance, the bottleneck of parallel LDPC decoding on GPU has been demonstrated to be the slow memory accesses [34]. To limit the impact of the mass memory latency, multi-level caches were introduced in modern CPUs. However, the memory access latency varies among different levels of caches and the sizes of faster caches tend to be smaller [35]. In view of the characteristics of the multi-cache architecture, reducing frame length and reusing cached data are efficient strategies employed to increase the memory access efficiency in parallel processing environment.

Specifically, in our implementation, we divide the original large sequence into multiple short frames with a fixed length of 64kb based on the following considerations. On one hand, the previous simulation results have shown that a rather high efficiency can be achieved with 64kb frame length, then larger frame lengths offer no significant improvement in efficiency improvement [22]. On the other hand, the latter frame can reuse the cached-data from the former frames when using fixed frame length, which decreases execution time. For instance,
the time-consuming shuffling operation can be speeded up by applying a pre-stored mapping table. If all frames are of the equal length, then only a single shuffling map is required. The latter frame does not need to reload the shuffling map from slower memory, which results in an improved throughput.

3.1.2 Multi Pipeline

While its use is less commonplace in Cascade implementations, pipeline technology is one of the optimum approaches used in hardware implementations to decrease the processing delay. Moreover, it is generally held that inside each reconciliation thread, the subsequent processing is delayed pending results of the parity comparison from the other party through the commutation channel. Such a stop-and-wait scheme affects the performance and causes communication delay. To augment this, we apply multi-pipeline technology among multi reconciliation threads in this study. Fig. 1 presents the layout of a typical four-stage pipeline technology. The figure illustrates that applying multi-pipeline technology can help circumvent the adverse effects of the communication delay, which would result in improved throughput. Specifically, in our implementation, all the threads are executed serially to avoid the overhead of thread switching. The gains from this optimization strategy will be validated in results of experiments reported in Section 4.

![Diagram of multi-pipeline](image)

**Fig. 1** Layout of four-stage multi-pipeline for multi reconciliation threads

3.1.3 Cascade Reconciliation

The flowchart outlining the information processing of the Cascade reconciliation module is presented in Fig. 2. From it, we deduce that, upon acquisition of the data from the sifted-key buffer, the DivideBinarySearch module performs binary search operation and allocates the divided blocks into the corresponding DivideBlocks buffers. Once the size of a buffer exceeds the preset frame length of 64kb, an idle module from the CascadeErrorCorrection group will be prompted to complete the error correction task. During error correction, each module works independently by using its respective state machine and storage space, but the interactive messages of each communication round are sent and received through a uniform network packet. Finally, the CascadeErrorCorrection module will output the corrected keys into the reconciled-key buffer and quit the working state as soon as the error correction task is completed.
3.2 Integrated-Optimization-Oriented Scheme

In this part, we mainly focus on the implementation scheme of the more complicated Cascade Error Correction module, including the optimizations of core parameters, storage scheme and backtracking process.

3.2.1 Cascade Parameter Optimization

Parameter optimization is long standing priority for studies on Cascade reconciliation. The original Cascade protocol calculated the block length of the first pass using the formula $0.73/QBER$, which is doubled for the subsequent three passes [18]. Though the efficiency still needs improvement, the number of communication rounds was low. To further enhance the reconciliation efficiency, most modified versions of Cascade protocols used different methods to calculate the block length of the first two passes and $N/2$ for the subsequent passes. Whereas the highlighted optimized parameters were acquired with the target of improving efficiency, in this study, the optimization target is no longer the efficiency improvement but the integrated optimization of both throughput and efficiency. For this reason, the previous optimized parameters are not prioritized. Furthermore, for integrated optimization, we present an adaptive parameter setting scheme that combines the advantages of the original and modified cascade protocols. The adaptive parameter settings are presented in Table 1. The block $k_{\text{initial}}$ and $k_{2,K'}$ are calculated by the Equations (4, 5) as described in [22], where $K' \in \{1, ..., \lfloor \log_2(k_{\text{initial}}) \rfloor \}$.
Table 1 Adaptive parameter setting scheme where the frame length is $N = 2^{16}$

| Combination Mode | $k_1$ | $k_2$ | $k_3$ | $k_4$ | $k_5$ | $k_6$ |
|------------------|-------|-------|-------|-------|-------|-------|
|                  | $k_{\text{init}}$ or $k_{\text{init}}/2$ | $k_{2,K'}$ or $k_{2,K'}/2$ | $N/16$ | $N/8$ | $N/4$ | $N/2$ |

$k_{\text{init}} = \min(2^{\lfloor \log_2(1/\epsilon) \rfloor}, N/2)$ (4)

$k_{2,K'} = \min(2^{\lfloor \log_2(4/\varepsilon_{\text{bit}}) \rfloor}, N/2)$ (5)

$\varepsilon_{\text{bit}} = \frac{1 - (1 - 2\varepsilon)^{2^{K'-1}}}{1 + (1 - 2\varepsilon)^{2^{K'}}}$ (6)

Following the layout presented, we highlight some merits of our proposed scheme from two aspects.

(1) First two passes. The values of $k_{\text{init}}$ and $k_{2,K'}$ can be regarded as benchmarks for assessing efficiency since they fully account for maximizing the amount of interactive information. Therefore, to further boost adaptability of the protocol on high-performance requirements, we intend to improve the throughput performance by sacrificing the efficiency properly with smaller block lengths. To do so, we adjust $k_1$ and $k_2$ based on $k_{\text{init}}$ and $k_{2,K'}$ respectively, to obtain four combination modes which are presented in Table 2. This approach potentially reduces the number of communication rounds, making it more adapted to high latency environments. The actual effects of the adaptive adjustment strategy will be demonstrated later in Section 4.

Table 2 Adaptive Combination of Block Lengths

| Combination Mode      | $k_1$ | $k_2$ |
|-----------------------|-------|-------|
| High-Efficiency       | $k_{\text{init}}$ | $k_{2,K'}$ |
| Medium-Efficiency     | $k_{\text{init}}$ | $k_{2,K'}/2$ |
| Medium-Throughput     | $k_{\text{init}}/2$ | $k_{2,K'}$ |
| High-Throughput       | $k_{\text{init}}/2$ | $k_{2,K'}/2$ |

(2) Subsequent four passes. For efficiency, the value of $N/2$ is commonly adopted as the block length of the subsequent passes. One substantial drawback of this approach is the low ability to detect error bits, which leads to an increasing number of passes and communication rounds. To solve this issue, in this paper, the common used $N/2$ is augmented by doubling block lengths to decrease the number of passes and communication rounds. Since the number of undetected errors in these passes is small, the negative effects on efficiency is limited but the throughput improvement is significant.

3.2.2 Complete-Binary-Tree-Based Storage Scheme

The storage consumption in Ref. [13] increases rapidly with the increasing QBER. This is attributed to the use of global backtracking list whose size grows quickly with increase in QBER. To overcome this problem, the data
structure of complete-binary-tree is applied instead of the global backtracking list. In this way, most of the relevant data are stored in the same data structure and only the index information is stored in the temporary list for each pass, thereby solving the issue of rapid increase in storage consumption with QBER.

Specifically, to store the relevant data during error correction, we use two identical complete binary trees, which are called parity tree and parity comparison tree, respectively. Fig. 3 illustrates the relationships between the logical and storage structure of a parity comparison tree for a block length of 4. As demonstrated in Fig. 3, the mapping of these two structures can be performed easily, which provides basis for the high-performance implementation. In terms of the storage structure, we use each byte of memory to store 8 data bits, the relevant data of the adjacent blocks are stored together. In such cases, some bits of the complete binary trees need to be marked during initialization. For instance, for block length of 4, the data bits 1, 2 and 3 are set to 1 while others are initialized to 0 as depicted in Fig. 3. Since most of the errors are corrected in the first two passes, the parity comparison trees are solely in the first two passes to improve the utilization of storage resource. In this way, the total number of trees needed in the six passes decreases from 12 to 8, which is approximate a 33% decrease.

![Fig. 3 Schematic illustration of parity comparison tree for block length of 4](image)

### 3.2.3 Parallel Backtracking Collision Detection

The backtracking collision (i.e., multiple corrected data backtrack to the same sub-block) are unavoidable, and the collisional data need to be eliminated from the backtracking list when applying parallel backtracking. This problem can be solved by querying the backtracking list. However, this approach will waste immense amounts of time which increases rapidly with QBER. Thus, the issue of how to detect backtracking collisions that need to be resolve to enhance throughput.

As presented in Fig. 3, the position 0 of each binary tree is unoccupied in the memory. Based on this, we design a strategy to make reasonable use of this unused position to benefit the backtracking collision detection. The descriptions of these two trees are summarized in Table 3. The parity comparison result of each complete block is stored into position 0, which ensures the
backtracking procedure works normally even in the absence of the parity comparison tree. In round 3 or later, we backtrack to the complete block rather than the smallest sub-block, which offers little effect on efficiency.

**Table 3** Description of the complete-binary-trees

| Tree                      | Valid Passes                      | Node No. | Meaning                                           |
|---------------------------|-----------------------------------|----------|--------------------------------------------------|
| Parity Tree               | All                               | 0        | Parity comparison result of node 1               |
|                           | Others (1,2,...)                  |          | Parity of the corresponding node                 |
| Parity Comparison Tree    | The previous two passes (1,2)     | 0        | Locking identifier when backtracking             |
|                           | Others (1,2,...)                  |          | Parity comparison result of the corresponding node |

The advantage of this scheme lies in its ability to curtail the frequent and redundant querying operations that add burdens on consumption. When backtracking to each block of the first two passes, the position 0 of the parity comparison tree will be checked first. If the block is not locked, the backtracking operation will be performed directly. Otherwise, the function SearchList() will be executed to detect a collision and determine whether the data is added to or removed from the backtracking list. The actual impact of the backtracking collision detecting strategy will be demonstrated later in the results of our experiments reported in the next section.

4 Experiments and Results

We start the experimental validation of our proposed solution by outlining its relative realization technology. Like in [19, 34], we apply OpenMP directives for parallel processing. For the practical implementations of shuffling and backtracking, we use an Arnold-Mapping-Based scheme [36] whose key parameters are updated periodically. For the time-consuming operations, such as shuffling or initialization of the parity tree, the pre-calculated lookup tables are applied to decrease the processing delays.

4.1 Experiments for Each Optimization

The experiment results for the individual improvements are shown in Fig. 4. Fig. 4(a) presents an assessment of the throughput improvement of the multi-pipeline optimization scheme relative to the benchmark of the Stop-Wait scheme in [13]. From it, we can be seen that the percentage improvement in throughput varies from 10% to 55%. Though the multi-pipeline scheme offers improvement in the throughput performance, the graph also shows that the effect of each multi-pipeline scheme decreases with the increasing communication delay. This is because the throughput improvement of multi-pipeline scheme mainly comes from resources expanded on computation and communication overhead. However, the contribution of computation overhead to the overall time spent decreases rapidly as the communication delay increases.
Consequently, for high communication delays, the communication time spent has been the dominating factor that influences the throughput performance. In this case, the contribution of the multi-pipeline strategy is minimal.

Next, we analyze the adaptation of different combination modes, which are listed in Table 2, to communication delays. In the experiment, the throughput with a latency of 1ms is regarded as the baseline and the rates of decline in throughput for different block-length combinations with increasing QBER are plotted in Fig. 4(b). As seen from the plot, the throughput decreases rapidly with increasing communication delay, especially when the high-efficiency mode is applied. When the communication delay reaches 5ms, the throughput decrease ratio has reaches 70%. Under the same conditions, the throughput decrease ratio is only 30% if the high-throughput mode is used. These results indicate that the adaptive combinations of block lengths fit well with the dynamics of communication delays with minimal degradation in efficiency.

Then the experimental results for backtracking collision detection are presented in Fig. 4(c). Therefrom we see that the average ratio of decline in collision reduction reaches up to 78%, which leads to corresponding savings in the communication cost. In addition, the percentage improvement in throughput varies from 8% to 70% with the increases in QBER from 1% to 8%. This is because the number of blocks and the percentage of backtracking time spent to the total time increase with QBER, thereby leading to a better collision detection effect. Nowadays, a typical DV-QKD system runs under a QBER of less than 3% for which the percentage improvement in throughput is approximately 20% [5].

In addition, since memory usage is a big issue in high performance Cascade implementation, we also compare the actual storage consumption between our work and Ref. [13] in Table 4. Because we use pipelined storage structure, the memory usage is slightly larger than that in Ref. [13] when QBER equals to 1%. However, since new storage scheme is applied, the amount of memory used increases significantly slower than Ref. [13].

| Table 4 | Memory usage |
|---------|--------------|
| Refs.   | QBER | Input Size (Mb) | Memory Usage (MB) |
| Ours    | 1.0%  | 30              | 48               |
| Ours    | 15.0% | 30              | 80               |
| Ref. [13]| 1.0%  | 30              | 38               |
| Ref. [13]| 15.0% | 30              | 256              |

4.2 Overall Performance Test

To evaluate the overall performance of our solution in real-world scenarios, we executed it on two computers connected by 50 km dedicated fiber, using 1000Mbps media converters that can convert 1000 Mbps Ethernet connections
(a) Throughput improvement of the multi-pipeline optimization scheme
(b) Rates of decline in throughput for the adaptive combination modes
(c) Effects of backtracking collision detection

Fig. 4 Experiments for the individual improvements

to a 1000Base-FX fiber connection. In the following experiments, we use four-stage multi-pipelines per processor core. The input buffer size of each pipeline (i.e. thread) is set to 10Mb. Each thread will terminate immediately when its input amount of data reaches 1Gb.

Table 5 presents a comparative analysis of our solution relative to the state-of-the-art CPU [13, 19], GPU [9] and FPGA [2] benchmarks. Among these, Ref. [13] was the previous fastest implementation by using Cascade protocol, while Ref. [19], Ref. [9] and Ref. [2] were the fastest LDPC implementation on CPU, GPU and FPGA platform, respectively.

Table 5 The Evaluation Platforms

| Product Collection | Ours | Ref. [13] | Ref. [19] | Ref. [9] | Ref. [2] |
|--------------------|------|-----------|-----------|-----------|-----------|
| Vertical Segment   | Intel CPU | Intel CPU | Intel CPU | Intel CPU | NVidia GPU | Intel FPGA |
|                    | i7-6700HQ | i7-6700HQ | i7-6700HQ | i9-9900K  | M2090     | Altera Stratix V |
| Number of Cores    | 4     | 4         | 4         | 8         | -         | -           |
| Base Frequency (GHz)| 2.6   | 1.9       | 3.4       | 3.6       | 1.3       | -           |
| Max Turbo Frequency (GHz) | 3.5   | 1.9       | 3.4       | 5.0       | -         | -           |
| Power Consumption (W) | 45    | 10        | -         | 45        | 95        | 225         |

In Fig. 5, we present a plot of QBER against throughput and efficiency relative to established methods reported in the literature. We note that the throughput of our solution is rather high, but it decreases with increasing QBER. Such a phenomenon is clearly due to the rapidly increasing number
of blocks to be processed which subsequently improves the computation cost. Though the throughput correlates inversely with QBER, the throughput and efficiency of our solution on i7-6700HQ surpasses those reported for comparative schemes within the whole range of QBER. To our best knowledge, the previous fastest reconciliation achieved a throughput of 130Mbps with an efficiency of 1.23 when correcting 1% QBER on two i9-9900K processors [19]. Compared to this result, a speedup factor of $\times 4.4$ is obtained with an efficiency closer to the theoretical limit. Similarly, from the plot in Fig. 5, we infer that our implementation performs at par with the benchmark methods in terms of level of throughput performance even when the Atom E3845 CPU is applied. We note that Intel Atom E3845 is an embedded platform with rather low power-consumption. Indeed, the performance on Atom E3845 is sufficient for the existing QKD systems. Once the throughput of reconciliation is insufficient, we only need to change a more powerful platform.

To further evaluate the actual performance of our proposed solution, we assessed the performance on real data. By using different operation parameters, we obtained two data sets obtained from a practical QKD system [37]. Our experiments are validated on Atom E3845 platforms with the high-efficiency combination mode. In addition, we use a pre-defined estimated QBER since the precise QBER is unknown to us. The experiment results are listed in Table 6. We can see that the throughput of up to 86Mbps with an efficiency of 1.028 was achieved on data set 2. Moreover, even if the estimated QBER is inaccurate, the efficiency degradation is not apparent. This fully validates the good adaptability of our solution to the fluctuating QBER.

### Table 6 Experiment results on real data sets

| Data Set No. | Actual QBER | Estimated QBER | $j$ | $j_{FER}$ | Throughput(Mbps) |
|--------------|-------------|----------------|-----|-----------|------------------|
| 1            | 2.0%        | 1.033          | 1.037| 40        |
|              | 2.0%        | 1.028          | 1.032| 57        |
|              | 3.0%        | 1.043          | 1.046| 76        |
| 2            | 2.6%        | 1.024          | 1.028| 68        |
|              | 2.6%        | 1.023          | 1.026| 82        |
|              | 3.6%        | 1.028          | 1.036| 86        |

Encouraged by the outlined performance, it can be surmised that our solution can contribute towards the development of practical QKD systems. It has shown promise in terms of surplus throughput which leads to low performance CPU platforms that are required to reduce overall system costs for most QKD systems (e.g., power consumption, volume, economic cost, etc.). Moreover, once the throughput is adequate to satisfy the processing demand, the secure key rate is determined principally by the reconciliation efficiency. In such case, a high efficiency performance can help to improve the distilling efficiency of the secure keys, thus improving the communication distance and the final secure key rate of a practical QKD system. This performance reinforces our conclusion that the proposed solution is applicable to nearly all discrete-variable (DV) QKD systems.
Fig. 5 Plot of throughput (upper panel) and efficiency (lower panel) where we note that our efficiencies on i7-6700HQ and Atom E3845 are the same when the same combination mode.

5 Conclusions

In this study, we first proposed a framework to improve the throughput of Cascade reconciliation. The framework increases utilization of computation resources and effectively deals with communication delay. Furthermore, we proposed an integrated-optimization-oriented implementation scheme that targets optimizations of core parameters, storage scheme and backtracking process. Execution of our high-efficiency mode over a 50km fiber, which yielded a
throughput of 398Mbps and 318Mbps with the efficiency of 1.026 and 1.032 as well as 1% and 3% corrections of QBER, respectively. These outcomes indicate the utility of our proposed solution across nearly all DV-QKD systems.

In ongoing and future work, we are exploring improvements to the proposed solution in two directions. First in terms of efficiency, we are considering the application of a backtracking list to backtrack to the sub-block in the pass of three or later stages of the process. This will facilitate better use of known bits and known parities that may enhance efficiency. Second, in terms of throughput, we are exploring a combination of binary search and hamming error correction as a way to efficiently reduce the number of communication rounds since only one communication round is needed in hamming error correction. However, hamming error correction may introduce new error bit when the block contain three or more errors. Therefore, the focus of the improvements to the scheme should consider designs that help to avoid such unexpected issues.

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Declarations

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• Conflict of interest/Competing interests The authors declare no conflicts of interest.
• Availability of data and materials Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.
• Code availability The code in this paper is not publicly available at this time but may be obtained from the authors upon reasonable request.
• Authors’ contributions Hao-Kun Mao and Qiong-Li contributed to the initial ideas. Abdullah M. Iliyasu refine the ideas. Peng-Lei Hao and Bassem Abd-El-Atty wrote the source code and completed the simulations. All authors contributed to writing the manuscript.

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