384x288 readout integrated circuit for MWIR and LWIR HgCdTe based FPA

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Abstract. The review of architecture and characteristics of 384x288 silicon readout integrated circuit with 25 μm pixel pitch for MWIR and LWIR HgCdTe based FPA is presented.

1. Introduction

The unique physical properties of the mercury-cadmium-telluride (MCT, HgCdTe) solid solution allow to realize infrared (IR) detectors with high sensitivity in the mid-wavelength infrared (MWIR) band (3 – 5 μm) and long-wavelength infrared (LWIR) band (8 – 12 μm). The most attractive method for fabrication multi element photovoltaic focal plane array (FPA) is fabricating the MCT diode in pixel of readout integrated circuits (ROIC). Some attempt to fabricate so-called monolithic IR detectors on the basis of MCT growth onto ROIC was carried out [1-5]. But it is clear that the development of monolithic detectors on the basis of HgCdTe can not used as a basic technology for development and fabricating multi element up to megapixel format FPA. Today all developers are used hybridization photo diode sensitive array and ROIC by «flip-chip» through indium bumps. Figure 1 shows the scheme of FPA fabrication which obtained by «flip-chip» hybridization. Usually MWIR and LWIR HgCdTe photodiode detectors are operated at liquid nitrogen temperature [6]. It is necessary to provide high detector sensitivity for registration low radiation fluxes in MWIR and LWIR spectral ranges in presence high background ones.

Figure 1. The scheme of hybrid HgCdTe FPA

The main purpose of a ROIC is a registration of photocurrents that are generated by FPA photodiodes and then a serial output of the accumulated information for imaging. The modern IR ROICs are fabricated by CMOS technology, which gradually replaced the CCD technology [7]. Operation at liquid nitrogen temperature requires as low as possible power dissipation of ROIC because of limitation of micro cryogenic cooler in refrigerating capacity. The modern ROIC should support the following features: integration then read (ITR) mode, integration while read (IWR) mode and window modes. Also, important requirements is frame rate, which is low in most serial available ROIC. The work objective was design modern high-speed low power ROIC with minimal number of control and reference signal pads.

The infrared flux of useful information is depending on the wavelength range and from the surrounding background. Usually it is necessary to detect small useful signal information from thermal object in MWIR and LWIR bands at high background flux intensity. Direct injection pixel cell architecture is suitable for the MWIR and LWIR bands. The electron capacity is the main characteristic of such cell. The increase of electron capacity leads to increase of image integration time and dynamic range [6]. The large dynamic
range gives better temperature resolution. A temperature resolution is minimum temperature difference between an object that can be detected by focal plane array (FPA). Another important parameter that determines the FPA speed is frame rate. Frame rate is limited by information output time and thus depends on a number of pixels, i.e. matrix format, a number of signal outputs and a maximum frequency of the output information from the ROIC. High frame rate allows to provide external signal integration, that improves the temperature resolution of FPA. In order to improve these characteristics in modern FPA ROIC the following techniques are used:

- **Subtract of DC component of the photocurrent.** This method allows to increase the dynamic range, especially where the proportion of the useful signal is small relative to the total flow of the IR radiation, detected by photodiodes array. But it does not give better temperature resolution.
- **The possibility of discrete switching of the charge capacity that allows to use the ROIC in conditions with different intensity of infrared radiation flux.**
- **Using the window mode.** This method allows to significantly increase the temperature resolution by reading information from reduced area of photosensitive elements array (PSEA). Reduction of the readout area reduces output information time, thereby increasing the frame rate.
- **Multiplexing of nearest pixels in order to increase charge capacity while reducing the spatial resolution.** Spatial resolution determines the number of elements that build the image. This method reduces the number of readout pixels, reducing the output time information.
- **Increasing the number of analog outputs.** The greatest contribution to power consumption of ROIC make analog output amplifiers. Therefore increasing their numbers imposes additional requirements to the cooling cryogenic coolers. Also in this case, the number of wires crossing the border of the cryostat increases, which increases the heat gain.
- **Increasing the frequency of the output information from ROIC.** Increasing the frequency output of the analog signal is limited by difficulty of transmission without distortion.
- **Using the built-in analog-to-digital conversion and digital outputs.** It allows to increase the frequency of the output information, but requires the use of more expensive ROIC production process.
- **Digital integration directly into the pixel unit cell.** It can significantly increase the dynamic range and, as a consequence, the temperature resolution. This type ROIC requires a very small ROIC production process and consequently more expensive [8].

### 2. Key features

The 384x288 ROIC with 25 μm pixel pitch for MWIR and LWIR HgCdTe photodiodes FPA was developed and tested. The samples were made by XC06 production process of XFab foundry. Figure 2 shows developed ROIC die photo. The column bus partition architecture is used in ROIC. Charge from the unit cell is transferred to the column bus and input column followers. This method allows to increase the area under the charge capacity, but requires further amplification of the attenuated signal [9]. The signal from the column followers multiplier for preamplifiers with adjustable gain and then transmitted to the output buffer. The decoders which are controlled by digital block perform selection of rows and columns.

Figure 3 shows a schematic of the ROIC direct injection pixel cell. The ROIC operates in the snapshot mode. ROIC can operate in ITR mode and also in IWR mode. The PMOS transistors VTC1 and VTC2 are for accumulating charge during integration in both ITR and IWR modes. It is possible to disable the capacity of transistor VT1 for reducing image integration time. It preserves the dynamic range where the average flux intensity is low enough, for example, when the ROIC is connected to MWIR FPA. PMOS transistor VT3 used to read the accumulated charge in both ITR and IWR modes, and is also used for accumulating charge during integration in the ITR mode. In IWR mode charge accumulated at previous frame is transferred to capacity of transistor VTC3 and closed transistor VT6 prevents discharge of VTC3 capacity during the accumulation of photocurrent onto VTC1 and VTC2. NMOS transistor VT1 is used for Antiblooming and also can be used as an imitator of the current to test an array of pixel cells. It allows to evaluate performance of the ROIC before hybridization with a photodiode array. Pin PHDK of the cell is connected via indium bump to the cathode of the FPA photodiode with common anode. NMOS transistor VT3 is direct injection transistor which used to set the offset voltage of photodiode.

Inside the ROIC 12-bit digital-to-analog converters (DAC) are installed. DACs can be used to generate a voltage for gates of direct injections transistors, and also a voltages for gates and drains of Antiblooming transistors (VT1, Fig. 3). The use of DACs allows to reduce the number of wires crossing the border of the cryostat. Also the signals generated by the DACs directly in ROIC are more noise-immune. It is possible to disable the DACs and use the external contact pads for supplying this signals.
The designed ROIC allows to readout accumulated video signal from the restricted area of PSEA, the so-called window mode. The minimum size of the window is equal to 4x4, which allows to detect moving target with an increased frame rate. In ROIC the serial interface is used. The operating modes of ROIC, the values build-in DACs, format and location of window, the number of signal outputs, preamplifier's gain, current consumption of the output buffers are determined by the configuration that loaded in internal registers via this serial interface. It allows to minimize the number of control pads of ROIC. The loading of registers is performed using the same input that is used to control the process of image integration. New values of registers can be loaded at the beginning of each frame. Thus, each frame can change the window size from which information is read. Thus the window size can be changed for each frame. Figure 4 shows ROIC timing diagrams of the in the ITR and IWR modes.
Figure 4. ROIC timing diagrams: a) ITR mode; b) IWR mode.

Figure 5 shows the thermal images obtained with LWIR FPA based on the developed ROIC. The noise equivalent temperature difference lower than 30 mK was obtained at integration time 600 μs and FOV 30 degrees.

Figure 5. The thermal images HgCdTe LWIR FPA.

3. Conclusion

Table 1 shows some characteristics of the developed ROIC.

| Parameter          | Value          |
|--------------------|----------------|
| Design rules       | 0.6 μm         |
| Pixel pitch        | 25 μm          |
| Detector type      | N on P         |
| Operating voltage  | 5 V            |
| Pixel charge capacity | > 21 Me−   |
| Output voltage swing | 3.4 V (ITR) |
|                    | 2.6 V (IWR)    |
Number of outputs | 1, 2, 4
Max. pixel rate per output | 20 MHz
Max. full window frame rate | 700 frames/sec
Max. power dissipation | < 100 mW
Operating temperature | from 70 to 300 K

Summing up, we list the basic functional features of the ROIC:

- Provides built-in digital-to-analog converters (DAC), which can be used to set the offset voltage of photodiodes and to control Antiblooming and build-in testing system of the pixel cells.
- Provides a serial interface for controlling the functionality of the ROIC.
- Provides reception and accumulation of electric charge from each FPA photodiode simultaneously for a predetermined time by direct injection technique.
- Enables reading signaling information simultaneously on four video outputs, also using only one or two video outputs.
- Operates in the ITR or IWR modes.
- Allow selection of rectangular submatrix of any size and location which will be readout video information.
- Provides the ability to adjust the bias circuit of the analog part of the ROIC.
- Allow selection the value of the charge capacity of the unit cell between two fixed values using the serial control interface.

4. References
[1] K. Zanio, R. Mattson 1992 *HgCdTe on Si fpr monolithic focal plane arrays* (Proc. SPIE, v. 1683) 179-190
[2] J.W. Cairns, L. Buckle, G.J. Pryce, J.E. Hails, J. Giess, M.A. Crouch, D.J. Hall, A. Hydes, A. Graham, A.J. Wrigh, C.J. Hollier, D.J. Lees, N.T. Gordon, T. Ashley 2006 *Integrated infrared detectors and readout circuits* (Proc. SPIE, v. 6206, p. 620614-1–620614-9)
[3] G.B. Dalton, P.N. Dennis, D.J. Lees, D.J. Hall, J.W. Cairns, N.T. Gordon, J.E. Hails, J. Giess 2008 *Development of non-hybridised HgCdTe detectors for the next generation of astronomical instrumentation* (Proc. SPIE, v. 7021, p. 702101-702105)
[4] S. Velicu, T.S. Lee, R. Ashokan C.H. Grein, P. Boieriu, Y.P. Chen, J. Dinan, D. Lianos 2003 *Monolithically integrated HgCdTe focal plane arrays* (Proc. SPIE, v. 5209) 14-32
[5] Maxim V. Yakushev, Sergei A. Dvoretsky, Alexander I. Kozlov, Irina V. Sabinina, Yuri G. Sidorov, Alexander V. Sorochkin, Boris I. Fomin, and Alexander L. Aseev 2010 *HgCdTe monolithic infrared detector* (Phys. Status Solidi C 7, No. 6) 1681-1683
[6] Rogalski A 2011 *Infrared Detectors – 2nd ed.* 662, 744 876
[7] Michel Zécri, Patrick Maillart, Eric Sanson, Gilbert Decaens, Xavier Lefoul, Laurent Baud 2008 *Advanced ROICs design for cooled IR detectors* (Proc. of SPIE Vol. 6940, 69402X)
[8] Kenneth I. Schultz, Michael W. Kelly, Justin J. Baker, Megan H. Blackwell, Matthew G. Brown, Curtis B. Colomero, Christopher L. David, Brian M. Tyrrell, and James R. Wey 2014 *Digital-Pixel Focal Plane Array Technology* (Lincoln Laboratory Journal v. 20, No. 2) 36-51
[9] Mottin E., Pantigny P., Boch R. 1996 *An improved architecture of IRFPA readout circuits* (Proc. SPIE v. 3061) 118-124