Advanced Microelectronics Metrology Workshop

A workshop titled “Advanced Metrology Needs for Addressing Critical Microelectronics Challenges” was held during the virtual NSLS-II and CFN Joint Users’ Meeting at Brookhaven National Laboratory (BNL) on May 25, 2022.

The workshop, consisting of facilities’ introductions by the organizers and seven invited talks from industry, academia, and national laboratories, provided a lively forum to discuss the current landscape of state-of-the-art metrology needs for semiconductor manufacturing and associated challenges for the future of microelectronics. The workshop panel engaged in a discussion on the potential roles of national laboratories in addressing semiconductor metrology challenges, particularly BNL facilities, including the National Synchrotron Light Source II (NSLS-II), Center for Functional Nanomaterials (CFN), and Instrumentation Division.

Dr. Satyavolu Papa Rao, vice president of research at NY CREATES, a non-profit affiliate corporation of the State University of New York (SUNY), delivered a keynote lecture providing an overview of NY CREATES and the Albany Nanotech Complex. He also discussed potential semiconductor research opportunities associated with the CHIPS Act and its National Semiconductor Technology Center (NSTC). Particularly addressed were the areas of heterogeneous integration, new materials, and advanced metrology, which are essential for enabling enhanced energy efficiency, connectivity, and ubiquity of future microelectronics. Dr. Papa Rao emphasized the potential roles of national laboratories and their user facilities such as synchrotron X-ray sources, stressing the need for easier user access for semiconductor research and wafer-scale, in-operando, and high-resolution metrology capabilities.

Three workshop organizers gave brief overviews of the microelectronics capabilities at BNL. Dr. Yong Chu gave an overview of the nanoscale X-ray imaging capabilities of the NSLS-II. The key capabilities include nanoscale three-dimensional (3D) tomography and strain imaging, which are highly effective in visualizing the internal defects and strain field at the interface layers. Dr. Chang-Yong Nam described the CFN’s capabilities in structural metrology by electron microscopy and the development and characterization of new microelectronics materials, including extreme UV (EUV) photoresists and hybrid memristors. Also highlighted was the Quantum Materials Press (QPress), a machine-vision-assisted, automatic stacking system for two-dimensional (2D) material heterostructures, potentially critical for enabling next-generation devices beyond today’s cutting edge. Dr. Gabriella Carini gave...
Dr. Joseph Kline, a Materials Engineer at National Institute of Standards and Technology (NIST), first provided a brief overview of the semiconductor industry, for which NIST is developing advanced packaging for heterogeneous integration, a crucial approach to drive continued advances in computing and communication hardware. The trend towards 3D heterogeneous integration was emphasized; this integration demands aggressive interconnect pitch scaling, robust optical interconnect technology, high-efficiency power delivery, and more efficient thermal management. He also pointed out the need for metrologies for yield optimization, performance characterization, reliability, debugging, and fault isolation.

Dr. Ravi Mahajan, an Intel Fellow of Intel Corporation, introduced state-of-the-art advanced packaging for heterogeneous integration, a crucial approach to drive continued advances in computing and communication hardware. He presented the materials challenges as associated with EUV lithography using dedicated beamlines at the Advanced Light Source (ALS) of Lawrence Berkeley National Laboratory (LBNL), including the Microfield Exposure Tool 5 (MET5). He presented the materials challenges associated with EUV lithography, describing the underlying material physics and the solutions achieved by employing a number of advanced X-ray metrology methodologies, such as resonant soft X-ray resonant scattering (RSoXS), standing-wave X-ray photoemission spectroscopy, and EUV reflectometry and scatterometry.

Dr. Edward Principe, the President of Synchrotron Research Inc., presented technical details on a novel soft X-ray imaging instrument called LARIAT (Large Area Rapid Imaging Analytical Tool) installed at the Spectroscopy Soft and Tender (SST1) beamline at NSLS-II, developed by NIST. LARIAT achieves rapid full-field imaging, collecting photoelectrons excited by an X-ray beam through a magnetic, optical system with a field of view up to 20 mm × 20 mm and a spatial resolution of ∼5 µm. This instrument is designed specifically for rapid semiconductor wafer inspection. He also presented a roadmap for achieving sub-20 nm resolution.

The workshop concluded with a panel discussion. The workshop speakers, participants, and organizers exchanged lively discussions on how the capabilities of synchrotron light sources and national laboratories could be more effectively employed to support research and development to address the microelectronics challenges. The panel pointed out that the proposal review process favors fundamental science over engineering research such as those associated with microelectronics, and there is a huge opportunity for the synchrotron capabilities to be better optimized for tackling the critical challenges in semiconductor research and engineering. Also noted was the need for accelerating data turnarounds for such industrial research. There was an overwhelming consensus on the practical barrier due to the lack of scientists knowledgeable in both microelectronics research and synchrotron techniques. A concept for an “Advanced Metrology Center for Microelectronics” was proposed. The center should be based at a synchrotron facility, provide a suite of beamlines and well-coordinated supporting capabilities of the hosting national lab (e.g., electron/optical metrology, nanofabrication, computational modeling, co-design, etc.), and deliver integrated multimodal characterizations and analysis, optimized for microelectronics research. The panel also emphasized that such a center must be staffed with scientists who are knowledgeable in semiconductor problems and synchrotron techniques.
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**Chang-Yong Nam**
Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, New York, USA

**Yong S. Chu**
National Synchrotron Light Source II, Brookhaven National Laboratory, Upton, New York, USA

**Satyavolu Papa Rao**
NY CREATE, Albany, New York, USA
SUNY Polytechnic Institute, Albany, New York, USA

**Gabriella Carini**
Instrumentation Division, Brookhaven National Laboratory, Upton, New York, USA

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