Scaling Behavior of Sub-100 nm InAlN/GaN HEMTs on Silicon for RF Applications

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Scaling behavior of sub-100 nm InAlN/GaN HEMTs on silicon for RF applications

Peng Cui\textsuperscript{1,*} and Yuping Zeng\textsuperscript{2,*}

\textbf{Abstract}—Due to the low cost and the scaling capability of Si substrate, InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions. In this paper, a high-performance 50-nm-gate-length InAlN/GaN HEMT on Si with a high on/off current ($I_{on}/I_{off}$) ratio of $7.28 \times 10^6$, an average subthreshold swing (SS) of 72 mV/dec, a low drain-induced barrier lowering (DIBL) of 88 mV, an off-state three-terminal breakdown voltage ($BV_{d}$) of 36 V, a current/power gain cutoff frequency ($f_{T}/f_{max}$) of 140/215 GHz, and a Johnson’s figure-of-merit (JFOM) of 5.04 THz-V is simultaneously demonstrated. The device extrinsic and intrinsic parameters are extracted using equivalent circuit model, which is verified by the good agreement between simulated and measured S-parameter values. Then the scaling behavior of InAlN/GaN HEMTs on Si is predicted using the extracted extrinsic and intrinsic parameters of devices with different gate lengths ($L_g$). It presents that a $f_{T}/f_{max}$ of 230/327 GHz can be achieved when $L_g$ scales down to 20 nm with the technology developed in the study, and an improved $f_{T}/f_{max}$ of 320/353 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrown ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

\textbf{Index Terms}—InAlN/GaN HEMT, Si substrate, $f_{T}/f_{max}$, scale behavior.

\textbf{Background}—InAlN/GaN HEMTs on Si substrate have attracted more and more attentions due to the low cost and the scaling capability of Si substrate[1-4]. L. Li et al. demonstrated a InAlN/GaN HEMT on Si with a gate length ($L_g$) of 55 nm and a source-drain spacing ($L_{sd}$) of 175 nm [5]using n$^{++}$-GaN regrowth source/drain contacts. The device presents a maximum drain current ($I_{d,max}$) of 2.8 A/mm, a peak extrinsic transconductance ($g_m$) of 0.66 S/mm, and a current/power gain cutoff frequency ($f_{T}/f_{max}$) of 250/204 GHz. H. Xie et al. reported that a record $f_T$ of 310 GHz was achieved on a InAlN/GaN HEMT on Si with a 40-nm gate length [6]. P. Cui et al. demonstrated an 80-nm gate-length InAlN/GaN HEMT on Si with a record high on/off current ($I_{on}/I_{off}$) ratio of $1.58 \times 10^6$, a steep subthreshold swing (SS) of 65 mV/dec, and a $f_T$ of 200 GHz, resulting in a record high $f_T \times L_g = 16$ GHz$\cdot$μm [7]. N. Chowdhury et al. demonstrated a complementary logic circuit (an inverter) on a GaN-on-Si platform with a record maximum voltage gain of 27 V/V at an input voltage of 0.59 V with $V_{DD} = 5$ V [8]. H. Xie et al. reported an InAlN/GaN HEMT on Si with a $f_T$ of 210 GHz and a three-terminal off-state breakdown voltage ($BV_{d}$) of 46 V, leading to a record high Johnson’s figure-of-merit (JFOM = $f_T \times BV_{d}$) of 8.8 THz-V [9].

However, to the best of our knowledge, the highest $f_T/f_{max}$ of 454/444 GHz and 348/340 GHz were achieved on 20-nm-gate-length AlN/GaN HEMT [10] and 27-nm-gate-length InAlN/GaN HEMTs on SiC [11], respectively. Although excellent performances have been demonstrated, InAlN/GaN HEMTs on Si still presents much room to be improved compared with GaN HEMTs on SiC substrate. Hence, exploring the possible limiting factors of InAlN/GaN HEMTs on Si is significant to further improve the device performance. In this paper, high-performance InAlN/GaN HEMTs on Si are fabricated and demonstrated. The extrinsic and intrinsic parameters of devices with different gate lengths are extracted and the scale behavior of InAlN/GaN HEMTs on Si is predicted. It presents that a $f_T/f_{max}$ of 230/327 GHz can be achieved when $L_g$ scales down to 20 nm with the technology developed in the study, and an improved $f_T/f_{max}$ of 320/353 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMTs with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

\textbf{Experiment}

\textbf{Figure 1(a)} shows the used lattice-matched $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ heterostructure, which is grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The epilayer structure consists of a 2-nm GaN cap layer, an 8-nm $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm $\text{In}_{0.12}\text{Ga}_{0.88}\text{N}$ back-barrier layer, and a 2-μm undoped GaN buffer layer. The electron sheet concentration and electron mobility measured by Hall measurements were $2.28 \times 10^{13}$ cm$^{-2}$ and 1205 cm$^2$/V$\cdot$s, respectively.

\textbf{Figure 1(b)} shows the detailed device fabrication steps. The device fabrication started with mesa isolation using Cl$_2$/CH$_4$/He/Ar inductively coupled plasma etching. Then Ti/Al/Ni/Au stack was deposited and annealed at 850°C for 40s in N$_2$ to form the alloyed ohmic contacts. The ohmic contact resistance is 0.3 Ω$\cdot$μm. An oxygen plasma treatment was then

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applied to form the oxide layer on top of the InAlN layer, which can effectively reduce the gate leakage current and improve RF performance [12-15]. Finally, a Ni/Au T-shaped gate with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm was fabricated by electron beam lithography. Figure 1(c) shows a plan-view scanning electron microscopy (SEM) image of the InAlN/GaN HEMT with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm. Figure 1(d) shows a SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

**Results and discussion**

A. DC performance

The DC current-voltage (I–V) measurements are carried out by using an Agilent B1500A semiconductor parameter analyzer. Figure 2(a) shows the output characteristic of the InAlN/GaN HEMT with a 50-nm gate length. The device on-resistance (R_{on}) extracted at gate-source (V_{gs}) of 0 V and drain-source voltage (V_{ds}) between 0 and 0.5 V is 1.33 Ω-mm. The gate-to-channel distance (L_{ch}) (including a 2-nm GaN, an 8-nm InAlN, and a 1-nm AlN) is 11 nm. Since L_{ch} is 50 nm, the device presents an aspect ratio (L_{ch}/L_{ch}) of 4.5. Due to the low L_{ch}/L_{ch}, the short-channel effects (SCEs) start to appear when V_{ds} is larger than 5 V and V_{gs} is between -4 to -1 V. At V_{gs} = 1 V, drain current (I_{d}) in saturation region presents a decrease with increased V_{ds}, an indication of the thermal effect.

Figure 2(b) shows the transfer characteristic with the extracted extrinsic transconductance (g_{m}) of the InAlN/GaN HEMT with a 50-nm gate length at V_{ds} = 10 V. The maximum saturation drain current (I_{d,max}) is 2.01 A/mm at V_{gs} = 1 V and V_{ds} = 10 V. The g_{m} perk (g_{m,peak}) is 493 mS/mm. To the best of our knowledge, the record high I_{d,max} of 2.8 A/mm and g_{m,peak} of 660 mS/mm were achieved on a 55-nm gate-length InAlN/GaN HEMT on Si with regrowth technology and L_{sd} of 175 nm [5]. The lower both I_{d} and g_{m,peak} in this study result from the regrowth-free technology and the larger source-drain spacing (L_{sd} = 600 nm).

Figure 3(a) shows the transfer and gate current (I_{g}) characteristics in semi-log scale of the InAlN/GaN HEMT with a 50-nm gate length at V_{gs} = 5 V and 10 V, respectively. At V_{ds} = 10 V, the device off-current (I_{off}) is 2.76 x 10^{-7} A/mm and the I_{off}/I_{on} ratio is 7.28 x 10^{6}, which are higher than the record reported values (I_{off} of 7.12 x 10^{-7} A/mm and I_{off}/I_{on} ratio of 1.58 x 10^{6}) achieved from the InAlN/GaN HEMT on Si [16]. An average subthreshold swing (SS) of 72 mV/dec over more than two orders of I_{g} is extracted from the transfer curve. The drain-induced barrier lowering (DIBL) of 88 mV/V is extracted at I_{g} = 10 mA/mm between V_{gs} = 10 V and V_{ds} = 5 V, which is the lowest value among the reported GaN HEMTs on Si. The lowest DIBL value suggests a suppressed SCEs for the sub-100nm gate-length device. Figure 3(b) shows the off-state three-terminal breakdown characteristic of the 50-nm InAlN/GaN HEMT measured at V_{gs} = +8 V. The device features a BV_{ds} of 36 V at a drain leakage current of 1 mA/mm.
using a two-port short/open/load/through method. On-wafer range from 1 to 65 GHz. The network analyzer is calibrated for the RF performance improvement by further decreasing the resistance (Ω·mm) for the RF performance improvement by further decreasing the resistance (Ω·mm). For the RF performance improvement by further decreasing the resistance (Ω·mm), the 140-GHz InAlN/GaN HEMT with peak values, presenting a good device linearity. 

\[ \frac{1}{2} \times B_{\text{Vds}}(\text{max}) = 10 \text{ V and } 5 \text{ V,} \]

\[ V_{\text{gs}} = -8 \text{ V of the InAlN/GaN HEMT with a 50-nm gate length. The } B_{\text{Vds}} \text{ of 36 V was determined.} \]

**B. RF performance**

The device RF performance is measured with a frequency range from 1 to 65 GHz. The network analyzer is calibrated using a two-port short/open/load/through method. On-wafer open and short structures is used to eliminate the effects of parasitic elements. Figure 4(a) shows the current gain (|b2|), unilateral gain (U), and the maximum stable gain (MSG) as a function of frequency at V_{\text{ds}} = 10 V, V_{\text{gs}} = -3 V after de-embedding. \( f_t \times f_{\text{max}} \) of 140/215 GHz for the InAlN/GaN HEMT with a 50-nm gate length is obtained by extrapolation of |b2| as a -20 dB/dec slope. An \( f_t \times f_{\text{max}} \) of 173 GHz is obtained, which is the highest record values among the reported InAlN/GaN HEMTs on Si with regrowth-free ohmic contact technology. To the best of our knowledge, the highest \( f_t \times f_{\text{max}} \) of 226 GHz \( f_t \times f_{\text{max}} = 250/204 \text{ GHz} \) was achieved on a 55-nm InAlN/GaN HEMT on Si with regrowth technology. Here for our device, the alloyed ohmic resistance \( R_C: 0.3 \text{ Ω-mm} \) is higher than the reported regrowth ohmic contact resistance \( R_C: 0.05 \text{ Ω-mm} \) [5]. This presents a high potential for the RF performance improvement by further decreasing the ohmic contact resistance. Due to \( f_t \times f_{\text{max}} \) of 140/215 GHz, products of \( f_t \times L_g \) and \( f_{\text{max}} \times L_d \) of 7.0 and 10.75 GHz·μm are achieved, respectively. Although neither passivation nor field plate technology is used, the 140-GHz InAlN/GaN HEMT with an \( B_{\text{Vds}} \) of 36 V presents a Johnson’s figure-of-merit (JFOM = \( f_t \times B_{\text{Vds}} \)) of 5.04 THz·V. Figure 4(b) shows the measured \( f_t \) and \( f_{\text{max}} \) of the 50-nm InAlN/GaN HEMT as a function of V_{\text{gs}}. Both \( f_t \) and \( f_{\text{max}} \) show a gradual decrease compared with their peak values, presenting a good device linearity.

**C. Equivalent circuit model**

Figure 5. (a) Equivalent-circuit model for InAlN/GaN HEMT. The intrinsic elements are shown in the red dashed box. (b) Comparison of the simulated and measured S-parameters for the InAlN/GaN HEMT with a 50-nm gate length at \( V_{\text{ds}} = 10 \text{ V and } V_{\text{gs}} = -3 \text{ V.} \)
The classical 16-element equivalent-circuit model is used for the InAlN/GaN HEMT, as shown in Figure 5 (a) [17, 18]. Based on this model, the device extrinsic and intrinsic parameters are extracted in Table I [17-19]. The slight discrepancy between the simulated and measured S-parameter values is observed in Figure 5 (b), verifying the accuracy of the extracted extrinsic and intrinsic parameters. The $f_T$ and $f_{max}$ can be calculated using [17, 20]

$$f_T = \frac{G_m}{2\pi (C_{gs} + C_{gd})(1/G_m + (R_s + R_g)) + (C_{gd} \cdot G_m/G_d)(R_s + R_g)},$$

$$f_{max} = \frac{f_T}{\sqrt{2\pi L_g \cdot R_s + R_g + 2\pi f_T \cdot R_s \cdot C_{gd}}}.$$  

where $G_m$ and $G_d$ are the intrinsic transconductance and drain-source conductance, respectively; $C_{gs}$ and $C_{gd}$ are the gate-source and gate-drain parasitic capacitance, respectively; $R_s$, $R_d$, $R_g$, and $R_l$ are the parasitic source access resistance, drain access resistance, gate electrode resistance, and input resistance, respectively.

The calculated $f_T/f_{max} = 145/218$ GHz is very close to the value ($f_T/f_{max} = 140/215$ GHz) extracted by extrapolation of $|h_{21}|^2$ with a -20 dB/dec slope, which confirms the excellent device RF performance. The high intrinsic transconductance/drain-source conductance ($G_m/G_d$) ratio of 10.6 contributes to the high $f_{max}$.

### D. Scaling behavior

The InAlN/GaN HEMTs with $L_g$ between 50 nm and 350 nm are fabricated. Figure 6(a) shows the measured $f_T/f_{max}$ of the InAlN/GaN HEMTs with different $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V. The devices with $L_g$ of 50, 70, 100, 150, 250, and 350 nm present $f_T/f_{max}$ of 140/215, 135/205, 120/170, 90/160, 60/136, 36/128 GHz, respectively. $f_T \times L_g$ and $f_{max} \times L_g$ are obtained in Figure 6(b). A $f_T \times L_g$ peak of 15 GHz·µm is achieved on the 250-nm-gate-length InAlN/GaN HEMT with a $f_T$ of 135 GHz. $f_{max} \times L_g$ presents a decrease from 44.8 GHz·µm ($L_g = 350$ nm) to 10.75 GHz·µm ($L_g = 50$ nm). The decrease of both $f_T \times L_g$ and $f_{max} \times L_g$ as $L_g$ scales down means that the effect of parasitic parameters is more pronounced, thus hindering the improvement of $f_T$ and $f_{max}$. Due to the large head length of T-shaped gate ($L_{head} = 400$ nm), the transistors features higher $f_{max}$ and $f_{max} \times L_g$.

### Table I

| Extrinsic parameters | Intrinsic parameters |
|----------------------|----------------------|
| $C_{pgd} = 1.16$ fF  | $C_{gs} = 444$ fF/mm |
| $C_{pgs} = 26.35$ fF | $C_{gd} = 104$ fF/mm |
| $C_{psh} = 26.21$ fF | $C_d = 318$ fF/mm |
| $L_s = 3.17$ pH      | $R_i = 0.90$ Ω mm |
| $L_g = 4.03$ pH      | $G_m = 573$ mS/mm |
| $L_d = 4.30$ pH      | $G_0 = 54$ mS/mm |
| $R_s = 0.43$ Ω mm   | $R_s/G_0 = 10.6$ |
| $R_d = 0.26$ Ω mm   | $\tau = 1.09$ ps |
| $R_L = 0.45$ Ω mm   | $f_{T, model} = 145$ GHz |
|                     | $f_{max, model} = 218$ GHz |

Figure 6. (a) Measured $f_T$ and $f_{max}$ as a function of $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V. (b) $f_T \times L_g$ and $f_{max} \times L_g$ as a function of $L_g$.

Figure 7. Measured and linear fitted (a) gate-source parasitic capacitance $C_{gs}$ and (b) gate-drain parasitic capacitance $C_{gd}$ as a function of $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V.
To shed more light on the scaling behavior, the extrinsic and intrinsic parameters of these devices are further extracted using the equivalent circuit model discussed above. $C_{gs}$ can be separated to two parts: gate-source intrinsic capacitance ($C_{gs,int}$) and gate-source extrinsic capacitance ($C_{gs,ext}$). It means $C_{gs} = C_{gs,int} + C_{gs,ext}$ [21]. $C_{gd}$ is the same with $C_{gs}$ and can also be written as $C_{gd} = C_{gd,int} + C_{gd,ext}$. Figure 7 shows the extracted $C_{gs}$ and $C_{gd}$ as a function of $L_g$. Both $C_{gs}$ and $C_{gd}$ present a linear dependence upon $L_g$. By linear fitting, the $C_{gs,ext}$ and $C_{gd,ext}$ are obtained from $C_{gs}$ and $C_{gd}$ at $L_g = 0$ nm [21], as shown in Figure 7. Here $C_{gs,ext}$ of 93.05 fF/mm and $C_{gd,ext}$ of 97.65 fF/mm are determined, respectively.

The total delay ($\tau$) of transistors can be written as [21] [22]

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \quad (2)$$

Here $\tau$ is partitioned into three components: transit time ($\tau_t$), parasitic charging delay ($\tau_{ext}$), and parasitic resistance delay ($\tau_{par}$).

$\tau_t$ is the transit time under the gate region. It is related to the gate length as well as the electron velocity ($v_e$) under the gate region, and can be calculated by [21] [22]

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{G_m} = \frac{L_g}{v_e}. \quad (3)$$

$\tau_{ext}$ is parasitic charging delay through $C_{gs,ext}$ as well as $C_{gd,ext}$, and can be written as [21] [22]

$$\tau_{ext} = \frac{C_{gs,ext} + C_{gd,ext}}{G_m}. \quad (4)$$

$\tau_{par}$ is parasitic resistance delay mainly associated with $R$, as well as $R_d$, and can be written as [21] [22]

$$\tau_{par} = C_{gd}(R_g + R_d)[1 + \left(\frac{C_{gs}}{C_{gd}}\frac{G_m}{G_n}\right)]. \quad (5)$$

**Figure 8.** Extracted delay ($\tau$) and electron velocity ($v_e$) as a function of $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V.

**Figure 9.** Extracted intrinsic transconductance ($G_m$) and intrinsic conductance ($G_n$) as a function of $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V.

**Figure 10.** Extracted delay components as a function of $L_g$. The delay ($\tau$) is partitioned into three components: transit time ($\tau_t$), parasitic charging delay ($\tau_{ext}$), and parasitic resistance delay ($\tau_{par}$).
Supplementary Information

Not applicable.

Abbreviations

HEMT: high-electron-mobility transistors; $I_{on}/I_{off}$: on/off current ratio; SS: subthreshold swing; DIBL: low drain-induced barrier lowing; $BV_{ds}$: off-state three-terminal breakdown voltage; $f_{T}/f_{max}$: current/power gain cutoff frequency; JFOM: Johnson’s figure-of-merit; $g_{m}$: extrinsic transconductance; MOCVD: metalorganic chemical vapor deposition; SEM: scanning electron microscopy; $I_{d}$: drain current; $I_{g}$: gate current; $L_{g}$: gate length; $L_{sd}$: source-drain spacing; $V_{gs}$: gate-source voltage; $V_{ds}$: drain-source voltage; $R_{on}$: on-resistance; SCEs: short-channel effects; $|h_{11}|$: current gain; U: unilateral gain; MSG: maximum stable gain.

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The authors declare that they have no competing interests.

Authors’ Contributions

P. C. and Y. Z. contributed to the research design, experiment measurements, data analysis, and manuscript preparation. All authors reviewed this manuscript.

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

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Competing interests

The authors declare that they have no competing interests.
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