Radiation tolerance tests of SRAM-based FPGAs for the potential usage in the readout electronics for the LHCb experiment

C. Färber, U. Uwer, D. Wiedner, B. Leverington and R. Ekelhof

Physikalisches Institut, Ruprecht-Karls-Universität Heidelberg, Im Neuenheimer Feld 226, 69120 Heidelberg, Germany
Experimentelle Physik 5, Technische Universität Dortmund, Otto-Hahn-Strasse 4, 44227 Dortmund, Germany

E-mail: Faerber@Physi.Uni-Heidelberg.de

ABSTRACT: This paper describes radiation studies of a SRAM-based FPGA as a central component for a upgrade of the LHCb Outer Tracker front-end electronics to a readout frequency of 40 MHz. Two Arria GX FPGAs were irradiated with 20 MeV protons to radiation doses of up to 7 Mrad. During and between the irradiation periods the different FPGA currents, the package temperature, the firmware error rate, the PLL stability, and the stability of a 32 channel TDC implemented on the FPGA were monitored. Results on the radiation tolerance of the FPGA and the measured firmware error rates will be presented. The Arria GX FPGA fulfills the radiation tolerance required for the LHCb upgrade (30 krad) and an expected firmware error rate of roughly $10^{-6}$ Hz makes the chip a possible component for the upgraded front-end electronics.

KEYWORDS: Front-end electronics for detector readout; Electronic detector readout concepts (gas, liquid); Radiation-hard electronics; CMOS readout of gaseous detectors
1 Introduction

The LHCb collaboration plans to increase the operation luminosity to $2 \cdot 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ by 2018, which is a factor of 10 higher than the original design luminosity. To profit fully from the increased luminosity the current maximum trigger rate of 1.1 MHz has to be overcome. This is achieved with a 40 MHz readout and a much more flexible software-based trigger system [1]. In addition to the maximum readout rate of the current readout electronics also the bandwidth of the current GBit transceivers (GOL chip with 1.6 GBit/s) are too low for the upgrade of the LHCb detector. These chips have to be replaced.

One possible solution for regions with lower radiation levels are modern SRAM-based FPGAs with high bandwidth transceivers. These devices provide a large number of logic elements to realize even large and fast applications such as multi channel TDCs with time resolutions below 1 ns. The use of commercial FPGAs would reduce investment in time and money. Therefore the radiation hardness of these chips is of high interest to the High Energy Physics community.

The total ionization dose (TID) hardness of commercial SRAM cells increases with the downscaling of the CMOS process, due to the fact, that the life-time of trapped positive charges in the gate oxide is dramatically decreased. Therefore the threshold voltage shifts are of little concern while the leakage currents have become important nowadays. For modern SRAM cells, produced in a commercial 90 nm CMOS process, a total ionization dose hardness of roughly 300 krad can be expected [2]. This makes the usage of modern SRAM-based FPGAs also possible for on-detector readout electronics, like for the LHCb Outer Tracker upgrade as proposed in this paper. For the
updated readout electronics an integrated ionization dose of 30 krad and an integrated flux of $4 \cdot 10^{12}$ 1 MeV neutron equivalent/cm$^2$ is expected. The large amount of neutrons at the position of the LHCb Outer Tracker readout electronics is caused by neutron emission of the calorimeters.

Especially for SRAM-based FPGAs the mis-configuration of the firmware due to irradiation has to be studied. It is very important to measure the cross section of bit flips in the configuration registers, to calculate the expected rate for the planned detector. Modern SRAM-based FPGAs have functions to detect errors in the firmware, which makes it possible to reprogram the FPGA in response to a configuration error.

2 FPGA irradiation test board

The FPGA irradiation test board (see figure 1) hosts an Arria GX (EP1AGX35DF780I6) FPGA [3], which is used as 32 channel TDC and GBit/s transceiver. Two optical links with SFP modules are connected to the 3.125 GBit/s transceivers of the Arria GX for the readout. Five radiation hard power regulators (LHC4913) are used to power the PCB. An I$^2$C bus is used for the monitoring and control of the FPGA. Furthermore two LEMO outputs are used for the clock signal monitoring. Four 80 pin connectors are placed on the PCB to connect the LHCb Outer Tracker pre-amplifier boards. The trigger and control signals can be connected through the front connector and three hex switches are used for the board address. The newly developed test board is completely pin compatible to the existing LHCb Outer Tracker readout electronics.

Furthermore eight parasitic resistors were used to monitor the different FPGA currents with an eight channel 14 bit ADC. The FPGA test board was actively cooled with a Peltier element. Furthermore, the FPGA package temperature was monitored during the whole irradiation campaign and stayed constant at $(30 \pm 1) ^\circ C$. 

Figure 1. FPGA irradiation test board. Parasitic resistors marked with red circles are used for indirect current measurements with the help of a multi channel 14 bit ADC. Two SFP modules are used for optical data readout with $2 \times 3.125$ GBit/s transceivers.
3 Irradiation environment

Two test boards, namely test board 1 (test board 2) were irradiated with 20 MeV protons up to a dose of 7 Mrad (31 Mrad) corresponding to an integrated proton flux of $1.2 \cdot 10^{13}$ protons/cm$^2$ ($5.3 \cdot 10^{13}$ protons/cm$^2$) which corresponds to $6 \cdot 10^{13}$ 1 MeV neutron equivalent/cm$^2$ ($3 \cdot 10^{14}$ 1 MeV neutron equivalent/cm$^2$). The average proton flux for the FPGA was varied in the different irradiation periods between $2 \cdot 10^7$ protons $\cdot$ Hz/cm$^2$–$6 \cdot 10^9$ protons $\cdot$ Hz/cm$^2$, and the different irradiation periods had durations between (5–45) min. The FPGA test board was attached to a frame (see figure 2) which was mounted on to a flange of a vacuum vessel. The proton beam exited the vessel through a 100 $\mu$m stainless steel window in the flange. In addition, it was possible to collimate the proton beam which allowed the measurement of the proton beam profile for the dosimetry (see next subsection 3.1).

3.1 Dose determination

The dose was determined from a simulation based on the measured proton beam profile and passive dosimeters. The proton beam profile was measured with a straw-tube detector which was installed downstream of the FPGA test board layer. The proton flux over the chip varied by $+40\% / -50\%$ however 70% of the chip area received at least the average flux. Throughout this paper only the average flux is considered. The beam current was measured with a Faraday cup inside the proton beam line. Figure 3 shows the simulation of the proton flux for a 1 nA proton beam. A 2-dimensional Gaussian fit to the data was used to parameterize the proton beam profile. During the irradiation periods only the beam intensity was changed assuming that the beam profile stayed unchanged. The energy loss of the protons along their trajectory was calculated to determine the integrated ionization dose (TID) of the different objects inside the proton beam. The energy loss of the protons for the different objects of the irradiation setup was calculated using the ATIMA program [4] from GSI. The energy loss of the protons inside the alanine sticks has been determined with the help of the stopping power from the PSTAR data base of the National Institute of Standards and Technology U.S.A. [5].
Figure 3. Beam simulation for a proton beam current of 1 nA.

The simulation was cross checked with six passive dosimeters (alanine) [6], grouped into pairs. The measured and simulated doses are in good agreement.

4 Total ionization dose results

The TID influence on the currents of different parts of the FPGA were monitored. Furthermore, the stability of the phase locked loop (PLL) and TDC implemented on the FPGA were checked.

4.1 Current measurements

Currents of different parts of the FPGA were monitored. These parts are the internal logic arrays (core current), the six I/O banks (I/O current), the voltage buffers of the configuration input pins and JTAG pins (configuration current), the phase locked loops (PLL current) and the GBit transceivers (analog currents and digital current). These currents were monitored with the help of the resistors marked with red circles in figure 1 and a multi channel ADC.

All currents were stable up to 150 krad. The first permanent current changes were observed in the FPGA core current shown in figure 4. During the irradiation periods small rises and drops of the current are visible which disappear after a power cycle of the FPGA. After 150 krad the value without irradiation increases and reaches a level of 106.5% after a TID of 7 Mrad. After 400 krad a decrease in the I/O current was observed which reaches a level of 94% after 7 Mrad. Also the configuration current and the current of the digital part of the transceivers show permanent changes in the percent level. The PLL current and the transceiver analog currents did not show permanent irradiation effects. All current changes are between 5%–20% and rather small. Judging from the current measurements the TID hardness of the Arria GX FPGA is high enough for the upgrade of the LHCb Outer Tracker.

4.2 PLL stability

Three clock signals were monitored with a 1 GHz oscilloscope to check the stability of the enhanced PLLs and the fast PLL of the transceivers. The frequency of the three clock signals as well as the phase between two clocks were measured with the oscilloscope. The enhanced PLLs were tested with the 312.25 MHz TDC clock and the 39 MHz system clock of the FPGA test board. Both were connected to the oscilloscope.
Figure 4. FPGA core current (green) of the first test board as a function of time. Also shown is the accumulated dose (black). In total the current rises by 6.5% after a integrated dose of 7 Mrad. Drops and rises of the current during the high intensity irradiations are visible, which are caused by mis-configured firmware and which disappear after reconfiguration of the FPGA.

The fast PLL of the GBit/s transceivers was tested with an optical data transmission link. One optical fiber was used to connect the GBit/s transmitter of the FPGA test board and the receiver of a Stratix IV development board [7]. The receiver recovers the transmitter clock which is used for the deserialization afterwards. This 156.12 MHz clock was wired to the oscilloscope.

The three frequencies were stable throughout the whole irradiation campaign for both FPGA test boards. The phase between the TDC clock and the system clock showed a shift from $-150^\circ$ to larger values up to $-100^\circ$ after 3 Mrad for test board 1. There is no phase measurement for the test board 2.

4.3 TDC stability

The TDC stability was monitored using measurements of the 19 MHz clock signal as hit signal hardwired to the TDC channel inputs. The 32 channel TDC uses a combination of a fast counter and phase shifted clocks for the fine timing. The TDC bin size is 790 ps and the double pulse resolution is below 25 ns.

Figure 5 shows the behavior for the TDC channel 9 of FPGA test board 1. The measured delay is stable at the value 13 up to a TID of 400 krad. For higher TIDs the time measurement shows a charge up effect, which is not visible in the plot. After an irradiation period the measured delay is shifted to larger values and during the break between the irradiation periods the measured delay falls back to the default value of 13. The test board 2 shows first degradation in the TDC stability after 4 Mrad.

5 Soft-error results

The SRAM cells for the configuration registers are not radiation tolerant by design. Therefore it is crucial to measure the cross section for firmware bit flips to calculate the expected upset rate of the FPGA configuration registers in the detector environment.
5.1 Proton cross section for configuration registers

The Arria GX FPGAs have a configuration register checker which sets a pin high once a single error was found. This pin was monitored with external electronics. After an error occurred the FPGA was power cycled to reprogram the FPGA. This procedure took roughly 1 s. The proton flux during this test was $2.3 \times 10^7$ protons · Hz/cm$^2$. This intensity corresponds to $5.4 \times 10^4$ times the expected dose rate for the LHCb Outer Tracker electronics. Test board 1 was used for this measurement during its first irradiation period.

The average time between a power cycle and a detected configuration register flip is $(27.9 \pm 3.2)$ s which corresponds to $(2.4 \pm 0.3)$ firmware errors/krad. The proton cross section was determined to be $1.6 \times 10^{-9}$ cm$^2$ per device or $1.6 \times 10^{-16}$ cm$^2$ per bit. This cross section is a factor 5–50 smaller than the cross sections for older SRAM-based FPGAs measured previously [8–10].

The firmware error rate was determined for an irradiation intensity of $1.5 \times 10^{-2}$ krad/s which corresponds to $5.4 \times 10^4$ times the expected LHCb Outer Tracker upgrade intensity. Scaling the error rate to the expected LHCb upgrade radiation environment, corresponding to $2.9 \times 10^{-7}$ krad/s, one firmware error every $1.5 \times 10^6$ s per chip is expected.

6 Conclusion

Two SRAM-based Arria GX FPGAs (EP1AGX35DF780I6) from Altera have been irradiated with 20 MeV protons up to a TID of 7 Mrad (31 Mrad) corresponding to an integrated proton flux of $1.2 \times 10^{15}$ protons/cm$^2$ ($5.3 \times 10^{13}$ protons/cm$^2$). The FPGAs sustained the TID of 30 krad expected for the upgrade of the LHCb Outer Tracker readout without measurable degradation. First effects due to the irradiation were seen after 150 krad in the FPGA core current which began to rise. All permanent current changes are between 5%–20% and rather small. In addition, the first malfunction of the TDC was detected after 400 krad which is consistent with the expected TID hardness of modern 90 nm CMOS SRAM cells [2].Furthermore the proton cross section for the FPGA configuration registers flips was measured, it is $1.6 \times 10^{-9}$ cm$^2$ per device or $1.6 \times 10^{-16}$ cm$^2$ per bit.
In the LHCb Outer Tracker upgrade environment a firmware upset rate of $6.6 \cdot 10^{-7}$ Hz/FPGA is expected which seems to be manageable.

Acknowledgments

We would like to thank the team of the Tandem van-de-Graaff Accelerator of the Max Planck Institute for Nuclear Physics in Heidelberg for their precious support and help during the irradiation campaign. In addition we would like to thank Mr. Esteban Rubio from the electronics department of the Physikalische Institut University Heidelberg for the help and development of the test board and the LHCb radiation safety group for the analysis of the passive dosimeters.

References

[1] LHCb collaboration, Letter of intent for the LHCb Upgrade, CERN-LHCC-2011-001 (2011).
[2] Y. Boulghassoul et al., TID damage and annealing response of 90 nm commercial-density SRAMs, in Proceedings of the European Workshop on Radiation Effects on Components and Systems (RADECS 2008), Jyväskylä Finland (2008), http://www.isi.edu/~draper/papers/Radecs_2008_Y-Boulghassoul_final.pdf.
[3] Altera Corporation, Arria GX device handbook (2009), http://www.altera.com/literature/hb/agx/arriagx_handbook.pdf.
[4] ATIMA web page, http://web-docs.gsi.de/~weick/atima/.
[5] PSTAR web page, National Institute of Standards and Technology, http://physics.nist.gov/PhysRefData/Star/Text/PSTAR.html.
[6] F. Coninckx, H. Schönbacher, A. Bartolotta, S. Onori and A. Rosati, Alanine dosimetry as the reference dosimetric system in accelerator radiation environments, Int. J. Radiat. Appl. Instrum. 40 (1989) 977.
[7] Altera Corporation, Stratix IV GX FPGA development board reference manual (2012).
[8] P. Antonioli et al., Radiation tests of key components of the ALICE TOF TDC readout module, in Proceedings of the 10th Workshop on Electronics for LHC Experiments and Future Experiments, Boston U.S.A. (2004).
[9] N.J. Buchanan and D.M. Gingrich, Proton induced radiation effects on a Xilinx FPGA and estimates of SEE in the ATLAS environment, ATLAS Note ATL-LARG-2001-011 (2001).
[10] E. Fuller, M. Caffrey, A. Salazar, C. Carmichael and J. Fabula, Radiation testing update, SEU mitigation and availability analysis of the Virtex FPGA for space re-configurable computing, in Proceedings of the IEEE Nuclear and Space Radiation Effects Conference, Reno U.S.A. (2000).