Mapping DEVS Models onto UML Models

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Abstract
Discrete event simulation specification (DEVS) is a formalism designed to describe both discrete state and continuous state systems. It is a powerful abstract mathematical notation. However, until recently it lacked proper graphical representation, which made computer simulation of DEVS models a challenging issue. Unified modeling language (UML) is a multipurpose graphical modeling language, a de-facto industrial modeling standard. There exist several commercial and open-source UML editors and code generators. Most of them can save UML models in XML-based XMI files ready for further automated processing. In this paper, we propose a mapping of DEVS models onto UML state and component diagrams. This mapping may lead to an eventual unification of the two modeling formalisms, combining the abstractness of DEVS and expressive power and “computer friendliness” of the UML.

1. INTRODUCTION

Discrete event simulation specification (DEVS [11]–[13]) is a powerful formalism for describing discrete event state systems. Various flavors of both formalism have been developed. In this paper, we are using classic DEVS with ports, which we call, simply, DEVS. Being hierarchical and encapsulated, the DEVS formalism can be naturally implemented in an object-oriented language, such as Java [9]. However, Java-based simulation environments have never been standardized (unlike the DEVS formalism).

An important drawback of the DEVS formalism is the lack of a standardized graphics representation. In [2], an attempt has been undertaken to develop DCharts, a graphics language for DEVS models. DCharts is a UML-based language; however, it does not strictly follow any UML standard. Moreover, the DEVS-to-DCharts transformation proposed in [2] collapses all DEVS states into one DCharts state, essentially eliminating the discrete state nature of DEVS models.

In [5], it is proposed that atomic DEVS models be represented with the help of UML sequence diagrams. However, the sequence diagrams show actual, rather than potential, flow of events. Because of this, a sequence diagram is limited to a particular scenario and cannot unambiguously describe the behavior of a system in its entirety.

An excellent mapping between DEVS models and UML state charts has been introduced in [10]. However, the paper does not suggest a formal mathematical way of constructing the state charts, and thus avoids the issue of the structural clash between DEVS continuous states and UML finite states. It also relies on the older versions of the UML (< 2.0), which did not have an explicit notion of time.

In this paper, we propose a consistent DEVS-to-UML mapping that takes care of all issues mentioned above. Further restricting the mapping to the executable UML (which is a proper subset of UML [7]) would make a seamless connection between a DEVS model and an UML simulation process, but this topic is beyond the scope of this paper.

2. DEVS FORMALISM

DEVS supports two complementary models of describing discrete systems: an atomic model that specifies the behavior of an elementary system, and a coupled model that allows us to form more complex models by structurally interconnecting atomic and other coupled models.

A DEVS atomic model is a state machine with input ports \( IP = \{ \pi_i^{in} \} \) and output ports \( OP = \{ \pi_i^{out} \} \). Events are associated with input and output ports (they happen at input ports and are generated at output ports). In general, states, unlike events, are not discrete.

2.1. Atomic Models

Atomic DEVS model \( M_a \) is a tuple of nine values \( M_a = \{ IP, OP, X, \Sigma, Y, \delta_i, \delta_{ext}, \lambda, t_a \} \). Here, IP and OP are sets of input and output ports.

\( \Sigma \) is a set of states \( \{ \sigma_i \} \). A DEVS state \( \sigma_i \) is uniquely identified with a set of state variables \( \gamma_i = \{ \gamma_{ij} \mid \sigma_i \neq \sigma_k \Leftrightarrow \exists j \mid \gamma_{ij} \neq \gamma_{kj} \} \).

\( X \) is a set of input events \( \{ x_i = (\pi_i^{in}, v_i) \} \), where \( \pi_i^{in} \in IP \) is the port name, and \( v_i \) is the event value. Every event has an associated timestamp, or scheduled time—the time when the event is triggered.

\( Y \) is a set of output events \( \{ y_i = (\pi_i^{out}, v_i) \} \), where \( \pi_i^{out} \in OP \) is the port name, or the event type, and \( v_i \) is the event value. The semantics of the model are as follows: the system stays in state \( \sigma_i \) for \( t_a(\sigma_i) \) time units (until a timeout event) or until an external event happens, whatever comes first. In the case of an external event \( x_j \), the system changes its state to \( \delta_{ext}(\sigma_i, x_j) \). In the case of a timeout, the system changes its state to \( \delta_{int}(\sigma_i) \) and generates an event of type \( \lambda(\sigma_i) \). In either case, the simulation time is implicitly advanced to the timestamp of the event that triggered the transition. The initial state of the model is not defined explicitly.
2.2. Coupled Models

Coupled models are used to compose atomic and other coupled models to produce more DEVS models in a hierarchical way (Figure 1).

![Figure 1. Atomic and coupled DEVs models](image)

Coupled DEVs model \( N \) is a tuple of ten values \( N = \{IP, OP, X, Y, D, M, E_{IC}, E_{OC}, IC, S\} \). Here, \( IP \) and \( OP \) are sets of external (not coupled) input and output ports. \( X \) is a set of input events \( x_i = (\pi_i^{in}, v_i) \), where \( \pi_i^{in} \in IP \) is the port name, and \( v_i \) is the event value, and \( Y \) is a set of output events \( y_i = (\pi_i^{out}, v_i) \), where \( \pi_i^{out} \in OP \) is the port name, and \( v_i \) is the event value.

\[ D = \{d_i\} \] is a set of references to the coupled components (atomic models or other coupled models), and \( M = \{M_d|d \in D\} \) is a set of the coupled components. \( E_{IC} \subseteq \{(\{N, IP\}, (d, IP_d))|IP_i \in IP, d \in D, IP_{di} \in IP_d\} \) is external input coupling that connects external input ports of the coupled model to the components’ input ports \( IP_d \). \( E_{OC} \subseteq \{(d, OP_d), ((N, OP_i)|OP_i \in OP, d \in D, OP_{di} \in OP_d\} \) is external output coupling that connects components’ output ports \( OP_d \) to the external output ports of the coupled model. \( IC = \{(a, OP_{ai}), (b, IP_{bj})|a, b \in D, OP_{ai} \in OP_a, IP_{bj} \in IP_b\} \) is internal coupling that interconnects output and input ports of the components. Finally, \( S : \{\epsilon_d|d \in D\} \rightarrow \epsilon_d \) is a selection function that resolves potential scheduling conflicts, when more than one event in different components has the same scheduled time.

Under the principle of closure, a coupled model looks externally like an atomic model and can be used anywhere in place of an atomic model.

A coupled model is simulated as an ensemble of its DEVs components. Output events generated by each individual component are propagated to the input ports of other coupled components or to the output ports of the model, according to the functions \( IC \) and \( E_{OC} \). In the former case, they are also converted into appropriate input events. Input events received by the model are propagated to the input ports of its components, according to the function \( E_{IC} \).

Classic DEVs formalism does not permit feedback loops: \((d, OP_{di}), (e, OP_{ej}) \in IC \Rightarrow \) \( d \neq e \).

3. UML Formalism

The Unified Modeling Language (UML [1]), a de-facto industrial modeling standard, seems to be a natural choice for a visual representation of DEVs. Besides being widely supported by both proprietary and open-source tools (such as Rose [6] and Poseidon [3]), it also has an associated XML-based representation, XMI, that makes it possible to process UML diagrams by application programs.

Of particular interest for us are UML state and component diagrams, which will be discussed in detail.

3.1. State Diagrams

A UML state diagram (also known as a statechart, Figure 2) is a visual representation of a finite state automaton with history. Many of the features of state diagrams, such as “do” activities, history states, junction and choice states, concurrent and composite states, are not essential for DEVS-to-UML mappings and will not be considered.

![Figure 2. A UML state diagram](image)

A state diagram is a tuple \( SD = \{S, S^*, S^0, P, T\} \). Here \( S = \{s_i \in G_i, \nu_i, q_i\} \) is a set of finite states. UML finite states are enumerated using state variable \( G \), such that \( s_i = s_j \iff G_i = G_j \). \( \nu_i(x) : \) any \( \rightarrow \) None is an “entry” action. This action is executed just before changing the current state of the model to \( s_i, q_i(x) : \) any \( \rightarrow \) None is an “exit” action. This action is executed just before changing the current state of the model from \( s_i \) to some other state.

A set of possibly continuous pseudostate variables \( H = \{h_k\} |H| \geq 0 \) extends the definition of a UML state. The pseudostate variables may or may not have different values in different states. They cannot be used to distinguish UML states in a state diagram. An optional class diagram of the UML system can be used to record these variables in the model (Figure 3).

![Figure 3. A UML class diagram that consists of only one class definition](image)

\[ S^* = \{s_i \in S\} \] is the set of the initial states of the diagram. Every diagram can have at most one initial state. Because DEVs formalism does not specify the initial state of the system, we will assume that in general \( S^* = \emptyset \).

\[ S^0 = \{s_i \in S\} \] is the set final (terminal) states of the diagram. Because the final state of a DEVs system is not defined, we will assume that in general \( S^0 = \emptyset \).

\( P = \{p_i\} \) is a set of discrete events. Each event \( p_i \) has the associated scheduled time \( \tau_j \) and a possibly empty set of other attributes.
Finally, $T = \{ s_{i1}, s_{e1}, p_1, g_1, a_1 | s_{i1}, s_{e1} \in S, p_1 \in P; g_1(x) : \text{range}(x) \rightarrow \{ \text{True}, \text{False} \}, a_1(y) : \text{any} \rightarrow \text{None} \}$ is a set of transitions. In UML notation, a transition from state $s_{i1}$ to state $s_{e1}$ on event $p_1$ with guard condition $g_1$ is denoted as $p_1[g_1]/a_1$. Action $a_1$ is executed just before the completion of the transition. The action is not allowed to change the UML state of the system.

The semantics of a UML state diagram prescribes that in the course of transition $t_i$ from state $s_j$ to state $s_k$ the "exit" action $q_1$ is executed first, followed by the transition action $a_i$, followed by the "entry" action $w_k$.

3.2. Component Diagrams

UML component diagrams have evolved substantially from version 1.x of the language to the current 2.0 [1], [8]. The direction of the evolution has favored the DEVS-to-UML mapping we are about to propose.

In the latest version of the language, deployment, object, and component diagrams have been merged into a single class of deployment/object/component (DOC) diagrams. These new DOC diagrams have a rich language suitable for elaborated models, but for the purpose of this paper we need to mention only components, interfaces, and ports.

![Figure 4. A UML component diagram](image)

A UML component diagram is a tuple $N^u = \{ M^u, Q^u, E^u, C^u \}$.

Here, $M^u = \{ M_i^u \}$ is a list of components in the diagram. Each component $M_i^u$ has list $P_i^u = \{ p_{ij} = (t_{ij}, i, j, d_{ij}) \}$ of externally visible ports. A UML port $p$ has a type. The type of the port specifies the names of the signals (events) that are acceptable through this port. For the purpose of this paper, we assume that the type of the port is the same as its name. A port can be unidirectional (input or output) or bidirectional. The direction of the port $\text{dir}(p_{ij})$ is defined by the type(s) of its interfaces. Since DEVS formalism does not support bidirectional ports, we will not consider them and consider only one interface $K = \{ n, d \}$ per port, where $n$ is the name of the interface and $d = \{ \text{required} | \text{provided} \}$ is its type. Required interfaces (“antennas”) define output ports, and provided interfaces (“lollipops”) define input ports.

A UML component represents either another UML component diagram, or a UML state diagram.

Set $Q^u \subseteq \{ (M_i^u, M_j^u) | M_i^u \subseteq M^n \land M_j^u \subseteq M^n \}$ defines the containment relation: component $M$ is a subcomponent of component $N$, or a nested component, if $(N, M) \in Q^u$. Let $Z(N) = \{ M_i | M_i \in M^n \land ((N, M_i) \in Q^u \lor \exists M_j : M_j \in Z(N)) \}$ be the set of children of $N$. The containment relation must satisfy additional conditions: (a) a component cannot be a subcomponent of itself: $\forall M \in M^n : (M, M) \notin Q^u$ and (b) if $M$ is a subcomponent of component $N$, then $N$ cannot be a subcomponent of $M$ or of any child of $M$: $(N, M) \in Q^u \iff (M, N) \notin Q^u \land M \in Z(M) : (M', N) \notin Q^u$.

Components $T_{N^u} = \{ T_i | T_i \in M^n \land \forall M \in M^n : (T_i, M) \notin Q^u \}$ are called top-level components. The set:

$$E^u \subseteq \{ ((M_i, p_{ik}), (M_j, p_{jl})) | M_i \in M^n \land M_j \in M^n \land (M_i, M_j) \in Q^u \land \exists p_{ik} \in P_i^n \land p_{jl} \in P_j^n \land \text{dir}(p_{ik}) = \text{dir}(p_{jl}) \}$$

is the external coupling that connects external ports of the component to the subcomponents’ ports using UML delegation connectors. External ports must be connected to the internal ports of the same direction. The set:

$$I^u \subseteq \{ ((M_i, p_{ik}), (M_j, p_{jl})) | M_i \in M^n \land M_j \in M^n \land \exists p_{ik} \in P_i^n \land p_{jl} \in P_j^n \land \text{dir}(p_{ik}) \neq \text{dir}(p_{jl}) \}$$

is the internal coupling that interconnects ports of the subcomponents of the same component using UML assembly connectors. Internal ports must be connected to the internal ports of the opposite direction. Graphically, this is accomplished by matching “antennas” and “lollipops”.

A simple UML component diagram (strictly speaking, a DOC diagram) is shown in Figure 4. It depicts two components M1 and M2. These components are in turn subcomponents of component A. Component A has two output ports E1Out and E2Out with interface ISend and one input port E3In with interface IRcv. The output ports of subcomponents M1 and M2 are connected to the corresponding output ports of the component A, the input port of A is connected to the input port of subcomponent M1. Finally, the output port E4Out of component M1 with interface ISend is connected to the input port E4In of component M2 with interface IRcv.

Composite structure diagrams, which only recently have become a part of the UML 2.0 proposal [4], offer even better mapping between DEVS models and UML models. However, the discussion of these diagrams is beyond the scope of this paper.

4. ATOMIC DEVS AND UML STATE DIAGRAMS

To map an atomic DEVS model into an UML state diagram, we need to map states, ports, transitions, and outputs.

4.1. States

In general, DEVS states are neither discrete nor finite, while UML states are always discrete and finite. To map a DEVS system onto an UML system, the DEVS state must be
discretized. This can be done by rearranging and grouping DEVS state variables $\gamma = \{\gamma_j\}$ according to their kind. Discrete and finite variables can be collected in one subgroup, and countable and continuous variables—into another subgroup:

$$\gamma = (\gamma_1, \ldots, \gamma_m, \gamma_{m+1}, \ldots, \gamma_n), 1 \leq m \leq n$$

- \(\text{range}(\gamma_j) < \infty, 1 \leq j \leq m\)
- \(\text{range}(\gamma_j) = \infty, m < j \leq n\)

Let's call the first group finite DEVS state variables, and the other group free DEVS state variables.

For any feasible combination of values of finite DEVS state variables $\{\gamma_i|1 \leq i \leq m\}$, a UML finite state can be constructed by simply enumerating this combination: $G_j = \Theta_{i=1}^{m} \gamma_i$, where the details of the function $\Theta$ are not important as long as it always maps distinct combinations of finite DEVS state variables onto distinct UML states.

All remaining DEVS free state variables $\{\gamma_i|m < i \leq n\}$ are mapped to UML pseudostate variables $H = \{h_i|1 \leq i < n - m\}$ one-to-one. They become attributes of finite states and will be manipulated during DEVS state transitions.

In the case of $m = 0$ a DEVS model has no finite state variables, and partitioning (3) is not possible. The UML state diagram will have only one final state. This case is presented in [2].

On the other hand, when $m = n$, the DEVS model has no free variables. Every feasible combination of the DEVS state variables maps onto a UML finite state, and the UML model has no pseudostate variables.

Not being a dynamic simulation language, UML does not enforce an explicit notion of time in all types of diagrams. In particular, UML state diagrams do not have explicit time. The simulation time has to be maintained implicitly, with model-wide variable $t_{\text{curr}}$ denoting the current simulation time.

For the purpose of computing state transitions, many DEVS models depend on the time $e_i$ spent by the model in state $\sigma_i$. To accommodate this need, we introduce another model-wide variable $t_e$—the time of the most recent state transition. An “entry” action $w_e$ can be added to every UML finite state that records the value of $t_e$:

$$
\text{def } w_e() : \\
\text{ } t_e = t_{\text{curr}}
$$

At any given time, the value of $e_i$ can be now computed as:

$$
\begin{align*}
  e_i &= t_{\text{curr}} - t_e & \text{if } i \text{ is the current state}, \\
  &\infty & \text{otherwise}.
\end{align*}
$$

4.2. Ports

DEVS input and output ports are mapped to UML events one-to-one:

$$\forall \pi_i \in (\text{IP} \cup \text{OP}) \exists p_j \in P.$$  

Input and output events are not distinguished in UML state diagrams.

DEVS formalism does not specify whether the same port can be used as an input port and an output port (whether $\text{IP} \cap \text{OP} = \emptyset$). We will assume that the DEVS ports are indeed unidirectional. This means that an event of a certain type can be only consumed or produced by a state diagram, but not both.

4.3. External Transitions

The heterogeneous structure of DEVS states and UML states produces heterogeneous structures of DEVS and UML state transitions. Among other things, a single DEVS external transition function $\delta_{\text{ext}}(\sigma_i, e, x_j) = (\pi^\nu_H, \nu) \ has \ to \ generate \ both \ proper \ UML \ state \ transitions \ and \ their \ associated \ guard \ conditions \ and \ actions.$

The total state $S_T$ of a UML model is defined by the current UML finite state and the values of the pseudostate variables:

$$S_T \equiv (s_i, H), |H| = n - m + 1.$$  

The total state $\Sigma_i$ of a DEVS model is defined by the values of all DEVS state variables:

$$\Sigma_i \equiv (\gamma_1, \ldots, \gamma_n) = \gamma_i.$$  

To reflect a transition from a DEVS state $\sigma_i$ to another state $\sigma_j$, the corresponding UML model has to change from a UML state $s_i = f(\gamma_i)$ to another UML state $s_j = f(\gamma_j)$ and also update the values of the pseudostate variables: $H_i = f(\gamma_i)$. Here, $f(\gamma)$: DEVS objects $\to$ UML objects is the polymorphic mapping function from the universe of DEVS objects to the universe of UML objects which has been partially defined above.

Action $a_i^f$ associated with a possible UML transition $t_{l=ijk} = \{(s_l, s_j, p_k, g_l^i, a_l^i)\}$ from state $s_i$ to state $s_j$ on event $p_k = f(\pi^\nu_{k})$ would be responsible for updating the values of pseudostate variables $H$. It may depend on the original values of the pseudostate variables, on the value of the event, and on $e_i$:

$$
\text{def } a_i^f(H, \nu, e): \\
H_j = z^f(H, \nu, e)
$$

Here, $z^f(H, \nu, e)$ is the explicit state update function:

$$
\begin{align*}
  z_i^f(H, \nu, e) &= H' \iff \\
  e &\geq 0 \land \\
  \delta_{\text{ext}}((s_i, H), e, (\pi^\nu_H, \nu)) &= (s_j, H') .
\end{align*}
$$

This function may be undefined for some or all values of $H, \nu$, and $e = e_i$. A condition for a possible UML transition is set $C^f_i$ constructed in the following way:

$$C^f_i = \{(H, \nu, e)|(H, \nu, e) \in \text{dom}(z^f_i)\}.$$  

The UML transition exists if and only if the corresponding condition is not an empty set:

$$t_i \in T \iff C^f_i \neq \emptyset.$$  

Note that multiple transitions from $s_i$ to $s_j$ may exist for different events $x_k$. In general, $s_i$ can be the same state as $s_j$ (loopback transitions are possible).
The guard condition \( g_k \) is a functional representation of the condition set \( C_k^i \):

\[
g_k^i(H, \nu, e) = \begin{cases} 
    \text{true} & (H, \nu, e) \in C_k^i, \\
    \text{false} & \text{otherwise}, 
\end{cases}
\]  

(7)

where \( e \) for state \( s_i \) is defined by Eq. 4. The transition is “fired” if event \( p_k \) occurs and \( g_k^i(H, \nu, e) \) is true.

### 4.4. Internal Transitions and Output Events

Internal transitions and generation of output events are regulated by the internal transition function \( \delta_{int}(\sigma_i) \), the time advance function \( t_a(\sigma_i) \), and the output function \( \lambda(\sigma_i) \).

The three functions cooperate in the sense that the first function computes the target state of the transition, the second schedules the transition, and the third generates an output event associated with the transition. DEV5 models allow to output events only during internal transitions.

As the external UML transitions, internal UML transitions need to advance the UML model to another state and to update the pseudostate variables.

Action \( a_i^t \) associated with a possible UML transition \( t_{i=\{i\}} = \{s_i, s_j, e, g_i^t, a_i^t\} \) from state \( s_i \) to state \( s_j \) on null event \( e \) would be responsible for updating the values of pseudostate variables \( H \). It may depend on the original values of the pseudostate variables.

Unlike an action associated with an external transition, \( a_i^t \) can generate output events. UML2.0 allows UML components to “send” events to any UML component \( M \), including the component that sends the event (“self”), either immediately, or later. Keyword “after” that is used to schedule an event in the future. Caret (′) represents the send operation. For example, “\( \hat{e} \) after \( t \) means “send event \( e \) to component \( M \) after time \( t \).”

The function \( \lambda(\sigma_i) \) defines whether an output event is generated during the transition or not, and if yes, what is the type (port) of the event \( \pi_{i_{out}} \) and its value \( \nu_i \). The value of the event can be stored in the UML model as its attribute. By construction, the name of the output event and the name of the output port of an atomic DEV5 model coincide:

\[
\text{def } a_i^t(H_i): \quad (\pi_{i_{out}}(\nu_i)) = \lambda(\sigma_i) \quad (\pi_{i_{out}}(\nu_i)) = H_j = z_i^j(H_i)
\]

Here, \( z_i^j(H) \) is the explicit state update function for internal transitions:

\[
z_i^j(H) = H' \iff \delta_{int}((s_i, H)) = (s_j, H').
\]  

(8)

This function may be undefined for some or all values of \( H \). A condition for a possible internal UML transition is set \( C_i^j \) constructed in the following way:

\[
C_i^j = \{ H \mid H \in \text{dom}(z_i^j) \}.
\]  

(9)

The internal UML transition exists if and only if the corresponding condition is not an empty set:

\[
t_i \in T \iff C_i^j \neq \emptyset.
\]

In general, \( s_i \) can be the same state as \( s_j \) (internal loop-back transitions are possible).

The guard condition \( g_k \) is a functional representation of the condition set \( C_i^j \):

\[
g_k^j(H) = \begin{cases} 
    \text{true} & H \in C_i^j, \\
    \text{false} & \text{otherwise}, 
\end{cases}
\]  

(10)

The time spent in DEV5 state \( \sigma_i \), before the transition is scheduled, is given by the function \( t_a(\sigma_i) \).

It is tempting to use the send/after apparatus to schedule the transition in the future. However, a transition is not an event and cannot be scheduled using “after” and “send”. Instead, we declare new timeout event \( e_i \) and schedule it at time \( t_{curr} + t_a((s_i, H_i)) \) be redefining the entry action \( w_i \) of state \( s_i \).

Event \( e_i \) becomes the trigger for the internal transition from state \( s_i \).

A situation may occur when a timeout event has been scheduled, and an external transition is triggered by another (input) event. In this case, the pending timeout must be canceled. UML2.0 does not allow to recall scheduled events. Instead, a guard condition can be changed to make sure that obsolete timeouts do not trigger internal transitions.

Let every UML state \( s_i \) have local variable \( y_i \) initialized to the reference to the most recently scheduled timeout event \( e_i \) in the entry action:

\[
\text{def } w_i(): \\
\quad t_a = t_{curr} \\
\quad y_i = \text{ref}(e_i) \\
\quad \text{if } (y_i == \text{ref}(e_i)) \land g_k^j(H) \text{ is true.}
\]

5. COUPLED DEVS AND UML COMPONENT DIAGRAMS

DEV5 coupled models and UML component diagrams have a very similar structure, which makes mapping DEV5 models onto UML component diagrams rather straightforward.

5.1. Components

A DEV5 coupled model \( N \) has only one top-level component and only one level of nesting. This corresponds to a UML component diagram \( N^u \) with \( T_N = \{T_0\} \) and such that \( \forall M_i \in M^u \setminus T_N, \forall M_j \in M^a \colon (M_i, M_j) \not\in Q^a \).

The top-level component \( T_0 \), therefore, represents the DEV5 coupled model itself, and for each DEV5 component \( M_i \in M \) there exists an UML component \( M_i^u \in M^u, M_i^a = f(M_i) \).

5.2. Ports

Both input ports \( IP \) and output ports \( OP \) of \( N \) are mapped to the corresponding UML ports of the top-level component \( T_0 \) with externally visible ports \( P_0^a \). Let port \( p_i \in IP \) carry input events of type \( x_i \in X \). Then for this port

\[
\exists p_i^u = f(p_i) = (t, ifc, d) \in P_0^a: d = \text{input} \land t = x_i.
\]

Let port
\( p_j \in \text{OP} \) carry output events of type \( y_j \in Y \). Then for this port \( \exists p^*_j = f(p_j) = (t, f, c, d) \in P^*_d : d = \text{output} \land t = y_j \).

Notice that input and output events are mapped to the port names implicitly.

5.3. Connectors

External DEVS coupling corresponds to external (delegation) UML connectors. External input coupling of input port \( p_i \in \text{IP} \) to an input port \( p^*_i = f(p_i) \) of component \( M_d \in M \) is mapped to a delegation connector from the corresponding port of \( T^d_0 \) to the corresponding port of \( M^*_d \): \( \forall c_i = (((N, \text{IP}), (d, \text{IP}_d)), E_{\text{OC}-3c^*_i} = ((T_0, p_0), (M^*_d, p_0)) : M^*_d = f(M_d) \wedge p_0 = f(\text{IP}_d) \wedge p_{kl} = f(\text{IP}_d) \). Respectively, external output coupling of an output port \( p^*_j = f(p_j) \) of component \( M_d \in M \) to output port \( p_i \in \text{OP} \) is mapped to a delegation connector from the corresponding port of \( M^*_d \) to the corresponding port of \( T^i_0 \): \( \forall c_i = (((d, \text{OP}_d), (N, \text{OP})), E_{\text{OC}-3c^*_i} = ((M^*_d, p_k), (T_0, p_0)) : M^*_k = f(M_d) \wedge p_0 = f(\text{OP}_d) \wedge p_{kl} = f(\text{OP}_d) \).

Internal DEVS coupling corresponds to internal (assembly) UML connectors. Internal coupling of port \( p^*_i = f(p_i) \) of component \( M_d \in M \) to port \( p^*_i = f(p_k) \) of component \( M_d \in M \) is mapped to an assembly connector from the corresponding port of \( M^*_d \) to the corresponding port of \( M^*_k \).

5.4. Selection function

There is no feasible way of mapping the DEVS selection function to a UML model. Fortunately, parallel DEVS models do not use this function at all.

6. CONCLUSION AND FUTURE WORK

In the paper, we proposed a mapping of discrete event specification (DEVS) models onto Unified Modeling language (UML) state and component diagrams. This diagrams are designed and optimized for computerized processing and are highly expressive, competitive, and widely used both in academia and industry. Successful automated DEVS-to-UML mapping techniques would enable seamless integration of the legacy of DEVS models into existing and emerging UML models.

As the future step, we plan to consider UML2.0 composite structure diagrams as more suitable representations of DEVS coupled models. An automated translator from the DEVS domain into the UML domain would substantially simplify the transformation. Limiting the output to the Executable UML is also considered.

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7. BIOGRAPHY

Dr. D. Zinoviev received his Ph.D. in Computer Science from SUNY at Stony Brook in 1997. He was working as a post-doc on the DARPA/NASA/NSA-sponsored Petalflops project of a hybrid technology, multi-threaded hypercomputer. In 2000, he joined the Computer Science Department of Suffolk University in the rank of Assistant Professor. His current research interests include simulation and modeling (network simulation, architectural simulation), operating systems, and software engineering.

REFERENCES

[1] G. Booch, J. Rumbaugh, and I. Jacobson. The Unified Modeling Language. User Guide. Addison Wesley, 1999.
[2] H. Feng. DCharts, a formalism for modeling and simulation based design of reactive software systems. Master’s thesis, School of Computer Science, McGill University, Montréal, Canada, February 2004.
[3] GentleWare. Poseidon for UML community edition v. 2.5.1. Available at http://gentleware.com.
[4] J. Hogg. UML 2.0 automates code generation from architecture. COTS Journal, May 2004. Available online at http://www.cotsjournalonline.com.
[5] S.-Y. Hong and T. G. Kim. Embedding UML subset into object-oriented DEVS modeling process. In A. Bruzzone and E. Williams, editors, Proc. SCSC 2004, pages 161–166, San Jose, CA, July 2004.
[6] IBM. Rational rose. Available at http://ibm.com/software/rational/.
[7] S. J. Mellor and M. J. Baker. Executable UML: A Foundation for Model Driven Architecture. Addison-Wesley, 2002.
[8] J. Rumbaugh, I. Jacobson, and G. Booch. The Unified Modeling Language Reference Manual. Addison Wesley, second edition, 2004.
[9] H. Sarjoughian and R.K. Singh. Building simulation modeling environments using systems theory and software architecture principles. In Proc. Advanced Simulation Technology Symposium, Washington DC, April 2004.
[10] S. Schulz, T.C. Ewing, and J.W. Rozenblit. Discrete event system specification (DEVS) and StateMate StateCharts equivalence for embedded systems modeling. In Proc. 7th IEEE International Conference and Workshop on the Engineering of Computer Based Systems, pages 308–316, April 2000.
[11] B.P. Zeigler. Multifaceted Modelling and Discrete Event Simulation, chapter 4, 7. Academic Press, 1984.
[12] B.P. Zeigler, Object-oriented Simulation with Hierarchical, Modular Models, chapter 3. Academic Press, 1990.
[13] B.P. Zeigler, H. Praehofer, and T.G. Kim. Theory of Modeling and Simulation, chapter 4. Academic Press, 2000.