Si-based system-in-package design with broadband interconnection for E-band applications

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Abstract This letter presents a silicon-based package design for E-band communication systems. As the primary concern to package, the radio-frequency (RF) interconnection from carrier board to the die is carefully designed based on the impedance transformation characteristic of the transmission line (TL). In addition, the simulation results show that the designed interconnection is robust to moderate process deviations. To verify the electrical performance of the designed interconnection, a dummy testing structure is designed, fabricated and measured. The measurement results show that the return loss is less than 10.6 dB in the commercial communication frequency range of 71-86 GHz for E-band applications.

Keywords: system-in-package, silicon interposer, E-band, RF interconnection, impedance matching

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

E-band communication systems covering 71-76 GHz and 81-86 GHz frequency bands have drawn great attention in recent years [1, 2, 3, 4, 5, 6]. As the frequency is up to millimeter-wave (MMW) bands, the size of antenna is comparable with RF chips, which makes the integration of chips and antenna possible. To achieve both high-performance and low-profile, the 3-dimensional (3-D) system-in-package (SiP) has been an attractive and efficient approach to produce MMW wireless systems [7, 8, 9, 10]. As present, low temperature co-fired ceramic (LTCC) [11, 12, 13, 14, 15], high-density interconnect (HDI) [16, 17, 18, 19, 20], and embedded wafer level ball grid array (eWLB) [21, 22, 23, 24, 25] have all been demonstrated for mass production of MMW SiPs. However, the selection for MMW SiP is a trade-off among compactness, cost, electrical performance and thermo-mechanical reliability [26]. Taking the advantages of high precision and short interconnection, SiP technology based on silicon process is a promising candidate for the realization of a low-cost, fully integrated MMW transceiver system [27, 28, 29, 30, 31]. However, more effort is needed to achieve high density integration of T/R modules and antenna array with broadband interconnection for E-band applications.

In this letter, a silicon-based package design is proposed for E-band communication systems. In order to obtain excellent RF performance, the discontinuous structures in the interconnection are matched to 50 Ω. In addition, the electrical performance of designed interconnection with regard to process deviations is considered. Finally, a dummy testing structure is designed and measured to evaluate the RF performance. The measurement results show that the return loss is below −10.6 dB over the frequency range of 71-86 GHz.

2. Design of the SiP

The cross-section diagram of the designed E-band SiP is depicted in Fig. 1, which enables integration of 16 transceiver dies and 8×8 antenna array. The SiP consists of three-stacked silicon interposers (namely W1, W2 and W3, respectively) with 200 μm thickness of each layer. Due to the lossy silicon substrate characteristics, the high-resistivity silicon is chosen. The resistivity, relative permittivity and loss tangent of the selected silicon substrate are 2000 Ω-cm, 11.9 and 0.02, respectively, which are given by the wafer company. As shown in Fig. 1, the interposer W1 is the carrier for the transceiver dies. Considering that the back surfaces of dies are metallized for heat dissipation, dies and interposer W1 are interconnected by bonding wires. In order to feed the 8×8 antenna array uniformly, dies are arranged in the 4×4 array. The multiple cavities of W2 provide space for wire-bonding and enhance isolation among RF signal paths. The interposer W3 is the carrier of the antenna array as well as the cover of cavities. In the designed SiP, the through-silicon via (TSV) is employed to shorten the interconnection, thereby reducing the loss. For the future applications, the whole package can be fixed on the printed circuit board by ball grid array (BGA).

To design the MMW package, the transition loss and matching for the RF path are the top concerns [32, 33, 34]. Depending on probe-based measurement, it is impossible to characterize the transmission performance directly from solder balls to dies. For measurement and impedance-matching purpose, the SiP is landed on a ceramic test board with the relative permittivity of 9.7 and loss tangent of 0.008.

Fig. 2
shows the detailed cross-sectional diagram of the RF channel from the test board to die. It can be seen that there are two re-distribution layers (RDLs) (namely M1, M2) covered by polyimide (PI) on the top side of W1, and one RDL (M3) on the bottom side of W1. The impedance keeps changing and proper impedance matching has to be done. According to the main discontinuous structures, the RF path is divided into three modules, involving BGA, TSV and bonding-wire, respectively. The input and output impedance of each module should be matched to $50\,\Omega$, then they can be connected by $50\,\Omega$ transmission Lines (TLs).

3. Design of the interconnection

3.1 Impedance matching strategy

Based on the microwave transmission theory, a load impedance $Z_L$ can be converted to $Z_{in}$ after passing through a TL according to Eq. (1).

$$Z_{in} = \frac{Z_0}{Z_0 + jZ_L \tan \theta}$$

(1)

Where $Z_0$ and $\theta$ are the characteristic impedance and electric length of the TL respectively. Impedance matching can be done by optimizing dimensions of matching TLs in electromagnetic simulation software, Ansys HFSS. The grounded coplanar waveguide (GCPW) is adopted as the TL type in the SiP. Since the RF signals are quite sensitive to the surroundings, simulation models in HFSS are as consistent as possible with the actual RF environment.

3.2 Impedance matching for bonding-wires

The loss and impedance-mismatching induced by wires will increase drastically, as the frequency is up to E-band. Therefore, double-wires bonding technique and compensation with capacitance for wires are employed. The simulation model in HFSS is illustrated in Fig. 3(a). One end of the bonding wires is connected to the ground-signal-ground pads with a dimension of $70\times70\,\mu\text{m}^2$ and a gap of $30\,\mu\text{m}$ on the die, the other is connected to the finger on the package. The diameter of wires is $18\,\mu\text{m}$ with an arc height of $60\,\mu\text{m}$, and dimensions of the finger on the under bump metallization (UBM) layer is optimized to compensate the inductance of wires. In addition, two impedance-matching lines on the UBM and M1 layer respectively are designed and optimized to compensate for the discontinuity induced by PI opening. The simulated S-parameters of the matched bonding-wire module can be seen in Fig. 3(b). The return loss is below $-16\,\text{dB}$ and the insertion loss is better than $1.02\,\text{dB}$ in 71-86 GHz.

3.3 Impedance matching for TSVs

As the key technology of vertical signal interconnection, TSVs with a diameter of $30\,\mu\text{m}$ are used to connect the RDLs on both sides of the interposer. In order to ensure RF performance, the discontinuity between the TSV and horizontal TL should be considered. Fig. 4(a) shows the impedance matching model for TSVs in HFSS. One of the TSVs serves as RF TSV to provide vertical electrical interconnection, while others serve as grounded TSVs to provide a grounded shield surrounding the vertical interconnection. The overall geometry is similar to coaxial structure. Moreover, the impedance-matching lines, whose length is equal to the radius of coaxial structure, are applied to both ends of the RF TSV. The radius of coaxial structure and the dimensions of impedance-matching lines are optimized in HFSS. The matched results are depicted in Fig. 4(b). It can be found that the return loss is below $-32\,\text{dB}$, and the insertion loss is better than $0.45\,\text{dB}$ over the frequency of 70-90 GHz. In addition, the passband of the compensation structure is extremely flat, which shows great advantages for broadband interconnection in E-band.

3.4 Impedance matching for BGA

The interconnection between the test board and the inter-
Fig. 4 (a) Impedance-matching model for TSVs in HFSS, (b) simulation results of impedance-matching for TSVs.

poser W1 is realized by solder balls. Based on the process, the diameter, height and pitch of solder balls after reflow are 290 μm, 152 μm and 400 μm, respectively. According to the ball map, the four grounded balls, which are closest to the RF ball, are retained to ensure the RF transmission. Furthermore, impedance-matching lines on M3 and M4 are co-designed to compensate the discontinuity caused by solder balls. Fig. 5(a) shows the impedance matching model for BGA in HFSS. It can be seen that two impedance-matching lines on M4 are applied to expand bandwidth. Moreover, grounded vias are made to connect the ground planes of test board and play a shielding effect on RF transmission.

Fig. 5 (a) Impedance-matching model for BGA in HFSS, (b) simulation results of two impedance-matching models for BGA.

To analyze the impact of via grounding on the RF performance, two models are simulated and compared in HFSS. Grounded vias are implemented in one model as shown in Fig. 5(a) while they are removed in the other. Note that the remaining design parameters are kept identical. Fig. 5(b) shows the simulated S-parameters of the two models. Compared with the structure without grounded vias, the structure in Fig. 5(a) holds better S-parameters. The return loss of the structure with grounded vias is below −12.7 dB in 71–86 GHz, while the worst return loss of the structure without grounded vias can be seen at 85 GHz with a value of −10.7 dB. Moreover, the insertion loss of the structure with grounded vias is around 2 dB less than the structure without grounded vias. It is clear that grounded vias are helpful to pursue better RF performance.

3.5 Parametric analysis

The matched separate interconnection modules can be connected by 50 Ω TLs. Then the whole interconnection design is complete. The RF performance is related to process deviations, mainly involving the arc height of wires $H_w$, the thickness of adhesive $a_d$, and the height of solder balls $H_s$. Fig. 6 shows the simulated S-parameters of proposed interconnection from carrier board to die with regard to the

Fig. 6 S-parameters with regard to process deviations: (a) the adhesive thickness $a_d$, (b) the arc height of wires $H_w$, (c) the height of solder balls $H_s$. 

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process deviations. It should be noted that the original designed values of $H_w$, $a_d$ and $H_s$ are 60 $\mu$m, 30 $\mu$m and 152 $\mu$m, respectively.

It can be found in Fig. 6 that dimensional errors caused by process deviations have an impact on the S-parameters, especially near the center frequency. Within the simulated parameters variation, the lower the solder ball, the better the return loss and the insertion loss will be in the operating frequency range. On the other hand, the thinner the adhesive and the shorter the arc height of wires, the better the insertion loss while the worse the return loss will be. Therefore, there is a trade-off between return loss and insertion loss. In addition, the thickness of the adhesive and the arc height of wires are restricted by the height of cavities, and the height of solder balls is determined by the process. Although the S-parameters of the interconnection vary with the process deviations, the return loss is still less than 10 dB in 71-86 GHz.

4. Measurement and discussion

4.1 Design of dummy testing structure for measurement

In order to evaluate the electrical performance of the designed interconnection, one dummy testing structure is utilized. For measurement purpose, the 50 $\Omega$ GCPW on the dummy die connects two symmetrical RF channels. Furthermore, extra 50 $\Omega$ TL_A and TL_B on the test board are applied to lead the interconnection to the probe pads, which are not covered by SiP therefore the probes for measurement can be attached on the test board. As illustrated in Fig. 7(b), the dummy testing structure is composed of 50 $\Omega$ GCPW on dummy die and two RF channels. Fig. 7(c) shows the completed SiP with test board. Considering that the stacking thickness and materials of the dummy die are the same as the test board while the thickness of real die is 125 $\mu$m as shown in Fig. 2, the thickness of the adhesive and the arc height of wires are adjusted to 40 $\mu$m and 14 $\mu$m but the other designed dimensions are unchanged.

4.2 Results and discussion

The sample was tested on the measurement platform, which includes the Keysight vector network analyzer (VNA) and Cascade Infinity GSG-150 high frequency probe, as shown in Fig. 8. After calibration of probes, the passive dummy testing structure was excited by the signal source in VNA. When the port1 was activated, the reflection energy at port1 and the transmission energy at port2 were measured by VNA, thus the ratio of reflection energy to incident energy was recorded as $S_{11}$ and the ratio of transmission energy to incident energy was recorded as $S_{21}$ in VNA. Nevertheless, the measured return loss is below $-10.6$ dB in 71-86 GHz, which indicates that the RF path is well matched to 50 $\Omega$ over a wide bandwidth. The $S_{11}$ and $S_{22}$ should be equal due to the symmetry of the testing structure. However, the input and output impedance of the matched interconnection are not exact 50 $\Omega$ and the 50 $\Omega$ TLs on test board are different in length, thus the dummy testing structure is asymmetric and the discrepancy is observed in the result of $S_{11}$ and $S_{22}$. Moreover, the discrepancy in the measurement result is more obvious due to additional process deviations.

The worst measured insertion loss is $-12.27$ dB at 74.64 GHz over the E-band frequency of 71-86 GHz, which is induced by two RF channels and a 2.58 mm length GCPW on dummy die. In order to reduce the effect of test board, two additional 50 $\Omega$ GCPWs, which have the same lengths as TL_A and TL_B in Fig. 7(b), were designed and measured, then they can be de-embedded from the dummy test-

Fig. 8 The measurement platform.
E-band applications. A feasible SiP solution with broadband interconnection for loss is below 0.48 dB/mm and the return loss of the RF path is better than 0.48 dB/mm and the return loss is below 4.7 dB over 71-86 GHz, and shows good agreement with the simulation result. Hence, it can be found that approximately half of the loss is induced by the 50 Ω GCPW on the test board. The total length of the dummy testing structure is around 26.2 mm, thus the average loss is better than 0.48 dB/mm over the E-band. The measured results show that the designed SiP allows broadband interconnection for E-band applications.

5. Conclusion

In this Letter, a silicon-based SiP for E-band communication systems is proposed. To ensure the RF performance, the interconnection from test board to die is designed. The measurement results show that the average insertion loss of the RF path is better than 0.48 dB/mm and the return loss is below -10.6 dB over the commercial communication E-band frequency of 71-86 GHz. The designed interconnection features the merit of broadband and shows tolerance to process deviations. This successful demonstration provides a feasible SiP solution with broadband interconnection for E-band applications.

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