PL-NMF: Parallel Locality-Optimized Non-negative Matrix Factorization

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ABSTRACT

Non-negative Matrix Factorization (NMF) is a key kernel for unsupervised dimension reduction used in a wide range of applications, including topic modeling, recommender systems and bioinformatics. Due to the compute-intensive nature of applications that must perform repeated NMF, several parallel implementations have been developed in the past. However, existing parallel NMF algorithms have not addressed data locality optimizations, which are critical for high performance since data movement costs greatly exceed the cost of arithmetic/logic operations on current computer systems. In this paper, we devise a parallel NMF algorithm based on the HALS (Hierarchical Alternating Least Squares) scheme that incorporates algorithmic transformations to enhance data locality. Efficient realizations of the algorithm on multi-core CPUs and GPUs are developed, demonstrating significant performance improvement over existing state-of-the-art parallel NMF algorithms.

CCS CONCEPTS

• Computing methodologies → Shared memory algorithms; Non-negative matrix factorization.

KEYWORDS

Parallel Machine Learning, Parallel Non-negative Matrix Factorization, Dimension Reduction

1 INTRODUCTION

Non-negative Matrix Factorization (NMF) is a key primitive used in a wide range of applications, including topic modeling [14, 22, 24], recommender systems [1, 9, 27] and bioinformatics [20, 25, 26]. Given a non-negative matrix \( A \in \mathbb{R}^{V \times D} \) and \( K \ll \min(V, D) \), NMF finds two non-negative rank-K matrices \( W \in \mathbb{R}^{V \times K} \) and \( H \in \mathbb{R}^{K \times D} \), such that the product of \( W \) and \( H \) approximates \( A \) [15]:

\[
A \approx WH
\]

NMF is a powerful technique for topic modeling. When \( A \) is a corpus in which each document is represented as a collection of bag-of-words from an active vocabulary, the factor matrices \( W \) and \( H \) can be interpreted as latent topic distributions for words and documents.

Several algorithms have been proposed for NMF. They all involve repeated alternating update of some elements of \( W \) interleaved with update of some elements of \( H \), with imposition on non-negativity constraints on the elements, until a suitable error norm (either Frobenius norm or Kullback-Leibler divergence) is lower than a desired threshold. Various previously developed algorithms for NMF differ in the granularity of the number of elements of \( W \) that are updated before switching to updating some elements of \( H \). The focus of prior work has been to compare the rates of convergence of alternate algorithms and the parallelization of the algorithms. However, to the best of our knowledge, the minimization of data movement through the memory hierarchy, using techniques like tiling, has not been previously addressed. With costs of data movement from memory being significantly higher than the cost of performing arithmetic operations on current processors, data locality optimization is extremely important.

In this paper, we address the issue of data locality optimization for NMF. An analysis of the computational components of the FAST-HALS (Hierarchical Alternating Least Squares) algorithm for NMF [3], is first performed to identify data movement overheads. The associativity of addition is utilized to judiciously reorder additive contributions in updating elements of \( W \) and \( H \), to enable 3D tiling of a computationally intensive component of the algorithm. An analysis of the data movement overheads as a function of tile size is developed, leading to a model for selection of effective tile sizes. Parallel implementations of the new Parallel Locality-optimized NMF algorithm (called PL-NMF) are presented for both GPUs and multi-core CPUs. An experimental evaluation with datasets used in prior studies demonstrates significant performance improvement over state-of-the-art alternatives available for parallel NMF.

The paper is organized as follows. In the next section, we present the background on NMF and related prior work. In Section 3, we present the high-level overview of PL-NMF algorithm. Sections 4 and 5 demonstrate details of our PL-NMF for multi-core CPUs and GPUs. In Section 6, we systematically analyze the data movement cost for PL-NMF and original FAST-HALS algorithms. Section 7 presents determination of the tile sizes based on data movement analysis. In Section 8, we compare PL-NMF with existing state-of-the-art parallel implementations.
2 BACKGROUND AND RELATED WORK

2.1 Non-negative Matrix Factorization Algorithms

NMF seeks to solve the optimization problem of minimizing reconstruction error between A and the approximation WH. In order to measure the reconstruction error for NMF, Lee et al. [15] adopted various objective functions, such as the Frobenius norm given two matrices and Kullback-Leibler divergence given two probability distributions. The objective function \( D(A\|WH) \) based on the Frobenius norm is defined in Equation 2.

\[
D_P(A\|WH) = \frac{1}{2} ||A - WH||^2_F = \frac{1}{2} \sum_{vd} (A_{vd} - (WH)_{vd})^2
\]

To efficiently minimize the objective functions (above), several variants of NMF algorithms have been developed: Multiplicative Update (MU), Additive Update (AU), Alternating Non-negative Least Squares (ANLS) and Hierarchical Alternating Least Squares (HALS). Table 1 describes the notations used in this paper.

Table 1: Common notations for NMF algorithms
| Notation | Description |
|----------|-------------|
| A        | Non-negative matrix |
| W        | Non-negative rank-K matrix factor |
| H        | Non-negative rank-K matrix factor |
| V        | Number of rows in A and W |
| D        | Number of columns in A and H |
| K        | Low rank |

Multiplicative update (MU) and additive update (AU) proposed by Lee et al. [15] are the simplest NMF algorithms. The MU algorithm updates two rank-K non-negative matrices W and H based on multiplicative rules and ensures convergence. MU strictly conforms to non-negativity constraints on W and H because the elements of W and H that have zero value will not be updated. Unlike MU algorithm, the AU algorithm updates W and H based on the gradient descent method and avoids negative update values using learning rate. However, some studies have reported that the use of MU and AU algorithms leads to weaknesses such as slower convergence and lower convergence rate [8, 11, 17].

Alternating Non-negative Least Squares (ANLS) is a special type of Alternating Least Squares (ALS) approach. At each iteration, the gradients of two objective functions with respect to W and H are used to update each of W and H one after the other. Kim et al. [12] proposed Alternating Non-negative Least Squares based Block Principle Pivoting (ANLS-BPP) algorithm. Under the Karush-Kuhn-Tucker (KTT) conditions, the ANLS-BPP algorithm iteratively finds the indices of non-zero elements (passive set) and zero elements (active set) in the optimal matrices until KTT conditions are satisfied. The values of indices that correspond to the active set will become zero, and the values of passive set are approximated by solving \( \min ||A - WH||^2_F \) which is a standard Least Squares problem.

As an alternative to the basic ANLS approach, Cichocki et al. [4] proposed Hierarchical Alternating Least Squares (HALS), which hierarchically updates only one k-th row vector of \( H \in \mathbb{R}^{K \times D} \) at a time and then uses it to update a corresponding k-th column vector of \( W \in \mathbb{R}^{V \times K} \). In other words, HALS minimizes the K set of two local objective functions with respect to K row vectors of H and K column vectors of W at each iteration. A standard HALS algorithm iteratively updates each row of H and each column of W in order within the innermost loop.

Based on the standard HALS algorithm, Cichocki et al. [3] further proposed the extended version of a new algorithm called FAST-HALS algorithm as described in Algorithm 1. Note that \( H_k \) and \( W_k \) indicate k-th row of H and k-th column of W, respectively. FAST-HALS updates all rows of H before starting the update to all columns of W, instead of alternately updating each row of H and each column of W at a time. Compared to MU algorithm, the FAST-HALS algorithm converges much faster and produces a better solution, while maintaining a similar computational cost as reported in [7, 12]. Interestingly, Kim et al. [12] have shown that FAST-HALS has also been found to converge faster than their ANLS-BPP implementation on real-world text datasets: TDT2 and 20 Newsgroups, while maintaining the same convergence rate (see Figure 5.3 in Kim et al. [12]).

2.2 Related Work on Parallel NMF

Since most of the variations of NMF algorithm are highly compute-intensive, many previous efforts have been made to parallelize NMF algorithms. As shown in Table 2, previous studies on parallelizing NMF can be broadly categorized into two groups based on implementation for multi-core CPUs [2, 5, 6, 10, 16, 18] versus GPUs [15, 19, 20]. Furthermore, each study used various NMF algorithms for parallel implementations.

Table 2: Previous studies on parallelization of NMF

| Author                  | Machine | Platform       | Algorithm       |
|-------------------------|---------|----------------|-----------------|
| Rattenberg et al. [2]   | CPU     | Shared-memory  | MU              |
| Fairbanks et al. [6]    | CPU     | Shared-memory  | ANLS-BPP        |
| Dong et al. [5]         | CPU     | Distributed-memory | MU            |
| Liu et al. [16]         | CPU     | Distributed-memory | MU            |
| Kannan et al. [10]      | CPU     | Distributed-memory | ANLS-BPP      |
| Lopes et al. [19]       | GPU     | Shared-memory  | MU, ALS         |
| Koika et al. [13]       | GPU     | Shared-memory  | ALS             |
| Mejia-Ria et al. [20]   | GPU     | Distributed-memory | MU, ALS       |

2.2.1 Shared-Memory Multiprocessor.

Battenberg et al. [2] introduced parallel NMF using MU algorithm for audio source separation task. Fairbanks et al. [6] adopted ANLS-BPP based NMF in order to find the structure of temporal behavior in a dynamic graph given vertex features. Both [2] and [6] developed the parallel NMF implementations on multi-core CPUs using Intel Math Kernel Library (MKL) along with shared-memory multiprocessor.

2.2.2 Distributed-Memory Systems.

Dong et al. [5] demonstrated that MU algorithm and shared-memory based parallel implementation have a limitation of slow convergence. To overcome these problems, they devised a parallel MPI implementation of MU based NMF that improves Parallel NMF (PNMF) proposed by Robila et al. [21]. Different NMF algorithms have previously used tiling/blocking to minimize data movement. Dong et al. [5] partitioned the two factor matrices, W and H, into
smaller blocks and each block is distributed to different threads. Each block simultaneously updates corresponding sub-matrices of the two matrices, and a reduction operation is performed by collective communication operations using Message Passing Interface (MPI). Similarly, Liu et al. [18] proposed matrix partition scheme that partitions the two factor matrices along the shorter dimension (K dimension) instead of the longer dimensions (V or D dimensions). Therefore, each matrix is divided up to more partitions compared to partitioning along the longer dimension, so that the data locality is increased and the communication cost is decreased when performing the product of two matrices. Kannan et al. [10] minimized the communication cost by communicating only with the two factor matrices and other partitioned matrices among parallel threads. Based on the ANLS-BPP algorithm, their implementation also reduced the bandwidth and data latency using MPI collective communication operations. Given an input matrix A and two factorized matrices W and H, they partitioned W and H into P multiple blocks (tiles) across V and D dimensions which are the number of rows in W and columns in H. Hence, the sizes of each block in W and H are (V/P)×K and (K×(D/P)), respectively. Doing so allows the matrix A to be partitioned into P tiles × P tiles. Then P different processors perform matrix multiplication with the different P tiles of W and H simultaneously. This data partition scheme is appropriate for block-wise updates of W and H based on ANLS-BPP algorithm. Unlike ANLS-BPP algorithm, FAST-HALS algorithm requires column-wise/row-wise sequential updates because there is a dependency between two consecutive columns/rows. Hence, FAST-HALS algorithm is not allowed to divide W and H across V and D dimensions. In our tiling approach, W and H are partitioned across K dimension, and the sizes of each block in W and H are V×(K/P) and (K/P)×D, respectively. Our key contribution is not tiling/blocking itself, but converting matrix-vector operations to matrix-matrix operations. Tiling enables us to do the latter.

### 2.2.3 GPU Platform.

Lopes et al. [19] proposes several GPU-based parallel NMF implementations that use both MU and AU algorithms for both Euclidean and KL divergence objective functions. Mejía-Roa et al. [20] presents NMF-mGPU that performs MU based NMF algorithm on either a single GPU device or multiple GPU devices through MPI for a large-scale biological dataset. Kotika et al. [13] presents MU and ALS based GPU implementations binding to the R environment. To our knowledge, our paper is the first to develop FAST-HALS based parallel NMF implementation for GPUs.

### 3 OVERVIEW OF APPROACH

In this section, we present a high-level overview of our approach to optimize NMF for data locality. We begin by describing the FAST-HALS algorithm [3], one of the fastest algorithms for NMF as demonstrated by previous comparison studies [12]. We analyze the data movement overheads from main memory, for different components of that algorithm, and identify the main bottlenecks. We then show how the algorithm can be adapted by exploiting the associativity of addition to make the computation effectively tileable to reduce data movement from memory, whereas the original form is not tileable.

### 3.1 Overview of FAST-HALS Algorithm

**Algorithm 1** FAST-HALS algorithm

| Line | Description |
|------|-------------|
| 1    | Initialize \( W \in \mathbb{R}^{V \times K} \) and \( H \in \mathbb{R}^{K \times D} \) with random non-negative numbers |
| 2    | repeat |
| 3    | // Updating \( H \) |
| 4    | \( R \leftarrow A^T W \) |
| 5    | \( S \leftarrow W^T W \) |
| 6    | for \( k = 0 \) to \( K - 1 \) do |
| 7    | \( H_k \leftarrow \max(\epsilon, H_k + R_k - H_k^T S_k) \) |
| 8    | end for |
| 9    | // Updating \( W \) |
| 10   | \( P \leftarrow A H^T \) |
| 11   | \( Q \leftarrow H H^T \) |
| 12   | for \( k = 0 \) to \( K - 1 \) do |
| 13   | \( W_k \leftarrow \max(\epsilon, W_k Q k + P_k - W Q k) \) |
| 14   | // Normalize \( W_k \) column vector with \( L_2 = \|W_k\|_2 \) |
| 15   | \( W_k \leftarrow \frac{W_k}{\|W_k\|_2} \) |
| 16   | end for |
| 17   | until convergence |

Algorithm 1 shows pseudo-code for the FAST-HALS algorithm [3] for NMF. It is an iterative algorithm that iteratively updates \( H \) and \( W \), fully updating all entries in \( H \) (lines 4-8) and then updating all entries in \( W \) (lines 10-15) during each iteration until convergence. While the updates to \( H \) and \( W \) are slightly different (due to normalization of \( W \) after each iteration), each of the updates involves a pair of matrix-matrix products (lines 4/5 and 10/11 for \( H \) and \( W \), respectively) and a sequential loop that steps through features (\( k \) loop) to update one row (column) of \( H(W) \) at a time. The computation within these \( k \) loops involves vector-vector operations and matrix-vector operations. From a computational complexity standpoint, the various matrix-matrix products and the sequential (\( K \) times) matrix-vector products all have cubic complexity (\( O(N^3) \) if all matrices are square and of side \( N \)). But as we show by analysis of data movement requirements in the next sub-section, the collection of matrix-vector products in lines 7 and 13 dominate. In the following sub-section, we present our approach to alleviating this bottleneck by exploiting the flexibility of instruction reordering via use of the associativity property of addition.

### 3.2 Data Movement Analysis for FAST-HALS Algorithm

The code regions with high data movement can be identified by individually analyzing each line in Algorithm 1. Lines 4 and 5 perform matrix multiplication. It is well known that \( \frac{\text{nw}}{\text{C}} \) is the highest order term in the number of data elements moved (between main memory and a cache of size \( C \) words) for efficient tiled matrix

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1 Floating-point addition is of course not strictly associative, but as shown later by the experimental results, the changed order does not adversely affect algorithm convergence.
multiplication of two matrices $A, (M \times K)$ and $B, (K \times N)^2$. Thus, the data movement costs associated with lines 4 and 5 are $\frac{2DKV}{\sqrt{C}}$ and $\frac{2KKV}{\sqrt{C}}$, respectively. The loop in line 6 performs matrix-vector multiplication and has an associated data movement cost of $K(3D + DK + K)$. Similar to lines 4 and 5, the data movement costs for lines 10 and 11 are $\frac{2V KD}{\sqrt{C}}$ and $\frac{2KKD}{\sqrt{C}}$, respectively. The loop in line 12 has an associated data movement cost of $K(VK + K + 6V + 1)$. The total data movement for Algorithm 1 is shown in Equation 3.

$$K(K(V + D)(1 + \frac{2}{\sqrt{C}}) + \frac{4VD}{\sqrt{C}} + 6V + 3D + 2K + 1) \quad (3)$$

The main data movement overhead is associated with loops in lines 6 and 12. For example, the combined fractional data movement overhead of lines 7 (within loop in line 6) and 13 (within loop in line 12) is 91% for the 20 Newsgroups dataset. If the operational intensity (defined as the number of operations per data element moved) is very low, the performance will be bounded by memory bandwidth and thus will not be able to achieve the peak compute capacity. Due to its low operational intensity, the performance of Algorithm 1 is limited by the memory bandwidth. Thus, the major motivation for our algorithm adaptation is to achieve better performance by reducing the required data movement.

### 3.3 Overview of PL-NMF

In this sub-section, we describe how the FAST-HALS algorithm is adapted by exploiting the flexibility of changing the order in which additive contributions to a data element are made. Before describing the adaptation, we first highlight the interaction between different columns of $W$ in the original algorithm. Figure 1 depicts the update of $W$ which corresponds to the lines 12 to 16 in Algorithm 1.

In Algorithm 1, the $t^{th}$ column of $W$ is updated as the product of $W$ with the $t^{th}$ column of $Q$ which is a matrix-vector multiplication operation. Since the update to $(t + 1)^{th}$ column depends on $t^{th}$ column, different columns ($t$: features) are updated sequentially. Let $W_{old}$ represent the values at the beginning of the current outer iteration, and let $W_{new}$ represent the values at the end of current outer iteration (updated values). Interaction between $W_{old}$ and $W_{new}$ is shown in Figure 2 which depicts the contributions from $W_{old}$ and $W_{new}$ to $W_{new,t}$. $W_{old}$ contributes to $W_{new,i}$ where $\forall ij \leq t$, and $W_{new,t}$ contributes to $W_{new,i}$ where $\forall ij > t$. In other words, the old value of column $t$ is used to update the columns to the left of $t$ (and self), and the new/updated value of column $t$ is used to update the columns to the right of column $t$.

$$W_{new,t} = W_{old}Q_{t} + W_{new,t}Q_{t}$$

Figure 3 shows the contributions of $W_{old,i}$ to $W_{new,i}$, $W_{old,i}$ contributes to $W_{new,i}$ where $\forall ij \leq t$, and $W_{new,i}$ contributes to $W_{new,i}$ where $\forall ij > t$. In other words, the old value of column $t$ is used to update the columns to the left of $t$ (and self), and the new/updated value of column $t$ is used to update the columns to the right of column $t$.

If we partition $W$ into a set of column panels (tiles) of size $T$, the interactions between columns can be expressed in terms of tiles as depicted in Figure 4. Similar to individual columns, the old value of tile $\tau$ is used to update the columns to the left of $\tau$ (phase 1), and the new/updated value of tile $\tau$ is used to update the tiles to the right of tile $\tau$ (phase 3). The updates to different columns with a tile (phase 2) is done sequentially.

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2 An extensive discussion of both lower bounds and data movement volume for several tiling schemes may be found in the recent work of Smith [23].
Algorithm 2 Parallel CPU implementation for updating $W$

Input: $A \in \mathbb{R}^{V \times D}$: input matrix, $W_{\text{old}}$ and $W_{\text{new}}$: $V \times K$ non-negative matrix factor, $H$: $D \times K$ non-negative matrix factor, $T$: Tile size, $\epsilon$: small non-negative quantity, $\gamma$: total number of tiles

1: $P \leftarrow AH^T$
2: $Q \leftarrow HH^T$
3: // Initialize $W_{\text{new}}$ using $W_{\text{old}}$ and $Q$
4: for $v = 0$ to $V - 1$ do
5:   for $k = 0$ to $K - 1$ do
6:     $W_{\text{new}}[v][k] \leftarrow W_{\text{old}}[v][k] \times Q[k][k]$
7:   end for
8: end for
9: // Phase 1
10: $\gamma \leftarrow K / T$
11: for tile_id = 0 to $\gamma - 1$ do
12:   $W_{\text{new}}[0:V-1][0:(tile \text{ id} \times T) - 1] \leftarrow$
13:     $\text{dgemm}(W_{\text{old}}[0:V-1][tile \text{ id} \times T:((tile \text{ id} \times T) + 1) \times T - 1],$
14:     $Q[tile \text{ id} \times T:((tile \text{ id} \times T) + 1) \times T - 1][0:(tile \text{ id} \times T) - 1])$
15: end for
16: // Phase 2 & Phase 3
17: for tile_id = 0 to $\gamma - 1$ do
18:   sum_square $\leftarrow 0$
19:   #pragma omp parallel for reduction(+:sum_square)
20: for $v = 0$ to $V - 1$ do
21:   sum $\leftarrow 0$
22:   $k \leftarrow tile \text{ id} \times T$
23:   #pragma omp simd reduction(+:sum)
24: for $t = 1$ do
25:   sum $\leftarrow sum + W_{\text{new}}[v][k] \times Q[t][k]$
26: end for
27: #pragma omp simd reduction(+:sum)
28: for $k = t$ to $(tile \text{ id} + 1) \times T - 1$ do
29:   sum $\leftarrow sum + W_{\text{old}}[v][k] \times Q[t][k]$
30: end for
31: $W_{\text{new}}[v][t] \leftarrow \max(\epsilon, W_{\text{new}}[v][t] + P[v][t] - \text{sum})$
32: sum_square $\leftarrow$ sum_square $+ W_{\text{new}}[v][t] \times W_{\text{new}}[v][t]$
33: end for
34: #pragma omp parallel for
35: for $v = 0$ to $V - 1$ do
36:   $W_{\text{new}}[v][t] \leftarrow W_{\text{new}}[v][t] / \sqrt{\text{sum} \text{ square}}$
37: end for
38: end for
39: // Phase 3
40: $W_{\text{new}}[0:V-1][((tile \text{ id} + 1) \times T:K-1) - 1] \leftarrow$
41: $\text{dgemm}(W_{\text{new}}[0:V-1][tile \text{ id} \times T:((tile \text{ id} + 1) \times T) - 1],$
42: $Q[tile \text{ id} \times T:((tile \text{ id} + 1) \times T) - 1][((tile \text{ id} + 1) \times T:K-1)]$
43: end for

The contributions to tiles to the left of current tile $t$ can be done as $W_{\text{new}}_{i,j} = W_{\text{old}}_{i,k} \times T_{(r \times T) + 1} \times Q_{x \times T}(\tau + 1 \times T)_{-1}$, where $\forall j < \tau \times T - 1$. Similarly, contributions to tiles to the right of current tile $t$ can be done as $W_{\text{new}}_{i,j} = W_{\text{new}}_{i,k} \times T_{(r + 1 \times T) - 1} \times Q_{x \times T}(\tau + 1 \times T)_{-1}$, where $\forall j > (\tau + 1) \times T$.

Figure 5: Computations of three phases for updating $W$.

4 DETAILS OF PL-NMF ON MULTICORE CPUs AND GPUs

4.1 Parallel CPU Implementation

Algorithm 2 shows our CPU pseudo-code for updating $W$. We begin by computing $AH^T$ (line 1). If $A$ is sparse, then the actual implementation uses mkl_dcsrmm() and cblas_dgemm(). Line 2 computes the $HH^T$ (using cblas_dgemm()). The $W$ values from the previous iteration are kept in $W_{\text{old}}$. We maintain another data structure called $W_{\text{new}}$ which represents the updated $W$ values. $W_{\text{new}}$ is initialized by the loop in line 4. By using Equation 4, phase 1 is done by the loop in line 11. Figure 5 illustrates the actual computations of tiled matrix-matrix multiplications for three sequential phases, where $\tau$ denotes the index of the current tile and $T$ is the size of each tile. For example, at current tile $t$, phase 1 performs multiplication of the same colored/patterned two sub-matrices (tiles) in $W_{\text{old}}$ and $Q$ to update the result matrix $W_{\text{new}}$.

$$W_{\text{new}}[i,: \cdot (r \times T) - 1] = W_{\text{old}}[i,: \cdot (r \times T) \cdot ((r + 1) \times T) - 1] \cdot Q[(r \times T) : ((r + 1) \times T) - 1, 0 : (r \times T) - 1]$$ (4)

The loop in line 17 performs phase 2 computations as formulated in Equation 5. In order to take advantage of the vector unit, the loops in lines 24 and 28 are vectorized. Additionally, a column-wise normalization for $W_{\text{new}}$ is performed within phase 2 (line 36).

$$W_{\text{new}}[i,: \cdot (r \times T) \cdot ((r + 1) \times T) - 1] = W_{\text{new}}[i,: \cdot (r \times T) : ((r + 1) \times T) - 1] \cdot Q[(r \times T) : ((r + 1) \times T) - 1, 0 : (r \times T) - 1] + P[i,: \cdot (r \times T) : ((r + 1) \times T) - 1]$$ (5)

The matrix-matrix multiplication in line 40 corresponds to the phase 3 computations using Equation 6. As depicted in Figure 5, the tiles involving phase 3 and phase 1 computations are different from each
other.

\[ W_{\text{new}}[:, ((r + 1) \times T): K - 1] = \]
\[ W_{\text{old}}[:, (r \times T): ((r + 1) \times T) - 1], \]
\[ Q((r \times T): ((r + 1) \times T) - 1, ((r + 1) \times T): K - 1) \]

Finally, our parallel CPU implementation completely substitutes lines 10 to 16 in Algorithm 1 for all lines in Algorithm 2. Similarly, \( H \) will be updated in the same fashion as updating \( W \) except for the normalization part.

### 4.2 Parallel GPU Implementation

**Algorithm 3** GPU implementation of updating \( W \) on host

**Input:** \( A \in \mathbb{R}^{L \times D} \): input matrix, \( W_{\text{old}} \) and \( W_{\text{new}}: V \times K \) non-negative matrix factor, \( H: D \times K \) non-negative matrix factor, \( T: \) Tile size, \( \epsilon: \) small non-negative quantity, \( \gamma: \) total number of tiles

1. \( P \leftarrow AH^T \)
2. \( Q \leftarrow HH^T \)
3. // **Phase 1**
4. \( vId \leftarrow K / T \)
5. for tile_id = 0 to \( V - 1 \) do
6. \( W_{\text{new}}[0:V-1][0:(tile_id \times T)-1] = \)
7. \( \text{cublasDgemm}(W_{\text{old}}[0:V-1][tile_id\times T:((tile_id + 1)\times T)-1], Q[tile_id\times T:((tile_id + 1)\times T)-1][0:(tile_id \times T)-1]) \)
8. end for
9. // **Phase 2 & Phase 3**
10. for tile_id = 0 to \( V - 1 \) do
11. // **Phase 2**
12. for \( t = tile_id \times T \) to \( (tile_id + 1) \times T - 1 \) do
13. \( \text{cudaMemset}(\text{sum\_square}, 0) \)
14. \( \text{update}_\text{W} \_\text{norm}(2) \)
15. \( \text{__cudaDeviceSynchronize}() \)
16. \( \text{update}_\text{W} \_\text{norm}() \)
17. \( \text{__cudaDeviceSynchronize}() \)
18. \( \text{end for} \)
19. // **Phase 3**
20. \( W_{\text{new}}[0:V-1][((tile_id + 1)\times T):K-1] = \)
21. \( \text{cublasDgemm}(W_{\text{new}}[0:V-1][tile_id\times T:((tile_id + 1)\times T)-1], Q[tile_id\times T:((tile_id + 1)\times T)-1][(tile_id + 1)\times T:K-1]) \)
22. \( \text{end for} \)

Similar to our CPU algorithm, our GPU algorithm also tries to minimize the data movement. Algorithm 3, 4 and 5 show the pseudo-code of our GPU algorithm. Since the overall structure of the GPU algorithm is similar to the CPU algorithm, this section only highlights the differences. Algorithm 3 runs on the host which is responsible for launching GPU kernels. The sparse matrix-dense matrix multiplication is implemented using \texttt{cusparseDcsrmv()}, and dense matrix-dense matrix multiplication is implemented using \texttt{cublasDgemm()}.

Algorithm 4 shows the pseudo-code for phase 2. In GPUs, the reduction across \( V \) (for normalization of \( W \)) can be performed using global memory atomic operations which are very expensive. Hence, our implementation uses efficient hierarchical reduction. The reduction within a thread block is done in 4 steps: i) in line 18, the reduction across the threads within a warp is done using efficient warp shuffling primitives, ii) all the threads with lane id 0 write the reduced value to shared memory (line 20), iii) in line 24, the first warp of the thread block loads the previously written values from shared memory and iv) all the threads in the first warp again performs warp reduction (line 26). In order to perform reduction across multiple thread blocks, we use atomic operations which is shown in line 29. Algorithm 5 shows the pseudo-code for normalization.

**Algorithm 4** GPU implementation of \( \text{update}_\text{W} \_\text{phase}\_2 \) kernel

**Input:** \( W_{\text{old}}, W_{\text{new}}, P, Q, \text{sum\_square}, t, T, V, K, \epsilon \)

1. \( vId \leftarrow \text{blockIdx.x} \times \text{ blockDim.x} + \text{ threadIdx.x} \) // threadID
2. \( \text{__shared__ shared\_sum}[1024/32] \)
3. \( \text{sum\_reduce} = 0.0\epsilon \)
4. if \( vId < V \) then
5. \( \text{sum} = 0 \)
6. for \( k = tile_id \times T \) to \( (tile_id + 1) \times T - 1 \) do
7. if \( k < t \) then
8. \( \text{sum} \leftarrow \text{sum} + W_{\text{new}}[vId + k \times V][k] \times Q[k \times K + t] \)
9. else
10. \( \text{sum} \leftarrow \text{sum} + W_{\text{old}}[vId + k \times V] \times Q[k \times K + t] \)
11. \( \text{end if} \)
12. \( \text{end for} \)
13. \( W_{\text{new}}[vId + t \times V] \leftarrow \max(\epsilon, W_{\text{new}}[vId + t \times V] + P[vId + t \times V] - \text{sum}) \)
14. \( \text{sum\_reduce} \leftarrow W_{\text{new}}[vId + t \times V] \)
15. \( \text{end if} \)
16. \( \text{sum\_reduce} \leftarrow \text{sum\_reduce} \times \text{sum\_reduce} \)
17. // **Warp-level reduction**
18. \( \text{sum\_reduce} \leftarrow \text{warp\_reduce}(\text{sum\_reduce}) \)
19. // **Block-level reduction**
20. if threadIdx.x \% 32 == 0 then
21. \( \text{shared\_sum}[\text{ threadIdx.x} / 32] \leftarrow \text{sum\_reduce} \)
22. \( \text{end if} \)
23. \( \text{__syncthreads}() \)
24. if threadIdx.x / 32 == 0 then
25. \( \text{sum\_reduce} \leftarrow \text{shared\_sum}[\text{ threadIdx.x}] \)
26. \( \text{sum\_reduce} \leftarrow \text{warp\_reduce}(\text{sum\_reduce}) \)
27. \( \text{end if} \)
28. if threadIdx.x == 0 then
29. \( \text{atomicAdd}(\text{sum\_square}, \text{sum\_reduce}) \)
30. \( \text{end if} \)

**Algorithm 5** GPU implementation of \( \text{update}_\text{W} \_\text{norm} \) kernel

**Input:** \( W_{\text{new}}, \text{sum\_square}, t, V \)

1. \( vId \leftarrow \text{blockIdx.x} \times \text{ blockDim.x} + \text{ threadIdx.x} \) // threadID
2. if \( vId < V \) then
3. return
4. \( \text{end if} \)
5. \( W_{\text{new}}[vId + t \times V] \leftarrow W_{\text{new}}[vId + t \times V] / \sqrt{\text{sum\_square}} \)
5 MODELING: DETERMINATION OF THE TILE SIZE

In this section, we first compare the data movement cost of our approach with original FAST-HALS algorithm. Then the data movement of our algorithm as a function of $T$ is developed to select effective tile sizes.

$$\sum_{i=0}^{K-1} iVT^2\left(\frac{1}{T} + \frac{2}{\sqrt{C}}\right) = VT^2\left(\frac{1}{T} + \frac{2}{\sqrt{C}}\right)\left(\frac{K^2-KT}{2T^2}\right)$$  (7)

$$\sum_{i=0}^{K-1} T(VT + T + V) = \frac{K}{T}VT(VT + T + V)$$  (8)

In our approach, $W$ is updated in three phases. Phases 1 and 3 can be implemented using matrix-multiplication, and the corresponding cost is shown in Equation 7, where $T$ represents the tile size and $C$ is the cache size. Phase 2 can be implemented using matrix-vector multiplication and the associated cost is shown in Equation 8. Since loading matrix $W$ dominates the data movement cost in phase 2, the cost of loading vectors can be ignored. Equation 9 shows the total data movement required for updating $W$.

$$vol(T) = V\left(\frac{1}{T} + \frac{2}{\sqrt{C}}\right)(K^2-KT) + \frac{K}{T}VT(W)$$  (9)

The cost of updating $H$ is similar to updating $W$. Compared to updating $W$, updating $H$ does not require accessing $Q$. In addition, since $H$ is not normalized, the cost associated with normalization is also not present.

The data movement cost of the original loop in line 12 in Algorithm 1 is $K(VK+K+6V+1)$. Hence, for the 20 NewsGroups dataset ($V=11,314$) with low rank $K=160$ on a machine with 35 MB cache, the data movement cost of original scheme is 300,525,600. However, in our scheme based on Equation 9, the cost is only 44,897,687 which is 6.7x lower than the original scheme.

The tile size $T$ affects the data movement volume and hence the performance. Equation 9 shows the total data movement of our algorithm as a function of $T$. Consider the case when there is only one tile ($T = K$). In this case, there is no work associated with phase 1 (contributions to left) and phase 3 (contributions to the right) as the first term of Equation 9 will become zero. The total data movement of phase 2 is $VK^2$ which is very high. Now consider the other extreme where the tile size is 1 ($T = 1$). In this case, phases 1 and 2 have very high data movement (> $VK^2$). Thus, when $T$ is high, the total data movements required for phases 1 and 3 are low, but phase 2 has high data movement. On the other extreme, when $T$ is low, the total data movements for phases 1 and 3 are high, but phase 2 has low data movement. Hence, we expect the combined data movement for all the phases to decrease as $T$ increases from 1 to some point and then the data movement will increase again as $T$ approaches $K$. Since performance is correlated with data movement, the performance as a function of tile size should show a similar trend and is shown in Figure 6.

$$\frac{d(vol(T))}{dT} = T^2\left(\frac{2}{\sqrt{C}} - 1\right) + K = 0$$  (10)

$$T = \sqrt{\frac{K}{2}}$$  (11)

In order to build a model to determine the tile size for a given $K$, the derivative of Equation 9 with respect to $T$ is set to zero (Equation 10). The solution to Equation 10 is shown in Equation 11. For a machine with cache size of 35 MB, the tile sizes computed by our model are 8.94, 12.64 and 15.49 for $K=80, 160$ and 240, respectively. Figure 6 shows that our model selected tile sizes that are optimal/near optimal.

6 EXPERIMENTAL EVALUATION

This section compares the time to convergence and convergence rate of PL-NMF with various state-of-the-art techniques.

6.1 Benchmarking Machines

Table 3 shows the configuration of the benchmarking machines used for experiments. All the CPU experiments were run on an Intel Xeon CPU E5-2680 v4 running at 2.4 GHz with 128GB RAM. The GPU experiments were run on an NVIDIA Tesla P100 PCIe GPU with 16GB global memory.

| Machine | Details |
|---------|---------|
| CPU     | Intel(R) Xeon(R) CPU E5-2680 v4 (28 cores), 128GB RAM, ICC version 18.0.3 |
| GPU     | Tesla P100 PCIe (56 SMs, 64 cores/MP, 16GB Global Memory, 4 MB L2 cache, CUDA version 9.2.88) |
### 6.2 Datasets

For experimental evaluations we used three publicly available real-world text datasets – 20 Newsgroups\(^3\), TDT2\(^3\), Reuters\(^3\). In addition, in order to represent the audio-visual context analysis in social media platforms, we used two image datasets – AT&T\(^4\) and PIE\(^5\). 20 Newsgroups, TDT2 and Reuters are sparse matrices, and AT&T and PIE are dense matrices. The 20 Newsgroups dataset contains a document-term matrix in bag-of-words representation associated with 20 topics. TDT2 (Topic Detection and Tracking 2) dataset is a collection of text documents from CNN, ABC, NYT, APW, VOA and PRI. Reuters dataset is a collection of documents from the Reuters newspaper in 1987. Both AT&T and PIE datasets contain images of faces in dense matrix format. The size of each image in AT&T and PIE datasets is 92×112 and 64×64 pixels, respectively. Table 4 shows the characteristics of each dataset.

#### Table 4: Statistics of datasets used in the experiments. \(V\) is the number of rows and \(D\) is the number of columns in non-negative matrix \(A\). For the text datasets, \(V\) is the vocabulary size and \(D\) is the number of documents.

| Dataset     | \(V\)       | \(D\)       | Total NNZ | Sparsity (%) |
|-------------|-------------|-------------|-----------|--------------|
| 20 Newsgroups | 26,214      | 11,314      | 1,323,869 | 99.6474      |
| TDT2        | 36,771      | 10,212      | 1,323,869 | 99.7519      |
| Reuters     | 18,933      | 8,295       | 389,455   |              |
| AT&T        | 400         | 10,304      | 4,121,478 | 0.0050       |
| PIE         | 11,554      | 4,096       | 47,321,408| 0.0080       |

#### 6.3 Performance Evaluation

##### 6.3.1 Convergence.

Figure 7 shows the relative error as a function of elapsed time of various NMF implementations for different \(K\) values. To ensure fairness, the number of threads in all CPU implementations were tuned per dataset and the best performing configuration was selected. For each dataset, the same randomly initialized non-negative matrices were used for all CPU and GPU implementations. Since the bionmf-MU-gpu implementation does not allow the input matrix to be sparse, we only compared our GPU implementation with bionmf-MU-gpu on AT&T and PIE dense image datasets. PL-NMF-cpu and PL-NMF-gpu consistently outperformed existing state-of-the-art CPU and GPU implementations on all datasets. As reported in previous studies, FAST-HALS produced a better convergence rate than other NMF variants. MU and ANLS-BPP algorithms suffered from a lower convergence rate on both sparse and dense matrices. As shown in Figure 8, planc-HALS-cpu was the only implementation which was able to maintain the same solution quality as ours. However, our implementation converged faster.

##### 6.3.2 Speedup.

Compared to the planc-HALS-cpu, our PL-NMF-gpu achieved 3.07×, 3.06×, 5.81×, 3.02× and 3.07× speedup per iteration on the 20 Newsgroups, TDT2, Reuters, AT&T and PIE datasets with \(K = 240\), respectively. As the relative error reduction per iteration is vastly different between MU and FAST-HALS algorithms, measuring the speedup per iteration between bionmf-MU-gpu and PL-NMF-gpu is not a fair comparison.

Figure 9 depicts the speedup of our PL-NMF-gpu over all CPU implementations. The y-axis in Figure 9 is relative error, and the x-axis is the ratio of elapsed time for all CPU implementations to reach a relative error to elapsed time for PL-NMF-gpu to approach the same relative error. All of the points in Figure 9 are greater than one. This indicates that PL-NMF-gpu is faster than all of the competing implementations. For example, when the compared models, i.e., PL-NMF-cpu, planc-HALS-cpu, bionmf-MU-gpu and planc-MU-cpu, converged to 0.12 relative error, the parallel PL-NMF-gpu achieved 3.49×, 9.74×, 26.41× and 287.1× speedup on PIE dataset, respectively.

#### Table 5: Breakdown of elapsed time in seconds for updating \(W\) on the 20 Newsgroups dataset. DMV: Iterative Dense Matrix-Vector Multiplications; DMM: Dense Matrix-Dense Matrix Multiplication; SpMM: Sparse Matrix-Dense Matrix Multiplication.

| Sequential | FAST-HALS NMF | elapsed time (s) | PL-NMF-cpu | elapsed time (s) |
|------------|---------------|-----------------|------------|-----------------|
| SpMM       | 0.048         | SpMM            | 0.048      |
| DMM        | 0.002         | DMM             | 0.002      |
| DMV        | 2.039         | Phase 1         | 0.005      |
|            |               | Phase 2 & 3     | 0.026      |

Table 5 shows the breakdown of elapsed time for each step in updating \(W\). Both sequential FAST-HALS NMF and PL-NMF-cpu implementations use the same mkl_dcsrmm() and cblas_dgemm() routines for SpMM and DMM operations. In Table 5, SpMM corresponds to line 10 in Algorithm 1 and line 1 in Algorithm 2, which

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\(^1\)http://dengcai.zjulearning.org:8081/Data/TextData.html
\(^2\)https://www.cl.cam.ac.uk/research/dtg/attarchive/facedatabase.html
\(^3\)http://dengcai.zjulearning.org:8081/Data/FaceDataPIE.html
\(^4\)https://github.com/rakshakannan/planc
\(^5\)https://github.com/bionmf-cntk/bionmf-gpu
Figure 7: Relative objective value over time on five datasets. According to current model, the $T$ values for $K = 80$, 160 and 240 are set to 10, 15 and 15, respectively. X-axis: elapsed time in seconds; Y-axis: relative error.
computes the same $A^TH^T$. Similarly, DMM corresponds to line 11 in Algorithm 1 and line 2 in Algorithm 2, which performs the same $HH^T$. The difference of updating $W$ is that PL-NMF-cpu performs phases 1, 2 and 3 instead of iteratively performing DMV computations. As expected, the updating time of $W$ is considerably decreased in our PL-NMF-cpu algorithm, indicating that the reformulation of the core-computations to matrix-matrix multiplication shows the benefit of our approach.

7 CONCLUSION

In this paper, we developed a HALS-based parallel NMF algorithm for multi-core CPUs and GPUs. The data movement overhead is a critical factor that affects performance. This paper does a systematic analysis of data movement overheads associated with NMF algorithm to determine the bottlenecks. Our proposed approach alleviates the data movement overheads by enhancing data locality. Our experimental section shows that our parallel NMF achieves significant performance improvement over the existing state-of-the-art parallel implementations.

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