Directly coupled adiabatic superconductor logic

Naoki Takeuchi¹, Kota Arai² and Nobuyuki Yoshikawa¹,²

¹ Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan
² Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan

E-mail: takeuchi-naoki-kx@ynu.ac.jp

Received 15 December 2019, revised 2 March 2020
Accepted for publication 8 April 2020
Published 1 May 2020

Abstract
Adiabatic superconductor logic (ASL) families are energy-efficient because they can operate with a switching energy much less than the $I_c\Phi_0$ product, where $I_c$ is the critical current for Josephson junctions, $\Phi_0$ is the flux quantum, and $I_c\Phi_0$ is generally on the order of $10^{-19}$ J. A switching energy of 0.03$I_c\Phi_0$ has been demonstrated by adiabatic quantum-flux-parametron (AQFP) logic, which indicates the possibility of extremely energy-efficient digital circuits using ASL. ASL uses signal transformers to propagate and invert the signal current; otherwise, it is difficult to design inverters. However, signal transformers are generally difficult to miniaturize. Therefore, to realize high-density and energy-efficient superconductor circuits, ASL that does not use signal transformers is required. In this paper, we propose ASL without signal transformers, which we call directly coupled quantum-flux-parametron (DQFP). DQFP logic is based on AQFP, but it can invert signal current without using signal transformers. We conducted numerical simulation of a DQFP inverter chain to show that DQFP logic can invert signal current without signal transformers, and that DQFP logic can operate adiabatically. Then, we designed and fabricated basic DQFP circuits, such as an inverter chain and a full adder. All the circuits were found to have wide operating margins. Our results indicate that DQFP logic is suitable for high-density and energy-efficient superconductor circuits.

Keywords: adiabatic logic, miniaturization, quantum flux parametron, superconductor digital circuit

(Some figures may appear in colour only in the online journal)

1. Introduction
Superconductor logic families [1–4] can operate with low power consumption at cryogenic temperatures, and thus are crucial in building cryogenic systems, such as single-photon image sensors [5–7] and quantum computers [8–10], in which superconductor digital circuits can be used as interface circuits for superconductor detectors or qubits. In general superconductor logic, the switching energy (energy dissipation per switching event) is approximately $I_c\Phi_0$, where $I_c$ is the critical current for Josephson junctions and $\Phi_0$ is the flux quantum; $I_c\Phi_0$ is only $3.1 \times 10^{-19}$ J for a typical $I_c$ of 150 µA. To achieve even smaller switching energy, adiabatic superconductor logic (ASL) families, which adopt adiabatic switching [11, 12], have been proposed. ASL includes the parametric quantron [11, 13], quantum flux parametron (QFP) [14], negative-inductance superconducting quantum interference device (nSQUID) [15], and adiabatic QFP (AQFP) [16], which is a version of QFP that uses Josephson junctions with small characteristic times (on the order of sub-picoseconds) to reduce energy dissipation. In ASL, the potential energy of a logic gate changes gradually from a single well to a double
well such that the logic state can change quasi-statically and adiabatically, which results in a switching energy much less than $I_s\Phi_0$. A switching energy of 0.03$f_0\Phi_0$ has been demonstrated with AQFP logic [17], indicating the possibility of extremely energy-efficient digital circuits using ASL.

ASL generally uses transformers (which we call signal transformers) to propagate and invert the signal current because magnetically coupled rf superconducting quantum interference devices (SQUIDs) are used as building blocks; otherwise, it is difficult to design inverters, as will be shown later. However, the signal transformers in ASL have the following problems. It is difficult to miniaturize transformers while maintaining coupling coefficients [18]. Also, in some logic such as AQFP, a signal transformer occupies a large part of the gate area [19]. Therefore, to realize high-density and energy-efficient superconductor circuits, ASL that does not use signal transformers is required. Rylov et al proposed DC powered parametric quantron [20] as ASL without signal transformers, which, however, was not practical due to narrow parameter margins. We showed that AQFP with $\pi$ Josephson junctions can operate without using signal transformers [21], where rf-SQUIDs with $\pi$ Josephson junctions are used to invert signal current. However, this approach is not possible using conventional fabrication processes for superconductor/insulator/superconductor Josephson junctions.

In this paper, we propose ASL without signal transformers, which we call directly coupled QFP (DQFP). DQFP logic is based on QFP/AQFP but can invert the signal current without using signal transformers. First, we show a typical schematic of an AQFP gate and explain why signal transformers are required in AQFP logic. Then, following an explanation of the operating principle of DQFP logic, we conduct numerical simulations of a DQFP inverter chain to show that the DQFP inverter can operate without signal transformers. We also show how other DQFP logic gates are designed. Finally, we demonstrate basic DQFP circuits, including an inverter chain, a buffer chain, a NOR gate, and a full adder.

2. Operating principle

Figure 1 schematically illustrates an AQFP gate. This gate is powered and clocked by an ac excitation current $I_s$, which produces an ac magnetic flux with an amplitude of $0.5\Phi_0$. The combination of $I_s$ and a dc offset current $I_d$, which produces a dc magnetic flux of $0.5\Phi_0$, allows AQFP circuits to be operated using only two ac current sources. The details of the excitation methods in AQFP logic can be found in the literature [19]. When $I_s$ increases and a total magnetic flux of $0.5\Phi_0$ is applied to the gate, either of the Josephson junctions $J_1$ and $J_2$ switches, depending on the polarity of the input current $I_{in}$. As a result, a state current $I_{out}$, the polarity of which represents the logic state, is generated through $L_q$: a positive $I_{out}$ represents a logical 1, and a negative $I_{out}$ represents a logical 0. Finally, the output current $I_{out}$ is generated via a signal transformer composed of $L_q$, $L_{out}$, and $k_{out}$. The logic function of this gate is determined by the polarity of $k_{out}$. This gate operates as a buffer for a positive $k_{out}$ because the polarity of $I_{out}$ is the same as that of $I_{in}$. Conversely, this gate operates as an inverter for a negative $k_{out}$ because the polarity of $I_{out}$ is opposite to that of $I_{in}$. Without signal transformers, it is difficult to design inverters because the polarity of $I_{out}$ is the same as that of $I_{in}$. This is why signal transformers are needed in AQFP logic gates.

Figure 2(a) illustrates a DQFP inverter, which does not include signal transformers. The operating principle of this gate is the same as that of AQFP gates. When an ac excitation current $I_s$ increases, either of the Josephson junctions $J_1$ and $J_2$ switches depending on the polarity of the input current $I_{in}$. The logic state for this gate is represented by the polarity of the
state current $I_{st}$, as with AQFP logic. A marked difference from the AQFP gate shown in figure 1 is that a dc-SQUID composed of $J_1$, $J_2$, $L_1$, and $L_2$ is inserted between the input and output ports in figure 2(a), whereas a dc-SQUID is inserted between the input port and ground in figure 1. Therefore, $I_{st}$ is output from the opposite side of the dc-SQUID to which the input current $I_{in}$ is applied, whereas $I_{q1}$ and $I_{in}$ share the same side of the dc-SQUID in the AQFP gate. As a result, the polarity of $I_{st}$ is opposite to that of $I_{in}$ after $J_1$ or $J_2$ switches: the DQFP gate shown in figure 2(a) operates as an inverter, even without signal transformers. It is noteworthy that $L_{q1}$ and $L_{q2}$ are added to make a closed loop composed of $L_{q1}$, $L_{q2}$, and the dc-SQUID; otherwise, the $LC$ product, or the potential energy shape, for the DQFP inverter changes significantly depending on the circuits connected to the DQFP inverter. Figure 2(b) illustrates a buffer used in DQFP logic, which is an AQFP gate with the signal transformer removed. The circuit parameters for the DQFP inverter and buffer are given in the caption of figure 2. The device parameters, such as sub-gap resistance, are based on the National Institute of Advanced Industrial Science and Technology (AIST) 10-kA cm$^{-2}$ Nb high-speed standard process (HSTP) [19].

Figure 4. Simulation results for the switching energy of a DQFP inverter. The switching energy approaches zero as the frequency decreases, which indicates that the DQFP inverter can operate adiabatically in the quasi-static limit.

### 3. Numerical simulation

We conducted numerical simulations using the Josephson circuit simulator JSIM [22] to show that the DQFP inverter can invert a signal current without signal transformers. Figure 3(a) schematically illustrates the DQFP inverter chain used in the numerical simulations. This inverter chain is powered and clocked by a pair of ac excitation currents ($I_{x1}$ and $I_{x2}$) with a phase difference of 90° [19]. $I_{x1}$ and $I_{x2}$ cause an ac magnetic flux with an amplitude of 0.5$\Phi_0$ to be applied to each gate, and $I_d$ causes a dc magnetic flux of 0.5$\Phi_0$ to be applied to each gate. The frequency $f$ of $I_{x1}$ and $I_{x2}$ corresponds to the given operating frequency. $\phi_1$ through $\phi_4$ represent excitation phases, by which logic operations are performed with a phase separation of 90°. Figure 3(b) shows the simulated waveforms of the DQFP inverter chain for $f = 5$ GHz, where $I_{in}$ represents the input current to the first inverter and $I_{st}$ through $I_{st4}$ represent the state currents [$I_{st}$ in figure 2(a)] of the first through the fourth inverters, respectively. This figure shows correct operation because the logic state $I_{st}$ is inverted by each DQFP inverter.

We also analyzed the switching energy for a DQFP inverter by integrating the product of the excitation currents and voltages over time [23]. Figure 4 shows the simulation results for the switching energy $E_{sw}$ as a function of $f$. The symbols are the simulation results, and the curve is a linear regression given by $E_{sw} = af$, where $f$ is in gigahertz and $a = 1.14 \times 10^{-22}$. This figure shows that $E_{sw}$ approaches zero as $f$ decreases, that is, $\Delta F = W$ in the quasi-static limit, where $\Delta F$ is the free energy change of the DQFP inverter, and $W$ is the work performed on the inverter by a power supply. Since the DQFP inverter does not conduct stochastic processes (i.e., entropy does not change), $\Delta F = \Delta E$, where $\Delta E$ is the energy change of the inverter. Thus, $\Delta E = W$ in the quasi-static limit, which indicates that the DQFP inverter can operate via quasi-static adiabatic processes.
4. Logic gate design

Since DQFP logic includes both inverters and buffers, DQFP logic gates can be designed in the minimalist way [24], where logic gates are designed using four types of building block cells: buffer, inverter, constant (which generates logical 0 s or 1 s), and branch (which is an inductor branch to merge or split the signal current). The constant cell can be designed by making the circuit parameters in the DQFP inverter (or buffer) asymmetrical [25]. Here we show an example of a minimalist design of DQFP logic gates. Figure 5(a) shows the layout of the DQFP inverter cell for the HSTP. The circuit parameters of the inverter were extracted using the 3D inductance extractor InductEx [26] and correspond to those shown in the caption of figure 2. This inverter adopts symmetrical layout to avoid unwanted parasitic magnetic coupling [24]. The area of this inverter is 20 \( \mu \text{m} \) (width) by 25 \( \mu \text{m} \) (height), which is only 62.5\% of that of the AQFP inverter cell for the HSTP (width of 20 \( \mu \text{m} \), height of 40 \( \mu \text{m} \)). This verifies that the gate area in ASL can be reduced by removing signal transformers. We also designed a DQFP buffer cell and a constant cell, the areas of which are the same as that of the DQFP inverter. Figure 5(b) shows how a three-input minority (MINO) gate cell, the output of which is determined by the minority vote of the inputs, is designed, where three DQFP inverter cells and a branch cell are put together. The output currents from the three inverter cells are merged by the branch cell, so that the output signal \( x \) is determined by \( x = (\neg a \land \neg b) \lor (\neg b \land \neg c) \lor (\neg c \land \neg a) \), where \( a, b, \) and \( c \) are the input signals. Various logic gates can be designed on the basis of this MINO gate cell; for instance, a NOR gate can be designed by replacing one of the three inverter cells in the MINO gate with a constant-0 cell (which generates logical 0 s).

5. Experiment

We built a DQFP cell library that included various DQFP logic cells using minimalist design. Then, we designed basic DQFP circuits using the cell library, such as an inverter chain, a buffer chain, a NOR gate, and a full adder. This full adder was designed using three MINO gates in a way similar to previous studies [27, 28], which designed a full adder using three majority (MAJ) gates (which are complementary to MINO gates). Figure 6 shows a micrograph of these DQFP circuits fabricated using the HSTP, which includes Nb/AlOx/Nb Josephson junctions and four Nb layers on a Si substrate (more details can be found in the literature [19]). We have not designed readout circuits for DQFP logic, so we used AQFP circuits to read out the output signals of the DQFP circuits. The AQFP circuits receive the signal currents from the DQFP circuits, and the de-SQUIDs coupled to the AQFP circuits generate voltage signals [16]. \( I_{x1} \) and \( I_{x2} \) are a pair of ac excitation currents to power and clock the DQFP circuits. \( I_{in}, I_{inb}, \) and \( I_{inc} \) are the input currents. The inverter and the buffer chains receive \( I_{inc} \); the NOR gate receives \( I_{inb} \); and the full adder receives \( I_{in}, I_{inb}, \) and \( I_{inc} \). \( V_{inv}, V_{buf}, \) and \( V_{inc} \) are the output voltages of the inverter chain, buffer chain, and NOR gate, respectively; and \( V_{cout} \) and \( V_{s} \) are the carry-out and sum signals of the full adder, respectively. We operated the DQFP circuits at 4.2 K in liquid He. Figure 7 shows the waveforms measured at 100 kHz. All the circuits operated correctly with wide operating margins with regard to \( I_{x1} \) and \( I_{x2} \): \( \pm 69\% \) and \( \pm 66\% \) for the inverter chain, \( \pm 41\% \) and \( \pm 39\% \) for the buffer chain, \( \pm 68\% \) and \( \pm 66\% \) for the NOR gate, and \( \pm 34\% \) and \( \pm 44\% \) for the full adder. This experiment indicates that DQFP logic can operate robustly in actual circuits. Note that circuit performance is the same between AQFP and DQFP circuits because in both circuits operated correctly with wide operating margins with regard to \( I_{x1} \) and \( I_{x2} \): \( \pm 69\% \) and \( \pm 66\% \) for the inverter chain, \( \pm 41\% \) and \( \pm 39\% \) for the buffer chain, \( \pm 68\% \) and \( \pm 66\% \) for the NOR gate, and \( \pm 34\% \) and \( \pm 44\% \) for the full adder. This experiment indicates that DQFP logic can operate robustly in actual circuits. Note that circuit performance is the same between AQFP and DQFP circuits because in both
Figure 6. Micrograph of basic DQFP circuits, including an inverter chain, a buffer chain, a NOR gate, and a full adder. The circuits were fabricated using the HSTP.

Figure 7. Measured waveforms at 100 kHz. All the circuits operated correctly with wide operating margins with regard to $I_{x1}$ and $I_{x2}$.

circuits the energy efficiency and operating frequencies are determined by junction parameters [29].

6. Conclusion

We proposed ASL called DQFP, which does not have signal transformers. DQFP logic can achieve signal inversion without using signal transformers, which generally occupy a large area in conventional ASL gates and are difficult to miniaturize. The area of a DQFP inverter cell was only 62.5% of that of an AQFP inverter cell. Importantly, DQFP logic gates can be further miniaturized by adopting high-kinetic-inductance layers [30] in future fabrication processes, whereas the signal transforms in conventional ASL cannot use this approach because kinetic inductances do not couple to each other. Ultimately, the area of a DQFP inverter cell will be dominated by that of the dc-SQUID including $J_1$ and $J_2$ (approximately 15 $\mu$m by 10 $\mu$m) because the dc-SQUID requires a transformer to apply excitation flux; thus, it is estimated that the gate area will be reduced to only 19% of that of the current AQFP design (20 $\mu$m by 40 $\mu$m). We conducted numerical simulations to show that the DQFP inverter can operate without using signal transformers. We designed various DQFP logic gates using minimalist design to establish a cell library. We then designed and fabricated basic DQFP circuits, including an inverter chain, a buffer chain, a NOR gate, and a full adder. All the circuits were found to have wide operating margins with regard to excitation current. Our results indicate the possibility of creating high-density and energy-efficient superconductor circuits using DQFP logic.

Acknowledgments

The present study was supported by PRESTO (No. JPMJPR1528) from the Japan Science and Technology Agency (JST) and KAKENHI (No. 18H01493 and No. 19H05614) from the Japan Society for the Promotion of Science (JSPS). The circuits were fabricated in the Clean Room for Analog-digital superconductivity (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST). We would like to thank C J Fourie for providing the 3D inductance extractor InductEx.

ORCID iDs

Naoki Takeuchi  https://orcid.org/0000-0003-0396-5222
Nobuyuki Yoshikawa  https://orcid.org/0000-0001-6191-6715

References

[1] Likharev K K and Semenov V K 1991 RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems  IEEE Trans. Appl. Supercond. 1 3–28
[2] Mukhanov O A 2011 Energy-efficient single flux quantum technology  IEEE Trans. Appl. Supercond. 21 760–9
[3] Herr Q P, Herr A Y, Oberg O T and Ioannidis A G 2011 Ultra-low-power superconductor logic  J. Appl. Phys. 109 103903
[4] Tanaka M, Ito M, Kitayama A, Kouketsu T and Fujimaki A 2012 18-GHz, 4.0-αJ/bit operation of ultra-low-energy rapid single-flux-quantum shift registers Jpn. J. Appl. Phys. 51 053102
[5] Takeuchi N, Yamashita T, Miyajima S, Miki S, Yoshikawa N and Terai H 2017 Adiabatic quantum-flux-parametron interface for the readout of superconducting nanowire single-photon detectors Opt. Express 25 32650–8
[6] Miyajima S, Yabuno M, Miki S, Yamashita T and Terai H 2018 High-time-resolved 64-channel single-flux quantum-based address encoder integrated with a multi-pixel superconducting nanowire single-photon detector Opt. Express 26 29045
[7] Sahu A, Celik M E, Kirichenko D E, Filippov T V and Gupta D 2019 Low-power digital readout circuit for superconductor nanowire single-photon detectors IEEE Trans. Appl. Supercond. 29 1301306
[8] Berkley A J, Johnson M W, Bunyk P, Harris R, Johansson J, Lanting T, Ladizinsky E, Tolkacheva E, Amin M H S and Rose G 2010 A scalable readout system for a superconducting adiabatic quantum optimization system Supercond. Sci. Technol. 23 105014
[9] Takeuchi N, Ozawa D, Yamanashi Y and Yoshikawa N 2010 On-chip RSFQ microwave pulse generator using a multi-flux-quantum driver for controlling superconducting qubits Phys. C Supercond. Appl. 470 1550–4
[10] Leonard E et al 2019 Digital coherent control of a superconducting qubit Phys. Rev. Appl. 11 014009
[11] Likharev K 1977 Dynamics of some single flux quantum devices: I. parametric quantum IEEE Trans. Magn. 13 242–4
[12] Koller J G and Athas W C 1992 Adiabatic switching, low energy computing, and the physics of storing and erasing information Workshop on Physics and Computation (IEEE) pp 267–70
[13] Likharev K, Rylov S and Semenov V 1985 Reversible conveyor computation in array of parametric quantronics IEEE Trans. Magn. 21 947–50
[14] Hosoya M, Hiro W, Casas J, Kamikawai R, Harada Y, Wada Y, Nakane H, Suda R and Goto E 1991 Quantum flux parametron: a single quantum flux device for Josephson supercomputer IEEE Trans. Appl. Supercond. 1 77–89
[15] Semenov V K, Danilov G V and Averin D V 2003 Negative-inductance SQUID as the basic element of reversible Josephson-junction circuits IEEE Trans. Appl. Supercond. 13 938–43
[16] Takeuchi N, Ozawa D, Yamanashi Y and Yoshikawa N 2013 An adiabatic quantum flux parametron as an ultra-low-power logic device Supercond. Sci. Technol. 26 035010
[17] Takeuchi N, Yamae T, Ayala C L, Suzuki H and Yoshikawa N 2019 An adiabatic superconductor 8-bit adder with 24k\textbeta T energy dissipation per junction Appl. Phys. Lett. 114 042602
[18] Tolpygo S K, Bolkhvovsky V, Rastogi R, Zarr S, Day A L, Weir T J, Wynn A and Johnson L M 2017. Developments toward a 250 nm, fully planarized fabrication process with ten superconducting layers and self-shunted josephson junctions 2017: 16th Int. Superconductive Electronics Conf. (ISEC) (IEEE) pp 1–3
[19] Takeuchi N, Nagasawa S, China F, Ando T, Hidaka M, Yamanashi Y and Yoshikawa N 2017 Adiabatic quantum-flux-parametron cell library designed using a 10 kA cm\textsuperscript{–2} niobium fabrication process Supercond. Sci. Technol. 30 035002
[20] Rylov S V, Semenov V K and Likharev K K 1985 Reversible Josephson-junction circuits IEEE Trans. Appl. Supercond. 1550–4
[21] Arai K, Takeuchi N, Yamashita T and Yoshikawa N 2019 Adiabatic quantum-flux-parametron with π Josephson junctions J. Appl. Phys. 125 093901
[22] Fang E and Van Duzer T 1989 A Josephson integrated circuit simulator (JSIM) for superconductive electronics application The 1989 Int. Superconductivity Electronics Conf. (ISEC '89) (Tokyo) pp 407–10
[23] Yamae T, Takeuchi N and Yoshikawa N 2019 Systematic method to evaluate energy dissipation in adiabatic quantum-flux-parametron logic J. Appl. Phys. 126 173903
[24] Takeuchi N, Yamanashi Y and Yoshikawa N 2015 Adiabatic quantum-flux-parametron cell library adopting minimalist design J. Appl. Phys. 117 173912
[25] Ando T, Takeuchi N, Yamanashi Y and Yoshikawa N 2016 Adiabatic quantum-flux-parametron constant cells using asymmetrical structures IEEE J. Trans. Fundam. Mater. 136 747–52 in Japanese
[26] Fourie C J 2015 Full-gate verification of superconducting integrated circuit layouts with InductEx IEEE Trans. Appl. Supercond. 25 130209
[27] Goto E 1959 The parametron, a digital computing element Proc. IRE 47 1304–16
[28] Inoue K, Takeuchi N, Ehara K, Yamanashi Y and Yoshikawa N 2013 Simulation and experimental demonstration of logic circuits using an ultra-low-power adiabatic quantum-flux-parametron IEEE Trans. Appl. Supercond. 23 1301105
[29] Takeuchi N, Yamanashi Y and Yoshikawa N 2015 Energy efficiency of adiabatic superconductor logic Supercond. Sci. Technol. 28 015003
[30] Tolpygo S K, Bolkhvovsky V, Oates D E, Rastogi R, Zarr S, Day A L, Weir T J, Wynn A and Johnson L M 2018 Superconductor electronics fabrication process with MoNx kinetic inductors and self-shunted Josephson junctions IEEE Trans. Appl. Supercond. 28 1100212