Analysis of Three Phase Nine Level Diode Clamped Multi Level Inverter

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Abstract: Compared to conventional inverter (square wave) multi-level inverter offers quality power owing to different voltage levels utilization in average and high voltage. Besides it also reduces Total Harmonic Distortion in the distributed system and dv/dt across power switches. This advantage is transcendentally appropriate for cascaded diode connected converter that can be worked to create more number of levels using asymmetrical voltage source because of their integrated arrangement. However, this benefit no longer exist because it requires many dc links (batteries or rectifiers) which is costlier. Substitute method of implementing single low voltage floating DC link is to recompense voltage distortion using Neutral-Point-Clamped (NPC) converter. This NPC output and controlled floating single DC-link voltage along with controlled PWM strategy reduces the THD. This improves the bandwidth and make simpler the current control scheme. These motivated the study and analyze the performance of a Diode Clamp based three phase nine level multilevel inverter usingnovel PWM approaches in MATLAB 2014b and PROTEUS for hardware development. Thus low power prototype is developed and its performance is shown.

Keywords—Multilevel Inverter, Pulse Width Modulation, Neutral Point Clamped, ATmega8

1. Introduction
Now day’s inverters play a vital role in both domestic and industries, since all the appliances and machines works in AC supply. Even though power generated in generating station is AC but its quality changes when reach consumers this problem is called as Power Quality issues [1]. There are many sensitive loads that may malfunction when this impure AC is feed, so in order to overcome this issue a dedicated inverters are provided that will operate continuously even when there is grid power. Inverters is also used when there is power interruption for the continuous operation of appliances. There are many types of inverters basically inverters are classified according to types of loads, source
and output waveform. According to load: Single-phase loads are generally low powered industrial and nominal domestic appliances [2]. Three-phase loads are generally industrial loads where voltage and frequency are to be controlled depending upon the load requirement. According to the source it is classified in to Voltage source, current source and Impedance source. According to output waveform: Square wave output inverter [3]. Modified sine wave output inverter and Sine wave output inverter. Square wave inverter was the first inverter developed since it have only two square pulse one on positive side and other on negative side representing AC square wave. The main drawback in using square wave inverter is it generate more harmonics in which damage the core of electrical components by producing more heat leading to core saturation. This also create electromagnetic interference (EMI effect) affecting the communication lines [4].

In order reduce the impact of square wave inverter the modified sine wave inverter is developed by increasing the number of modulation pulse and voltage source where in which termed as Multilevel Inverters (MLI). The MLI is again classified in to different types such as (i) symmetrical MLI (ii) Asymmetrical MLI and Hybrid MLI[5][6] In Asymmetrical MLI the number of switches and switching sequence are not identical in both cycles. In symmetrical MLI the number of switches and switching sequence are identical for both positive and negative half cycles. Fig.1. Multilevel Inverter Topologies.[7][8]

2. Sinusoidal PWM signal

The topology above has a three phase output where the three phase voltages are 120° out of phase. Each phase requires a separate PWM signal, but the method for producing the PWM signal is the same. The difference in the PWM signals come from the control voltage signal, control.[9][10] The control signals have a frequency and the same phase difference of 120° as the voltages of the phase outputs. The frequency is the desired fundamental frequency of the inverter output voltage which will not look like the control signal and will contain voltage components at harmonic frequencies. With the similarities between the phases, generation of the pulse width modulation signals is illustrated for only one phase[11]. A block diagram for the generation of PWM signals is shown in Fig.2. The control input is the desired waveform characteristic to be seen at the phase output.
Usually, this is a sine wave of fixed or variable frequency with normalized amplitude. The repetitive waveform input is a triangle wave with a frequency considerably higher than the frequency of the control signal.[20] Thus, the triangle wave becomes a carrier frequency for the control signal. This relationship gives the modulation characteristic of the switch control signal. See (a) for an illustration where \( f_{tri} \) is the repetitive waveform signal with a frequency \( f_s \).[12][13]

The comparator operates on two conditions: \( i;\text{controi}<i^*\text{tri} \) and \( i;\text{controi}>u\text{tri} \). For \( i;\text{controi}<i^*\text{tri} \), the output of the comparator is a logic high signal and the top switch (TA+) is closed. For \( i;\text{controi}>u\text{tri} \), the output of the comparator is a logic low signal and the bottom switch (TA) is closed. These conditions give the results shown.[16] The values of the logic signal from the comparator are such that the devices being driven by the signals are in a completely on or completely off state. When in one of these states, the phase output voltage has a value of either the positive DC bus or the negative DC bus, resulting in the waveform[14]

The significant conception in a multi-level inverter is to accomplish higher AC power by means of a series of semiconductor switches such as power MOSFET, IGBT, SCR or even GTO with more number autonomous DC supply to execute transformation of single level to stair-cased different voltage output.[15] When discussing about DC supply many sources like batteries, super capacitors, fuel-cell, PV cells and other renewable energy. These types of MLI are suitable in medium voltage and medium-power applications owing to their capacity to produce better output waveforms with improved harmonic spectrum and attain desired voltage with a restricted rating.[17][18]

3. Multilevel Inverter Topologies

The Neutral Point Clamped (NPC) multilevel inverter was introduced by Nabae, et al., in 1981.[7] Capacitors, batteries, and sustainable power are ordinary sources which can be organized in single or different associations. The general grouping of MLI dependent on their foundation is pictured in Fig. 1. From the Figure 1 we come to know different types of MLI, however, in this paper only Neutral Point Clamped (NPC) is focused mainly about the implemented and control category are examined in detail. NPC inverters have been generally actualized because of its high ability in medium power applications with the moderately high effectiveness.[19] The NPC topology uses more capacitor pairs of each pair with identical voltage multiple capacitors rating in series to deliver different level of stair-case voltage waveform. The Figure.2 shows the PWM generation for each phase in three phase system.[20]

The NPC inverters are effective in system frequency transferring range, and hence this inverter topology is effectively used in low voltage grid interfacing system. Principle frequency switching
produces eminent degree of voltage, current and THD henceforth extra reactors are needed to moderate that issues which can expand the execution cost. Additionally, the increase in number of clamping diodes and capacitors decreases the dependability of the system. But even then this configuration reduces the harmonic by adding zero-voltage level. Since more clamping diodes, switches and uneven capacitor are used the application of this NPC-MLI is limited. Few such applications are SVC facts device, speed control of drives and interconnection of high voltage systems.[21]

Nine-Level Diode Clamped Multilevel Inverter (DC-MLI)

The block diagram of the proposed 9 level inverter using ATmega8 microcontroller is shown in the Figure. 4. This 9 level Diode Clamped MLI (DC-MLI) is also referred to as the Neutral Point Clamped (NPC) symmetrical MLI because of its basic nine-level structured staircase waveform. In this every level switching of the voltage utilizes a pair of diodes and switches except zero level. For the proposed system single DC link with (n-1) number of pairs of clamping diodes are required, with m is the number of different level of voltage. Subsequently for three phase 9 level NPC, 8 switches, 12clamping diodes, and 4common DC link capacitors are needed per phase as shown in Figure.6. From the given each phase of the MLI is divided in to two half cycle positive and negative, with two capacitors C1, C2, C3 and C4 delivers power on the positive cycle and C1', C2', C3' and C4' delivers power on the negative cycle which are connected in series. Here the point “O” represents the midpoint of two capacitor bank series Cn and Cn'. The 4 levels of positive cycle output voltages are Vdc, 3Vdc/4, Vdc/2, Vdc/4and 0 as the mid-point similarly and for negative cycle as–Vdc/4, -Vdc/2, -3Vdc/4 and –Vdc. The positive cycle switches are represented as Sa1, Sa2, Sa3 and Sa4 and for negative cycle switches are Sa1', Sa2', Sa3' and Sa4'.

\[
C = n-1 \quad (1)
\]
\[
S = 2(n-1) \quad (2)
\]
\[
D = (n-1)(n-2) \quad (3)
\]

Table 1: 9-level NPC MLI voltage levels and state of switches

| Voltage (V) | State of Switches |
|-------------|------------------|
| Vdc         | Sa1  Sa2  Sa3  Sa4  Sa1'  Sa2'  Sa3'  Sa4' |
| 1 1 1 1 O O O O |
| 3Vdc/4      | O  O  O  O  O  O  O  O |
| Vdc/2       | O  O  O  O  O  O  O  O |
| Vdc/4       | O  O  O  O  O  O  O  O |
| 0           | O  O  O  O  O  O  O  O |
| -Vdc/4      | O  O  O  O  O  O  O  O |
| -Vdc/2      | O  O  O  O  O  O  O  O |
| -3Vdc/4     | O  O  O  O  O  O  O  O |
| -Vdc        | O  O  O  O  O  O  O  O |

Table 1 shows the 9-level NPC MLI voltage levels and state of switches. The order of switching could be explained as following: For voltage level VA = Vdc, all the switches in the upper arm ie positive cycle Sa1 to Sa4. For 3Vdc/4switch ON Sa2 – Sa4 and Sa1’. For Vdc/2, switch ON Sa3 – Sa4 and Sa1’ and Sa2’. For Vdc/4 switch ON Sa4 and Sa1’ – Sa3’. For zero voltage level all the switches are turned OFF. For –Vdc/4 switch ON Sa4’ and Sa1-Sa3. For –Vdc/2 switch ON Sa1-Sa2 and Sa3’-Sa4’. For –3Vdc/4 switch ON Sa1 and Sa2’ – Sa4’. For –Vdc all the switches in the negative cycle Sa1’ – Sa4’ are turned ON. This sequence of switching and its output staircase waveform is shown in the Figure.3.
4. Synopsis of Control Strategy

The control strategy for the NPC-MLI is similar to a conventional converter in that a control voltage signal, a repetitive triangle wave signal, and a comparator function are used to produce the gate signals. The control voltage signal for each phase of the NPCI is the same signal used in the conventional converter, and likewise for the triangle wave as shown in Figure 2. [22]

The basic diode clamped MLI topology of one phase of three phase is shown in the Figure 6 which clearly pictures the number of DC source, capacitors, switches and diodes required. The MATLAB simulation of the circuit of the proposed 9-level diode clamped-MLI is shown in the Figure 7 for the purpose of performance analysis where it is found complicate in PROTEUS. The novel controlled PWM generation circuit diagram of the proposed 9-level diode clamped MLI is shown in the Figure 8 by generating the ref sinusoidal signal. The Figure 9 shows THD value of the proposed NPC-MLI circuit with series filter added. The Figure 10 and 11 shows the waveform of line and phase output voltage respectively. The Figure 12 shows the project level Hardware prototype of the proposed single 9-level NPC-MLI with 8 MOSFET switches IRF840 and pulse signal is generated using ATmega8 with RPS for supplying power to microcontroller and accessories like driver circuit. The step down transformers are used to supply reduced power for circuit operation and also acts as DC source to the NPC-MLI with bridge and filter circuit [23-24]
Fig.5. Single phase Diode clamped 9-level inverter Proteus using ATmega8

Fig.6. Single phase Diode clamped Inverter topology in MATLAB

NPCI Control Strategy
The design process concerning the control strategy uses both MATLAB and PROTEUS software packages. The PROTEUS software permits simulation of the desired topology of converters, control strategy and shows the implementation of the system with the available components in the market by the manufacturer with the same characteristics. The simulation diagram of the proposed 9 level NPC-MLI is shown in the Figure.5. Available Methods for Generation of Gate Drive Signals The gate drive signal generation involves both hardware and software. The hardware-based drive signals employ data storage devices (ROMs, EPROMS, etc.) or specific analog circuits. The data storage method requires that the drive signals be created and coded off-line for implementation on a specific storage device. Many interactive software programs are capable of generating the drive signals via digital waveform comparisons, and the data can be converted to the required device format. Implementing the data storage approach takes little time to construct and requires only basic external components and integrated circuits to store the data and to extract the data from the storage device. However, this
method provides limited flexibility without reprogramming the storage device, and the frequency response is limited to the frequency response of the storage device and associated circuitry [25-27]. The second hardware approach relies solely on electronic circuit design. The control circuit does exactly what the software program in the storage device method does, but in real time. Three major components of the gate drive circuit are the triangle wave generator, reference wave generator, and comparator ladder. This hardware approach is circuit design intensive and somewhat time consuming to construct.

The complexity of the circuits is limited by the overall goals of the circuit and the availability of integrated analog circuits. The analog approach enjoys a larger degree of flexibility than the storage device method, and the frequency response is limited only by the delay time from input to output of the circuit (i.e., real time). The software-based method utilizes microprocessor-generated signals. The microprocessor is programmed with a similar algorithm as used in the hardware method. The algorithm for the microprocessor can be very robust and complex, but, once it is loaded onto a device, reprogramming is required to change the algorithm. Usually, a microprocessor will require an output interface circuit(s) and possibly external program memory. The main advantage of the microprocessor approach is the robustness and flexibility that can be incorporated into the program. Typically, extremely fast microprocessors (digital signal processors [DSPs]) are required to execute the programs. When a flexible and robust drive circuit is required, the cost of the DSP and related external hardware can be justified. [28-30]

5. Simulation Experimental

![Fig.7. Three phase 9 level NPC-MLI simulation circuit](image)

![Fig.8. Control circuit of PWM generation](image)
Fig. 9. Total Harmonic Distortions of 9-level NPC-MLI

Fig. 10. 9-level NPC-MLI Line Voltage
Fig. 11. 9-level NPC-MLI Phase Voltage

Fig. 12. Hardware prototype of 9-level NPC-MLI
6. Conclusion
Here 9 levels Diode Clamped-MLI performance is analysed with variable capacitor as source using a novel control strategy. The supplementary converter is not future necessary to upgrade the total capacity of the converter. The developed circuit output voltage values are VPH is 240V and VL is 400V with the THD of 0.26% with adding some series filters. Relatively, the key goal is to increase the controllability and improve the capacity of this 9 level diode clamped MLI at low switching frequency. The projected system utilizing diode as clamping devices, with a common DC bus which is sufficient for three phase system. Capacitors divides voltage from a single DC source. For n-levels, n-1 switches and capacitors are essential. Capacitors are pre-charging is in sets. Output voltage is limited. The projected variable dc-link and switching pattern can be reformed to incorporate in hybrid topologies.

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