Modelling and Controlling of Induction Heating Unit for Induction Cooking Application

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Abstract. A study on the control methodology of voltage source inverter (VSI) fed series resonant circuit for induction heating has been done in this work with the goal that converter can be worked at about unity power factor. In this work, phase locked loop (PLL) has been accustomed to bring the converter’s switching frequency near to the natural frequency of series coil and capacitor branch of induction heater. Using this control method, the effectiveness of induction heater can be improved and necessity of input power is turned out to be less when compare to the fixed frequency operation. This control technique gives reliable operation of voltage source inverter fed circuit for varying load. Controlled phase locked loop gives increment or decrement in resonance frequency corresponding to the phase difference in voltage and current of resonant circuit. The coil of the induction heater is utilized as load in the resonant circuit of inverter. This power control procedure enables the inverter to operate near to the natural frequency for controlling power at all level. In this work, ZVS (zero-voltage switching) and ZCS (zero-current switching) condition has been obtained, and the switching losses are minimized. Pulse density modulated (PDM) power control method has been simulated to control the output power of a half bridge VSI fed induction heater.

Keywords—Dynamic frequency tracking using PLL (phase locked loop), PDM (Pulse density modulation) technique, lossless snubber circuit, Blanking time

1. Introduction
Since, Coal furnace and other conventional heating procedures were being utilized for industrial and domestic heating which prompts extreme wastage of energy and cause ecological issues. The induction heating framework has been developing constantly for local, business and industrial heating procedures which has higher effectiveness, quick, precise, affordable and has turned out to be prominent innovation utilized in modern industry and house hold appliances. Induction heating provides great reduction in losses, local and faster heating. The productivity of induction heating with the advancement in semiconductor technology has innovation which has turned out to be progressively reliable because of quick, precise and cost-effective and lossless switches, microcontroller and high frequency power supply and so forth. Single-stage voltage source fed inverters (VSI) has basically two types of topology one is half bridge another is full bridge [1]. In spite of the fact that these techniques are applied at low power application, they are broadly utilized in power supplies and as of now to shape expand high-control static power topologies, for example, the multi cell setups. Fig.1 demonstrates the power circuit for a half-bridge connected VSI [2], where basically two capacitors needs to produce
neutral point in between which is \( N \), with the end goal that every capacitor are needed to up a steady voltage \( V_{dc}/2 \). Since the extracted output power of inverter is proportional to fundamental frequency a set of capacitors \((C_1 \text{ and } C_2)\) is required. The two switches \( S_1 \) and \( S_2 \) should not be triggered at the same time to avoid short circuit over the dc link input source voltage so that \( V_{dc} \) can be produced successfully to energize the inverter. There are two characterized states (state 1 and state 2) and one vague state (state 3) [3]. So the modulating strategy should be such that the triggering of both switches should not be simultaneously. At any moment either the top switch or the base switch of the inverter leg should be ON.

Output power can be controlled in inverter by varying the frequency. The advantage of this technique respect to other power control technique is that it doesn’t required power control technique towards DC link voltage side. In this inverter system power control can be obtained by shifting the phase angle \( \phi \) of the output considering that the input voltage \( V_o \) of the series combination of coil capacitor resonating circuit has a square wave. The \( Q \) (Quality factor) is high so that load current \( I_o \) must be nearly sinusoidal through the resonant circuit. Power can be obtained as depicted in eq. (9) [3];

The impedance of the resonant circuit of half bridge VSI fed inverter shown in Fig. 1 can be expressed by expression (3) and (4).

\[
L_{eq} = L_1 + \frac{\omega M^2 R}{R_L^2 + \omega L_2^2} = L_1 - A^2 L_2 \\
R_{eq} = R + \frac{\omega M^2 R}{R_L^2 + \omega L_2^2} = R + A^2 R_L
\]

where \( A = \frac{\omega M}{(R_L^2 + \omega L_2^2)^{1/2}} = \frac{M}{L_2} \) at \( \omega L_2 \gg R_L \)

![Diagram](image)

**Figure 1: Proposed VSI fed resonant converter**

\[
Z = R_{eq} + j \left( \omega_c L_{eq} - \frac{1}{\omega C} \right) \\
Z = R_{eq} \left[ 1 + Q^2 \left( n - \frac{1}{n} \right)^2 \right]^{1/2} \\
\phi = \tan^{-1} \left[ Q \left( \frac{\omega_c}{n} \right) \right]
\]

Where \( \omega_c \) and \( \omega_r \) is the angular velocity corresponding to switching frequency and resonance frequency. The output-voltage \( V_o \) having fundamental component has been shown in equation (5) and can be obtained by Fourier analysis of \( V_{dc} \) as follows
\[
V_c = \frac{2V_{dc}}{\pi} \sin \omega_c t \quad \text{for} \quad 0 < \omega_c < 2\pi
\]  

(5)

The current through resonant circuit \( I_o \) has been expressed by equation (6)

\[
I_o = I_m \sin (\omega_c t - \Phi)
\]  

(6)

\[
\frac{i_o}{i_m} = \left[ \frac{n + \frac{1}{n}}{1 + Q^2 \left( n - \frac{1}{n} \right)} \right]^{1/2}
\]  

(7)

\[
\frac{i_o}{i_m} = 24.2
\]  

(8)

The contribution of fundamental current to deliver the active power is 24.2 time more than 3rd harmonic as shown in expression (8)

The expression for \( P_{out1} \) is as follows:

\[
P_{out1} = \frac{1}{2} I_m^2 R_{eq1}
\]  

(9)

This output power is useful power which inverter delivers to the load corresponding to the fundamental frequency.

2. Control System

2.1. Mathematical Model of Control System having PLL (phase locked loop)

In this section mathematical model has been described for organizing the control structure. The XOR of \( V_r \) and the yield voltage \( V_o \) of inverter has been obtained by passing \( V_r \) and \( V_o \) through zero crossing followed by XOR gate. The output has been filtered which produces a DC voltage at every sample time, and the voltage is the \( y(k) \) as expressed by (10)

\[
y(k) = V_r \oplus V_o
\]  

(10)

\[
e(k) = y(k) - 0.5
\]  

(11)

In the above formula, \( e(k) \) is output of XOR followed by adder. The average value of which is the input of LPF (low pass filter) [4]. Considering the transient state operation following relationship has been obtained between \( \Phi \) and \( T \) of the resonant circuit of the inverter.

\[
\Phi(T) = \tan^{-1} \left( \frac{R_C \omega(T)}{1 - \left( \frac{\omega(T)}{\omega_0} \right)^2} \right)
\]  

(12)

Assuming transient operation, the above relationship can be obtained which is approximately valid for slowly variation in period \( T \). Furthermore, equation (13) can be described as follows which is the output of the filter [1].

\[
y(k + 1) = y(k) + T \left( -\frac{1}{\tau} y(k) + \frac{1}{\tau} \frac{\Phi(T(k))}{\pi} \right)
\]  

(13)

The new state of the time period \( T(k + 1) \) at resonance is the function of the present state of itself, integral gain \( K_I \) and \( e(k + 1) \) is as expressed by equation (14).

\[
T(k + 1) = T(k) + K_I e(k + 1)
\]  

(14)
Here $K_i$ is the integral gain of the integrator and non-linear function $\Phi$ is function of $T(k)$ depicted above by equation (12), equations (13) and (14). By applying Taylor’s formula following linearized expression can be obtained of non-linear function $\Phi(T)$.

$$\phi(T) = \phi(T_0) + \frac{d\phi}{dt|_{T_0}} (T - T_0)$$

Where

$$\frac{d\phi}{dt|_{T_0}} = -\frac{1}{\pi R C_a}$$

From the equations (3), (4), (5), we can get

$$\Delta y(k+1) = \left(1 - \frac{T}{\tau}\right) \Delta y(k) - \frac{T}{\pi^2 \tau^2} \Delta T(k)$$

(16)

$$\Delta T(k+1) = K_i - \frac{K_i T}{\tau} \Delta y(k) + \left(1 - \frac{K_i T}{\pi^2 \tau^2}\right) \Delta T(k)$$

(17)

Further expression (16) and (17) are modified and expressed by state space having system matrix $A$ can be written as

$$C = \begin{bmatrix} \Delta y \\ \Delta T \end{bmatrix}^T$$

$$A = \begin{bmatrix}
\left(1 - \frac{T}{\tau}\right) & -\frac{T}{\pi^2 \tau^2} \\
K_i - \frac{K_i T}{\tau} & \left(1 - \frac{K_i T}{\pi^2 \tau^2}\right)
\end{bmatrix}$$

By applying stability test of jury we can obtained the range of gain $K_i$ for stability of control technique.

3. Power Control

A control technique named as inverter’s PDM method followed by suitable power control of the output has been simulated. This inverter’s PDM method runs and stops alternatively to inverter switches. Previously frequency control inverter methods had switching modes called as 1st and 2nd mode, whereas the inverter with PDM (pulse density modulation) method has mode 3 additionally, during which the inverter’s yield voltage becomes zero. Both the switching frequency and the supply voltage of inverter are maintained constant during which the inverter’s yield voltage becomes zero. Both the switching frequency and the supply voltage of inverter are maintained constant during these modes of the PDM. The phase-locked loop (PLL) control circuit has been implemented for tracking of dynamic frequency as well as power control, which provides gate pulses as output for inverter to reach resonant condition. Mode 3 has ordinarily been utilized in pulse density modulation for the inverters having switching sequence of the PDM. The inverter has voltage source as input with the amplitude of $V_{dc}$. PDM provides gate pulse to inverter switches so that it has $V_{dc}$ as input upto 14th cycle, whereas it provides as a zero voltage for two cycle as implemented (it can be control manually and automatically as per requirement of power control) if control range is provided upto sixteen resonant cycles, resulting power also varies, in comparison to the full power performance. Therefore, the inverter’s output can be constrained by altering average square wave voltage with adjusting the pulse density and PDM prevents the resonant circuit from the switching losses, since ZVS and ZCS is obtained [5][6][7]. Fig. (2) describes the alternate run and stop of resonant current having PDM technique. The output current is continuous because the time constant $\tau >> T$ otherwise it becomes discontinuous. Additionally, dc component must be avoided in the switching to ignore saturation of flux. In simulation it has been observed that each pulse has the combination of first and second mode in the switching pattern that a small dc component of average voltage is produced due to asymmetry in the circuit and which would not saturate the core, because ON state unavoidable resistances of the MOSFET’s. Considering the transient state, the load current $i_o$ can be expressed by following expression (20) when the supply of the inverter has $V_{dc}$ [7].
By observing the shape of the load current, it depicts the first-order response, in spite of the VSI fed resonant circuit it has the second-order system. This PDM technique is enough to produce the amplitude of the load current fluctuated.

The shape of $i_o$ is given by [5].

$$i_o(t) = I_{max} \left(1 - e^{-\frac{t}{\tau}}\right) + I_{o0} e^{-\frac{t}{\tau}} \quad (0 \leq t \leq T_A)$$

$$i_e(t) = i_e(T_A) e^{-\frac{(t-T_A)}{\tau}} \quad (T_A \leq t \leq T)$$

Here $I_{o0}$ initial value of $i_E$.

Hence average output power $P$ will be

$$P = \frac{1}{T} \int_{0}^{T} v_o i_o dt$$

$$P = \frac{1}{T} \int_{0}^{T} 4 \frac{V_{dc}}{\pi} \sin wt \cdot i_e(t) \sin(wt - \phi) dt$$

$$P = \frac{2}{\pi} V_{dc} \cos \phi \frac{1}{T} \int_{0}^{T} i_e(t) dt$$

$$P = P_{max} \left\{ T_A + \tau \left( \frac{1 - e^{-\frac{T}{\tau}}}{1 - e^{-\frac{T}{\tau}}} \right) \left( e^{-\frac{T}{\tau}} - e^{-\frac{T_A}{\tau}} \right) \right\}$$

The output power will be maximum in case of $T_A/T = 1$. Here time constant $\tau$ is greater than the time period $T$ then output current becomes continuous. Otherwise if $\tau$ is less than time period $T$ then the output current becomes discontinuous.

4. Switching Frequency

It is well known that inverter supply maximum power to the load and minimum switching losses if the inverter is having switching frequency at natural or natural frequency of the load (if the load response is resonating in nature). Practically it is impossible to obtain resonance frequency using any kind of control technique due to variation in magnetic permeability and parasitic inductance. But the switching losses can be minimize using lossless snubber capacitor and PDM techniques which has been discuss in detail in the section 3, 4, 5 and 6. Observing the voltages across switch $S_1$ which is
blocked while $S_1$ is not triggered (off state) for half of the cycle. In this situation, there are two possible states. The first state when $S_1$ is triggered and conducting and $S_2$ is off, whereas the second when $S_2$ is triggered and conducting and $S_1$ is off. Since the ZVS and ZCS takes place, the lossless snubber capacitor will ensure very low switching losses because ZVS and ZCS occur while turning on the switches [8]. Following three switching condition may occur which is describe as below.

4.1. Inductive Load Switching ($f_{sw} > f_r$)

If the inverter operates at lagging power factor and operating frequency of inverter is slightly greater than the resonance frequency then the switching is said to be inductive load switching.

![Waveform of Voltage and Current at Inductive Load Switching](image)

Figure 3: Wave form of voltage and current of switch at inductive load switching

Fig. 3 depicts the waveforms corresponding to voltage and current of the switches. In this case one can clearly say that voltage leads the current. Analyzing the Fig. 6(a), 6(b), 6(c) and 6(d) the current $I_o$ conducts through $S_1$ in first mode of operation. Then, $V_o$ changes polarity, $S_1$ is turned off causing switching is hard because inductive current creates huge voltage stress across the switch. Switch $S_2$ is turned on with positive load current. Finally, $S_2$ is turned off, causing the huge losses in the switches and switches may damage. Thus inductive load switching is not desirable and should be avoided.

4.2. Capacitive Load Switching ($f_{sw} < f_r$)

If the inverter operates at leading power factor and switching frequency is slightly less than the resonance frequency then the switching is said to be capacitive load switching. Fig. 4 depicts the waveforms corresponding to voltage and current of the switches. In this case one can clearly say that voltage lags the current. Analyzing the Fig. 6(a), 6(b), 6(c) and 6(d), the current $I_o$ conducts through $S_1$ in first mode of operation. Then, $I_o$ changes its direction due to which the reverse current flows through the switch $S_1$. Then switch $S_1$ is turned off causing switching without current becoming zero due to switching losses in the switch. After this, $S_2$ are turned on with negative load current $I_o$. Finally, $S_2$ is turned off, causing the huge losses in the switches and switches may damage.
Figure 4: Wave form of voltage and current of switch at the capacitive load switching

4.3. Resonance Frequency \( (f_{\text{sw}} = f_r) \)

Fig. 5 shows that the inverter has been operated at desirable switching resulting in zero phase difference between \( I_o \) and \( V_o \), i.e., resonance frequency condition is obtained and proper commutation of the switches has been done. Analyzing the voltages across \( S_1 \), the voltage is blocked by \( S_1 \) for half of the cycle while they are off. Under these conditions, there is possibility of two switching states. The 1st state occurs when \( S_1 \) conducts and the 2nd state when \( S_2 \) conducts. This case will ensure very low losses during switching.

Figure 5: Wave form of voltage and current of switch at the resonance frequency

5. Snubber Circuit

5.1. Lossless Snubber Circuit

A lossless snubber circuit consists only one capacitor without any resistor and this capacitor is connected in parallel with each switches. Considering the Fig. 6(b) to be first, load or resonant current flows through \( S_1 \), assuming the voltages of the snubber capacitors \( C_{S1} \) is zero initially and voltage...
across $C_s2$ is the same as input supply voltage or dc link voltage $V_{dc}$. $S_f$ can be turned off with ZCS condition.

While commutating the switch, the capacitors $C_S1$ are being charged, while $C_S2$ is being discharged as shown in Fig. 6(c). Since the $C_S1$ and $C_S2$ have comparative similar capacitance value, the current $i_o/2$ flows through the $C_f$, $C_S1$ and through load whereas the remaining current flows through the $C_S2$, $C_2$, and through load. Further when the voltages across $C_S2$ reach zero, the free-wheeling diodes $D_2$ (body diode of Mosfet) starts conducting as depicted by Fig. 6(d). $S_2$ is triggered with the gate pulse while load current flowing through $D_2$ becomes zero and thus ZVS can be achieved as soon as the direction of the $I_o$ verge to change the direction. Since short circuit of MOSFET’s would short the snubber capacitor hence lossless snubber circuit would not work well while operating the inverter at the leading power factor. Thus the VSI inverter having snubber circuit should be operated at lagging power factor [5].

6. Blanking Time
Considering the VSI (voltage source inverter) fed half bridge inverter is equipped with lossless snubber circuit. Suppose the peak value of the current is $I_o$ then the instantaneous current can be expressed as the following equation (24) [5].

$$i_o = -I_o \sin (\omega t)$$

The $V_c$ (voltage of the snubber capacitor) starts to rise when the switch is turned off at the time of $T_{off}$, and expressed by following equation given by
\[ V_c(t) = \frac{1}{\pi C} \int_{t}^{t_{off}} \frac{i_{off}}{2} dt \]  

(25)

Where \( C_s \) represents the snubber capacitor, \( T_D \) is required time for snubber capacitor voltage \( V_c(t) \) to charge up to \( V_{dc} \), and can be obtained by substituting into (26) and expressed as follows[9][10].

\[ V_c(-T_d) = V_d \]  

(26)

\[ T_d = \frac{1}{wC} \left( \cos wT_{off} + 2wC \frac{V_d}{i_{peak}} \right) \]  

(27)

The \( V_c \) reaches \( V_d \) at \( t = 0 \) gives the minimum value of \( T_{off} \) as follows

\[ T_{min} = \frac{1}{w} \cos^{-1} \left( 1 - 2wC \frac{V_d}{i_{peak}} \right) \]  

(28)

\( T_{min} \) is the minimum delay time as shown in above expression for incoming switch, which has to be triggered, will be provided for obtaining successful ZVS and ZCS. This condition provides minimum voltage spikes across the switches.

7. Result and Discussion

![Figure 7: Wave form of output voltage (green) and current (blue)](image)

![Figure 8: Waveforms of capacitor voltage (purple) and coil voltage (indigo)](image)

The VSI fed induction heater normally operates at high frequency. The objective of this study is to simulate a pulse density modulated (PDM) inverter for 25 kHz for induction heating. This technique is capable of adjusting the output power in all working condition performing both ZVS and ZCS switching to minimize losses. A half bridge induction cooking having dynamic frequency control has been simulated and result has been shown in Fig. 7. The system reaches at resonance very quickly.
Coil and capacitor voltage has been shown in Fig. 8. It clear from the Fig. 7 and Fig. 8 that resonance condition has been obtained with pulse density modulated power control technique.

8. Conclusion
The objective of this paper is to develop a phase locked loop controlled, pulse density modulated DC-AC single phase resonant inverter for induction cooking application. In this paper the study of existed phase locked loop control technique has been done and simulated for the voltage source inverter to operate at resonance frequency. This control strategy provides reliable operation of voltage source inverter fed resonant circuit for varying load and it is achieved by controlled phase locked loop which provides increase or decrease in frequency corresponding to the phase difference in voltage and current of resonant circuit. The implementation of pulse density modulation has been performed in the inverter near to resonance frequency or natural frequency for all output levels.

References
[1] Cui Y. L., He K., Fan, Z. W., & Fan H. L. 2005, August, Study on DSP-based PLL-controlled superaudio induction heating power supply simulation in International Conference on Machine Learning and Cybernetics IEEE, Vol. 2, pp. 1082-1087.
[2] Wang, Y., & Cao, F. 2008, December. Induction heating power supply temperature control based on a novel fuzzy controller, in International Conference on Computer and Electrical Engineering IEEE, pp. 615-618.
[3] Han, W., Chau, K. T., & Lam, W. H., 2019, All-utensil domestic induction heating system in Energy Conversion and Management, 195, pp. 1035-1043.
[4] Peng, Y., Xu, J., & Li, Y., 2008, October, Modeling and simulation of an improved PLL-controlled circuit for series resonant inverter, in International Conference on Electrical Machines and Systems IEEE, pp. 1786-1788.
[5] Fujita, H., & Akagi, H., 1996, Pulse-density-modulated power control of a 4 kW, 450 kHz voltage-source inverter for induction melting applications, in IEEE transactions on industry applications, 32(2), pp. 279-286.
[6] Fujita, H., & Akagi, H., 1999, Control and performance of a pulse-density-modulated series-resonant inverter for corona discharge processes, in IEEE Transactions on Industry Applications, 35(3), pp. 621-627.
[7] Esteve, V., Sanchis-Kilders, E., Jordán, J., Dede, E. J., Cases, C., Maset, E., & Ferreres, A. 2011, Improving the efficiency of IGBT series-resonant inverters using pulse density modulation, in IEEE transactions on industrial electronics, 58(3), pp. 979-987.
[8] Roy, M., & Sengupta, M. 2017, A commutation strategy for IGBT-based CSI-fed parallel resonant circuit for induction heating application. in Sādhanā, 42(2), pp. 153-161.
[9] Han, W., Chau, K. T., Jiang, C., & Liu, W., 2018, All-metal domestic induction heating using single-frequency double-layer coils, in IEEE Transactions on Magnetics, 54(11), pp. 1-5.
[10] Pham, H. N., Fujita, H., Ozaki, K., & Uchida, N., 2012, Dynamic analysis and control for resonant currents in a zone-control induction heating system, in IEEE Transactions on Power Electronics, 28(3), pp. 1297-1307.