Investigate Dynamic Performance of a New Non-isolated High Step-Up Dc-Dc Quadratic Boost Converter

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Abstract: High step-up dc-dc boost converters are an essential element in many new energy generation technologies such as wind generation system, photovoltaic or solar systems etc. The conventional Dc-Dc converter typically used with high voltage transformation ratio which to increase the cost of magnetic transformer components. Several transformer-less topologies have been failing to achieve a high step-up ratio with a better dynamic performance at lower price and size. In this paper, high voltage gain modules based on new quadratic Dc-Dc boost converter topology. The detail of the structure and perform basic mathematical analysis of the proposed converters are presented. Expressions for the conduction and switching losses of the semiconductors have been derived. The performance of the proposed converter tested using Matlab simulation and laboratory experimental setup where 10V is given as the input voltage and the output voltage of the proposed converter is around 110V attained. The voltage stress across for the proposed converter and traditional quadratic boost converter is 60 volt and 61 volts respectively. The proposed converter has a high voltage gain at the output, and the voltage stress across the switch is lower than the output voltage without working at the extremely duty cycle.

Keywords: Dc-Dc boost converter, low duty cycle, voltage stress, high voltage gain module.

1. Introduction

With the increasing environmental pollution, renewable energy sources such as photovoltaic power generation and fuel cells have been rapidly developed. In the micro-grid, the output voltage of photovoltaic panels (usually between 25 and 45 V) is raised to the grid-connected inverse [1]. The converter design problem becomes more complicated in order to address the design issues of the high-voltage with pre-specified parasitic [2], [3]. For high dc voltage conversion ratio, these converters operate with an extreme value of duty cycle. This operating mode results in increasing the losses associated with the circuit components degrading the efficiency the extreme duty cycle may even cause malfunction of the semiconductor switches due to the very short conduction time [4]. In [5], [6] proposed transformer-less dc-dc converters with large conversion ratios. They also proposed a family of quadratic dc-dc converters which achieve high conversion ratios at high efficiencies with lower switching stresses as compared to classical buck-boost and buck-boost converters. For high voltage and high power applications, these converters would require high voltage valves of series active switches, high voltage capacitors and have no modular
structure. In [7], a comparative theoretical study of three dc-dc topologies shows that the voltage-fed full-bridge converter can be attractive from the energy efficiency point of view. The limitation is that this topology incorporates an isolation transformer and requires snubber capacitors to achieve soft switching and also needs an output inductor which creates high voltage spikes on the diodes of the output bridge. In [8], [9], Introduce a dc-dc step-up converter with the extended cell, but the drawback of this topology consists many semiconductor switches which cause the losses across the switches, and the voltage gain of this topology is not high enough in most application. If we increase the switching frequency to attain the high voltage gain the overall losses of the semiconductor component will increase, and efficiency will decrease. In [10], [11], the dc-dc boost converter with voltage lift cell technics is discussed; the main disadvantage of this kind of boost converter is that the surface of semiconductor switches has high transit current, which causes to increase the conduction losses. In [12]–[14], a step-up dc-dc boost converter with coupling inductors is introduced; the main drawback of these type of boost converters is complicated to design because the adjust the turn ratio of coupling inductors is complex, and the voltage stress across the semiconductor switches is equal to the output voltage. In [15]–[18], a number of an isolated step-up dc-dc boost converter present however isolated types of boost converter can give high voltage gain, but on the other hand the cost of isolated converter is high, and size increased because of transformer; also efficiency of isolated converter is low because transformer losses are much higher as compare to non-isolated converters. Furthermore, using the technique switched-inductors to replace traditional inductors, some non-isolated high step-up converters have been introduced in [19]. Similarly, [20], [21] introduce a switched capacitor techniques can also be utilized in Dc-Dc converter topologies to achieve high voltage gain. In [14], [21]–[23], the traditional dc-dc quadratic boost converter is introduced; however, the main disadvantage of the traditional quadratic boost converter is losses across the semiconductor switch is equal to total voltage gain [24]–[27].

In this paper, a modified topology of the non-isolated Dc-Dc boost converter with high step-up modules is presented. The structure and working method of the proposed converter are presented in detail. Mathematical analysis of the proposed converters was carried out. The proposed topology proved theoretically, and experimental in term of getting high voltage gain and voltage stress across the switch is lower than the output voltage as compared to the traditional quadratic boost converter.

2. Related Work

The most popular and widely used dc-dc converters are the buck, boost, buck-boost converters. The underlying concept of these circuits depends on chopping the input dc voltage with a specific duty cycle to generate a desired output voltage level. The switching frequency is usually maintained at a constant value, and the pulse width (on state duration) is modulated. Fig. 1 shows the Dc-Dc boost converter circuits. This circuits is simple in construction but suffer from limitations preventing their use on high-power and high-voltage applications.

![Fig. 1. The quadratic Boost Converter circuit.](image)

Fig. 1 shows the conventional quadratic boost converter consists one switch, three Diodes \( D_1, D_2, D_0 \), two
capacitors $C_2$, $C_0$ and two inductors $L_1, L_2$. The conventional quadratic boost converter voltage stresses are according to Eq. (1) are equal to the output voltage. However, the disadvantage quadratic boost converter is step-up switching structure not suitable because there are not energy storing elements [28].

$$M = \frac{1}{(1-D)} V_i$$

$$V_{s\text{-Stress}} = V_0$$

Here

$M$: Voltage gain, $D$: Duty cycle, $V_i$: Input Voltage, $V_0$: Output Voltage, $V_{s\text{-stress}}$: Stress on the semiconductor switch.

3. Proposed Method

Fig. 2 shows the proposed dc-dc boost converter with high voltage gain module.

![Proposed converter](image)

3.1. State-I

In state-I when semiconductor switch $S$ (ON), diodes $D_1, D_6,$ and $D_5$ are off mode and diode’s $D_2, D_3$ have remained forward biased. Inductor $L_1$ energized by source voltage which is equal to capacitor $C_2$ voltage, inductor $L_2$ energized from $C_1$ voltage, in this state the series connection of $C_3$ and $C_4$ resulting voltage around $2V_{c2}=C_3+C_4$. Inductor $L_3$ energized by capacitors $C_1$ and $C_2$ respectively. Inductor’s current $L_1, L_2$, and $L_3$ increased by $V_s/L_1, Vc_1/L_2$ and $2V_{c2}-V_0/L_3$ respectively. In this state the proposed converter mathematical equations of derived as follows.

$$V_{L_1} = V_{c_2} = V_s$$

$$V_{L_2} = V_{c_1}$$

$$V_{L_3} = 2V_{c_2}-V_0$$

3.2. State-II

In this state, when the semiconductor switch $S$ remain turned OFF, diodes $D_2$, $D_3$ are reverse biased and $D_1, D_6, D_5$ are in conducting mode. Inductors $L_1, L_2,$ and $L_3$ are in discharging mode and their current fall with a slope of $V_s-Vc_1/L_1, Vc_1+Vc_2/L_2$ and $Vc_3-V_0/L_3$ respectively. In this state voltages equation of $V_{L_1}, V_{L_2}$ and $V_{L_3}$ derived below.

$$V_{L_2} = V_{c_1} = V_s$$

$$V_{L_2} = V_{c_1} + V_{c_2}$$
Fig. 3 shows the steady-state waveform of the proposed converter, where we can easily understand the waveform of ripple current and ripple voltages in each state.

\[ V_{L2} = V_{c3} - V_0 \]  \hspace{1cm} (8)

The proposed topology voltage gain \((M)\) is derived by solving the above Equations (3 to 8) as follows,

\[
M = \frac{2-D+D^2}{(1-D)^2} 
\]  \hspace{1cm} (9)

Eq.(10) obtained for voltage stress across the semiconductor switch \(S\),

\[
V_{S\text{-Stress}} = \frac{V_2 - V_{c2}}{1+D} 
\]  \hspace{1cm} (10)

3.3. \textbf{DC Conversion Ratio}

The proposed topology voltage gain \((M)\) is derived by solving the above Equations (3 to 8) as follows,

\[
M = \frac{2-D+D^2}{(1-D)^2} 
\]  \hspace{1cm} (9)

4. \textbf{Experimental Prototype}

The experimental prototype of the proposed converter is implemented with 110W scaled down a system running on terminal voltages of 10V, 110V. In contrast to iron core inductors, this inductor has low core losses (25 W or 0.5% at full load) for the parameters shown in Table 1. In contrast to air-core inductors, this inductor uses less amount of copper to give the same dc resistance. The inductor has a dc resistance of 15 mΩ and uses Litz wire to minimize the skin and proximity effects. The inductor’s dc resistance contributes to 0.6 % of the converter’s losses at full load. The capacitors used are SCRN245R which has film-paper dielectric. Each capacitor unit has a capacitance of 10 µF and rated for 100A RMS, 6.5 KVA.
Table 1. Parameters of Proposed Converter

| Parameter          | Symbol | Value   |
|--------------------|--------|---------|
| Output Power       | $P_0$  | 110W    |
| Input Voltage      | $V_s$  | 10VDC   |
| Output Voltage     | $V_0$  | 110VDC  |
| Load Resistance    | $R_L$  | 100Ω    |
| Frequency          | $F_S$  | 100kHz  |
| Inductor’s         | $L$    | 200uH   |
| Capacitor’s        | $C$    | 10uF    |
| Duty cycle         | $D$    | 0.6     |

5. Experimental Results and Discussions

The simulation and experimental results of the proposed converter performed according to parameters in Table 1. Proper matching is observed between the experimental waveforms and theoretical ones as depicted in Fig. 4.

Fig. 4. Experimental and simulation results of the proposed converter.
Fig. 4 (a) PWM signal of semiconductor switch S is depicted. Fig. 4 (b) shows the source voltage of the proposed converter, which is 10V. Fig. 4(c) shows the voltage gain of the proposed converter, which is very high and very near according to voltage gain Eq. (9), which verify the advantage of using the new topology compared to the conventional converter. For the same input source voltage, the output voltage was, 10V and 61.25V for the standard quadratic boost converter and proposed topology respectively according to Eq.(1). Fig. 4 (d) shows the waveform of voltage stress across the switch S which is 62.5 volt. Fig. 4 (e, f, g, h) shows the voltage of the capacitor of $V_{C_1}$, $V_{C_2}$, $V_{C_3}$, and $V_{C_4}$ respectively, which are very near 25V, 10V, 72.25V and 72.25V. Thus from experimental results, it is verified that the proposed topology has many advantages over conventional quadratic boost converter, such as from proposed topology we can get high voltage gain without working at extremely duty cycle and voltage stress across the switch in proposed topology is almost half of the output voltages.

Fig. 5 depicted the voltage gain of the proposed converter and conventional quadratic boost converter at a different duty cycle. Where we can easily observe that at any duty cycle, the suggested converter output voltage is almost double as compared to the conventional quadratic boost converter.

Table 2, comparison results carried out at the same input voltage 10VDC is given to all the other five topologies and including the proposed topology, where output voltages are given, where it can be observed that the output voltage of the proposed topology is higher at 110VDC as compare to other output results. In addition, clearly, show that the proposed quadratic boost converter with voltage multiplier cell (VMC) is higher than other modified converters. The output voltages of the proposed converter are 110V, and the output voltage of traditional boost converter is 25V, the conventional quadratic boost converter is 62.5V, boost converter with voltage lift cell is 50V, the modified quadratic boost converter is 31.5V and boost converter with extension module is 35V.

| Topology Name                               | Vs     | V0     | Voltage Gain |
|---------------------------------------------|--------|--------|--------------|
| Proposed topology                           | 10VDC  | 110V   | 11%          |
| Conventional quadratic boost converter[28]  | 10VDC  | 62.5V  | 6.25%        |
| Boost converter with voltage lift cell[22]  | 10VDC  | 50V    | 5%           |
| Boost converter with extension cell[26]     | 10VDC  | 35V    | 3.5%         |
| Three level quadratic boost converter[12]   | 10VDC  | 31.5V  | 3.15%        |
| Traditional boost converter[27]             | 10VDC  | 25V    | 2.5%         |

6. Conclusions

In this paper, a new topology of quadratic boost converter has been proposed for high voltage gain
applications. The proposed converters do not contain isolation transformers or coupled inductor and can be designed for single or double pole dc systems. The converters operate only in DCM with self-current commutation and the potential use of thyristors as active switches. Active switches turn-off at zero voltage, and turn-on at zero current to reduce switching losses. Experimental prototyping was implemented, and it is concluded that the conduction losses are much higher than switching losses and have a significant impact on the efficiency of the proposed converters, this is due to the higher average current in the active switches of the step-up converters. The above combination of features is not available in any other dc-dc converter topologies to date. The proposed topology is beneficial to the renewable energy system, Photovoltaic (PV) system, and so forth.

Conflict of Interest

The authors confirm that there are no known conflicts of interest associated with this publication, and there has been no significant financial support for this work that could have influenced its outcome.

Author Contributions

All authors are equally contributed.

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