Characterization of three phase solid state VAR compensation scheme in three phase pulse width modulation voltage source inverter

Mbunwe Muncho Josephine¹, Ezema Ejiofor Edwin², Ngwu Anene Augustine³, CV Anghel Drugarin⁴, Mohammad Rehan Ajmal⁵ and M Ayaz Ahmad⁶

¹Department of Electrical Engineering, University of Nigeria Nsukka, Nigeria
²Electrical/Electronic Engineering Department, Madonna University, Nigeria
³Enugu State Rural Electrification Board, Nigeria
⁴Department of Electronics and Informatics Engineering “Eftimie Murgu”, University of Resita, Resita, Romania
⁵Department of Biochemistry, Faculty of Science, P.O. Box 741, University of Tabuk, 71491, Saudi Arabia
⁶Physics Department, Faculty of Science, P.O. Box 741, University of Tabuk, 71491, Kingdom of Saudi Arabia

E-mail: muncho.mbulanwe@unn.edu.ng

Abstract. The principle of a three phase solid state VAR compensation (SSVC) system that uses a three-phase pulse width-modulated (PWM) Voltage-Source Inverter (VSI) is presented and analyzed. The proposed SSVC system can compensate for leading and lagging displacement power factor and the PWM is used as a means of reducing the size of reactive components. The significant aspect of the presented VAR compensator is the adjustment of the angle difference between the static fundamental circuit output voltage and the utility supply voltage in order to optimize the alternating current (a.c.) power factor to a non-linear load. The SSVC system is analyzed under self-controlled DC bus voltage operating conditions. Other areas of investigation include the design of SSVC reactive components. The dynamic analysis is carried out in a d-q reference frame to verify the performance of the VAR compensator in terms of speed of response and stability. Analysis and stability plots generated confirm a high performance static VAR compensator. Finely, the findings of present research work were found within good agreement with some other workers.

1. Introduction

The adverse effect of low power factor and its resultant large reactive power on generation, transmission, distribution and consumption of electricity power cannot be overemphasized. This is more prevalent in industrial, commercial and residential areas where most of electrical loads on the mains are mostly inductive in nature like arc welding machines, induction motors [1], [2], fluorescent lightings etc. In such loads, the current lags voltage thereby resulting in low power factor with its attendant large reactive power [3].

In modern day electronics, the use of static power converters in the form of inverters and converters has become prevalent. These static converters are non-linear in nature and thus generate
and inject harmonic current into the utility power mains. These harmonic current causes electromagnetic interferences. The level of injected harmonics being allowed on the utility power mains should not exceed 5% of the distortion of the utility power line sinusoidal wave form [4].

This work examines the dynamic characteristics of a three phase solid state volt-ampere reactive compensator for improving the ac power input to a non-linear load to unity or as close to unity as possible. This scheme equally removes the undesired harmonics on the utility power line. A static VAR compensator (SVC) is a set of electrical devices for providing fast-acting reactive power on high voltage electricity transmission network [5]. The SVCs are part of the Flexible AC transmission system [6] device family, regulating voltage, power factor, harmonics and stabilizing the system.

This proposed VAR compensator will enhance and optimize an existing power network. As the transmission networks of the world tend toward higher power transfers and longer lines, they will be driven to become more efficient to meet rising energy demands [7]. SVCs are typically placed near high and rapidly varying loads, such as arc furnaces, where they can smooth flicker voltage [8]. Static VAR compensators installed at appropriate locations in any network will help in stabilizing weak system [5], minimize line losses, increase power transfer capability and provide greater dynamic voltage control. Improved power factor by the VAR compensator will bring about the following benefits:

- dynamic reactive power compensation
- steady-state and transient stability enhancement
- voltage regulation
- power transfer capacity increase
- three-phase voltage balancing
- reduced transmission losses
- flicker mitigation
- oscillation damping

Generally, static VAR compensation is not done at line voltage; a bank of transformers steps the transmission voltage (for example, 230 kV) down to a much lower level (for example, 9.0 kV) [8]. This arrangement reduces the size and number of components needed in the SVC, although the conductors must be very large to handle the high currents associated with the lower voltage.

2. **Three phase solid state VAR compensation operation**

The three-phase solid-state VAR compensator uses a three-phase Pulse-Width Modulated (PWM) Voltage Source Inverter (VSI). This is shown in Figure 1 [9]. The inverter is connected to the ac mains via a reactor, $X_1$, where the $X_1$, is a first-order low-pass output filter which reduces the harmonic components of currents flowing into the utility grid.

At the dc side of the VAR compensator a dc capacitor is connected if a self-controlled dc bus is used as shown in Figure 1. This capacitor has the function of maintaining a dc voltage free from ripples at the input of the inverter. It also stores reactive power. The solid-state VAR compensator is connected to the load through as second order low-pass filter $X_2$ and $X_C$. 
Figure 1. Solid state VAR Compensator using self-controlled d.c. bus

From Figure 1, a single phase equivalent circuit and the phasor diagram of the VAR compensator at fundamental frequency are as shown in Figures 2 and 3.

Figure 2. Single phase equivalent circuit

Figure 3. Phasor Diagram

In both the above Figures 1 and 2, various symbolic representations were such as followings:

- \( V \) = line-to-neutral voltage of the ac mains
- \( E_1 \) = Fundamental component of the inverter phase-to-neutral ac voltage.
- \( I \) = Fundamental component of the a.c. mains current (inverter output current)
- \( \delta \) = Phase-shift angle between the source voltage, \( V \) and the inverter ac voltage, \( E_1 \).

Further, the apparent power from the a.c. source was determined by mathematical relation given below:

\[
S = V I^* = |V| |I^*| \angle \delta \tag{1}
\]

\[
I^* = \frac{|V| \angle \delta - |E_1| \angle \sigma}{-1X} \tag{2}
\]

\[
S = \frac{VE_1}{X} \sin \delta - j \left( \frac{VE_1}{X} \cos \delta - \frac{V^2}{X} \right) \tag{3}
\]

As can be seen from Figure 1, the load is simultaneously being fed by the inverter and the ac mains. The action of the VAR compensator could be summarized under no-load and load conditions as explained below.
2.1. No-load condition
At no-load condition, the real power supplied by the ac source takes care of the losses of the reactor and the inverter. The inverter fundamental component amplitude output ac voltage, $E_1$, is a function of the d.c. bus voltage, $V_{d.c}$, thus $E_1$ increases or decreases if the capacitor is charged or discharged [10].

2.2. Load condition
On load condition, the real power from the ac mains feeds both the load and the inverter. The VAR compensator responds to the fluctuations in load power consumption by providing extra power required by the load or absorbing excess power from the load. When there is an increase in the load power factor (the load drawing more active power), the inverter transiently supply this extra power requirement by the load. This action discharges the capacitor thereby reducing $E_1$. In compensating for the power factor, the value of $E_1$ has to be made equal in value to the respective value of $V$ by charging the dc capacitor. This is achieved by increasing the phase-shift angle, $\delta$, in order to increase the real power supplied by the ac source which actually charges the capacitor. When the load power factor decreases, the load is consuming less power the compensator absorbs the excess power which is used in charging the capacitor, raising the magnitude of $E_1$. When $\delta$ is reduced, the ac source power is lowered thereby discharging the capacitor and bringing $E_1$ back to the appropriate value.

In summary, real power flows to the compensator when the load power factor is lagging (the load takes less active power) and the compensator supplies real power if load power factor is leading (load needs more active power).

2.3. Pulse width modulation (PWM) switching pattern
By comparing a reference voltage from the ac mains with the generated voltage from the inverter, the gate signal of the three-phase pulse modulator voltage-source inverter (VSI) is generated. The resulting voltage error is then fed into a Proportional-plus-Integral (PI) controller. This error signal is amplified by the controller while at the same time stabilizing the system. The integral controller removes steady-state error caused by voltage and current disturbances. The PI controller output forms the gating signal (switching pattern). This is stored in an EPROM, and is being applied to the solid-state switches continuously. Within a half cycle, the inverter switches are turned on/off several times while the output voltage is being controlled by varying the width of the pulses. Elimination of lower order harmonic component of the inverter output voltage is achieved by Selective Harmonic Elimination (SHE) technique. This is done by selecting the number of pulses per half cycle in the output voltage. With the removal of the low frequency voltage components from the output, the inverter appears like short-circuit to the current harmonics generated by the non-linear load. The current harmonic components are left largely to circulate through the VSI rather than the ac source. The magnitude of the current harmonic flowing into the ac source is being determined by the value of the reactor $X$ and the PWM switching pattern applied to the inverter.

2.4. Phase shift angle control
By adjusting the dc bus voltage through small variation in the amount of real power absorbed by the inverter using the closed loop control (shown in Figure 4), the amplitude of the inverter output voltage is controlled. The phase shift angle increases when the load power factor increase and vice versa. The EPROM is being addressed by the counter and $\delta$ is increased or reduced by adjusting the reset pulse of the counter. From the reference voltage variations, (from ac mains), the control system changes the input voltage of the voltage controlled oscillator, (VCO). The reference voltage changes according to the load power factor fluctuations. In compensating for a variation in power factor, a new value of $\delta$ is needed. By reading the stored switching pattern [11], the VCO provides the correct value for the phase shifting angle $\delta$. 
3. Transient analysis of the VAR compensator

The transient response of the VAR compensator is being determined by the speed of response of the dc capacitor ($V_{d.c.}$) to changes in phase-shift angle $\delta$ [10]. This analysis is based on Figure 3 above which represents the equivalent circuit per phase of the VAR compensator. The following assumptions are made in deriving the mathematical model.

i. The ac source is a balanced, three phase ripple-free voltage.

ii. The equivalent circuit represents only fundamental components of current and voltages.

iii. The delay due to the EPROM reset pulse is negligible in comparison to the system response.

iv. The system is linearized since the variations in the phase shift angle $\Delta \delta$ are small.

R = total equivalent resistance for the compensator losses. If $\delta$ oscillate around a mean value $\delta_0$ between $\delta_0 - \Delta \delta$ and $\delta_0 + \Delta \delta$ with a frequency $\omega_0$ then we get the relation

$$\delta(t) = \delta_{max} \cos(\omega_0 t) = R e[\delta_{max} e^{j\omega_0 t}]$$  \hspace{1cm} (4)

From the equivalent circuit:

$$V(t) - e(t) = R i(t) + \frac{d}{dt}$$ \hspace{1cm} (5)

In d-q axis, the voltage and current oscillations in response to the phase-shift angle, $\delta$ were represented such as:

$$V(t) = R e \left[ (V_d + j V_q) e^{j(\omega_0 t + \Delta \delta)} \right]$$ \hspace{1cm} (6)

$$e(t) = R e \left[ (e_d + j e_q) e^{j(\omega_0 t + \Delta \delta)} \right]$$ \hspace{1cm} (7)

$$i(t) = R e \left[ (i_d + j i_q) e^{j(\omega_0 t + \Delta \delta)} \right]$$ \hspace{1cm} (8)

where $\omega_0 = 2\pi f_0$ and $f_0$ is the ac source frequency.

Further, from equations (4, 5, 6 and 7) we get the following two mathematical relations:

$$\left[(V_d + j V_q) - \left(s_d + j s_q\right)\right] e^{j(\omega_0 t + \Delta \delta)} = R \left(i_d + j i_q\right) e^{j(\omega_0 t + \Delta \delta)} + L \frac{d}{dt} \left(i_d + j i_q\right) e^{j(\omega_0 t + \Delta \delta)}$$ \hspace{1cm} (9)

and

$$L \frac{d^2}{dt^2} \left(i_d + j i_q\right) e^{j(\omega_0 t + \Delta \delta)} = L \left(\frac{d}{dt} \left(i_d + j i_q\right) e^{j(\omega_0 t + \Delta \delta)} \right) + L \left(i_d + j i_q\right) \frac{d^2}{dt^2} e^{j(\omega_0 t + \Delta \delta)}$$ \hspace{1cm} (10)

A small handling of these equations on the application of small disturbance to the variables, neglecting the second order terms and applying Laplace transform, the equation left in matrix form yields.

$$\begin{bmatrix} \Delta V_d - V_{d_0} \Delta \delta \\ \Delta V_q + V_{d_0} \Delta \delta \end{bmatrix} - \begin{bmatrix} \Delta e_d - e_{d_0} \Delta \delta \\ \Delta e_q + e_{d_0} \Delta \delta \end{bmatrix} = \begin{bmatrix} (R + SL) - \omega_0 L \\ \omega_0 L + (R + SL) \end{bmatrix} \times \begin{bmatrix} \Delta i_d - i_{d_0} \Delta \delta \\ \Delta i_q + i_{d_0} \Delta \delta \end{bmatrix}$$ \hspace{1cm} (11)

The derivation of the transfer function of the S.S.V. and the phasor diagram of the perturbed system has been shown in Figure 5.
Some symbolic meanings of the Figure 5 is given as: \( E_1 \) = the reference phasor, \( V \) tends to oscillates about its constant values, \( v_{do} \) and \( v_{qo} \) with amplitudes \( \Delta v_d \), \( \Delta v_q \) and \( \omega_d \) is the frequency. And the phasor diagram has been depicted in Figure 6.

![Figure 5. Generalized phasor diagram of the perturbed system](image)

![Figure 6. A pictorial representation of phasor diagram](image)

Further, we evaluate the following mathematical relations based on above phasor diagram and used it for final calibrations in the present experimental work.

\[
\begin{align*}
V_{d0} &= V \cos \delta \\
-\Delta V_q &= V \Delta \delta \cos \delta \\
V_{q0} &= V \sin \delta \\
\Delta V_d &= V \Delta \delta \sin \delta
\end{align*}
\]

(12) \hspace{1cm} (13) \hspace{1cm} (14) \hspace{1cm} (15)

Placing equations (13) and (14) in (11) and working on them, filtering the steady state current that actually provide the losses of the VAR components since the loses are small and applying Laplace transforms yields equation (16) as the transfer function of the compensator.

\[
\frac{\Delta V_{dc}}{\Delta \delta} = \frac{3k_i q_o (L^3 s^2 + 2RLs + \omega_o^2 L^2 + R^2) + 3k^2 \omega_o LV_{dc0}}{2CL^3 s^3 + 4RCLs^2 + (2\omega_o^2 L^2 C + 2R^2 C + 3k^2 L)s + 3k^2 R}
\]

(16)

4. Simulation of the transient response

Having derived the transfer function of the SSVC, the transient response is verified using chosen values of the parameters shown below. The transient response is verified by applying Bode plots [12], [13].

The parameter values were used as: \( C = 900 \mu \text{F} \); \( L = 25mH \); \( R = 0.5\Omega \); \( V_{dc0} = 120V \); \( i_{qo} = 5A \); \( k = 1 \); \( f_s = 50Hz \).
Figure 7 results when subsequent values of the dc capacitor are used and the roots of the characteristics equation plotted. From the plot, it could be seen that as the value of C increases, the real negative roots approach the imaginary axis ($j\omega$-axis), making the system less stable. The dominant poles are negative equally corresponding to larger constants, the system response falls as the value of C increases. Similarly, the root locus of the system transfer function for subsequent values of the inductor L is shown in Figure 8. Here the real negative roots and the complex-conjugate roots affect the frequency response of the system. These roots both move closer to the ($j\omega$-axis), as the value of L increases. This gives unstable system and decreasing response speed.

![Figure 7. Root locus for various ranges of dc capacitor C](image)

![Figure 8. Root locus for various ranges of Inductor L](image)

5. Conclusions and final remarks

Bode plots were used in carrying out the transient analysis. Using root-locus technique for further analysis revealed that the stability of the SSVC can be enhanced by reduction in the values of the reactive components. The SSVC under review uses Selective Harmonic Elimination (SHE) technique of PWM to minimize low frequency harmonic component of the inverter ac output voltage. This reduces the size, weight and cost of reactive elements. The amount of reactive power that can be transferred from the SSVC system to the ac load is inversely proportional to the size of the ac output filters. Voltage stress across the converter is greatly minimized since the PWM switching pattern is on...
lower switching frequencies. This enables the converter to deliver higher levels of output power. This leads to improved efficiency. In the process of power factor displacement compensation, fast, accurate and continuous VAR control is achieved without computation of the required reactive power. Since the PWM switching patterns are stored in an EPROM, logic and hardware design are highly simplified. Current surges and resonances from peripheral low-frequency current sources are avoided. With the overview of the SSVC above, it is capable of ensuring amongst others, the function of VAR compensators on power system which are dynamic reactive power compensation, Steady-state and transient stability enhancement, Voltage regulation, Power transfer capacity increase, three-phase voltage balancing, reduced transmission losses, Flicker mitigation and Oscillation damping.

Acknowledgements
All the authors would like to highly acknowledge the keen support and help in video/digital presentation of articles in the International Conference on Applied Sciences (ICAS2020) during May20-22, 2020, at Hunedoara, Romania. Really it was great privilege and honor to all of us to get an opportunity of online presentation during this COVID19 pandemic all over the world. And a special thanks to Professor Ludovic Dan Lemle, on the behalf of the Organizing Committee (ICAS2020).

References
[1] Kyeong-Hwa Kim, Myung-Joong Youn 2002 Performance comparison of PWM inverter and variable DC link inverter schemes for high-speed sensorless control of BLDC motor, Electronics Letters 38(21) 1294-1295 http://dx.doi.org/10.1049/el:20020848
[2] Kolahdooz A, Shakeri M 2010 A new BLDC motor for propulsion application, International Review of Electrical Engineering (IREE) 5(5) 1872-1878
[3] ***Tel-ATrain 1987 A Study guide to Applied Electricity”, Tel-A-Train, Inc.
[4] Weedy B M 1987 Electric Power System, JohnWiley & sons
[5] Deb Anjan K 2000 Power Line Ampacity System, CRC Press, pp 169-171
[6] Song Y H and Johns A T 1999 Flexible AC transmission systems, IEEE Press, London
[7] Ryan H M 2001 High voltage Engineering and Testing, IET pp160-161
[8] Arrillaga J and Watson N R 2003 Power system Harmonics, Wiley, p126
[9] Benjamin C Kuo and Farid Golnaraghi 2003 Automatic Control System, John Wiley & Sons, Inc.
[10] Rashid Mohammed H 1993 Power Electronic – circuits, Devices, and Application, Prentice Hall
[11] Hyun-Lark Do and Sin-Woo Lee 2014 Two-Switch CRM Resonant DC-DC Converter with Soft-Switching Operation, International Review of Electrical Engineering (IREE) 9(4) 681
[12] Yoshisihiko Sumi, Yoshinobu Harumoto, Taizo Hasegawa, Masao Yano, Kazuo Ikeda and Toshiaki Matsura 1981 New Static VAR control Using Force Commutated Inverter, IEEE Transactions on Power Apparatus and Systems 100(9) 4224
[13] Mbunwe M J, M Ayaz Ahmad and Mustaf S K 2020 An effective energy saving design strategy to maximize the use of electricity, Journal of Mathematical and Computational Science 10(5) 1808-1833