ACCELERATING THE SpMV KERNEL ON STANDARD CPUs BY EXPLOITING THE PARTIALLY DIAGONAL STRUCTURES

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ABSTRACT

Sparse Matrix Vector multiplication (SpMV) is one of basic building blocks in scientific computing, and acceleration of SpMV has been continuously required. In this research, we aim for accelerating SpMV on recent CPUs for sparse matrices that have a specific sparsity structure, namely a diagonally structured sparsity pattern. We focus a hybrid storage format that combines the DIA and CSR formats, so-called the HDC format. First, we recall the importance of introducing cache blocking techniques into HDC-based SpMV kernels. Next, based on the observation of the cache blocked kernel, we present a modified version of the HDC formats, which we call the M-HDC format, in which partial diagonal structures are expected to be more efficiently picked up. For these SpMV kernels, we theoretically analyze the expected performance improvement based on performance models. Then, we conduct comprehensive experiments on state-of-the-art multi-core CPUs. By the experiments using typical matrices, we clarify the detailed performance characteristics of each SpMV kernel. We also evaluate the performance for matrices appearing in practical applications and demonstrate that our approach can accelerate SpMV for some of them. Through the present paper, we demonstrate the effectiveness of exploiting partial diagonal structures by the M-HDC format as a promising approach to accelerating SpMV on CPUs for a certain kind of practical sparse matrices.

Keywords Sparse Matrix Vector multiplication (SpMV), Sparse Linear Algebra, Diagonally Structured Matrix, Multi-core CPU

1 Introduction

Sparse Matrix Vector multiplication (SpMV), which computes the product of a sparse matrix and a dense vector, is one of basic building blocks in sparse linear algebra algorithms. Numerous algorithms such as those for solving linear systems of equations and eigenvalue problems [Barrett et al., 1994, Saad, 2003], e.g. Krylov subspace methods, repeat the SpMV computations, and its execution time is usually dominant in their overall computational time. This fact has motivated various studies for accelerating the SpMV computation.

Compared with dense matrix vector multiplication, a characteristic technology in SpMV is storage format, i.e. how to store the information of a sparse matrix in a computer. The sparsity of a matrix needs to be exploited to reduce both the memory footprint and arithmetic cost. A straightforward format is the coordinate (COO) format [Saad, 2003], in which the row index, column index, and value of each nonzero element are stored. One of popular formats is the compressed sparse rows (CSR) format [Barrett et al., 1994, Saad, 2003], in which the information of row index is
compressed to reduce the memory footprint. It is worth noting that both the COO and CSR formats can store the information of an any sparse matrix without zero padding, which means the explicit store of zero elements.

The COO and CSR formats have nice versatility, however they are sometimes unsuitable for recent computer architectures, e.g. GPU. In order to exploit the advantages of recent computer architectures, e.g. SIMD, multi-thread, and hierarchical memory system, other storage formats are required. One of familiar formats that are designed for the suitability for the recent computer architectures is the ELLPACK (ELL) format [Kincaid et al., 1989], and its variants, e.g. Sliced ELL [Monakov et al., 2010] and SELL-C-σ [Kreutzer et al., 2014], are also known. As a result of improving the suitability, zero padding is basically needed in these formats.

A sparse matrix appearing in scientific computations often has a not random but structured sparsity pattern derived from its original problem or analytical method, e.g. discretization by FEM or FDM. Although the applicability is limited, assuming a specified sparsity pattern and designing a specialized storage format is a promising approach to accelerating SpMV. Because it is known that some specific sparsity patterns frequently appear in applications, it will be a feasible approach to adaptively select an appropriate format for a target matrix in practical situations [Elafrou et al., 2018].

In the presented research, we focus on the diagonally structured sparsity pattern, which often appears in a sparse matrix derived by the FEM or FDM discretization based on a structured grid; a typical example is a heptadiagonal matrix obtained by the FDM discretization for 3-dimensional Poisson’s equation. Although not fully diagonally structured, partial diagonal structures can be observed in a matrix in such analyses, and the SpMV computation for this kind of matrices has a strong demand in the field of computational science.

As a specialized storage format for matrices with such the sparsity pattern, the diagonal (DIA) format [Saad, 2003] has been already known. Yuan et al. [2010] considered optimizing SpMV using the DIA format and presented approaches to improving a SpMV kernel naively using the DIA format. They introduced a technique of splitting a matrix into the SpMV kernel in order to increase the reusability of the vector data. In addition, an idea of combining the DIA and CSR formats was also presented. A similar approach was reported by Yang et al. [2014], where optimization of SpMV on GPU for quasi-diagonal matrices was considered. A hybrid format that combine the DIA and CSR formats is now familiar as the HDC (Hybrid DIA-CSR) format.

As far as the authors know, only the paper by Yuan et al. [2010] deals with DIA-based SpMV on standard CPUs. This paper indicated the potential of exploiting diagonal structures by the DIA format, however, the following points remain unclear:

- All experiments were carried out in sequential computing on 4-core Intel Xeon and AMD CPU. However, a recent CPU has more cores, and parallel computing is now standard for it; for example, sequential computing often cannot fully use the memory bandwidth.
- There is flexibility in splitting a matrix and combining the DIA and CSR formats. However, their impact on the performance of SpMV has been not clear.
- Speedup over the SpMV kernel using the CSR format was reported for test matrices appearing in practical applications. However, both mechanisms for the speedup and the validity of the obtained speedup have not been fully discussed.

To clarify these points is crucial for using DIA-based SpMV kernels in practical situations.

Our purpose in this research is to make the potential of DIA-based SpMV kernels on recent CPUs more clear. Taking the above unclear points into account, we conduct our research and provide the following contributions:

- We review the characteristics of DIA-based SpMV kernels and recall the importance of introducing cache blocking techniques into them.
- We present a modified version of the HDC format, which we call the M-HDC format, based on the observation of the cache blocked HDC-based SpMV kernel. We expect that the M-HDC format more efficiently picks up partial diagonal structures than the HDC format.
- We conduct theoretical analyses based on performance models, in which the expected performance improvement is theoretically investigated.
- We carry out detailed experiments on state-of-the-art multi-core CPUs using thread parallelized kernels. First, we investigate the performance behavior for typical matrices, so-called stencil matrices, and clarify the detailed characteristics of each SpMV kernel. Next, we report the performance for matrices appearing in practical applications, which are provided in the SuiteSparse Matrix Collection [Davis and Hu, 2011], and establish that there are matrices whose SpMV computation on recent CPUs can be accelerated by employing the M-HDC format.
We show the validity of the experimental results by comparing with the theoretical analyses, which clarifies the mechanisms of obtaining the performance improvement by exploiting partial diagonal structures in SpMV.

Through the present paper, we demonstrate that exploiting partial diagonal structures by the M-HDC format is a promising approach to accelerating SpMV on CPUs for a certain kind of practical sparse matrices.

The rest of the paper is organized as follows: in Section 2 we briefly summarize related work. In Section 3, we review the HDC format and the SpMV kernel based on it, together with the CSR and DIA formats. In Section 4, we consider introducing a cache blocking technique into the HDC-based SpMV kernel and propose the M-HDC format. In Section 5, we construct performance models and theoretically analyze the expected performance improvement by the SpMV kernels based on the HDC and M-HDC formats. In Section 6, we present the results of numerical experiments and discuss them. Finally, we give the conclusion remarks.

2 Related work

Enormous numbers of studies that aim for accelerating SpMV have been conducted. Basic optimization techniques in the days before multi-core CPUs and GPUs became common in scientific computing are summarized by Vuduc [2003]. With the appearance of the GPGPU computing, many attempts for the efficient SpMV computing on GPUs have been reported, such as an early study by Bell and Garland [2009], which spotlighted the suitability of ELLPACK for SpMV on GPU. Because we focus on the SpMV computation on standard CPUs in the present paper, we refer only the recent survey paper by Filippone et al. [2017], in which a detailed list of storage formats for SpMV on GPUs is provided.

As discussed in the paper by Vuduc [2003], one of basic optimization techniques for SpMV on CPU is blocking. It aims for increasing the reusability of data in memory [Im et al., 2004, Mellor-Crummey and Garvin, 2004, Nishtala et al., 2007] and reducing the amount of data transfer [Pinar and Heath, 1999, Vuduc and Moon, 2005]. It was reported by Vuduc and Moon [2005] that sparse matrices in practical applications often have block sub-structures, and thus these blocking techniques has been regarded as one of important and basic optimization techniques.

After multi-core CPUs and SIMD architectures became common, optimization techniques for parallelization, especially the SIMD vectorization, have attracted research interests. We can find studies for early hardware in Williams et al. [2009] and Liu et al. [2013]. For the efficient use of SIMD units, more suitable formats for SIMD than CSR were proposed, such as SELL-C-[sigma] [Kreutzer et al., 2014], CVR [Xie et al., 2018], and CCF [Almasri and Abu-Sufah, 2020], and improvement for the traditional CSR format to exploit SIMD units was also studied [Liu and Vinter, 2015, Bian et al., 2020]. Another important issue in SpMV on multi-core CPUs is load balancing as reported by Ohshima et al. [2014], and a solution for this issue was studied in Merrill and Garland [2016]. This issue generally becomes more difficult in symmetric SpMV, and some techniques were presented by Muro et al. [2019] and Elafrou et al. [2019].

In this research, we focus the DIA format, which itself is one of well-known formats explained in textbooks such as Saad [2003]. As mentioned in Section 1, the paper by Yuan et al. [2010] presented optimization techniques based on the DIA format, and several important points still remain unclear. Yang et al. [2014] also reported the similar approach for SpMV on GPUs. In the paper by Godwin et al. [2012], an optimization technique for SpMV on GPUs by exploiting block diagonal structures was discussed.

Recently, a library for SpMV, named SparseX, was presented by Elafrou et al. [2018], in which a storage format is adaptively optimized depending on an input matrix. The basic idea in this approach is appropriately selecting blocking techniques for each input matrix, which is based on their early studies [Karakasis et al., 2009, 2013]. It is also worth noting that the Intel MKL library now provides so-called inspector-executor sparse BLAS routines [Fedorov, 2020], in which the structure of an input matrix is first analyzed to optimize the SpMV kernel. These trends in the development of numerical libraries indicate that adaptive approaches become promising for accelerating SpMV, and the demand of preparing specialized optimization techniques for sparse matrices that have typical structures increases. Our research results contribute to the more efficient use of diagonal structures in these adaptive-type numerical libraries.

3 The HDC format

In this section, we first give brief reviews on the CSR and DIA formats, together with standard implementations of the SpMV kernels using them. Then, we explain a hybrid storage format combining the DIA and CSR formats, namely the HDC format, and the SpMV kernel using it.
3.1 Preliminary

Let

- $A$: an $n \times n$ general (nonsymmetric) real sparse matrix,
- $x$: an $n$ dimensional real vector (input),
- $y$: an $n$ dimensional real vector (output),

and consider computing SpMV:

$$y = Ax.$$ 

We denote the number of the nonzero elements in a matrix as $N_{nz}$. We use $i$ and $j$ as the indexes of the row and column in a matrix (and related loop indices in a pseudo-code), respectively. We use a sparse matrix in Figure 1 for demonstrating how a matrix is stored in each storage format, which we call Example matrix throughout this paper. We present a pseudo-code of a SpMV kernel in the C language style with thread parallelization and SIMD vectorization using OpenMP directives. Corresponding to this, we employ the zero-based indexing for both arrays and elements in a matrix (i.e. row and column indexes).

3.2 The CSR format

The CSR (Compressed Sparse Row) format [Barrett et al., 1994, Saad, 2003], also known as the CRS (Compressed Row Storage) format, is one of standard storage formats in sparse matrix computations. The CSR format is applicable to a sparse matrix that has an any sparse pattern. The CSR format consists of three arrays: $\text{val}[]$, $\text{col\_ind}[]$, and $\text{row\_ptr}[]$. From the first row ($i = 0$) to the last row ($i = n - 1$), the value and column index of nonzero elements are continuously stored in $\text{val}[]$ and $\text{col\_ind}[]$, respectively. The row partition information (the leading index in $\text{val}[]$ and $\text{col\_ind}[]$ for each row) is stored in $\text{row\_ptr}[]$ together with $N_{nz}$ stored in the last (i.e. $n$-th) position. Figure 2 shows how Example matrix is stored in the CSR format.

Figure 3 presents a standard implementation of the SpMV kernel using the CSR format, which we call the CSR kernel hereafter. Here, in the innermost loop (i.e. the loop on $k$), the vector $x$ (the array $x[]$) is accessed via the array $\text{col\_ind}[]$, which is so-called indirect access.

3.3 The DIA format

The DIA (DIAgonal) format [Saad, 2003] is a storage format that focuses on diagonally structured sparse matrices. For each element in a matrix, let

$$\text{offset} := i - j,$$

and define a diagonal line as a set of elements that have a same offset. We call a diagonal line nonzero if it has at least one nonzero element. The DIA format consists of two arrays: $\text{val}[] []$ and $\text{offset}[]$. All of the values including
#pragma omp parallel for private(i, k, s)
for (i = 0; i < n; i++) {
    s = 0;
    #pragma omp simd reduction(+:s)
    for (k = row_ptr[i]; k < row_ptr[i+1]; k++) {
        s += val[k] * x[col_ind[k]];
    }
    y[i] = s;
}

Figure 3: The CSR kernel: a SpMV kernel using the CSR format.

val[0][][]
0 0 0 0 0 0 0 0 0
val[1][][]
0 0 0 0 11 0 16 19
val[2][][]
1 4 7 10 12 14 17 20
val[3][][]
2 5 8 0 13 15 0 0
val[4][][]
3 6 9 0 0 0 0 0

Figure 4: An example of the DIA format: Example matrix is stored in the DIA format.

#pragma omp parallel private(i, k, off, is, ie)
{
    #pragma omp for simd
    for (i = 0; i < n; i++)
    y[i] = 0;

    for (k = 0; k < n_diags; k++)
    {  
        off = offset[k];
        is = max(0, -off);
        ie = min(n, n-off);
        #pragma omp for simd
        for (i = is; i < ie; i++)
        {  
            y[i] += val[k][i] * x[i+off];
        }
    }
}

Figure 5: The DIA kernel: a SpMV kernel using the DIA format.

zero(s) in each nonzero diagonal line are continuously stored in val[][], and their offset are stored in offset[]. Figure 4 demonstrates how Example matrix is stored in the DIA format; Example matrix has five nonzero diagonal lines, and its k-th nonzero diagonal line’s values and offset are stored in val[k][] and col_offset[k], respectively.

Figure 5 gives a pseudo-code of the SpMV kernel using the DIA format (the DIA kernel), where n_diags is the number of nonzero diagonal lines. Since the value of off does not change in the innermost loop (i.e. the loop on i), the array x[] is sequentially accessed in the manner of direct access. Compared with indirect access, this is a preferable feature in terms of the memory access. In addition, if the number of zero elements explicitly stored in the nonzero diagonal lines is sufficiently small, the DIA format is superior to the CSR format in terms of the memory access cost; the memory access cost of offset[] in the DIA format is much smaller than that of col_ind[] in the CSR format. However, if the nonzero diagonal lines contain a large number of zero elements, which means that a sparse matrix is far from diagonally structured, both the computation and memory access cost are increased by explicitly stored zero elements.
3.4 The HDC format

In practical applications, we often deal with sparse matrices that are not fully diagonally structured. However, some of those matrices have partial diagonal structures, and combining the DIA and CSR format might provide better SpMV performance than simply using the CSR format. This is the reason why we consider the HDC (Hybrid DIA-CSR) format [Yang et al., 2014].

The fundamental idea behind the HDC format is storing only nonzero diagonal lines that have sufficient number of nonzero elements in the DIA format and storing other nonzero elements in the CSR format. There are several rules of selecting nonzero diagonal lines to store in the DIA format, and in this paper, we employ the following rule: let \( N_{nz}^{(d)} \) be the number of the nonzero elements in the diagonal line whose offset is \( d \) \((-n + 1 \leq d \leq n - 1)\), then we store a diagonal line in the DIA format if

\[
\frac{N_{nz}^{(d)}}{n} \geq \theta,
\]

where \( \theta (0 \leq \theta \leq 1) \) is a threshold that is given by a user.

The HDC format consists of the arrays in both the DIA format (\( \text{dia}\_\text{val}[][], \text{dia}\_\text{offset}[] \)) and the CSR format (\( \text{csr}\_\text{val}[], \text{csr}\_\text{col}\_\text{ind}[], \text{csr}\_\text{row}\_\text{ptr}[] \)). Figure 6 shows an application of the HDC format to Example matrix, and Figure 7 illustrates how it is stored in the HDC format. In this example, we set \( \theta = 0.6 \), and two diagonal lines whose number of nonzero elements is larger than 4.8 (= 8 \times 0.6) are stored in the DIA format. Compared with the example shown in Figure 4, the number of explicitly stored zero elements is reduced in Figure 7.

Figure 8 outlines the SpMV kernel using the HDC format, which we call the HDC kernel. This is just a combination of the SpMV computation using the CSR format (the first part) and that using the DIA format (the second part).

4 Cache blocking for HDC-based SpMV

In this section, we introduce a cache blocking technique into the SpMV kernel using the HDC format. Next, we propose a modified version of the HDC format that is more suitable for cache blocking. The modified format is expected to more efficiently pick out partial diagonal structures than the HDC format.
4.1 Motivation

In the SpMV computation, the memory access cost for the input and output vectors is not negligible because $N_{nz} = cn \ll n^2$, where $c$ is a small number. It is well know that the data of the matrix cannot be reused in the matrix-vector multiplication (whichever a matrix is dense or sparse), but the data of the vectors can be reused. Therefore, we analyze the memory access patterns for the vectors in the SpMV kernel using each storage format.

First, we consider the SpMV kernel using the CSR format. Figure 3 clearly shows that the memory access for the vector $y$ has a good temporal locality (Figure 9 (a)), and as the result, only one write is required for each element of $y$ by using a register. On the other hand, the locality of the memory access for the vector $x$ depends on the sparse pattern of the matrix $A$.

Next, we consider the SpMV kernel using the DIA format. From Figure 5, we can find that the temporal locality of the memory access for both the vectors $x$ and $y$ is relatively low. If $n$ is sufficient large, it is difficult to efficiently use the cache memory; for each element of $y$ (and $x$), we need the access to the main memory $n_{diags}$ times (Figure 9 (b)).

Compared with the SpMV kernel using the CSR format, the SpMV kernel using the DIA format has the following advantages:

- direct access to the the data of vector $x$,
- less memory access cost, i.e. almost no access cost to the array that stores the index information such as $\text{col}\_\text{ind}[]$ in the CSR format.

However, the following issues are expected:

- inefficient memory access to the vectors when $n$ is sufficiently large,
- additional cost (both in computation and memory access) for explicitly stored zero elements.

In order to overcome the first issue, we introduce a cache blocking technique into the SpMV kernel using the DIA format.
4.2 A cache blocking technique for SpMV using the HDC format

We consider improving the cache efficiency in the memory access for \( y \) in the SpMV kernel using the DIA format. Since the memory access pattern for \( x \) depends on the sparse pattern of \( A \), we here discuss only the memory access for \( y \).

In order to increase the temporal locality of the memory access for \( y \), we partition the rows into blocks and execute the SpMV computation block by block. Hereafter, we denote the block width as \( bl \) and assume that \( n \) can be divided by \( bl \) for the simplicity. This technique is illustrated in Figure 10. By setting an appropriate \( bl \), the data of \( y \) can remain on the cache memory through their related SpMV computation. On the other hand, this technique has a drawback that the memory access cost for \( \text{offset}[] \) increases; roughly \( n/bl \) times as many as the case without the cache blocking technique. The pseudo-code of the cache blocked SpMV kernel using the DIA format is shown in Figure 12 (the B-DIA kernel).

Then, we discuss cache blocking techniques for SpMV using the HDC format. Although a straightforward way is simply applying the above technique to the DIA-related part in SpMV using the HDC format, we employ an aggressive cache blocking technique, as illustrated in Figure 11. In our technique, we combine the computation in SpVM using the CSR format and that in the DIA format so as to further improve the temporal locality of the memory access for \( y \). For each block, we first execute SpMV using the CSR format and then do that using the DIA format. Figure 13 gives the pseudo-code of the SpMV kernel using the HDC format with the cache blocking technique (the B-HDC kernel), where \( n_{\text{blocks}} \) is the number of blocks (i.e. \( n_{\text{blocks}} = n/bl \)).
1 #pragma omp parallel for private(ib, i, k, off, is, ie)
2 for(ib = 0; ib < n_blocks; ib++) {
3  #pragma omp simd
4   for(i = ib*bl; i < (ib+1)*bl; i++) {
5      y[i] = 0;
6   }
7
8   for(k = 0; k < n_diags; k++) {
9      off = dia_offset[k];
10     is = max(ib*bl, −off);
11     ie = min((ib+1)*bl, n−off);
12     #pragma omp simd
13     for(i = is; i < ie; i++) {
14        y[i] += dia_val[k][i] * x[i+off];
15     }
16  }
17 }

Figure 12: The B-DIA kernel: a cache blocked SpMV kernel using the DIA format.

1 #pragma omp parallel for private(ib, i, k, s, off, is, ie)
2 for(ib = 0; ib < n_blocks; ib++) {
3  //SpMV using the CSR format
4   for(i = ib*bl; i < (ib+1)*bl; i++) {
5      s = 0;
6      #pragma omp simd reduction(+:s)
7      for(k = csr_row_ptr[i]; k < csr_row_ptr[i+1]; k++) {
8         s += csr_val[k] * x[csr_col_ind[k]];
9      }
10     y[i] = s;
11  }
12
13  //SpMV using the DIA format
14  for(k = 0; k < n_diags; k++) {
15     off = dia_offset[k];
16     is = max(ib*bl, −off);
17     ie = min((ib+1)*bl, n−off);
18     #pragma omp simd
19     for(i = is; i < ie; i++) {
20        y[i] += dia_val[k][i] * x[i+off];
21     }
22  }

Figure 13: The B-HDC kernel: a cache blocked SpMV kernel using the HDC format.

4.3 The modified HDC format

Taking the cache blocking technique described in the previous subsection into account, we modify the HDC format, which we call the M-HDC format. Since the computation is performed block by block in the cache blocked SpMV computation using the HDC format, it seems to be natural to select elements to store in the DIA format for each block rather than for a whole matrix.

We call a set of elements that belong to a same diagonal line and a same block partial diagonal line, and define \( \tilde{N}_{nz}^{(d,ib)} \) as the number of nonzero elements in the partial diagonal block whose offset is \( d \) and that belongs to the \( ib \)-th block. Then, we store a partial diagonal line in the DIA format if

\[
\frac{\tilde{N}_{nz}^{(d,ib)}}{\text{bl}} \geq \theta.
\]
Figure 14: Selected diagonal lines in the application of the M-HDC format to Example matrix \((bl = 4)\): underlined elements are stored in the DIA format.

\[
\begin{pmatrix}
1 & 0 & 2 & 0 & 0 & 3 & 0 & 0 \\
0 & 4 & 0 & 5 & 0 & 0 & 6 & 0 \\
0 & 0 & 7 & 0 & 8 & 0 & 0 & 9 \\
0 & 0 & 0 & 10 & 0 & 0 & 0 & 0 \\
11 & 0 & 0 & 0 & 12 & 0 & 13 & 0 \\
0 & 0 & 0 & 0 & 14 & 0 & 15 & 0 \\
0 & 0 & 16 & 0 & 0 & 0 & 17 & 0 \\
18 & 0 & 0 & 19 & 0 & 0 & 0 & 20
\end{pmatrix}
\]

Figure 15: An example of the M-HDC format \((bl = 4)\): Example matrix is stored in the M-HDC format.

\[
\begin{array}{l}
dia_{\text{val}}[0][] \quad 1 \quad 4 \quad 7 \quad 10 \\
dia_{\text{val}}[1][] \quad 2 \quad 5 \quad 8 \quad 0 \\
dia_{\text{val}}[2][] \quad 3 \quad 6 \quad 9 \quad 0 \\
dia_{\text{val}}[3][] \quad 11 \quad 0 \quad 16 \quad 19 \\
dia_{\text{val}}[4][] \quad 12 \quad 14 \quad 17 \quad 20 \\
dia_{\text{col}}_{\text{offset}}[] \quad 0 \quad 2 \quad 5 \quad -4 \quad 0 \\
dia_{\text{ptr}}[] \quad 0 \quad 3 \quad 5 \\
csr_{\text{val}}[] \quad 13 \quad 15 \quad 18 \\
csr_{\text{col}}_{\text{ind}}[] \quad 6 \quad 7 \quad 0 \\
csr_{\text{row}}_{\text{ptr}}[] \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 2 \quad 2 \quad 3
\end{array}
\]

Figure 16 presents the pseudo-code of the SpMV kernel using the M-HDC format, which we call the M-HDC kernel. Compared with the B-HDC kernel, the rage of \(k\) for accessing \(dia_{\text{val}}[k][]\) slightly changes; the range is obtained via \(dia_{\text{ptr}}[]\) instead of 0 through \(n_{\text{diags}}\). The memory access pattern for \(y\) in the M-HDC kernel is essentially the same as that in the the B-HDC kernel excepting the effect by the differences in the selection of (partial) diagonal lines, and the M-HDC format is expected to more efficiently exploit partial diagonal structures in a matrix than the original HDC format; it might store more nonzero elements and less zero elements in the DIA part. Therefore, for certain sparse matrices, the M-HDC kernel is expected to provide higher performance than the other SpMV kernels already mentioned in this paper.

5 Analysis based on performance models

In this section, we provide a theoretical analysis based on performance models. Our objective here is to show the efficiency of the cache blocking technique introduced into the SpMV kernels using the DIA format. We first give a preliminary for performance modeling. Next, supposing that an input matrix is ideal for the DIA format, namely so-called stencil matrices, we analyze the performance of the SpMV kernel using the DIA format in the cases with and without the cache blocking technique. Finally, for a general matrices, we analyze the performance of the cache blocked SpMV kernel using the HDC format and that using the M-HDC format.

5.1 Preliminary

According to the paper by [Kreutzer et al., 2014], we construct performance models for SpMV kernels in the following approach. Let \(P^*\) be the performance (i.e. Flop/s) of a SpMV kernel (* represents the kernel’s name), and \(T^*\) be the
#pragma omp parallel for private(ib, i, k, s, off, is, ie)
for(ib = 0; ib < n_blocks; ib++) {
    // SpMV using the CSR format
    for(i = ib*bl; i < (ib+1)*bl; i++) {
        s = 0;
        #pragma omp simd reduction(+:s)
        for(k = csr_row_ptr[i]; k < csr_row_ptr[i+1]; k++) {
            s += csr_val[k] * x[csr_col_ind[k]];
        }
        y[i] = s;
    }
}

// SpMV using the DIA format
for(k = dia_ptr[ib]; k < dia_ptr[ib+1]; k++) {
    off = dia_offset[k];
    is = max(ib*bl, −off);
    ie = min((ib+1)*bl, n−off);
    #pragma omp simd
    for(i = is; i < ie; i++) {
        y[i] += dia_val[k][i] * x[i+off];
    }
}

Figure 16: The M-HDC kernel: a SpMV kernel using the M-HDC format.

execution time (i.e. sec) of the kernel. Then, we define

\[ P(*) = \frac{2N_{nz}}{T(*)} . \]

(1)

In this analysis, we focus the case that an input matrix is sufficiently large, that is, the whole data of the matrix and vectors in SpMV cannot be accommodated in the cache memory. Accordingly, we assume that the execution time of SpMV is determined by the amount of data transferred from/to the main memory. Letting \( V(*) \) be the amount (i.e. byte) of the data, we write

\[ T(*) = \frac{V(*)}{w_{mem}} , \]

(2)

where \( w_{mem} \) is the effective bandwidth (i.e. byte/s) of the main memory. We assume that \( w_{mem} \) does not depend on SpMV kernels. In this modeling, we ignore the latency in the main memory access and all of the cost in the data movement from/to the cache memory.

From Equations 1 and 2, we can obtain the relative performance, i.e. the speedup, of the kernel A over B as

\[ \frac{P(A)}{P(B)} = \frac{T(B)}{T(A)} = \frac{V(B)}{V(A)} = 1 + \frac{V(B) - V(A)}{V(A)} . \]

(3)

Now, we explain how to model \( V(*) \) for each SpMV kernel. We break down \( V(*) \) as

\[ V(*) = V_A(*) + V_x(*) + V_y(*) , \]

(4)

where \( V_A(*) \), \( V_x(*) \), and \( V_y(*) \) are the amount of the data corresponding to the matrix \( A \), the right-hand side vector \( x \), and the left-side vector \( y \), respectively. Since the data of \( A \) and \( y \) are continuously accessed in all kernels, \( V_A(*) \) and \( V_y(*) \) are obtained by simply counting the number of the data access. On the other hand, the data access for \( x \) is generally discontinuous in the CSR kernel but continuous in the DIA kernel. Hence, \( V_x(*) \) need to be carefully modeled.

5.2 Analysis for stencil matrices

First, we analyze the performance in an ideal case for the DIA format, precisely, the case where an input matrix is perfectly diagonally structured. We consider a matrix appearing in the finite difference analysis, which is so-called
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stencil matrix. For the simplicity, we assume that all elements in \( N_{\text{diag}} \in \mathbb{N} \) diagonal lines are nonzero but other elements are zero, which implies

\[
N_{nz} \simeq N_{\text{diag}} n.
\]

5.2.1 Model for the CSR kernel

From Figure 3, we can write

\[
V_A^{(CSR)} \simeq b_{fp}N_{nz} + b_{int}N_{nz} + b_{int}n,
\]

\[
\simeq b_{fp}(N_{\text{diag}} + bN_{\text{diag}} + bn),
\]

\[
V_x^{(CSR)} \simeq b_{fp} \gamma^{(CSR)} N_{nz}
\]

\[
\simeq b_{fp} \gamma^{(CSR)} N_{\text{diag}} n,
\]

\[
V_y^{(CSR)} \simeq b_{fp} n,
\]

where \( b_{fp} \) and \( b_{int} \) are the data size for a floating point number and an integer number, respectively, and \( b \) is their ratio:

\[
b := \frac{b_{int}}{b_{fp}}.
\]

For example, \( b_{fp} = 8 \) in FP64 (double precision), and \( b_{int} = 4 \) in INT32.

In the above modeling of \( V_A^{(CSR)} \), we introduce \( \gamma^{(CSR)} \) as a parameter that represents the effect of the cache memory in the access for \( x \). \( \gamma^{(CSR)} \) belongs to the range of

\[
1 \geq \gamma^{(CSR)} \geq \frac{n}{N_{nz}} \simeq \frac{1}{N_{\text{diag}}}.
\]

Here, \( \gamma^{(CSR)} = 1 \) means the worst situation, in which the main memory is accessed every time, and \( \gamma^{(CSR)} \simeq 1/N_{\text{diag}} \) means the best situation, in which each element of \( x \) is loaded only once from the main memory (and from the cache memory in other times). On a current processor, all of the data in the same cache line is ordinarily together loaded from the main memory, and discontinuous access thus tends to cause an excess transfer due to unnecessary data in the same cache line. We need to take this into account when modeling \( V_x^{(CSR)} \) for a general sparse matrix, however it is ignorable under the assumption with stencil matrices; the next element of an element of \( x \) is used in the calculation for the next row.

5.2.2 Model for the DIA kernel

Under the assumption that \( n \) is sufficient large, we presume every access to \( x \) and \( y \) require the data transfer from/to the main memory in the DIA kernel. Thus, from Figure 5, we can write

\[
V_A^{(DIA)} \simeq b_{fp}N_{\text{diag}} n,
\]

\[
V_x^{(DIA)} \simeq b_{fp}N_{\text{diag}} n,
\]

\[
V_y^{(DIA)} \simeq b_{fp}\left( \frac{1}{y[i]=0} + 2N_{\text{diag}} \right) n.
\]

5.2.3 Model for the B-DIA kernel

With an appropriate block length, we suppose that only the final result of \( y \) is stored to the main memory; all of the intermediate results are loaded from (or stored to) the cache memory. The cache hit rate in loading \( x \) is also expected to be improved, which is modeled in the same way as in the CSR kernel, with the parameter \( \gamma^{(B-DIA)} \). Taking these considerations into account, from Figure 12 we can write

\[
V_A^{(B-DIA)} \simeq b_{fp}N_{\text{diag}} n,
\]

\[
V_x^{(B-DIA)} \simeq b_{fp}\gamma^{(B-DIA)} N_{\text{diag}} n,
\]

\[
V_y^{(B-DIA)} \simeq b_{fp} n,
\]

where

\[
1 \geq \gamma^{(B-DIA)} \geq \frac{1}{N_{\text{diag}}}.
\]
5.2.4 Comparison between the DIA and CSR kernels

We have

\[
\frac{V_{(CSR)} - V_{(DIA)}}{V_{(DIA)}} \simeq \frac{b(N_{\text{diag}} + 1) - (3 - \gamma_{(CSR)})N_{\text{diag}}}{4N_{\text{diag}} + 1}.
\]  

(9)

From Equation 7 and \(N_{\text{diag}} \geq 1\), we can bound

\[
\frac{2b}{5} \geq \frac{b(N_{\text{diag}} + 1)}{4N_{\text{diag}} + 1},
\]

(10)

and

\[
\frac{(3 - \gamma_{(CSR)})N_{\text{diag}}}{4N_{\text{diag}} + 1} \geq \frac{2}{5}.
\]

(11)

Thus, from Equation 3, we can obtain

\[
\frac{3 + 2b}{5} \geq \frac{P_{(DIA)}}{P_{(CSR)}}.
\]

(12)

Generally, we can assume

\[b_{fp} \geq b_{int} \iff 1 \geq b,
\]

(13)

and under this assumption, we have

\[1 \geq \frac{P_{(DIA)}}{P_{(CSR)}}.
\]

(14)

This result indicates that the DIA kernel (i.e. straightforward use of the DIA format in SpMV) cannot provide the performance improvement over the CSR kernel even if the input matrix is ideal for the DIA format.

The first term in the numerator in Equation 9 represents the positive effect in the DIA kernel; no array (excepting the small array offset []) is necessary for storing the position of the nonzero elements of \(A\) in the DIA format. On the other hand, the second term represents the negative effect; the data of \(x\) and \(y\) need to be moved from/to the main memory much more than in the CSR kernel. The result in Equation 14 tells us that the negative effect is usually larger than the positive effect.

5.2.5 Comparison between the B-DIA and CSR kernels

We first consider the difference between \(\gamma_{(CSR)}\) and \(\gamma_{(B-DIA)}\). Regardless the B-DIA or CSR kernel, the cache hit rate in the access for \(x\) is high if diagonal lines are close to each other, and low if far from. From this fact, we assume that the rate depends only on the sparse pattern (i.e. the position of each diagonal lines), which implies

\[\gamma_{(CSR)} \simeq \gamma_{(B-DIA)} \simeq \gamma, \quad 1 \geq \gamma \gtrsim \frac{1}{N_{\text{diag}}}.\]

(15)

Then, we compare the B-DIA kernel with the CSR kernel; we have

\[
\frac{V_{(CSR)} - V_{(B-DIA)}}{V_{(B-DIA)}} \simeq \frac{b(N_{\text{diag}} + 1) + (\gamma_{(CSR)} - \gamma_{(B-DIA)})N_{\text{diag}}}{(1 + \gamma_{(B-DIA)})N_{\text{diag}} + 1} \simeq \frac{b(N_{\text{diag}} + 1)}{(1 + \gamma)N_{\text{diag}} + 1}.
\]

(16)

From Equation 15 and \(N_{\text{diag}} \geq 1\), we can bound

\[b \geq \frac{b(N_{\text{diag}} + 1)}{(1 + \gamma)N_{\text{diag}} + 1} > \frac{b}{2}.
\]

(17)

Thus, we can obtain

\[1 + b \gtrsim \frac{P_{(B-DIA)}}{P_{(CSR)}} \gtrsim 1 + \frac{b}{2}.
\]

(18)

This result assures that the B-DIA kernel provides a speedup over the CSR kernel; the speedup increases as \(b\) becomes large.

Comparing Equation 16 with 9, only the positive effect provided by the DIA format remains; the negative effect in the DIA kernel is removed by the cache blocking technique introduced in the B-DIA kernel.
5.2.6 Comparison between the B-DIA and DIA kernels

We also compare the B-DIA kernel with the DIA kernel; we have

\[
\frac{V^{(DIA)} - V^{(B-DIA)}}{V^{(B-DIA)}} \simeq \frac{(3 - \gamma^{(B-DIA)})N_{\text{diag}}}{(1 + \gamma^{(B-DIA)})N_{\text{diag}} + 1}.
\]

(19)

From Equation 8 and \(N_{\text{diag}} \geq 1\), we can bound

\[
3 > \frac{(3 - \gamma^{(B-DIA)})N_{\text{diag}}}{(1 + \gamma^{(B-DIA)})N_{\text{diag}} + 1} \geq \frac{2}{3},
\]

(20)

and we can obtain

\[
4 \simeq \frac{P^{(B-DIA)}}{P^{(DIA)}} \simeq \frac{5}{3}.
\]

(21)

This result clearly shows the impact of the cache blocking technique in the B-DIA kernel.

5.3 Analysis for general matrices

Next, we analyze the performance of the B-HDC and M-HDC kernels for general matrices. Hereafter, we denote the average of the number of nonzero elements per row as

\[
c := \frac{N_{\text{nz}}}{n},
\]

(22)

5.3.1 Model for the B-HDC kernel

Let \(\beta\) be the rate of the nonzero elements still stored in the CSR part in the HDC format, which we call the CSR rate. We define the filling rate of the DIA part as

\[
\alpha := \frac{(1 - \beta)N_{\text{nz}}}{N_{\text{diag}} n} = \frac{(1 - \beta)c}{N_{\text{diag}}},
\]

(23)

where \(N_{\text{diag}}\) is the number of diagonal lines in the DIA part.

Then, we can write

\[
V^{(B-HDC)}_A \simeq b_{\text{fp}} \beta N_{\text{nz}} + b_{\text{int}} \beta N_{\text{nz}} + b_{\text{int}} n + b_{\text{fp}} N_{\text{diag}} n
\]

\[
= b_{\text{fp}} \left( \beta(c + bc) + b + \frac{(1 - \beta)c}{\alpha} \right) n.
\]

(24)

Since modeling \(V^{(*)}_x\) is difficult for a general matrix, we simply write

\[
V^{(CSR)}_x \simeq b_{\text{fp}} v_x n,
\]

(25)

and

\[
V^{(B-HDC)}_x \simeq b_{\text{fp}} (v_x + \Delta v_x) n, \quad \Delta v_x \geq 0,
\]

(26)

where \(\Delta v_x\) represents the difference from the CSR kernel. The reason why we assume \(\Delta v_x \geq 0\) is that additional access will be required in the B-HDC kernel due to the zero elements explicitly stored in the DIA part. On the other hand, we can write

\[
V^{(B-HDC)}_y \simeq b_{\text{fp}} n.
\]

(27)

5.3.2 Comparison between the B-HDC and CSR kernels

Our target here is deriving the upper bound of the performance improvement of the B-HDC kernel over the CSR kernel. In this situation, letting \(\Delta v_x = 0\) (for the simplicity) is acceptable. Then, we have

\[
\frac{V^{(CSR)} - V^{(B-HDC)}}{V^{(B-HDC)}} \simeq \frac{b(1 - \beta)c - (1 - \beta) \left( \frac{1}{\alpha} - 1 \right) c}{\beta(c + bc) + b + \frac{(1 - \beta)c}{\alpha} + v_x + 1}.
\]

(28)
Since $v_x \geq 1$, $\alpha \leq 1$, and $\beta \geq 0$, we can bound

$$b > \frac{b(1 - \beta)c - (1 - \beta)\left(\frac{1}{\alpha} - 1\right)c}{\beta(c + bc) + b + \frac{(1 - \beta)c}{\alpha} + v_x + 1},$$

(29)

where the upper bound is obtained when $v_x = 1$, $\alpha = 1$, $\beta = 0$, and $c \to \infty$. Finally, we have

$$1 + b > \frac{P(B-HDC)}{P(CSR)}.$$

(30)

This result is consistent with the upper bound in Equation [18].

We give an interpretation for Equation 28; the first term in the numerator represents the amount of the reduced index data in the CSR part in the HDC format, and the second term represents the amount of additionally required value data (for zero elements in diagonal lines) in the DIA part of the HDC format. From Equation 28, we can find that

$$b(1 - \beta)c \geq (1 - \beta)\left(\frac{1}{\alpha} - 1\right)c \iff \alpha \geq \frac{1}{b + 1}$$

(31)

is required for the efficient use of the B-HDC kernel; for example, if we use FP64 and INT32,

$$\alpha \geq \frac{1}{2 + 1} = \frac{2}{3}$$

(32)

is required.

5.3.3 Model for the M-HDC kernel

Now, we consider the M-HDC kernel. Let $\tilde{\beta}$ be the CSR rate in the M-HDC format. Instead of $\alpha$ in the B-HDC kernel, we introduce the average filling rate as

$$\tilde{\alpha} := \frac{(1 - \tilde{\beta})N_{nz}}{n_{b}} = \frac{(1 - \tilde{\beta})cn}{\sum_{ib=0}^{n_{b}} N_{diag}^{(ib)} b_l},$$

(33)

where $n_{b} (= n/bl)$ and $N_{diag}^{(ib)}$ are the number of row blocks and the number of diagonal lines in the $ib$-th row block, respectively. Then, we can write

$$V_{A}^{(M-HDC)} \simeq b_{fp} \beta N_{nz} + b_{int} \beta N_{nz} + b_{int} n + b_{fp} \sum_{ib=0}^{n_{b}} N_{diag}^{(ib)} b_l$$

$$= b_{fp} \left(\beta(c + bc) + b + \frac{(1 - \tilde{\beta})c}{\tilde{\alpha}}\right)n.$$

(34)

As well as in the case of the B-HDC kernel, we write

$$V_{x}^{(M-HDC)} \simeq b_{fp}(v_x + \Delta\tilde{v}_x)n, \quad \Delta\tilde{v}_x \geq 0,$$

(35)

where $\Delta\tilde{v}_x$ is the difference from the CSR kernel. We also write

$$V_{y}^{(M-HDC)} \simeq b_{fp} n.$$

(36)

5.3.4 Comparison between the M-HDC and CSR kernels

The only difference between the B-HDC and M-HDC kernels is the definition of the filling rate and the CSR rate. Therefore, by replacing $\alpha$ and $\beta$ in the B-HDC kernel with $\tilde{\alpha}$ and $\tilde{\beta}$, respectively, we can obtain the same results for the M-HDC kernel as for the B-HDC kernel.

We expect that the M-HDC format more efficiently picks up partial diagonal structures, which means $\tilde{\alpha} > \alpha$ (less zero elements in the DIA part) and $\tilde{\beta} < \beta$ (more nonzero elements in the DIA part). From Equation 28, we can observe that the performance improvement over the CSR kernel becomes larger in this situation, which indicates the superiority of the M-HDC kernel to the B-HDC kernel.
Figure 17: Estimated upper bound of the speedup of the B-HDC (or M-HDC) kernel over the CSR kernel based on the performance models, which is calculated by Equation 28.

5.3.5 Examples

Using Equation 28, we demonstrate $P(B\text{-HDC})/P(\text{CSR})$ (or $P(M\text{-HDC})/P(\text{CSR})$). We set $v_x = 1$ and $c = N_{nz}/n = 10, 50, 100$, and the calculated results are shown in Figure 17. Since there is no essential difference between $\alpha$ and $\tilde{\alpha}$ and between $\beta$ and $\tilde{\beta}$, we hereafter do not distinguish between them and describe $\alpha$ and $\beta$ for the simplicity. From Figure 17, for significant speedup (e.g. $1.1 \times$ speedup), both sufficient small $\beta$ (e.g. $\beta \leq 0.5$) and large $\alpha$ (e.g. $\alpha \geq 0.8$) are required. On the other hand, $c$ makes almost no differences; the theoretical upper bound is 1.5, and it is almost achieved when $c = 50$.

6 Experimental results

In this section, we report the experimental results. Our goal here is evaluating the effectiveness of the cache blocking techniques, namely the B-DIA, B-HDC, and M-HDC kernels, on recent multi-core CPUs. First, we explain the experimental settings including the computational environments and report the effective memory performance. Next, we presents the results for stencil matrices, which correspond to the analysis in Section 5.2. Finally, we show the results for general matrices.

6.1 Settings

6.1.1 Computational environments

We used a single computational node of three different supercomputer systems, each of which equips multi-core CPUs with different microarchitectures: Intel Broadwell, Skylake, and Cascade Lake. The specifications of these environments are listed in Table 1. In every environment, we occupied a node during our program execution, which means that programs by other users did not run on the node at the same time. We assigned a thread per core; we used totally 36 cores on Broadwell, 40 cores on Skylake, and 56 cores on Cascade Lake. In all environments, we set the thread affinity compact.

6.1.2 Implementation

We implemented the following SpMV kernels:

- the CSR kernel (Figure 3),
- the DIA kernel (Figure 5),
- the B-DIA kernel (Figure 12),
- the HDC kernel (Figure 8),
- the B-HDC kernel (Figure 13),
- the M-HDC kernel (Figure 16).

Programs of all kernels were written in C language and thread parallelized using OpenMP. FP64 (double precision) and INT32 were used in the programs.
Table 1: Specifications of the computational environments used in the performance evaluation.

| Notation in this paper | Broadwell | Skylake | Cascade Lake |
|------------------------|-----------|---------|--------------|
| System name            | Laurel 2  | Grand Chariot | Oakbridge-CX |
| Site                   | Kyoto Univ., Japan | Hokkaido Univ., Japan | The Univ. of Tokyo, Japan |
| CPU                    | Xeon E5-2695 v4 | Xeon Gold 6148 | Xeon Platinum 8280 |
| Microarchitecture      | Broadwell | Skylake | Cascade Lake |
| Frequency              | 2.10GHz   | 2.4GHz | 2.7GHz |
| #cores                 | 18        | 20    | 28 |
| L1 cache size (data)   | 32KB/core | 32KB/core | 32KB/core |
| L2 cache size          | 256KB/core | 1MB/core | 1MB/core |
| L3 cache size          | 2.5MB/core | 1.375MB/core | 1.375MB/core |
| Node                   |           |        |            |
| #CPUs                  | 2         | 2      | 2           |
| Memory size            | 128GB     | 384GB  | 192GB       |
| Peak FLOPS             | 1.21TFLOPS | 3.07TFLOPS | 4.84 TFLOPS |
| Peak Memory BW         | 153.6GB/s | 255.9GB/s | 275.0GB/s |

Software

| Compiler               | icc 18.0.5 | icc 19.0.5.281 | icc 19.0.5.281 |
| Math Library           | MKL 2018.0.4 | MKL 2019.0.5 | MKL 2019.0.5 |

1 for(loop = 0; loop < n_loops; loop++){
  2    t0 = omp_get_wtime();
  3    for(ite = 0; ite < n_ites; ite++){
  4        kernel(...);
  5    }
  6    t1 = omp_get_wtime();
  7    time = (t1 − t0)/n_ites;
  8    save_timing_result(time, ...);
  9 }

Figure 18: The outline of how to measure the execution time of a kernel.

Programs were compiled by the Intel compiler (icc), whose version in each environment is listed in Table 1 with the following options:

- Broadwell: -O3 -qopenmp -xHost -no-vec -no-simd
- Skylake: -O3 -qopenmp -xCORE-AVX512 -no-vect -no-simd
- Cascade Lake: -O3 -qopenmp -xCORE-AVX512 -no-vec -no-simd

We prepared two routines for each kernel: with the SIMD vectorization and without the SIMD vectorization. A routine with the SIMD vectorization was generated by using the OpenMP directive (i.e. omp_simd), where some loops (for details, see the pseudo-code of each kernel) were explicitly vectorized by the directive. Otherwise, loops were not vectorized because compiler’s vectorization was prevented by the options (-no-vec -no-simd).

6.1.3 Timing

We used omp_get_wtime for timing. The execution time of a kernel was measured in the manner shown in Figure 18 measuring the execution time for repeating a kernel n_ites times, and calculating the average time for a single kernel execution. The above measurement was conducted n_loops times, and the best result was chosen to be evaluate.

6.2 Benchmark on the memory performance

Since SpMV kernels are memory bound, it is worth understanding the effective memory performance in recent multicore systems. We prepared two kernels that measured the effective memory performance: a kernel with only direct indexing (Figure 19 we call direct) and a kernel with indirect indexing (Figure 20 we call indirect). Here, arrays A[], B[], and C[] were FP64, and I[] was INT32. Since I[I] = i, the access pattern to the array C[] was not changed in the kernel with indirect indexing.
```c
#pragma omp parallel for simd private(i)
for(i = 0; i < N; i++) {
    C[i] += A[i] * B[i];
}
```

Figure 19: Memory benchmark kernel only with direct indexing.

```c
#pragma omp parallel for simd private(i)
for(i = 0; i < N; i++) {
    C[i] += A[i] * B[I[i]]; // I[i] = i
}
```

Figure 20: Memory benchmark kernel with indirect indexing.

![Graphs showing memory performance comparison](image)

Figure 21: Effective memory performance: comparison between the direct and indirect indexing, and between with and without the SIMD vectorization.

We measured the execution time of these two kernels for various array size (i.e. $N$); the execution time was measured in the same manner as for SpMV kernels (see Figure 18). We set $n_{ites} = 1,000$ and $n_{loops} = 20$. The performance of each kernel was calculated as

$$ (\text{bytes/s}) = \frac{MN}{\text{(execution time)}}, $$

where $M = 32$ (3 loads and 1 store for 8 byte data) in the direct kernel, and $M = 36$ (additional 1 load for 4 byte integer data).

The obtained results are presented in Figure 21. Here, in each environment, we compare four kernels: direct with SIMD, direct without SIMD, indirect with SIMD, and indirect without SIMD. From the graphs, we obtain the following important observations:

- When $N$ is sufficiently large, i.e. the total data amount is larger than the size of the cache memory, there is no difference in the performance between among the four kernels.
- If $N$ is not large, the SIMD vectorization makes a remarkable performance increase for the direct kernels but little for the indirect kernels.
- As already known, the performance and its behavior are drastically different between the cases that $N$ is sufficiently large (i.e. the out-of-cache case) and not large (i.e. the in-cache case).

### 6.3 Experiments for stencil matrices

With stencil matrices, we evaluated the performance of the CSR, DIA, and B-DIA kernels; this part corresponds to the analysis in Section 5.2. We prepared the following three types of stencil matrices: given the matrix size $n$,

- **1D-3Point stencil matrix**: $a_{ij} \neq 0$ if $j = i, i \pm 1$.
- **2D-5Point stencil matrix**: $a_{ij} \neq 0$ if $j = i, i \pm 1, i \pm n_x$, where $n_x := \lfloor \sqrt{n} \rfloor$.
- **3D-7Point stencil matrix**: $a_{ij} \neq 0$ if $j = i, i \pm 1, i \pm n_x, i \pm n_x^2$, where $n_x := \lfloor \sqrt[3]{n} \rfloor$.

We generated test matrices with various $n \in [1 \times 10^4, 5 \times 10^7]$, and measured the performance of the kernels under the settings $n_{ites} = 1,000$ and $n_{loops} = 20$. 

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The obtained results are presented in Figure 22. From the graphs, we have the following observations:

- When $n$ is sufficiently large (i.e., the out-of-cache case), there is no difference between with and without the SIMD vectorization. In this case, the B-DIA kernel outperforms the CSR kernel, but the DIA kernel underperforms. These results are consistent with the theoretical analysis in Section 5.2. The obtained performance differences are due to the differences in the amount of the data access cost to the main memory.
- When $n$ is not large (i.e., the in-cache case), whether with or without the SIMD vectorization makes a remarkable performance difference for the DIA and B-DIA kernels but almost no difference for the CSR kernel. This is easily expected from the memory performance presented in the previous section; the DIA and B-DIA kernels have no indirect indexing, but the CSR kernel has it. Additionally, the CSR kernel is less suitable for the SIMD vectorization because its most inner loop is usually really short. In this case, the B-DIA kernel (with SIMD) outperforms other kernels. However, the performance of each kernel more fluctuates than that in the out-of-cache case, and more careful investigation is needed.

Now, we compare the obtained performance differences among the CSR, DIA, and B-DIA kernels (with the SIMD vectorization). In Figure 23, we present the obtained relative performance for $n = 5 \times 10^7$ together with their estimation from Equations 9, 16, and 19. In the estimation, we set $\gamma = \gamma^{(\text{CSR})} = \gamma^{(\text{B-DIA})}$ $1/3 (N_{\text{diag}} = 3, 1D-3Point)$, $1/5 (N_{\text{diag}} = 5, 2D-5Point)$, and $3/7 (N_{\text{diag}} = 7, 3D-7Point)$. When $N_{\text{diag}} = 7$, the two diagonal lines with offset $\pm n^2$ are far from the other diagonal lines, and their corresponding elements of $x$ are expected to be loaded from the main memory. This is the reason why $\gamma = 3/7$ when $N_{\text{diag}} = 7$. From the graphs, we can find that the obtained relative performance are almost equivalent among the three environments. In addition, the obtained results are basically close to the estimation, which supports the reasonability of the analysis in Section 5.2.

Finally, we investigate the relationship between the performance of the B-DIA kernel and the block width $bl$. For the case of $n = 1 \times 10^7$, we show the performance of the B-DIA kernel with each $bl$ in Figure 24 together with the performance of the DIA kernel. From the graphs, we can find the effect of the cache blocking technique excepting the cases that the block width is too small (roughly $n < 10$) or too large ($n > 10^4$). In all environments and for all matrices, block width around $bl = 5000$ provides the highest performance, however sensitive optimization is not necessarily required as the graphs show; in the range of $10 \leq bl \leq 10^4$, significant performance differences are not observed.

### 6.4 Experiments for matrices in practical applications

We next conduct experiments using matrices provided in the SuiteSparse Matrix Collection [Davis and Hu 2011], which represent the characteristics of practical applications. Using such matrices, we confirm the importance of the cache blocking techniques employed in the B-HDC kernel and the potential of the M-HDC kernel for SpMV with matrices appearing in practical applications.

#### 6.4.1 Matrix selection and experimental settings

As test matrices, from the SuiteSparse Matrix Collection, we selected 20 matrices that are nonsingular, real, unsymmetric, large (in terms of $N_{nz}$), and not derived from graph problems. Since our main interest is to examine the out-of-cache performance of each kernels, we selected large matrices. In this research, we have more interests in computational science or engineering problems, e.g., matrices derived from the FDM or FEM discretization, than graph problems. This is why we imposed the last condition. Table 2 lists the information of the selected matrices.

We performed four kernels: the CSR, HDC, B-HDC, and M-HDC kernels. For all kernels, the SIMD vectorization was applied. In the HDC, B-HDC, and M-HDC kernels, we set their parameters as follows:

- $\theta = 0.5, 0.6, 0.7, 0.8, 0.9$
- $bl = 10, 50, 100, 500, 1000, 5000, 10000$

We measured the execution time in the way described in Section 6.1.3 and set $n_{\text{loops}} = 20$ and $n_{\text{ites}} = 1000$.

#### 6.4.2 Overall results

As the baseline, we give the performance (Flop/s) of the CSR kernel in each environment (Figure 25). The results shown in Figure 25 are both the performance itself and the correlation of performance among three environments, seem to be consistent with the the theoretical memory performance (Table 1) and the effective memory performance (Figure 21).
Figure 22: Measured performance of the CSR, DIA, and B-DIA kernels for stencil matrices.

Figure 23: Performance comparison for stencil matrices with $n = 5 \times 10^7$. 

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Figure 24: Relationship between the performance of the B-DIA kernel and the block width for stencil matrices with \( n = 1 \times 10^7 \).

Table 2: Matrices selected from the SuiteSparse Matrix Collection as test matrices for the experiments.

| No. | Matrix name         | \( N_{nz} \)   | \( n \)   | \( N_{nz}/n \) | Kind                                      |
|-----|---------------------|----------------|----------|----------------|-------------------------------------------|
| 1   | HV15R               | 283,073,458    | 2,017,169| 140            | Computational fluid dynamics problem      |
| 2   | vas_stokes_4M       | 131,577,616    | 4,382,246| 30             | Semiconductor process problem             |
| 3   | ML_Geer             | 110,879,972    | 1,504,002| 74             | Structural problem                        |
| 4   | vas_stokes_2M       | 65,129,037     | 2,146,677| 30             | Semiconductor process problem             |
| 5   | nv2                 | 52,728,362     | 1,453,908| 36             | Semiconductor device problem              |
| 6   | dgreen              | 38,259,877     | 1,200,611| 32             | Semiconductor device problem              |
| 7   | RM07R               | 37,464,962     | 381,689  | 98             | Computational fluid dynamics problem      |
| 8   | vas_stokes_1M       | 34,767,207     | 1,090,664| 32             | Semiconductor process problem             |
| 9   | ss                  | 34,753,577     | 1,652,680| 21             | Semiconductor process problem             |
| 10  | ML_Laplace          | 27,689,972     | 377,002  | 73             | Structural problem                        |
| 11  | FullChip            | 26,621,990     | 2,987,012| 9              | Circuit simulation problem                |
| 12  | Transport           | 23,500,731     | 1,602,111| 15             | Structural problem                        |
| 13  | CoupCons3D          | 22,322,336     | 416,800  | 54             | Structural problem                        |
| 14  | rajat31             | 20,316,253     | 4,690,002| 4              | Circuit simulation problem                |
| 15  | circuit5M_dc        | 19,194,193     | 3,523,317| 5              | Circuit simulation problem                |
| 16  | Freescale1          | 18,920,347     | 3,428,755| 6              | Circuit simulation problem                |
| 17  | TSOPF_RS_b2383      | 16,171,169     | 38,120   | 424            | Power network problem                     |
| 18  | memchip             | 14,810,202     | 2,707,524| 5              | Semiconductor device problem              |
| 19  | test1               | 12,968,200     | 392,908  | 33             | Semiconductor device problem              |
| 20  | ohne2               | 11,063,545     | 181,343  | 61             | Semiconductor device problem              |

Then, we present the relative performance (i.e., speedup) of the HDC, B-HDC, and M-HDC kernels over the CSR kernel in Figure 26. For discussing the results in Figure 26, we also give Figure 27 which illustrates the CSR rate in each kernel when \( \theta = 0.5 \). From Figures 26 and 27, we have the following observations:
Figure 26: Relative performance of the HDC, B-HDC, and M-HDC kernels over the CSR kernel for the test matrices selected from the SuiteSparse Matrix Collection.

- Matrix #12: almost all the nonzero elements are stored in the DIA format. This is why the performance of the B-HDC and M-HHC kernels for this matrix stands out among all the test matrices. This result most clearly shows the effectiveness of the cache blocking technique; the B-HDC kernel outperforms the HDC kernel, especially on Broadwell and Cascade Lake.

- Matrices #5, #6, #11, and #19: more than the 90% nonzero elements are still stored in the CSR format in both the HDC (B-HDC) and M-HDC kernels. Thus, in terms of the whole performance of SpMV for these matrices, there are almost no differences among three kernels.

- Matrices #1, #3, #10, #13, #14, and #17: there is a sufficient gap in the CSR rate between the HDC and M-HDC kernels, which means that the M-HDC kernel can pick up partial diagonal structures but the HDC
A P

Figure 27: The CSR rate in the HDC (or B-HDC) and M-HDC kernels for the test matrices selected from the SuiteSparse Matrix Collection.

and B-HDC kernels cannot. For these matrices, we can find a significant performance improvement of the M-HDC kernel over the B-HDC kernel.

- Other matrices: since the CSR rate of the HDC and M-HDC kernels are not small, the performance differences among three kernels are not noteworthy, however we can find the tendency that the B-HDC kernel is better than the HDC kernel, and that the M-HDC kernel is superior to the B-HDC kernel.

From these experimental results, we confirm the effectiveness of the cache blocking technique employed in the B-HDC kernel and the potential of the M-HDC kernel; among 20 test matrices derived from practical applications, we can find matrices that the M-HDC kernel advantageously works for.

6.4.3 Detailed analysis for representative matrices

Now, we report detailed analyses for matrices #1, #3, #10, #13, #14, and #17, which well represent the characteristics of the M-HDC kernel.

First, in Figure 28, we give the relationship of the filling rate \( \alpha \), the CSR rate \( \beta \), and the performance to the parameters \( bl \) and \( \theta \), together with the best parameter setting in each situation (matrix and environment). From Figure 28, we have the following observations:

- The filling rate: \( \alpha \geq \theta \) is assured in theory, and high \( \alpha \) is obtained in practice even when \( \theta \) is not large, e.g. when \( \theta = 0.6 \), the obtained \( \alpha \) is roughly higher than 0.8 in almost all the cases. We can also find that \( bl \) has little effect on \( \alpha \).

- The CSR rate: we can find a clear impact of \( bl \) and/or \( \theta \) on \( \beta \); i.e. both in #3, #10, and #13, mainly \( bl \) in #14 and #17, and mainly \( \theta \) in #1. The tendency that smaller \( bl \) and/or \( \theta \) bring lower \( \beta \) can be observed, which is easily expected.

- Performance: the impact of \( bl \) and/or \( \theta \) on the obtained performance can be clearly found, and its main factor seems to be caused by \( \beta \). In the matrix #17, the performance is significantly low when \( bl = 5000 \) and \( 10000 \). This is reasonable because its \( n \) is less than 40000 and only partial threads work using such \( bl \). We can find that \( bl = 50 \) or 100 basically provide (near) the best performance in every environment, although there are a few exceptions. Typically \( bl = 10 \) brings lower \( \beta \) than \( bl = 50 \), however its performance is not the best due to the disadvantage of increasing the memory access of the offset information in the M-HDC kernel.

Next, we confirm the accuracy of the estimation by the performance models explained in Section 5, e.g. the examples shown in Figure 17. Based on Equation 28 with the assumption that \( v_x = 1 \), by substituting the obtained \( \alpha \) and \( \beta \), which are shown in Figure 28 and \( c = N_{nz}/n \), we have an estimation of the relative performance of the M-HDC (or B-HDC) kernel over the CSR kernel, denoted \( RP_{est} \). Then, we compare it with the obtained results, denoted \( RP_{exe} \). We calculate the relative error \( RE \) as

\[
RE := \frac{RP_{est} - RP_{exe}}{RP_{exe}},
\]

and plot them in Figure 29. From Figure 29, we have the following observations:
• When $10 \leq bl \leq 1000$, the accurate estimations are obtained in many cases, i.e. basically $|RE| \leq 0.05$ excepting a few cases. Moreover, basically $RE \leq 0$, and this fact is consistent with our remark that a kind of upper bound is obtained by the models, as mentioned in Section 5.

• We can find the degradation of the accuracy for $bl = 10$ and 5000 (or 10000); the obtained performance is lower than the estimation. As its reasons, we guess the increase of accessing cost to the offset information when $bl = 10$ and the inefficient work of the cache blocking technique when $bl$ is too large.

• The significant large error in Matrix #17 with large $bl$ is due to the inefficient use of threads, as already mentioned in the observation on the Figure 28.

• A tendency that $RE$ becomes large is observed on Cascade Lake, however we currently have not insights for its reasons.

What is important in practical situations is how to set the parameter $bl$ and $\theta$ appropriately. For this matter, based on the observations on Figures 28 and 29, we suggest a policy as follows:

• $bl$ should be selected from $50 \lesssim bl \lesssim 500$. At least, we should avoid too small or too large $bl$.

• $\theta$ has much less impact on the performance than $bl$, and simply setting $\theta = 0.6$ will be acceptable.

• The performance depends mainly on the CSR rate, and calculating it in advance is thus informative. Moreover, for the above range of $bl$, the presented models, i.e. Equation 28 are expected to provide accurate estimations, and we can roughly know the obtained performance in advance.

• Theoretically, $RP$ does not depend on environments, and an optimal setting of $bl$ and $\theta$ do not change. This indicates that we can reuse the knowledge of selecting parameters across different environments.

• If $n$ of a target matrix is not sufficiently large compared with the number of threads, we have to pay additional attention to fully using the threads.

6.4.4 Performance comparison with the MKL routines

Finally, to make the evaluation of the obtained performance more clear, we compare them with routines provided in the Intel MKL library. For matrices #1, #3, #10, #13, #14, and #17, we measured the performance of two MKL routines: the traditional CSR based routine ($mkl_dcsrgemv$) and the Inspector-Executor (IE) routine ($mkl_sparse_d_mv$) [Fedorov, 2020]. In the use of the IE routine, we initially stored a matrix in the 4-array CSR format ($mkl_sparse_d_create_csr$), then set the information of how many times SpMV repeats via $mkl_sparse_set_mv_hint$, and called the optimization function ($mkl_sparse_optimize$), before the execution of SpMV.

In Figure 30 we present the relative performance of the M-HDC kernel (with the best setting of $bl$ and $\theta$), the MKL CSR routine, and the MKL IE routine over the (our in-house) CSR kernel in three environments. From Figure 30 we have the following observations:

• The relative performance of the MKL CSR routine is basically around 1.0, which validates the obtained performance of our CSR kernel. This also means that almost no room of performance optimization for CSR-based SpMV kernels even by a hardware vendor, i.e Intel.

• Excepting matrix #17, the M-HDC kernel outperforms the MKL IE routine. This fact strengthens the potential of the M-HDC kernel.

• For matrix #17, the MKL IE routine shows the remarkable performance, however we currently have no insights on this result due to little open information on the technology in the MKL IE routine.

6.5 Summary of the experiments

We give a brief summary of the experiments as follows:

• Through the experiments with stencil matrices, the effectiveness of using the DIA format with the cache blocking technique (i.e. the B-DIA kernel) was confirmed, and it was totally different in the in-cache and out-of-cache cases; in the in-cache case, the B-DIA kernel provides the better use of the SIMD vectorization, and in the out-of-cache case, it reduces the amount of the memory access cost.

• The experiments using 20 test matrices selected from the SuiteSparse Matrix Collection demonstrated that the cache blocking technique (i.e. the B-HDC kernel) is effective for some matrices appearing in practical applications. Moreover, it was fond that the M-HDC kernel more efficiently works for some matrices than the B-HDC kernel.
• Through the detailed analyses for the representative matrices, we figured out the impact of the parameter $b_l$ and $\theta$ in the M-HDC kernel on the performance and confirmed the accuracy of the estimation by the performance models. We also presented the policy of how to choose the parameters in practical.

• Comparison with the MKL routines, especially the MKL IE routine, also proved the potential of the M-HDC kernel.

Since we compared the B-HDC and M-HDC kernels with the CSR kernel, it is a natural question to ask the comparison with SpMV kernels using ELLPACK type formats. As mentioned above, in the case that a matrix is sufficiently small, i.e., in the in-cache case, the efficiency of the SIMD vectorization is one of vital factors as our experimental results, namely Figure 22 show. For this case, comparison with kernels using ELLPACK type formats is important, which remains as our future work. In contrast to the in-cache case, when a matrix is sufficiently large, i.e., in the out-of-cache case, we can presume that the efficiency of the SIMD vectorization rarely affects the SpMV performance, which is reason we compared with only the CSR kernel in our experiments. Actually, in the papers by [Kreutzer et al., 2014] and [Almasri and Abu-Sufah, 2020], we can find that almost no performance improvement by ELLPACK type kernels over the CSR kernel was obtained for sufficiently large matrices on standard multi-core CPUs. Here, it is worth noting that this tendency differs on many-core CPUs such as Intel Xeon Phi; the effectiveness of SpMV kernels using ELLPACK type formats was reported by [Kreutzer et al., 2014], [Alappat et al., 2020], and [Nakajima et al., 2021].

7 Conclusion

In this research, we considered accelerating the SpMV computation on standard CPUs by exploiting diagonally structured sparsity patterns, which often appear in practical applications. We focused the HDC format, which combines the DIA and CSR formats, and recalled introducing cache blocking techniques into the SpMV kernel using the HDC format. Based on the observation of the cache blocked HDC kernel, we presented a modified version of the HDC format, which we call the M-HDC format, so as to more efficiently pick up partial diagonal structures. We carried out theoretical analyses based on performance models and theoretically provided the expected performance improvement by the B-HDC and M-HDC kernels over the CSR and HDC kernels.

Then, we conducted comprehensive experiments on the state-of-the-art multi-core CPUs. From the experiments using typical matrices, namely stencil matrices, we clarified the detailed performance characteristics of each kernel; it was shown that the impact of the SIMD vectorization on the performance of SpMV totally changes between the in-cache and out-of-cache cases. It is confirmed that the amount of data transferred from/to the main memory is much more crucial than the SIMD vectorization when a matrix is sufficiently large. By the experiments using practical matrices, it was established that there are matrices whose SpMV can be accelerated by exploiting the partial diagonal structures, which is realized by using the M-HDC format. The obtained experimental results were consistent with the theoretical results based on the performance models. This fact supports our approach to exploiting partial diagonal structures by the M-HDC format for accelerating SpMV. Through the present paper, we demonstrated the effectiveness of exploiting partial diagonal structures by the M-HDC format as a promising approach to accelerating SpMV on CPUs for a certain kind of practical sparse matrices.

In addition to the potential of the SpMV kernel using the M-HDC format, an important insight has been also provided. As shown in the experimental results, namely Figure 22, the impact of the SIMD vectorization on the SpMV performance is clearly different between the in-cache and out-of-cache cases. Although many approaches have been recently proposed for the efficient SIMD vectorization on modern CPUs, we should pay attention to the appropriate problem setting to efficiently use them. For substantially large matrices, they may provide little speedup over the CSR kernel on standard CPUs.

A remained important task is involving the presented approach into application programs or numerical libraries. In the case of using application programs, it is better to store a matrix in the M-HDC format directly without converting from other formats. In this case, an efficient implementation to find out partial diagonal structures in a targeted problem such as a discretized model is needed. In the case of introducing into numerical libraries, a matrix is expected to be given in a well-used format such as the CSR format, and the cost for converting to the M-HDC format is one of vital issues. In our research, we did not consider this cost and employed a naive way of finding partial diagonal structures, and developing a way that will be accepted in the practical use of numerical libraries is crucial. It will be also important to appropriately determining whether the M-HDC format should be used or not for a given matrix.

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Figure 28: Relationship to the parameters $b_l$ and $\theta$: the left two show the filling rate ($\alpha$) and the CSR rate ($\beta$), and the right three show the relative performance of the M-HDC and B-HDC kernels over the CSR kernel in three environments, respectively. An ellipse denotes the best case in each situation. As the performance of the B-HDC kernel, the best case among different $b_l$ candidates is presented. It is worth noting that $\alpha$ and $\beta$ do not depend on $b_l$ in the B-HDC kernel, and that the B-HDC kernel is essentially equivalent to the case of setting $b_l = n$ in the M-HDC kernel in terms of $\alpha$ and $\beta$. 

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Figure 29: Accuracy of the estimation by the performance models; let $RP$ be the relative performance of the M-HDC (or B-HDC) kernel over the CSR kernel, $RP_{est}$ and $RP_{exe}$ denote the estimated and obtained values, respectively, and $(RP_{est} - RP_{exe})/RP_{est}$ is plotted in each graph.
Figure 30: Relative performance of the M-HDC kernel, the MKL CSR routine, and the MKL IE routine over the (in-house) CSR kernel; for the M-HDC kernel, the performance by the best setting of $b_l$ and $\theta$ is plotted.