Parametric and topological methods of bulk CMOS IP-blocks yield improvement

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Parametric and topological methods of bulk CMOS IP-blocks yield improvement

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Abstract. This paper presents the study of the main reasons for the yield loss of modern nanometer VLSIs. The methods of the yield improvement are described on the basis of the impact of parametric and catastrophic reasons for its loss.

1. Introduction
Every step down in the rules of CMOS design (lower than 0.35 um) makes the capabilities of the technological process no longer meet the requirements of the scaling laws. The technological process is complicated by the increase in the number of process steps and stronger requirements thereof. The formation of topological structures by photolithographical means becomes more difficult, leading to lithographical distortions, and as a consequence, increases the influence of different topological variations of the design performance. In this regard, there is a trend of product yield loss.

The modern methodology of designing the digital parts of the IP blocks and VLSI is based on digital standard cells libraries. In modern chips the number of such standard cells reaches millions for the entire area of the crystal, so the main VLSI quality parameters are determined by the quality of standard cells libraries as a whole.

The problem of yield decrease is widely reported in literature. Thus, for example, in [1] a method for the statistical analysis of yield is described. In [2] and [3] are proposed the methods to improve the yield only at the system level of designing. The methods described in [4] are effective; however, they do not allow to reach the maximum yield percent within a project.

In this paper, we tried to give a detailed analysis of the main reasons of yield loss and recommended methods of its improvement.

2. The reasons of design yield loss
Generally, factories provide developers with design rules, verified by the research of the test crystals during the technology characterization. After that, the manufacturer guarantees a 99% level yield of the crystal with limited area and difficulties. Therefore, any occurring reasons of defects are considered by the manufacturer as owing to the poor quality of the design. However, even with the proper level of control of technological steps and cleanness of processes in world practice, there are reasons of the yield decrease that are specifically due to non-ideal technology processes [5].

In general, the reasons for yield loss are divided into the following categories:
1. Catastrophic – these represent functional failures and usually occur due to defects such as small particles falling during the polishing or the etching of metals with very high routing density. In such cases there can occur a short circuit (Figure 1), a break in a topological layer, the inability of the contact to form or the possibility for a hidden defect to be produced. The last one appears either during the failure tests, or during the normal operation of the circuit already as part of the equipment, which is much more critical.

![Figure 1. Short circuit between parallel metals](image)

2. Parametric – these represent the parametric mismatch in performance, power consumption or some other parameters of the circuit. The variation of the technological parameters of the transistors, low temperature tolerance and the variation of the supply voltage can have a significant impact on the circuit yield if these effects are not taken into account during the design and if they are the key parameters in the requirements of the circuit. As a rule, modern technological processes guarantee that transistors can work in a wide range of supply voltages and temperatures and that the parameters variation does not exceed ±3σ. However, during manufacturing there are additional variations in topological layers that lead to changes of parasitic structures and hence the whole of the circuit parameters. The variations occur between the crystals on the wafer, between the wafers in one lot and between wafer lots due to the variations of doping profiles, thickness and width of the dielectrics, metal etching features, etc.

It should be noted that both catastrophic and parametric reasons of yield loss may be both random and systematic. For example, the contact defects may occur as a result of the random strikes of particles or the mismatch of photomasks, which lead to systematic defects of the contacts.

Thus, the above-mentioned reasons of yield loss are more relevant for the present development trend of the microelectronics industry. In the development of VLSI for the high reliability applications all possible causes of yield loss should be taken into account and the effects of different variations should be minimized. Otherwise, regardless of the yield loss reasons, the company-developer suffers economic and time costs.

3. Manufacturing yield improvement
One of the most important step in the modern technological process is the use of computational lithography techniques [6]. Such techniques are applied when the minimum size of the structure is less than the wavelength of the exposure light. The most accessible for analysis among them is the correction of optical proximity effect (OPC), as it affects only the image of the topological layer on the photomask. The use of OPC allows to set the right parameters of the structures produced on the wafer, improve the process stability and the crystal yield rate. OPC is based on the use of special masks, which are calculated taking into account the light wave properties in order to achieve higher resolution and lower distortion in the formation of the elements on the wafer at a given wavelength. In Table 1 are presented the types of typical yield loss reasons due to the optical proximity effect.

Each type of the topology defects due to the optical proximity effect in a different rate affects the reliability. Shorts and breaks in the layers have the most negative impact and lead to failures in the circuit functioning. Defective contacts or vias may occur as a result of its insufficient overlay by the corresponding layers, or by the shift of photomasks, or may be struck by microparticles as well as from its burnout by the large current.
| Name                  | Description                                                                 | Illustration |
|-----------------------|-----------------------------------------------------------------------------|---------------|
| Short                 | Topological short circuit                                                   |               |
| Open                  | Layer gap                                                                   |               |
| Insufficient contact  | Insufficient contact or via overlay by metals or poly                       |               |
| Pinch                 | Metal narrowing or widening                                                  |               |
| Edge placement error  | Rounding of structure corners                                               |               |
The last one is the result of bad design of the electromigration rules. The narrowing in the middle of a long wire is a potential place of rupture and the widening can produce shorts when wires are routing parallel in the minimum distance with a high density. Such interconnection defects are caused by the capillary forces acting on resists sides during washing [5]. The yield loss due to the defects in interconnections can also be caused by the unpredictable influence of the parasitic parameters. The variation of the widths of long wires which are parallel can cause a significant change in the side parasitic capacitance which will affect the circuit time parameters. The variations of the time parameters can also be caused by changes in the geometric parameters of the transistors due to the rounding of the topological layers in the U- and L-shaped structures (Table 2).

Thus, the typical distortion of the topological layers can be corrected at the stage of OPC by introducing special topology correction figures [7]. There are three types of correction figures:

1. Change in the nominal layer size by a value of the violation during the photolithography and etching.
2. The introduction of additional lines (assist line) to create the effect of high density structures. The differences in the forming of single and high density structures are the result of the diffraction of light rays on the adjacent layers, so the high density structures are illuminated by larger light density.
3. The introduction of additional figures (serif) or cut-outs on the corners of layers (anti serif) in the rectangular form of to rectify the corners in order to minimize the effects of its rounding.

As a rule, correction figures are introduced in the topology by the manufacturer in automated mode using special software and are aimed at minimizing the causes of catastrophic yield decrease. From the perspective of the influence of the variations, the manufacturer does not know the accuracy requirements of different topology parts. Therefore, the possibility of OPC in improving yield is limited and it is required an additional set of rules and guidelines for the developers to design circuits with taking into account their suitability for mass production. These rules and recommendations are available in some factories. They are based on the analysis of the technology violations during the stages of the manufacturing process. In the world practice this direction of the design is called Design for Manufacturability (DFM).

4. Methods of improvement of yield level
The possibility to achieve the maximum yield value within a given project depends on the quality of the digital and PAD standard cell libraries used in the physical and circuit design synthesis. Therefore, the methods of the yield improvement firstly should be applied on the lowest level of the project abstraction.

During the development of the standard cell libraries and IP blocks we used the following methods to improve the yield:

– the use of the additional set of layout design rules that reduce the risk of short circuits and breaks in the layers, as well as minimize the effects of the structures corners rounding on the geometric parameters of the transistors;
– transistors placement in the same orientation for a better compensation after the masks shifts and other mismatches in the operations of lithography;
– doubling contacts and vias at the place and route step where no hard limitations on the area and traceability, it should be noted that the number of contacts and vias depends on the power of the cell as there are the electromigration requirement;
– the use of methods for calculating precision circuits (like Monte Carlo) with the prediction of the technological parameters variation impact on the timing. Since the calculation of Monte Carlo is rather resource-intensive process, the number of iterations carried out is often limited. In precision circuits we also used transistors with higher width and length to reduce the influence of the relative variation of the transistors geometrical parameters;
– the uniformity of dummies placement to meet the requirements of dummies DRC check. It helps to avoid local layer deformation;
– the power and ground grid optimization – large number of vias, increased metals width and its doubling help to reduce the value of the power and ground buses total resistance and consequently to eliminate its impact on the local supply voltage drops in IP-blocks;
– the antenna effect elimination – during the plasma chemical etching and polishing of the metals the charge is accumulated on the wires, this charge can be the reason of the active elements breakdown or the threshold voltages shifts. When exceeding the specified area of the interconnection limitations in IP-blocks the diodes are placed directly in front of the transistors gates.

Thus, these design methods applied at the level of standard cell libraries and IP-blocks allow to improve the yield of VLSI as a whole achieving a compromise on the basic electrical and geometrical parameters.

At the step of IP-blocks integration as part of VLSI it is also recommended to apply similar methods. To achieve the maximum effect we recommend to provide additional reserves on the setup-hold parameters at the step of the design timing verification. It is necessary because of the inaccuracies occurring during the photomask OPC, and the corresponding errors in the timing characterization of the library cells.

It should be noted that the yield is largely determined by the complexity of the project which depends on the die size, the number of basic cells, IP-blocks and functional content. The simplification of the project can be achieved by the initial HDL-code optimization at the behavioral level. If there are some additional requirements, for example, radiation tolerance, the specialized libraries should be used. It is also required to analyze its structural and topological solutions for the manufacturability and their influence on the design yield.

5. Conclusion
In this work we analyzed the main and the most common reasons of the modern VLSI yield loss as well as the factors that determine the yield, presented the methods of its improve. These methods should be applied at the steps of the circuit and topological synthesis and the project optimization. They are invariant to the level of design rules and can improve not only the yield percentage but the other quality characteristics of the project.

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