Leakage current reduction for a double-leg boost converter by switching transition synchronisation

Matthias Zehelein¹ Ⓒ, Johannes Ruthardt¹, Maximilian Nitzsche¹, Tobias Tymosch¹, Jörg Roth-Stielow¹
¹Institute for Power Electronics and Electrical Drives, University of Stuttgart, Pfaffenwaldring 47, 70569 Stuttgart, Germany
二线城市: matthias.zehelein@ilea.uni-stuttgart.de

Abstract: With wide-bandgap transistors, the leakage current through the parasitic transistor to heat sink capacitance is increased with the operation at higher switching transition voltage slopes. This study presents a modulation synchronisation method for a double-leg boost converter to reduce these leakage currents. Having a similar leakage current path, the transistors turn-on transition of one leg is synchronised on the turn-off transition of the second leg.

1 Introduction

The use of wide-bandgap transistors (e.g. GaN and SiC) in power electronics is spreading. Therefore, the electromagnetic compatibility (EMC) becomes an important issue designing power electronic devices. With increasing voltage slopes at the switching transition, the common-mode leakage current of the device rises. These transistors demand an advanced electrical and thermal design, which reduces parasitic inductances and saves volume but increases parasitic capacitances to ground, when using a compact and efficient heat sink setup.

The usual approach for reducing the leakage current is to use electromagnetic interference (EMI) filter stages. However, with higher voltage slew rates, the predominating leakage current harmonics become highly frequent. Therefore, one solution is to use more expensive materials for components in the passive filters.

There are already various approaches for active EMI suppression in the literature (e.g. [1, 2]). Most of them are based on a closed-loop control principle using an amplifier to damp the leakage currents and to improve the EMC [3]. This principle can be flexibly used in many applications. However, its performance depends on the sensing, feedback, and amplification circuit’s bandwidth. In [4], the bandwidth of the active EMI filter reached up to 5 MHz, and Wang et al. [5] proposed a hybrid filter to also damp frequencies above the cutoff frequency of the active filter at ~3 MHz.

To overcome this drawback, Biskoping et al. [6] presented a method to use the gate circuit for current injection in order to cancel out the EMI emitted by the switching transitions. This approach uses an additional filter for the inverse current generation which is also critical relating to parameter variations.

This paper investigates the reduction of the leakage current with an active switching transition synchronisation of a boost converter with two half-bridge legs for the use in a photovoltaic (PV) inverter. Especially, in PV inverters, the ground leakage current is a relevant parameter for the operation safety and has to meet the requirements for EMC.

Fig. 1 depicts a single-phase PV inverter, which usually consists of two basic components [7]. A boost converter provides a wide input voltage range for a flexible PV module configuration and maximum power point tracking. The inverter converts direct current into alternating current. In this paper, the boost converter and its leakage current caused by switching transitions are in the focus of investigation.

2 Boost-converter setup

2.1 Converter topology

Fig. 2 shows the schematic of the boost converter. It consists of two legs with an inductor and a half-bridge at each leg. At the input and the output, a capacitor is used for smoothing the input \( v_{pv} \) and output voltage \( v_{dc} \). With the half-bridge configuration, an active clamping is realised to reduce conduction losses. Therefore, \( S_{hs1} \) and \( S_{hs2} \) are switched inverted to \( S_{ls1} \) and \( S_{ls2} \).

Working with two half-bridge legs gives the opportunity to synchronise the switching transition of both legs in an appropriate manner. Usually, it is done to reduce the current ripple for the input capacitor \( C_{in} \) by a 180° phase shift of the switching commands \( S_{ls1} \) and \( S_{ls2} \) for both legs. This operating mode is considered for reference in the following comparison.

The half-bridge legs are equipped with metal-oxide-semiconductor field-effect transistors using SiC (SiC-MOSFETs) (C2M0280120D), to reduce the switching losses and to operate at high output voltages up to \( v_{dc} = 900 \) V. The period time of the switching interval of each leg is \( T = 5 \) μs.

2.2 Parasitic capacitance transistor to heat sink

SiC-MOSFET, mounted in a TO-247 package, is thermally connected to an aluminium heat sink, which is connected to ground and electrically isolated by an isolation pad. This setup results in a parallel plate capacitor between the transistors back plate and the heat sink. As the back plate of the used transistors is on drain potential, the capacitance \( C_{fet,bs} \) between the low-side transistor’s back plate to the ground is critical with respect to potential jumps. Depending on the absolute permittivity \( \varepsilon \) of the isolation pad, the
The basic solution is shown in Fig. 4 where the switching patterns of leg 1 with its inverse switching transition of leg 2. Depending on the switching behaviour of the SiC-MOSFETs, the leakage current path is excited with an oscillation. For a destructive interference of the leakage currents $i_{p1}$ and $i_{p2}$, the excitation should be equal to its inverse.

### 3.2 Switching transition analysis

To analyse the switching behaviour of the SiC-MOSFETs, a double pulse test is carried out at ambient temperature. Fig. 5 shows the measured drain-source voltage waveforms $v_{ds}$ for different inductor currents from 1 to 5 A in the upper diagram. On the left, it describes the behaviour of the switch-on transition, and on the right, it describes the behaviour of the switch-off transition. The lower diagram depicts the slew rates of the voltage waveforms, which should be equal for switch-on and switch-off for a good leakage current reduction.

During the switch on transition, the SiC-MOSFETs' switching behaviour is responsible for the slew rate of the switching node. Fig. 5 shows that the switch-on voltage slew rate is nearly constant for all current values. As for the switch-off transition, the switching node is charged with the inductor current, the slew rate depends on the inductor current value. In this case, the voltage slew rate increases with the inductor current.

### 3.3 Realisation of synchronisation

In this application, the effective synchronisation time delay $t_{\text{delay, sync, eff}}$ also depends strongly on the switching behaviour of the transistors. An additional delay time $T_{\text{add}(i_{\text{mean}})}$ is added to compensate the current depending delay (2). Therefore, calibration measurements for different inductor currents were carried out and the optimal $T_{\text{add}(i_{\text{mean}})}$ is determined empirically. Due to a high inductance value, the current ripple is very small in the considered operating points, which leads to $i_{\text{1} \to \text{2}} = i_{\text{1,mean}}$

$$t_{\text{delay, sync, eff}} = T_{\text{ls1,on}} + T_{\text{add}(i_{\text{mean}})} \tag{2}$$
The control system is implemented on a microcontroller (TI TMS320F28335) with its integrated PWM module. The additional time delay $T_{\text{add}(i)}$ is determined by increasing this value until the oscillation on $i_{\text{pe}}$ is damped maximally. Fig. 6 depicts the resulting time delays which were necessary. It shows the measured time delays as circles, as well as the uncertainty of the measurement due to the quantisation of the possible phase shift as error bars. For the application, the measurement results are fitted with a second-order polynomial (3), visible as the solid line:

$$T_{\text{add}(i_{\text{mean}})} = a_2 \cdot i_{\text{mean}}^2 + a_1 \cdot i_{\text{mean}} + a_0$$  \hfill (3)

### 4 Experimental results

#### 4.1 Prototype

A prototype of the boost converter is built up. Fig. 7 shows the top view of the power electronic board. On the left, the gate drive circuit is located, which is electrically isolated from the signal circuitry. The MOSFETs are located on the backside close to the DC-link capacitors and aligned to the line. The two inductor coils are mounted next to each other on the board, and the sensing circuitry is on the right side.

#### 4.2 Test setup

Fig. 8 shows the test setup. The voltage power supply sets a constant voltage $v_{\text{pv}}$. The capacitance $C_{\text{pe}}$ models the parasitic capacitance of the voltage power supply to ground. $C_{\text{pe}}$ of the voltage power supply, which is used, is $\sim 130 \, \text{nF}$. To decouple the power supply, a common mode choke is added. With the optional capacitance $C_{\text{opt}}$, the leakage current path can be varied by choosing different values. The boost converter is connected to the input voltage $v_{\text{pv}}$, and it delivers a constant output voltage $v_{\text{dc}}$ at its output clamps. For decoupling the load resistor $R_{\text{dc}}$, a second common mode choke is used. Both common mode chokes are realised with a Magnetec M-113-02 core with eight (at $v_{\text{pv}}$) and seven (at $v_{\text{dc}}$) windings. The boost converter's heat sink is connected to ground. The connection cable between the heat sink and ground is used for measuring the leakage current $i_{\text{pe}}$ with a Pearson current monitor 2877, which has a cutoff frequency of 200 MHz.

#### 4.3 Measurement results

For validating the basic principle, measurements at different operating points were performed. The leakage current $i_{\text{pe}}$ is measured and the root mean square value is calculated offline for an interval of $T_{\text{meas}} = 0.4 \, \text{ms}$.

First, all measurements were carried out with $C_{\text{opt}}$ not assembled. Fig. 9 shows the effective leakage current $i_{\text{pe},\text{rms}}$ in dependence on different mean inductor currents $i_{\text{mean}}$ for two different voltage setups. All results without synchronisation are marked as a cross ($\times$), while an asterisk * marks all synchronised results. The operating points show a reduced leakage current value when synchronised. The mean relative current reduction with synchronisation is 18% for boosting from 80 to 200 V and 16% for boosting from 200 to 380 V.

To analyse the dependence of the leakage current on the link voltage $v_{\text{dc}}$, a second series of measurement is performed; see Fig. 10. The inductor currents are kept constant to $i_{\text{mean}} = 3.5 \, \text{A}$, as well as the current waveforms of the inductors $i_{\text{l1}}$ and $i_{\text{l2}}$. The corresponding measured waveform for boosting from 80 to 200 V at $i_{\text{mean}} = 3.5 \, \text{A}$ is shown in Fig. 12 for the operation without $C_{\text{opt}}$ and in Fig. 13 for the operation with $C_{\text{opt}} = 1.5 \, \text{nF}$. The gate-source voltages of both lowside transistors $v_{\text{gs,ls1}}$ and $v_{\text{gs,ls2}}$ as well as the current waveforms of the inductors $i_{\text{l1}}$ and $i_{\text{l2}}$ are shown in both figures. The bottom diagram depicts the measured leakage current $i_{\text{pe}}$, respectively. The left-hand side
results are measured without synchronisation and the right-hand side results are measured with synchronisation turned on.

In Figs. 12 and 13, the leakage current is excited at the time when a switching transition occurs. Although the reduction in Fig. 12 is smaller than in Fig. 13, the number of excitations is reduced by 1 and also the peak current value of this excitation is lowered. In Fig. 13, this effect is seen more distinctive. The measurements show that the inductor current $i_{l1,l2}$ waveforms of both legs are well synchronised even for a reduction of the input capacitor $C$ current ripple at the considered operating points. It has to be mentioned that this is strongly dependent on the conversion ratio of the DC–DC converter's operating point. For the synchronisation, the input capacitor current ripple becomes larger at high or low conversion ratios of the DC–DC converter.

5 Conclusion and outline

With the presented synchronisation, the leakage current caused by switching transients in an interleaved boost converter is reduced for two of four switching actions in each switching period. In spite of the impact of the transistor’s switching behavior, the achieved reduction is between 16 and 22%, which is a very good result without the need of additional hardware elements. Especially for interleaved DC–DC converters, which work at a conversion ratio of 0.5 for buck or 2 for boost mode, the synchronisation has hardly any disadvantages, because the current ripple is still reduced effectively.

When using a cascaded buck-boost converter both switching transitions of each converter leg can be synchronised. Therefore the buck and boost stage of the converter can be operated with an inverted pulse pattern to cancel the leakage currents. As the inductor current is equal in both switching legs the slew rate of the switching node is much easier to control. So the reduction of the leakage current should be further improved with this converter topology and the synchronisation strategy.

6 References

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