Quantum Dots and Etch-Induced Depletion of a Silicon 2DEG

L. J. Klein¹, K. L. M. Lewis¹, K. A. Slinker¹, Srijit Goswami¹, D. W. van der Weide², R. H. Blick², P. M. Mooney³, J. O. Chu³, S. N. Coppersmith¹, Mark Friesen¹, and Mark A. Eriksson¹

¹Department of Physics, University of Wisconsin-Madison, Madison, WI 53706-1390,
²Electrical and Computer Engineering Department, University of Wisconsin-Madison, Madison, WI 53706-1691,
³IBM Research Division, T. J. Watson Research Center, NY 10598

The controlled depletion of electrons in semiconductors is the basis for numerous devices. Reactive-ion etching provides an effective technique for fabricating both classical and quantum devices. However, Fermi level pinning can occur, and must be carefully considered in the development of small devices, such as quantum dots. Because of depletion, the electrical size of the device is reduced in comparison with its physical dimension. To investigate this issue, we fabricate several types of devices in silicon-germanium heterostructures using two different etches, CF₄ and SF₆. We estimate the depletion width associated with each etch by two methods: (i) conductance measurements in etched wires of decreasing thickness (to determine the onset of depletion), (ii) capacitance measurements of quantum dots (to estimate the size of the active region). We find that the SF₆ etch causes a much smaller depletion width, making it more suitable for device fabrication.

PACS numbers:

I. INTRODUCTION

Recently, there has been a renewed interest in modulation doped, silicon-germanium quantum wells. Modulation doped field-effect transistors (MODFETs) are potentially attractive for communications applications because of their low noise, low cost, high speed, and compatibility with CMOS logic. They are also the basis for the high-mobility devices used in quantum dot quantum computing and spintronics, where quantum coherence plays a key role. Indeed, it is expected that silicon will exhibit the most desirable coherence properties of any semiconductor (except perhaps carbon) because of its weak spin-orbit coupling and the availability of spin-zero nuclear isotopes. In the context of quantum computing, the goal is to fabricate coupled quantum dots containing individual electrons whose spins act as qubits. We have made recent progress towards this goal, overcoming several materials and fabrication challenges.

In this paper, we report on Coulomb blockade and single electron tunneling experiments in which the number of electrons in a silicon quantum dot can be held constant for up to 11 hours. This fulfills an important milestone towards qubit fabrication. During the 1990’s, advances in materials science and growth techniques led to the development of high quality silicon-germanium quantum wells containing two-dimensional electron gases (2DEGs) with low-temperature electron mobilities of order 6 × 10⁶ cm²/V·s. Further progress was hampered by difficulties with leakage currents and parallel conduction paths, and unavoidable defects associated with the growth of strained heterostructures. However, spurred on by quantum computing, and new technologies like atomic layer oxide deposition, some important technological hurdles have been overcome. Reactive ion etching has emerged as an important fabrication tool and a viable alternative to top-gating. In this procedure, devices like quantum dots are formed by physically carving the 2DEG. External side gates for electrostatic control can be fabricated in nearby regions of 2DEG by the same method.

In this procedure, devices like quantum dots are formed by physically carving the 2DEG. External side gates for electrostatic control can be fabricated in nearby regions of 2DEG by the same method.

Here, we estimate the depletion width of etched samples by two different methods. First, we use the etch process to fabricate arrays of wires with different widths. Through conductance measurements, we observe the onset of depletion in the narrowest wires and a linear dependence of conductance vs. wire width for larger wires. Second, we determine the capacitance of etched quantum dots. Through realistic device simulations, we estimate the electrical size of the dots, and the corresponding depletion widths. The estimates for wires and dots are in reasonable agreement. However, the two etches used here, CF₄ and SF₆, cause very different depletion widths: 200-250 nm for CF₄, and a vanishing width for SF₆. We attribute these differences to the number or nature of the surface states.

The controlled depletion of electrons in semiconductors is the basis for numerous devices. Reactive-ion etching provides an effective technique for fabricating both classical and quantum devices. However, Fermi level pinning can occur, and must be carefully considered in the development of small devices, such as quantum dots. Because of depletion, the electrical size of the device is reduced in comparison with its physical dimension. To investigate this issue, we fabricate several types of devices in silicon-germanium heterostructures using two different etches, CF₄ and SF₆. We estimate the depletion width associated with each etch by two methods: (i) conductance measurements in etched wires of decreasing thickness (to determine the onset of depletion), (ii) capacitance measurements of quantum dots (to estimate the size of the active region). We find that the SF₆ etch causes a much smaller depletion width, making it more suitable for device fabrication.

PACS numbers:
II. GROWTH AND FABRICATION

A Si/SiGe heterostructure was grown by ultra-high vacuum chemical vapor deposition (UHVCVD). The 2DEG sits near the top of an 8 nm strained silicon quantum well, grown on a strain-relaxed Si$_{0.7}$Ge$_{0.3}$ buffer layer. The 2DEG is topped with a 14 nm Si$_{0.7}$Ge$_{0.3}$ spacer layer, and a 14 nm Si$_{0.7}$Ge$_{0.3}$ supply layer with phosphorus donors. The final structure is capped with 35 Å of silicon, as shown in Fig. 1.

Ohmic contacts were formed with the 2DEG by evaporating Au with 1% Sb and sintering at 400°C for 10 minutes. For all experiments described below, the contacts are made prior to reactive-ion etching. Using a hall-bar geometry, the electron density of the 2DEG is found to be $4 \times 10^{11}$ cm$^{-2}$, with a mobility of 40,000 cm$^2$/Vs at 2 K.

The devices studied here were fabricated by electron beam lithography and subsequent CF$_4$ or SF$_6$ reactive-ion etching. Extensive studies of this process have shown that for most ion species (including those used here), the etch rate of SiGe increases with germanium content. However, other factors, like rf power, gas pressure, plasma creation processes, and preferential sputtering of silicon, also affect the etch rate. As a consequence, it is quite difficult to etch uniformly through compositionally varying heterostructures.

For the devices used in this work, the heterostructures were etched to a depth of approximately 120 nm – far deeper than the 2DEG layer. Fig. 2 shows scanning electron microscope (SEM) images of our 3-gate dot and our 6-gate dot. We observe some rounding near the bottom of the trenches, and a prominent silicon ledge of width ~ 100 nm, due to the preferential etching of germanium (see Fig. 1). The undercutting below the silicon ledge is slightly non-uniform.

In the following, we measure the depletion widths from the inner perimeter of the silicon ledge. Inside this ledge, the silicon layer remains mainly intact. However, the contained 2DEG is depleted, due to strain effects and the close proximity to surface trap states. In the unetched, “bulk” regions of our devices, we observe differing depletion widths, depending on the etch.

III. ETCHED WIRES

Nine wires were patterned on two different chips using the CF$_4$ reactive-ion etch. The wires had different widths, ranging from 200 nm to 1350 nm, and all the devices were electrically isolated from one another. A typical device is shown in Fig. 3.

As discussed above, the wires have an electrical width smaller than their physical width, due to the depletion of the 2DEG near the etch boundaries. This effect has been studied previously in patterned wires. Here, we investigate edge depletion through transport measurements. The conductance of the wires should be proportional to their electrical width. For progressively narrow wires, the 2DEG will eventually cease to conduct. The onset of zero conductance therefore indicates full depletion, and provides an estimate of the depletion width. We assume the depletion width is the same for all the wires on a given chip, due to identical fabrication conditions.
FIG. 3: Atomic force microscope image of a fabricated wire. The darker regions are etched, leaving a narrow channel between the leads.

In Fig. 4, the two-point conductance is plotted for each of the wires, as a function of their physical width. Two-point measurements were used instead of four-point measurements in order to maximize the number of wires on a given chip for a given cool-down. Each data point represents an individual wire. The two chips are identified by different symbols. All the measurements are made at 2 K.

As expected, the wire conductance was found to vary approximately linearly with the physical width. A line fit through the higher data points intersects the $x$-axis at about 400 nm for both chips, suggesting a depletion width of about 200 nm on either side of the wires.

### IV. QUANTUM DOTS

Several quantum dots were fabricated by reactive ion etching. Here, we report on the two dots shown in Fig. 2. Although similar etching procedures were applied in the two cases, the 3-gate dot used the CF$_4$ etch, while the 6-gate dot used the SF$_6$ etch. All the components of the devices (dot, leads, and gates) were etched from the same 2DEG, with no additional metal top-gates. Because of the considerable etch depth (120 nm), we could detect no current flow between the side gates and the dots. However, in other experiments, not reported here, small leakage currents were observed for shallower etch depths (<100 nm). We conjecture that dislocation arms running underneath shallow etch trenches may connect the gates to the dot in such devices. Here, all side gates were contacted ohmically and grounded, unless otherwise noted.

The source and drain leads, together with the quantum dot, are formed from a single structure. However, the necks between the dot and the source-drain leads are designed to give transport resistances slightly larger than the resistance quantum $e^2/h \approx 25 \text{k}\Omega$. Thus, the necks form tunnel barriers, even when the side-gates are grounded. By adjusting the voltages on different side-gates, we can tune the number of electrons on the dot and the tunnel couplings to the source and drain leads. Additional details are provided in Ref. 16.

Several types of transport measurements are performed on the dots. First, we measure the current through the quantum dot while varying the voltage of a side-gate $V_g$,
but holding the bias voltage between the source and drain constant. As shown in Fig. 5 we observe periodic oscillations of the transport current through the quantum dots. The peaks indicate charge quantization in the dots, with successive peaks corresponding to an increment of one electron.

The spacing between consecutive peaks $\Delta V_g$ is governed primarily by the plunger gate capacitance, $C_g = e/\Delta V_g$, which determines the energy of the dot relative to the leads. For the 3-gate dot, we observe gate capacitances between 0.7 and 1.3 aF. Note that, because of the larger separations (and weaker couplings) between dots and gates in side-gate devices, various combinations of gates can be used for plunging, giving slightly different capacitances. For the 6-gate dot, we tie together two of the six gates ($g_1$ and $g_5$ in Fig. 2) to produce the gate voltage $V_g$, while grounding the other gates. The resulting data in Fig. 5(b) correspond to a gate capacitance of 11 aF. Thus, the 6-gate dot has a much larger gate capacitance than the 3-gate dot, signaling a smaller depletion width in the former.

A stability plot for the 6-gate dot is shown in Fig. 6. The data were taken over an 11 hour window, in which no switching events occurred. This represents a significant improvement over the 3-gate dot, as reported in Ref. 16. In part, we attribute the enhancement to the etching process: the SF$_6$ etch appears to generate a lower density of surface states, and a corresponding lower frequency of charge switching. However, the measurement was also performed in a 3.6 T magnetic field, known to reduce charge noise.

The shape of the Coulomb diamonds in Fig. 3 provides further information about the dot capacitance $C_{\Sigma}$. In the conventional theory of Coulomb blockade, transport phenomena are explained in terms of the chemical potentials of the $N$-electron dot, and the left and right leads, $\mu_{\text{dot}}(N)$, $\mu_L$, and $\mu_R$, respectively. At low temperatures, transport across the dot occurs only when $\mu_L > \mu_{\text{dot}}(N) \simeq \mu_{\text{dot}}(N + 1) > \mu_R$. Such considerations allow calculations of the shape of the diamonds. The resulting height (from tip to tip) is given by $2e/C_{\Sigma}$, from which we determine $C_{\Sigma}$.

In Ref. 16 we determined $C_{\Sigma} = 3.2$ meV for the 3-gate dot. For the 6-gate dot, the analysis has large error because of the broad conductance peaks in Fig. 5(b). We find $C_{\Sigma} \simeq 230$ aF, with a charging energy of 0.70 meV.

We can use these capacitance values to estimate the diameter of the electrically active regions of the quantum dots. Treating the dot as a conducting disk surrounded by an infinite dielectric obtains the conductance formula

$$C_{\Sigma} = 4\epsilon D,$$

where $\epsilon = 11.4\epsilon_0$ is the low-temperature dielectric constant of silicon and $D$ is the diameter of the disk. (Note that in our calculations, we assume materials parameters consistent with silicon, rather than Si$_{0.7}$Ge$_{0.3}$. This is convenient because (i) the dielectric constants of the two materials differ by only 6% at room temperature; (ii) low temperature parameters for SiGe are not well known.) Eq. (1) is clearly an approximation. It does not incorporate the complex structure of the real device. In particular, it does not take into account the bending of the electric field lines at the vacuum interface or the metallic leads. For side-gate devices, the interface has a stronger effect, so that Eq. (1) over-estimates $C_{\Sigma}$ for a given $D$. In Sec. V we treat this problem more carefully using numerical techniques.

From Eq. (1), we can back-out an estimate for the electrical width of the dot (as opposed to the actual physical width), using our estimates for the dot capacitance. For the 3-gate dot, we find an electrical diameter of 124 nm, compared to a physical width of 720 nm (measured from the silicon ledge). For the 6-gate dot, we find an electrical width of 570 nm. Within our error bars, this is the same as its physical width, given by 560 nm. Since the approximations leading to Eq. (1) underestimate the size of the dot, the depletion width in the 6-gate dot must be

![FIG. 6: Stability plot for the 6-gate dot, as function of gate and source-drain voltages. Measurements were performed at 300 mK, and show no switching events over the 11 hour measurement window. Diamonds are drawn as a guide to the eye.](image)

![FIG. 7: Simulation geometry for the 3-gate dot.](image)
vanishingly small. Thus, the capacitance measurements indicate a much larger depletion width for the 3-gate dot.

Based on our measurement of the electron sheet density, far from the etched boundaries, and our estimates of the dot diameters, we can determine the number of electrons in our dots. Using Eq. (1), we find 50 electrons for the 3-gate dot. (A better estimate for the dot diameter, in the following section, gives 170 electrons.) For the 6-gate dot, we estimate 1000 electrons. We point out that in spite of this large number, single electron charging effects are still prominent, and the operation is very stable.

V. MODELING OF THE QUANTUM DOT

We can improve on the estimate of Eq. (1) by performing more accurate numerical modeling of the physical device. We specifically consider the 3-gate dot of Fig. 4.

The three-dimensional model geometry used in our simulations is shown in Fig. 7. The solid regions correspond to dielectric material, which we model with silicon materials parameters, as discussed above. The exclusions in the solid are metallic, corresponding to undepleted 2DEG regions in the gates and leads. These are properly modeled by fixed-voltage boundary conditions.

Since the depletion width is not known initially, we perform our simulations for many different 2DEG boundaries. A top-view of several of the boundaries is shown in Fig. 8. The curves overlay an AFM image of the device. The depletion boundaries are taken to be equidistant from the physical boundaries. This separation corresponds to the depletion width. The necks between the dot and the source-drain leads are assumed to be fully depleted, as consistent with experimental evidence.

The capacitance matrix, relating charges to voltages for a system of conductors, is given by $Q = \sum C_{ij}V_j$. The conventional capacitances correspond to the diagonal coefficients $C_{ii}$. These are computed in our simulation by setting the voltages on all the gates to zero, except for the conductor of interest. Thus, the calculation of $C_2$ proceeds by setting the voltage of the quantum dot to 1 V, and the other gates to 0 V. The resulting charge on the quantum dot is equal to its capacitance in units of Farads (F).

In this way, a finite element analysis obtains the capacitance of the dot as a function of its size. For the experimental value $C_2 = 50$ aF, our simulations give a corresponding dot diameter of 233 nm, and a depletion width of 244 nm. This dot size is nearly two times larger than the estimate of Eq. (1). Thus, the numerical result more closely matches the estimate obtained in Sec. III and confirms our expectation that Eq. (1) should underestimate the true electrical diameter.

VI. DISCUSSION

We have seen that devices fabricated with the CF$_4$ and SF$_6$ etches exhibit some important differences. For the CF$_4$ etch, we observe a significant depletion width, while for the SF$_6$ etch, the electrical width of the dot is nearly the same as its physical width. We believe these differences can be attributed to a change in the number or the nature of surface charge states caused by the different etching procedures. Yet, there is a contradiction, which is most striking for the SF$_6$ dot. Although the dot itself remains undepleted, this cannot be true for the adjacent tunnel barriers. How can we understand this apparently non-uniform depletion?

There are several competing effects which contribute to the observed behavior. The dominant effect is electrostatic. The surface states attract charge from the supply layer, forming a band that pins the Fermi level near midgap. The redistribution of charge induces electric fields, which bend the conduction band locally. The depletion of the 2DEG near the silicon ledge therefore depends on the number of filled traps, and their position in the band gap. In the vicinity of the quantum dot, the density of trapped charge at the etch boundary is high, due to the convergence of side-gates and other structures. Thus, there should be a local enhancement of the depletion width, due to electrostatic effects. By this argument, we might expect a larger depletion width in a quantum dot than a wire. Indeed, this seems to be the case for our experiments.

Because the walls of the tunnel barriers are so closely spaced, we also expect this part of the device to exhibit enhanced depletion. To model the electrostatics of the surface states, we perform a simulation of the 6-gate dot, introducing a uniform charge density on both the top and etched surfaces. (The boundary of the etched structures is taken to be the inner perimeter of the silicon ledge,
FIG. 9: Atomic Force microscope image of the 6-gate dot in Fig. 2. The silicon ledge is observed as a $\sim 100$ nm rim around each gate.

rather than the outer perimeter – see Fig. 9.) For simplicity, we do not include screening by the 2DEG. Such a model is incomplete, but it provides insight into the effects of surface charge. The computed electrostatic potential gives a good approximation of the locally varying conduction band. In a real device, depletion occurs when the band energy lies above the Fermi level. In our model, depletion occurs when the potential is larger than a particular equipotential line.

Two possible depletion boundaries are shown in Fig. 10. The solid line describes a situation most consistent with the SF$_6$ etch and the 6-gate quantum dot. Here, the dot and the leads show almost no depletion, while the tunnel barriers are fully depleted. The tips of the side-gates are also partially depleted, as most evident in the narrower gates. The dashed line shows a different equipotential with much greater depletion. Because Poisson’s equation is linear, the same outcome could be obtained with the former equipotential criterion, but a larger surface charge density. (In contrast, the self-consistent simulations discussed below are non-linear.) The dashed line shows significant depletion of the quantum dot, as well as in the source, the drain, and the side-gates. The overall picture is consistent with our measurements in the 3-gate dot. We conclude that devices using the CF$_4$ etch are more strongly affected by the electrostatics of surface states.

In addition to electrostatic effects, quantum kinetic energy can also contribute to the depletion of a narrow tunnel barrier. Typically, such effects become noticeable in devices smaller than $\sim 100$ nm. In Fig. 2 we see the minimum barrier width (not including the silicon ledge) can be as small as 80 nm. Treating the barrier as a square well gives the transverse confinement energy $\hbar^2 \pi^2 / 2m^* L_b^2 = 0.3$ meV, where $L_b$ is the barrier width. If the effective width of the barrier is further reduced by the electrostatic potential from the surface charges, the confinement energy can easily reach several meV. Since this is a characteristic energy scale for quantum dot devices, it is reasonable to assume that confinement effects may also play a role in the depletion of narrow channels.

To facilitate the development of etched devices, it would be desirable to perform simulations that include both electrostatic and quantum mechanical effects, while allowing charge to move between the trap states, the supply layer, and the 2DEG, to satisfy electrochemical equilibrium. A goal would be to determine the charge profile and the depletion boundary self-consistently. A recent theory by Fogler has made steps in this direction by determining the depletion boundary self-consistently. Charge redistribution and quantum effects are not yet included in the theory.

VII. CONCLUSIONS

We have obtained experimental estimates for the 2DEG depletion width in etched silicon heterostructures by (i) a conductance technique involving etched wires and (ii) a capacitance technique involving etched quantum dots. For the CF$_4$ etch, the two estimates give 200 nm and 244 nm, respectively. For the SF$_6$ etch, we observe a small or vanishing depletion width by the capacitance technique. Thus, SF$_6$ appears especially useful for fabricating small devices.

By means of simulations, we have shown that the depletion width is locally varying in etched devices, as consistent with the experimental observations. The shape of the depletion boundary depends many factors, presenting a challenge for device design. However, we believe that theoretical and numerical tools should be available in the near future.

The proximity between gates and dots forms an important control issue, since it determines the capacitive
coupling of the side-gates. For the devices studied here, the minimum separation between undepleted regions in neighboring dots or side-gates is about 200 nm in SF$_6$-etched devices, reflecting the width of the silicon ledge. We believe this level of control will enable the development of many types of silicon devices for experiments and applications. In the context of quantum computing, this work forms a promising step towards silicon qubits. Ultimately, such devices will require a fabrication resolution as small as 50-150 nm. We anticipate that improvements in theoretical design tools, and etching and top-gating techniques, will enable us to achieve this goal.

Acknowledgment

The authors would like to acknowledge Mariana Lazar for providing her imaging code. This work was supported by NSA and ARDA under ARO contract number W911NF-04-1-0389, and by the National Science Foundation through the ITR program (DMR-0325634), the QuBIC program (EIA-0130400), and the MRSEC program (DMR-0079983).

1. S. J. Koester, K. L. Saenger, J. O. Chu, Q. C. Ouyang, J. A. Ott, M. J. Rooks, D. F. Canapari, J. A. Tornello, C. V. Jahnnes and S. E. Steen, Electronics Lett., 39, 1684 (2003).
2. D. Loss and D. P. DiVincenzo, Phys. Rev. A 57, 120 (1998).
3. R. Vrijen, E. Yablonovitch, K. Wang, H. W. Jiang, A. Balandin, V. Roychowdhury, T. Mor, and D. DiVincenzo, Phys. Rev. A 62, 012306 (2000).
4. M. Friesen, P. Rugheimer, D. E. Savage, M. G. Lagally, D. W. van der Weide, R. Joynt, and M. A. Eriksson, Phys. Rev. B 67, 121301(R) (2003).
5. M. Friesen, C. Tahan, R. Joynt, and M. A. Eriksson, Phys. Rev. Lett. 92, 037901 (2004).
6. B. E. Kane, Nature (London), 393, 133 (1998).
7. E. Yablonovitch, H. W. Jiang, H. Kosaka, H. D. Robinson, D. S. Rao, and T. Szkopek, Proc. IEEE 91, 761 (2003).
8. M. A. Eriksson, M. Friesen, S. N. Coppersmith, R. Joynt, L. J. Klein, K. Slinker, C. Tahan, P. M. Mooney, J. O. Chu, and S. J. Koester, Quant. Inform. Proc. 3, 133 (2004).
9. F. Schäffler, D. Többen, H.-J. Herzog, G. Abstreiter and B. Holländer, Semicond. Sci. and Technol. 7, 290 (1992).
10. K. Ismail, M. Arafà, K. L. Saenger, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. 66, 1077 (1995).
11. N. Sugii, K. Nakagawa, Y. Kimura, S. Yamaguchi and M. Miyao, Semicond. Sci. and Technol. 13, A140 (1998).
12. T. Okamoto, M. Ooya, K. Hosoya, and S. Kawaji, Phys. Rev. B 69, 041202(R) (2004).
13. K. Lai, W. Pan, D. C. Tsui, S. Lyon, M. Muhlderger, and F. Schäffler, Phys. Rev. Lett. 93, 156805 (2004).
14. S. Kanjanachuchai, T. J. Thornton, J. M. Fernández, and H. Ahmed, Semicond. Sci. and Technol. 13, 1215 (1998).
15. A. Notargiacomo, L. Di Gaspare, G. Scappucci, G. Mariotini, F. Evangelisti, E. Giovine, and R. Leoni, Appl. Phys. Lett. 83, 302 (2003).
16. L. J. Klein, K. A. Slinker, J. L. Truitt, S. Goswami, K. L. M. Lewis, S. N. Coppersmith, D. W. van der Weide, M. Friesen, R. H. Blick, D. E. Savage, M. G. Lagally, C. Tahan, R. Joynt, M. A. Eriksson, J. O. Chu, J. A. Ott, and P. M. Mooney, Appl. Phys. Lett. 84, 4047 (2004).
17. Y. Zhang, G. S. Oehrlein, E. de Frasart, and J. W. Corbett, J. Vac. Sci. Technol. A 11, 2492 (1993).
18. M. Holzmann, D. Többen, G. Abstreiter, M. Wendel, H. Lorenz, and J. P. Kotthaus, and F. Schäffler, Appl. Phys. Lett. 66, 833 (1995).
19. R. G. van Veen, A. H. Verbruggen, E. van der. Drift, F. Schäffler, and S. Radelaar, Semicond. Sci. and Technol. 14, 508 (1999).
20. E. Giovine, A. Notargiacomo, L. Di Gaspare, E. Palange, F. Evangelisti, R. Leoni, G. Castellano, G. Torrioli, and V. Foglietti, Nanotechnol. 12, 132 (2001).
21. L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, in Mesoscopic Electron Transport, edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön, (Kluwer, Dordrecht, 1997), 105.
22. M. H. Devoret and H. Grabert, in Single Charge Tunneling, 2nd ed., edited by H. Grabert and M. H. Devoret, (Wiley, New York, 1992), 1.
23. R. Ahuja, C. Persson, A. F. da Silva, J. S. de Almeida, C. M. Araujo, and B. Johansson, J. of Appl. Phys. 93, 3832 (2003).
24. J. D. Jackson, in Classical Electrodynamics, 2nd ed. (Wiley, New York, 1975). Wiley, 1975).
25. We use the commercial finite element software FEMLAB (www.comsol.com).
26. S. M. Sze, in Physics of Semiconducting Devices, 2nd ed. (Wiley, New York, 1981).
27. C. W. J. Beenakker and H. van Houten, Sol. State Phys. 44, 1 (1991), and reference therein.
28. M. M. Fogler, Phys. Rev. B 69, 245321 (2004).