Design and Power Dissipation Consideration of PFAL CMOS V/S Conventional CMOS Based 2:1 Multiplexer and Full Adder

Manvinder Sharma¹ · Digvijay Pandey² · Pankaj Palta¹ · Binay Kumar Pandey³

Received: 23 April 2021 / Accepted: 17 June 2021 / Published online: 2 July 2021
© Springer Nature B.V. 2021

Abstract
With the integration of circuits, number of gates and transistors are increasing per chip area. However with integration in every digital circuit, the energy due to switching of gate doesn’t decrease at same rate as gates are increased per chip area. Due to this, power dissipation becomes significant and also reduction of heat becomes more complicated and expensive. The CMOS (complementary metal oxide semiconductor) Logic family is preferred for digital circuits due to its performance and impeccable noise margins over other families. However, in CMOS based circuits dynamic power requirement is becoming major concern in digital circuits. The aim of this paper is to carry out work that is focused on reducing the power dissipation in circuits, which increases with down scaling of circuits. The experimental work is carried out on 2:1 multiplexer and full adder circuit. Adiabatic logic with positive feedback (PFAL) is applied to redesign the circuit with input power taken as sinusoidal source of 3.3 V and analysis is done for power dissipation between conventional based CMOS circuit and PFAL based CMOS circuit. In comparison with the conventional CMOS based 2:1 multiplexer circuit, the designed PFAL based CMOS 2:1 multiplexer circuit has lesser power dissipation which is measured as 80.871 picoWatts as compared to conventional CMOS circuit which has 6.9090 nanoWatts with the same behavior of circuit. Also for full adder conventional CMOS circuit has 48.0452 picoWatts while PFAL based full adder has 3.9089 picoWatts.

Keywords Low power design · Adiabatic · PFAL · Multiplexer · Adder, CMOS (complementary metal oxide semiconductor)

1 Introduction
For high speed performance in computing and other applications which involve processing, computing and analysis of any signal, digital CMOS circuits have been used mostly. Several pros over other families which include perfect logic levels, impeccable noise margins, better performance and almost negligible static power dissipation CMOS logic family is preferred. As we need faster processing of signals, the demand of these circuits is high and is going to increase in near future. Faster speed in computing is achieved with the increase in number of transistors integrated over a chip. However such improvement in performance is accompanied with increase in energy dissipation and power dissipation [1]. The disadvantage of higher energy and power dissipation is that the circuits require more expensive packaging and expansive cooling technology which decreases reliability also increases cost. As the level of clock frequency and on-chip integration will continue to grow as per the demands of faster computing, the energy and power dissipation of these high performance circuits is a perilous design issue [2]. To achieve Tera Instructions per seconds (TIPS) high end microprocessor employ billions of transistor on chip at clock rates over 30 GHz, with this rate of speed power dissipation of circuit is projected to extend to thousands of watts. Such power dissipation density introduces reliability concerns like hot carrier, thermal stress and electromigration which degrade the performance of circuits. Also for the requirement of low power chips or
low battery consuming chips the higher power dissipation circuits will consume more power from the battery [3–5]. For the portable digital systems that run on batteries like notepads, laptops, tablets etc. the prime concern is low power consumption and this also increases the battery longevity.

The power consumed by any device is the energy consumed per unit time.

\[ E = \int_{t_0}^{t_f} P(t) \, dt \]  

For a given operation the energy (E) required is integral of power (P) consumed over operation time (T_{op}).

The power of digital CMOS circuit is given by

\[ P = C \cdot V_{DD} \cdot V_s \cdot f \]  

Where \( V_{DD} \) is supply voltage, \( f \) is clock frequency, \( C \) is capacitance being recharged and \( V_s \) is voltage swing of signal.

The energy consumption can be given by

\[ E = n \cdot C \cdot V_{DD} \cdot V_s \]  

In this equation energy consumption is independent of clock frequency. As the battery life is determined by energy consumption it is imperative to reduce energy as compared with power. However power is critical for heat dissipation considerations. So optimization of both factors energy as well as power is required [6].

In CMOS circuit, power dissipation is composed of static and dynamic power dissipation. Static power dissipation is power dissipated in steady state and is given by

\[ P_{static} = I_{static} \cdot V_{DD} \]  

Where \( I_{static} \) is current when circuit is in steady state or in the absence of switching activity. However theoretically, in static state there is no direct path from \( V_{DD} \) to ground (pMOS) and no transistor is on state (nMOS) there is no static power dissipation [7, 8]. But in practice Metal-Oxide-Semiconductor (MOS) is not a perfect or impeccable switch due to this there is always substrate injection current and leakage current which introduces static power dissipation [9-11]. For 5 Volts of \( V_{DD} \), substrate injection current for a nMOS device (W/L = 10/0.5) is in order to 1–100 \( \mu A \) [12].
Another subcategory of static power dissipation is ratioed logic. As CMOS family is ratioed family pull up of pMOS is in always on state which also acts as load for pull down nMOS network. In low state, when gate output is low there is direct path for current from \( V_{DD} \) to ground. In this state static current flows. So in CMOS family static power consumption is considerable. Figure 1 shows the CMOS Inverter operation.

Dynamic power dissipation is introduced in the circuit while switching activity, or in transition state. During the transient activity, at a point which is \( V_{tn} \) (nMOS threshold point) and \( V_{DD} - V_{tp} \) (pMOS threshold point) both pMOS and nMOS are turned on. A short circuit exists in this duration and current has path from \( V_{DD} \) to ground. With the cautious designing of edges of transition this effect can be minimized to ten to 15% of power of total. The other factor affecting dynamic dissipation is due to charging of parasitic capacitance and discharging of parasitic capacitance within the circuit [13]. In fig. 1, the parasitic capacitance is shown as a output as a capacitor. Considering one full cycle of operation from \( V_{DD} \) to GND and from GND to \( V_{DD} \), the process of charging the capacitor draws energy from the power supply which is equal to \( C \cdot (V_{DD})^2 \). Half power is stored in capacitor while half is dissipated in pMOS, during operation ground to \( V_{DD} \), the capacitance is discharged and energy is dissipated in nMOS. For each time the capacitance switches, energy equals to \( C \cdot (V_{DD})^2 \) is dissipated. The dynamic dissipation can be formulated as

\[
P_{\text{dyn}} = \alpha C V_{DD}^2 f
\]  

(5)

Where, \( \alpha \) is expected number of 0 to 1 transitions per data cycle, \( f \) is clock frequency.

2 PFAL Modeling Design

The dissipation takes most of power dissipation almost 90%. To reduce this dissipation, designers can decrease node capacitance, minimize switching events, reduce voltage swing or also can smear grouping of these. But in all these methods before power dissipation, energy which is drawn from power supply is used once. However, if we introduce recycling of energy drawn from power supply, the energy efficiency of logic circuits can be achieved [14]. The possibility of reusing energy drawn from the supply and reducing the energy dissipation during switching is offered by a class of circuits known as Adiabatic logic circuits. In this logic, the energies stored in capacitance are reused instead of being dissipated as heat. This is also known and energy recovery CMOS. By only switching the transistors under certain conditions and slowing switching process one can achieve very low power dissipation in the circuit [15, 16].

Figures 2, 3, 4 shows adiabatic switching process. Instead of constant voltage source [17], the capacitance is charged by constant current source, \( R \) shows resistance of pMOS.

A constant charging current corresponds to linear voltage ramp.

Initially, let us assume capacitance voltage \( V_C = 0 \).
Fig. 7 Conventional CMOS based 2:1 Multiplexer

Fig. 8 Conventional CMOS based Full Adder

Fig. 9 PFAL CMOS 2:1 Multiplexer
IR be the voltage across switch

P(t) in the switch = I^2R

Energy during charge = (I^2R) T

\[ I = \frac{CV}{T} \rightarrow T = \frac{CV}{I} \]  

\[ E = (I^2R)T = \left( \frac{CV}{T} \right)^2 RT = \frac{C^2V^2R}{T} \]  

\[ E = E_{\text{diss}} = \left( \frac{RC}{T} \right) CV^2 = \left( \frac{2RC}{T} \right) \left( \frac{1}{2} CV^2 \right) \]
E is energy dissipated, Q is charge transfer to load, C is load capacitance, R is Resistance of MOS Switch, V is final value of voltage and T is time spent at load.

From Eq. 9, if the charging time (T) is greater than 2RC, the energy dissipation can be made small by increasing charging time. Opposed to conventional CMOS, the dissipated energy is proportional to R instead of capacitance and voltage swing. Reducing on resistance of pMOS will reduce energy dissipation.

To reuse the power a different type of power supply is used in the adiabatic logic. The source needed for adiabatic operation is usually a sinusoidal or a trapezoidal source. This supply can also act as clock for circuit. Fig. 5 shows trapezoidal power supply. The four phases idle, evaluate, hold and recovery shows the process. Idle is equal to 0 and hold is equal to 1. While in evaluate phase, depending upon input the load capacitance charges up or does not and in recovery phase the charge held on capacitance is recovered.

Positive feedback adiabatic logic (PFAL) is the category under adiabatic logic family. As compared to other families like ECRL, 2 N-2P2P, CAL this PFAL has lowest energy consumption [18, 19]. It is robust against technological parameter variations. The core of PFAL is adiabatic amplifier, latch made by two nMOS and two pMOS. The two n-trees relaize logic functions as well as it can generate both positive and negative outputs which can be used as per requirement. Figure 6 shows general schematic of PFAL gate [20, 21]. Two latches M1 and M2 and M3 and M4 formed by pMOSandnMOS.

In mentor graphic design architect IC conventional CMOS based 2:1 multiplexer is modeled and analyzed for power dissipation which is shown in Figs. 7 and 8 shows conventional CMOS based full adder which is modeled and analyzed.
Using the discussed methodology, PFAL based 2:1 multiplexer and full adder is designed and modeled in Mentor graphic design architect IC and is shown in Figs. 9 and 10 respectively. The designs are simulated in ELDONET tool.

3 Results and Discussions

First, The design structure includes PFAL based CMOS which is modeled in Mentor Graphic tool named Design Architect using standard TSMC 0.35 μm CMOS technology. At an operating temperature of 27 °C input voltage 3.3 V supply is provided. The ELDONET tool is used to simulate and check the results for power dissipation for conventional CMOS and PFAL designed circuits.

For the conventional circuit V_DD is taken as constant DC source with a value of V_DD equals to 3.3 V. The circuits are shown in Figs. 7 and 8. For PFAL circuit the reconstruction is done from conventional circuit using same method to make PFAL circuits. The circuits are modeled and shown in Figs. 9 and 10. The source for the circuit is taken as SIN source and sine ac wave is provided as power supply of 3.3 V.

The design is simulated in ELDONET environment. The Figs. 11 and 12 shows results after simulation of conventional 2:1 Multiplexer. The calculated power dissipation after simulation of conventional 2:1 multiplexer is 6.9090 nano Watts.

PFAL 2:1 multiplexer is simulated and results as power dissipation is shown in Figs. 13 and 14. The calculated power dissipation in this circuit is 80.8716 p Watts. It can be observed that the power dissipation is reduced with high rate with the same working of circuit. Figure 15 shows the comparison of power dissipation for 2:1Multiplexer.

The Figs. 16 and 17 shows results after simulation of conventional CMOS based Full Adder. The calculated power dissipation after simulation is 48.0452 picoWatts.

PFAL CMOS based full adder is simulated and results as power dissipation is shown in Figs. 18 and 19. The calculated power dissipation in this circuit is 3.9089 picoWatts. It can be observed that the power dissipation is reduced with the same working of circuit. Figure 20 shows the comparison of power dissipation for both full adder circuit.
Table 1 shows the different circuit modeled and simulated in eldonet environment and their power dissipation.

After the simulation of all circuits (convention CMOS 2:1 multiplexer, Conventional CMOS full adder, PFAL CMOS 2:1 multiplexer and PFAL full adder) it can be clearly seen that the power dissipation of the circuit using PFAL is reduced to a much lower value. However the circuit for PFAL has increased the number of gates required to perform any logic but it is also providing both original and its complement outputs. This can eliminate the requirement of other circuit where complement of output is also required for many applications.

4 Conclusion

While rate of integration of transistor per chip area is increasing day by day leading to more power dissipation. For reducing power dissipation, expansive heat cooling methods are employed. Also power dissipation directly affects the device performance in reliability terms and performance of circuit. For this concern, the primary focus of designers is on reducing the power dissipation in the digital circuits. In this experimental work, adibatic logic based approach for reducing and reusing the power and energy dissipation is discussed, simulated and compared with conventional used circuits. Using adibatic logic based PFAL method, 2:1
The data samples have been taken from multiple sources.

Declarations

Conflict of Interests/Competing Interests The authors declare that they have ‘no known conflict of interests or personal relationships’ that could have appeared to influence the work reported in this paper.

Acknowledgements The authors would like to express gratitude to Department of Technical Education and Chandigarh Group of Colleges, Landran, Punjab India. The authors would also like to thank to Vice Chancellor, Dr. A.P.J. Abdul Kalam Technical University, and Uttar Pradesh, India.

Contributions All authors approve the final manuscript.

Availability of Data and Material The data samples have been taken using PFAL.

Code Availability The relevant code with the manuscript is also available and would be available, if will be asked to do so later.

Funding The author(s) received no financial support for the research, authorship, and/or publication of this article.

References

1. Samaali H, Perrin Y, Galisultanov A, Fanet H, Pillonnet G, Basset P (2019) MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation. Nano Energy 55:277–287
2. Barla P, Shet D, Joshi VK, Bhat S (2020) Design and analysis of LIM hybrid MTJ/CMOS logic gates. 2020 5th International Conference on Devices, Circuits and Systems (ICDCS). IEEE, pp 41–45
3. Gavaskar K, Malathi D, Dhivya R, Dimple Dayana R, Dharun I (2020) Low power design of 4-bit simultaneous counter using digital switching circuits for low range counting applications. 2020 5th International Conference on Devices, Circuits and Systems (ICDCS). IEEE, pp 316–320
4. Swami N, Khatri B (2020) High performance CMOS circuit design. AIP Conference Proceedings 2220:020187. https://doi.org/10.1063/5.0002200
5. Schmickl S, Faseth T, Pretl H (2020) An RF-energy harvester and IR-UWB transmitter for ultra-low-power battery-less biosensors. IEEE Trans Circuits Syst I: Regular Papers 67(5):1459–1468
6. Varadharajan SK, Nallasamy V (2017) Low power VLSI circuits design strategies and methodologies: A literature review. 2017 Conference on Emerging Devices and Smart Systems (ICEDSS). IEEE, pp 245–251
7. Sengupta SI, Sen D, Roy S, Chanda M, Sarkar SK (2019) DC Performance Analysis of High-K Adiabatic Logic Circuits in Sub-Threshold Regime for RF Applications. Sens Lett 17(6):487–496
8. Xu L, Lee J, Saligane M, Blaauw D, Sylvester D (2021) Design techniques of integrated power management circuits for low power edge devices. 2021 IEEE Custom Integrated Circuits Conference (CICC), pp 1–4. https://doi.org/10.1109/CICC51472.2021.9431508
9. Raghav HS, Bartlett VA, Kail I (2018) Investigating the effectiveness of without charge-sharing quasi-adiabatic logic for energy efficient and secure cryptographic implementations. Microelectron J 76:8–21
10. Ganavi MG, Premananda BS (2020) Design of low power reduced complexity Wallace tree multiplier using positive feedback adiabatic logic. in advanced computing and intelligent engineering, pp. 139–150. Springer, Singapore
11. Mani B, Gupta S, Kumar H (2020) Adiabatic Design Implementation of Digital Circuits for Low Power Applications. Micro-Electronics and Telecommunication Engineering, pp. 275–287. Springer, Singapore
12. Blotti, Saletti R (2004) Ultralow- power adiabatic circuit semi-custom design. IEEE Trans VLSI Syst 12(11):1248–1253
13. Pown M, Sandeep S, Lakshmi B (2020) Investigation of Homo and hetero-junction double-gate tunnel-FET-based adiabatic inverter circuits. IETE J Res:1
14. Sharma M, Singh H (2018) SIW based leaky wave antenna with Semi C-shaped slots and its modeling, design and parametric considerations for different materials of Dielectric. 2018 Fifth International Conference on Parallel, Distributed and Grid Computing (PDGC). IEEE, pp 252–258
15. Sri Penugonda R, Ravishankar V (2020) Design of low power SRAM cell using adiabatic logic. J Phys Conf Ser 1716(1):012039
16. Patil S, KanchanaBhaaskaran V (2017) Optimization of power and energy in FinFET based SRAM cell using adiabatic logic. 2017 International Conference on Nextgen Electronic Technologies: Silicon to Software (ICNETS2), IEEE, pp 394–402
17. Kamarthi K, Acharya A, Kadam P (2017) Low power multiplier design using adiabatic SCRL logic. 2017 IEEE International Conference on Circuits and Systems (ICCS). IEEE, pp 255–260
18. Chamanian S, Uluşan H, Koyuncuoğlu A, Muhtaroğlu A, Külah H (2018) An adaptable interface circuit with multistage energy
19. Athas WC, Koller JG, Svensson LJ (1994) An energy-efficient CMOS line driver using adiabatic switching. Proceedings of 4th Great Lakes Symposium on VLSI. IEEE, pp 196–199
20. Sharma M, Singh S, Khosla D, Goyal S, Gupta A (2018) Waveguide diplexer: design and analysis for 5G communication. 2018 Fifth International Conference on Parallel, Distributed and Grid Computing (PDGC). IEEE, pp 586–590
21. Anitha K, Jayachira R (2016) Design and analysis of CMOS and adiabatic 1:16 multiplexer and 16:1 demultiplexer. International Journal of Reconfigurable and Embedded Systems (IJRES) 5(1)

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.