Fault-tolerance of ancilla preparation for logical Toffoli gate of a family of Calderbank-Shor-Steane codes

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Abstract

Fault-tolerant quantum computation using quantum error-correcting codes requires fault-tolerant constructions of nontransversal gates. Shor proposed a fault-tolerant construction of a nontransversal gate, i.e., the Toffoli gate for a family of the Calderbank-Shor-Steane codes which has even-weight stabilizer generators and odd-weight logical operators. In fact, as shown in this paper, error propagations in the ancilla preparation of Shor’s construction lead to logical errors. This work provides a solution to this problem through the insertion of bit flip error correction. Finally, error rates of a modified construction are evaluated with use of the concatenated Steane codes, and the same accuracy threshold as transversal gates is obtained in cases where ancillary systems can be prepared just in time.

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I. INTRODUCTION

To achieve large-scale quantum computation, fault-tolerant quantum computation using quantum error-correcting codes has been proposed [1–9]. Fault-tolerant implementation of a quantum algorithm requires the realization of all unitary operations in a universal gate set for encoded systems, but quantum error-correcting codes have operations in universal gate sets which cannot be implemented with only bitwise operations on the encoded qubits [10]. These gate operations are called nontransversal, and it is necessary to make fault-tolerant constructions of them. This problem can be solved using ancilla-assisted operations [11, 12], and Shor proposed a fault-tolerant construction [11] for a nontransversal gate, i.e., the Toffoli gate of a family of the Calderbank-Shor-Steane (CSS) codes [13, 14] which has even-weight stabilizer generators and odd-weight logical operators. In the ancilla preparation of Shor’s construction, bitwise controlled operations between logical (i.e., encoded) states and parity states are performed, and use of a sufficient number of the parity states guarantees fault-tolerance against bit flip errors on the parity states. However, as shown in this paper, local errors on the logical states propagate through the bitwise controlled operations and lead to logical errors. This indicates that the ancilla preparation of Shor’s construction is not sufficient for fault-tolerance.

In this paper, the error propagations through the bitwise controlled operations between the encoded ancilla systems and auxiliary systems are shown first. Then, a modification of the ancilla preparation is proposed for fault-tolerance. Finally, error rates are evaluated for the concatenated Steane codes, which are a member of the family of CSS codes, and the accuracy threshold is obtained.

II. ERROR PROPAGATIONS IN ANCILLA PREPARATION OF SHOR’S CONSTRUCTION AND A MODIFICATION FOR FAULT-TOLERANCE

First, we state the conventional definition of fault-tolerance of logical gate constructions. A gate construction is said to be fault-tolerant if logical errors occur at a rate of $O(p^{t+1})$ in the circuit, where $p$ is the rate of a local error on a bare qubit per time step and $t$ is defined as $t = \lfloor (d - 1)/2 \rfloor$ for the minimum distance $d$ of the quantum code. This means that the fault-tolerant gate construction does not reduce the performance of the quantum code.
The goal state of the ancilla preparation is $|\bar{A}\rangle = |\bar{0}\bar{0}\rangle + |\bar{0}\bar{1}\rangle + |\bar{1}\bar{0}\rangle + |\bar{1}\bar{1}\rangle$. The overbars mean that the states are logical. The circuit for the ancilla preparation of Shor’s construction is shown in Fig. 1. Each of the upper three horizontal lines represents one logical qubit from an encoded block, but not the encoded block itself. The input state $|\bar{+}\bar{+}\bar{+}\rangle|\text{cat}\rangle$ is easily prepared, where $|\bar{+}\rangle = |\bar{0}\rangle + |\bar{1}\rangle$ and $|\text{cat}\rangle = |00\ldots0\rangle + |11\ldots1\rangle$. In this paper, the systems prepared as $|\bar{+}\rangle$ and $|\text{cat}\rangle$ are respectively referred to as “Toffoli ancilla system” and “auxiliary system.” In particular, the Toffoli ancilla systems are referred to as the first, the second, and the third from the top downward. The circuit consists of the sequence of unitary gates (enclosed by the dashed line) and the following logical NOT operation controlled by a parity of the auxiliary system (enclosed by the dotted line). Each of the operations, including the Toffoli gate, is performed bitwisely. The sequence of unitary gates is actually repeated $O(d)$ times with different auxiliary systems, and the logical NOT operation on the third Toffoli ancilla system is performed only when a majority vote of the parities is odd. This is done in order to guarantee fault-tolerance against errors occurring on the auxiliary systems. The sequence of bitwise Hadamard, CNOT, and Toffoli gates transforms $|\bar{A}\rangle|\text{cat}\rangle$ into $|\bar{A}\rangle|\text{even}\rangle$ and $|\bar{B}\rangle|\text{cat}\rangle$ into $|\bar{B}\rangle|\text{odd}\rangle$, where $|\bar{B}\rangle = \bar{X}_{T_3}|\bar{A}\rangle$ ($\bar{X}_{T_3}$ is the logical NOT operation on the third Toffoli ancilla system), and $|\text{even}\rangle$ and $|\text{odd}\rangle$ are respectively the superposition of codewords including even and odd 1’s with the equivalent coefficients. The product state $|\bar{+}\bar{+}\bar{+}\rangle$ equals $|\bar{A}\rangle + |\bar{B}\rangle$. Therefore, after the parity measurements, if a majority vote of the parities is even, the resultant logical state is $|\bar{A}\rangle$. Otherwise, if a majority vote of the parities is odd, the logical NOT operation on the third Toffoli ancilla system prepares $|\bar{A}\rangle$. The CNOT and Toffoli gates propagate the bit flip error(s) on the control(s) and the phase flip error on the target. Specifically, through the CNOT gate, the bit flip error on the control and the phase flip error on the target create the same error on the other qubit. On the other hand, through the Toffoli gate, the phase flip error on the target creates the controlled $Z$ error between the controls, and the bit flip error on a control creates the CNOT error between the other control and the target. In the ancilla preparation of Shor’s construction, the targets of the bitwise controlled operations are the auxiliary systems of the parity state $|\text{even}\rangle$. Since parity states are robust against phase flip errors, the propagations of phase flip errors from the auxiliary systems damages the Toffoli ancilla systems bitwisely, and hence the circuit is tolerant of phase flip errors. In contrast, the circuit is intolerant of bit flip
errors on the Toffoli ancilla systems, because the bit flip errors on the Toffoli ancilla systems propagate to different auxiliary systems in sequence. The use of multiple auxiliary systems does not make the circuit tolerant of these forms of error propagations.

Let us analyze the bit flip error propagations through the bitwise controlled operations. We first examine a bit flip error on the third Toffoli ancilla system. This bit flip error propagates through the bitwise CNOT gate. In the ancilla preparation of Shor’s construction, if the third Toffoli ancilla system includes the bit flip error on the $i$th qubit, then the state after the sequence of unitary gates is $X_{T_{3,i}}(|\overline{A}\rangle |\text{odd}\rangle + |\overline{B}\rangle |\text{even}\rangle)$, where $X_{T_{3,i}}$ is the bit flip error on the $i$th qubit of the $j$th Toffoli ancilla system. An occurrence of the bit flip error before the $(t+1)$th bitwise CNOT gate gives the output state $X_{T_{3,i}}(|\overline{A}\rangle |\text{even}\rangle^{\otimes k} |\text{odd}\rangle^{\otimes t+1} + |\overline{B}\rangle |\text{odd}\rangle^{\otimes k} |\text{even}\rangle^{\otimes t+1})$, where $0 \leq k \leq t$, corresponding to its occurrence between $k$th and $(k+1)$th bitwise CNOT gates. We can see that majority votes of the parities of these states lead to the incorrect decision of the corresponding Toffoli ancilla state, and as a result, the logical bit flip error occurs on the third Toffoli ancilla system.

Next, we examine bit flip error occurrences on the first and second Toffoli ancilla systems. These bit flip errors propagate through the bitwise Toffoli gate. We can analyze these error propagations, without loss of generality, under the assumption that the bit flip error occurs on the $i$th qubit of the first Toffoli ancilla system. For this bit flip error, after the error propagation, the CNOT error occurs between the $i$th qubit of the second Toffoli ancilla
system and the ith qubit of the auxiliary system. This erroneous state is

$$X_{T_1,i} \cdot C_{X_{T_2,i},A_i}(|\bar{A}\rangle|\text{even}) + |\bar{B}\rangle|\text{odd})$$

$$= X_{T_1,i}[(P_{0,T_2,i}|\bar{A}\rangle + P_{1,T_2,i}|\bar{B}\rangle)|\text{even}]$$

$$+ (P_{1,T_2,i}|\bar{A}\rangle + P_{0,T_2,i}|\bar{B}\rangle)|\text{odd}],$$

where $C_{X_{T_2,i},A_i}$ is the CNOT operation whose control and target are respectively the ith qubit of the second Toffoli ancilla system and the ith qubit of the auxiliary system, and $P_{0,T_2,i}$ and $P_{1,T_2,i}$ are respectively the projector to $|0\rangle$ and $|1\rangle$ on the ith qubit of the second Toffoli ancilla system. The bit flip error $X_{T_1,i}$ propagates through every bitwise Toffoli gate after its occurrence. The erroneous state corresponding to an occurrence of the bit flip error $X_{T_1,i}$ before the $(t + 1)$th bitwise Toffoli gate is as follows:

$$X_{T_1,i}(P_{0,T_2,i}|\bar{A}\rangle|\text{even}) \otimes |\bar{B}\rangle|\text{odd})$$

$$+ P_{0,T_2,i}|\bar{B}\rangle|\text{odd}) \otimes |\bar{A}\rangle|\text{even})$$

$$+ P_{1,T_2,i}|\bar{A}\rangle|\text{even}) \otimes |\bar{B}\rangle|\text{odd})$$

$$+ P_{1,T_2,i}|\bar{B}\rangle|\text{odd}) \otimes |\bar{A}\rangle|\text{even}) \otimes t + 1],$$

where $0 \leq k \leq t$, corresponding to its occurrence between kth and $(k + 1)$th bitwise Toffoli gates. When $k$ is nonzero, the parities of the third and fourth terms have us make the incorrect decision in distinguishing $|\bar{A}\rangle$ from $|\bar{B}\rangle$. This incorrect decision occurs with probability 0.5 for State (2), leading to the logical bit flip error on the third Toffoli ancilla system. When $k$ is zero, after the parity measurement, we obtain a state $X_{T_1,i}[P_{j,T_2,i}|\bar{A}\rangle + P_{j,T_2,i}|\bar{B}\rangle]$, where $j$ is 0 or 1, depending on the parities. With use of the equalities $P_0 = 1 + Z$ and $P_1 = 1 - Z$, this state can also be represented as $X_{T_1,i}[(1 + X_{T_3}) + (-1)^j Z_{T_3}(1 - X_{T_3})]|\bar{A}\rangle$. This representation shows that this state includes the logical bit flip error on the third Toffoli ancilla system. Furthermore, we obtain only unsuitable states through syndrome measurement for phase flip errors. Because of these error propagations through the bitwise CNOT and Toffoli gates, Shor’s construction cannot be considered fault-tolerant.

Now, as shown in Fig. 2, a modification of the ancilla preparation is proposed for fault-tolerance. BFEC represents error correction for bit flip errors, and it stops bit flip errors from propagating through controlled operations of the following cycles. BFEC operations after the last cycle are not necessary for fault-tolerance, and an operation of error correction for
FIG. 2. A fault-tolerant ancilla preparation for the logical Toffoli gate.

phase flip errors in the ancilla preparation is optional. With use of the equalities $P_0 = 1 + Z$ and $P_1 = 1 - Z$, State $\ket{\Pi}$ is rewritten as

$$X_{T_1, i}(\ket{\bar{A}} + \ket{\bar{B}})((\text{even}) + (\text{odd}))$$

$$+ Z_{T_2, i}(\ket{\bar{A}} - \ket{\bar{B}})((\text{even}) - (\text{odd})). \tag{3}$$

If we operate syndrome measurement for phase flip errors with this state, then we obtain either of $\ket{\bar{A}} + \ket{\bar{B}}$ or $Z_{T_2, i}(\ket{\bar{A}} - \ket{\bar{B}})$, depending on the syndrome. A sequence of the bitwise operations transforms $(\ket{\bar{A}} - \ket{\bar{B}})\ket{\text{cat}}$ into $\ket{\bar{A}}(\text{even}) - \ket{\bar{B}}(\text{odd})$, and we can obtain $\ket{\bar{A}}$ by operations according to a result of parity measurement. Therefore, the state $\ket{\bar{A}} - \ket{\bar{B}}$ is also suitable for an input state of the ancilla preparation, and we can insert error correction for phase flip errors in the ancilla preparation.

Some might think that the error propagations are not a problem, because error correction after every gate and storage prevents the sequential error propagations. However, frequent operations of error correction are not necessarily optimal, and can lead to a worse error rate [4]. Therefore, the requirement of prevention of the sequential error propagations, e.g., through error correction, is an important restriction.

III. AN EVALUATION OF ERROR RATES

We evaluate error rates and accuracy thresholds for a modified logical Toffoli gate, using the concatenated Steane codes. Our circuit for the logical Toffoli gate of the Steane code is shown in Fig. 3. EC represents error correction for both bit and phase flip errors. The cat states for the ancilla preparation are generated as shown in Fig. 4. The circuit enclosed by the dotted line creates a cat state of four qubits, which is used for error correction. The circuit enclosed by the dashed line, or the whole circuit provides a cat state of seven qubits,
FIG. 3. A fault-tolerant logical Toffoli gate of the Steane code.

which is used as an auxiliary system in the ancilla preparation. We use the outputs only when each measurement result is zero. In this analysis, we basically follow Gottesman’s method \[4\]. In particular, we use the following equation for error correction:

\[
p^{(j+1)} = 21[p^{(j)2} + 4p^{(j)}p_{EC}^{(j)} + 8p_{EC}^{(j)2}],
\]

where \(j\) means a level of concatenation, and \(p^{(j)}\) and \(p_{EC}^{(j)}\) correspond to errors occurring before and in syndrome measurement, respectively. In cases where we can prepare ancillary systems just in time, \(p_{EC}^{(j)} = 9p_{s}^{(j)} + 12p_{g}^{(j)}\), where \(p_{s}^{(j)}\) and \(p_{g}^{(j)}\) are rates of storage and gate errors for the \(j\)th level of concatenation, respectively. Furthermore, assuming the same rate for the gate and storage errors occurring on a bare qubit, i.e., \(p_{g}^{(0)} = p_{s}^{(0)}\), we obtain

\[
p_{g}^{(j)} = p_{s}^{(j)} = p_{th} \epsilon^{2^j},
\]

where \(p_{th} \approx 1.3 \times 10^{-5}\) and \(\epsilon = p_{g}^{(0)}/p_{th} = p_{s}^{(0)}/p_{th}\).

To obtain recurrence relations for error rates of adjacent levels of concatenation, we evaluate logical error rates with use of error rates for bare qubits. Logical errors come from errors accumulated on Toffoli ancilla systems, incorrect decisions in the majority vote of parities, and incorrect results of the measurement of data systems. Contributions of the
FIG. 4. Circuits for preparation of cat states consisting of four qubits (enclosed by the dotted line) and seven qubits (enclosed by the dashed line).

accumulated errors to logical errors are

\[
21[A_i^2 + 4A_ip_{EC} + 8p_{EC}^2] \\
+ 21[B_i^2 + 4B_ip_{EC} + 8p_{EC}^2] \\
+ 21[C_i^2 + 4C_ip_{EC} + 8p_{EC}^2] \\
+ 21[D_i^2 + 4D_ip_{EC} + 8p_{EC}^2],
\]  

(6)

where \(A_i, B_i, C_i,\) and \(D_i\) are rates of bit or phase flip errors accumulated on each qubit of the \(i\)th Toffoli ancilla system, respectively corresponding to the period between the preparation of \(|000\rangle\text{cat}\) and the first EC operations, between the first and the second EC operations, between the second and the third EC operations, and between the third and the last EC operations.
operations. We can evaluate $A_i, B_i, C_i$ and $D_i$ as follows:

\begin{align*}
A_{1, \text{bit}} &= p_s + p_g + p_{T1, \text{bit}}, \\
A_{2, \text{bit}} &= p_s + p_g + p_{T2, \text{bit}}, \\
A_{3, \text{bit}} &= t_T p_s + 2p_g, \\
B_{1, \text{bit}} &= C_{1, \text{bit}} = 2p_s + p_{T1, \text{bit}}, \\
B_{2, \text{bit}} &= C_{2, \text{bit}} = 2p_s + p_{T2, \text{bit}}, \\
B_{3, \text{bit}} &= C_{3, \text{bit}} = (t_T + 1)p_s + p_g, \\
D_{1, \text{bit}} &= D_{2, \text{bit}} = (t_m + 2)p_s + 2.5p_g, \\
D_{3, \text{bit}} &= (2t_m + 3.5)p_s + 4.75p_g, \\
A_{1, \text{ph}} &= 2p_s + 4p_g + p_{T1, \text{ph}} + p_{\text{cat, bit}}, \\
A_{2, \text{ph}} &= 2p_s + 4p_g + p_{T2, \text{ph}} + p_{\text{cat, bit}}, \\
A_{3, \text{ph}} &= t_T p_s + 3p_g + p_{\text{cat, bit}}, \\
B_{1, \text{ph}} &= C_{1, \text{ph}} = 4p_s + 2p_g + p_{T1, \text{ph}} + p_{\text{cat, bit}}, \\
B_{2, \text{ph}} &= C_{2, \text{ph}} = 4p_s + 2p_g + p_{T2, \text{ph}} + p_{\text{cat, bit}}, \\
B_{3, \text{ph}} &= C_{3, \text{ph}} = (t_T + 1)p_s + 2p_g + p_{\text{cat, bit}}, \\
D_{1, \text{ph}} &= (2t_m + 3.75)p_s + 4p_g, \\
D_{2, \text{ph}} &= (2t_m + 3.75)p_s + 4.25p_g, \\
D_{3, \text{ph}} &= (t_m + 1.5)p_s + 3p_g, 
\end{align*}

where $t_T$ and $t_m$ are operation times of the Toffoli gate and the measurement, and $p_{Ti, \text{bit}}$ and $p_{Ti, \text{ph}}$ are respectively the bit and phase flip error rates of the Toffoli gate corresponding to either of two controls ($i = 1, 2$) or the target ($i = 3$). The error rate $p_{\text{cat, bit}}$ corresponds to the bit flip error on each qubit of auxiliary systems of seven-qubit cat states.

Next, we go on to a rate of the incorrect decisions in the majority vote of parities. The rate of the parity error for the first auxiliary system is $p_{\text{cat, ph}} + 7(2p_s + 5p_g + p_{T3} + p_m)$, where $p_{\text{cat, ph}}$ is the total error rate for phase flip errors on the prepared seven-qubit cat state, but not the error rate for each qubit of the system, and $p_m$ is the error rate of the measurement. Each rate of the parity error for the second and third auxiliary systems is
\( p_{\text{cat,ph}} + 7(5p_s + 2p_g + p_{T3} + p_m) \). Therefore, the error rate of the parity majority vote is

\[
2[p_{\text{cat,ph}} + 7(2p_s + 5p_g + p_{T3} + p_m)] \\
\times [p_{\text{cat,ph}} + 7(5p_s + 2p_g + p_{T3} + p_m)] \\
+ [p_{\text{cat,ph}} + 7(5p_s + 2p_g + p_{T3} + p_m)]^2. 
\] (24)

This error rate is added only to the logical bit flip error rate of the third Toffoli ancilla system.

Finally, we view error rates of the measurement of data systems. The error of the measurement of the first data system leads to the first and third logical bit flip errors and the second logical phase flip error; the error of the measurement of the second data system leads to the second and third logical bit flip errors and the first logical phase flip error. These error rates are \( 21[p_s + p_g + p_m]^2 \). The error of the measurement of the third data system leads to the first, second, and third logical phase flip errors, and its error rate is \( 21[0.5p_s + 2.5p_g + p_m]^2 \).

Adding the above rates of the accumulated errors, the error of the majority vote, and the errors of the measurement of data systems, we obtain representations of the logical error rates with the error rates for bare qubits. Using these representations, we obtain the recurrence relations for error rates of adjacent levels of concatenation. To calculate the error rates of each level, we evaluate the following time step and error rates: \( t_T = 6 \), \( p_{\text{cat,bit}} = 5p_s + p_g \), and \( p_{\text{cat,ph}} = 26p_s + 20p_g \). Assumptions for the time step and error rate of the measurement are also made as follows: \( t_m = 1 \) and \( p_m = p_g \). We also calculate error rates for the three operands of the Toffoli gate of the zeroth level of concatenation on the basis of a decomposition [15] into two-qubit operations (See Fig. 5). This decomposition gives the following error rates:

\[
p^{(0)}_{T1,\text{bit}} = 2p_s^{(0)} + 3p_g^{(0)}, 
\]

\[
p^{(0)}_{T2,\text{bit}} = 2p_s^{(0)} + 5p_g^{(0)}, 
\]

\[
p^{(0)}_{T3,\text{bit}} = 6p_s^{(0)} + 9p_g^{(0)}, 
\]

\[
p^{(0)}_{T1,\text{ph}} = 4p_s^{(0)} + 10p_g^{(0)}, 
\]

\[
p^{(0)}_{T2,\text{ph}} = 3p_s^{(0)} + 7p_g^{(0)}, 
\]

\[
p^{(0)}_{T3,\text{ph}} = 3p_s^{(0)} + 5p_g^{(0)}. 
\]

(25) (26) (27) (28) (29) (30)

The error rates of the Toffoli gate for each level are shown in Table I with the omission of multiplication by \( 10^{-5} \varepsilon^2 \). The error rates of the Toffoli gates are monotonically decreasing in
FIG. 5. A decomposition of the Toffoli gate into two-qubit operations. $V = e^{-i\frac{\pi}{4}}e^{i\frac{\pi}{4}}X$.

TABLE I. The error rates of the Toffoli gates of the concatenated Steane codes with the omission of multiplication by $10^{-5}e^{2^j}$. We can obtain each error rate by multiplying the value in the table and $10^{-5}e^{2^j}$.

| $j$ | $P_{T1,\text{bit}}$ | $P_{T2,\text{bit}}$ | $P_{T3,\text{bit}}$ | $P_{T1,\text{ph}}$ | $P_{T2,\text{ph}}$ | $P_{T3,\text{ph}}$ |
|-----|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 0   | 6.5                 | 9.1                 | 20                  | 18                  | 13                  | 10                  |
| 1   | 5.9                 | 6.1                 | 8.3                 | 8.4                 | 7.8                 | 6.8                 |
| 2   | 5.8                 | 5.8                 | 7.2                 | 7.4                 | 7.3                 | 6.8                 |
| 3   | 5.8                 | 5.8                 | 7.1                 | 7.3                 | 7.3                 | 6.8                 |
| 4   | 5.8                 | 5.8                 | 7.1                 | 7.2                 | 7.3                 | 6.8                 |
| 5   | 5.8                 | 5.8                 | 7.1                 | 7.2                 | 7.3                 | 6.8                 |

levels of concatenation, and are 4.5 to 5.6 times of the error rate of transversal operations for sufficiently large levels of concatenation. On the basis of the monotonic decreases of the error rates, we can conclude that an accuracy threshold of the Toffoli gates of the concatenated Steane codes is same as transversal operations.

IV. CONCLUSION

In this paper, it has been shown that logical errors are generated through error propagations in the ancilla preparation of Shor’s construction for the logical Toffoli gate of a family of the CSS codes which has even-weight stabilizer generators and odd-weight logical operators. To solve this problem, a modification of the inserts of bit flip error correction has been proposed. The requirement of prevention of the sequential error propagations is an important restriction on optimization of frequency of error correction. Finally, error rates of a modified logical Toffoli gate have been evaluated with use of the concatenated Steane
codes, and the same accuracy threshold as transversal gates has been obtained. Previous proposals of fault-tolerant computation with use of Shor’s construction of the logical Toffoli gate should be revisited. This work would be helpful for reevaluations of the previous proposals and for future works.

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