High Throughput Multidimensional Tridiagonal Systems Solvers on FPGAs

Kamalavasan Kamalakkannan, Istvan Z. Reguly, Suhaib A. Fahmy and Gihan R. Mudalige

Abstract—This paper presents a design space exploration for synthesizing optimized, high-throughput implementations of multiple multi-dimensional tridiagonal system solvers on FPGAs. Re-evaluating the characteristics of algorithms for the direct solution of tridiagonal systems, we develop a new tridiagonal solver library aimed at implementing high-performance computing applications on Xilinx FPGA hardware. Key new features of the library are (1) the unification of standard state-of-the-art techniques for implementing implicit numerical solvers with a number of novel high-gain optimizations such as vectorization and batching, motivated by multiple multi-dimensional systems common in real-world applications, (2) data-flow techniques that provide application specific optimizations for both 2D and 3D problems, including integration of explicit loops commonplace in real workloads, and (3) the development of a predictive analytic model to explore the design space, and obtain rapid resource and performance estimates. The new library provide an order of magnitude better performance when solving large batches of systems compared to Xilinx’s current tridiagonal solver library. Two representative applications are implemented using the new solver on a Xilinx Alveo U280 FPGA, demonstrating over 85% predictive model accuracy. These are compared with a current state-of-the-art GPU library for solving multi-dimensional tridiagonal systems on an Nvidia V100 GPU, analyzing time to solution, bandwidth, and energy consumption. Results show the FPGAs achieving competitive or better runtime performance for a range of multi-dimensional mesh problems compared to the V100 GPU. Additionally, the significant energy savings offered by FPGA implementations, over 30% for the most complex application, are quantified. We discuss the algorithmic trade-offs required to obtain good performance on FPGAs, giving insights into the feasibility and profitability of FPGA implementations.

Index Terms—Multidimensional tridiagonal solvers, high level synthesis, field programmable gate arrays.

1 INTRODUCTION

Tridiagonal systems of equations are solved in a wide range of High Performance Computing (HPC) applications, particularly as part of the numerical approximation of multi-dimensional partial differential equations (PDEs). In computational finance, the frequently used Alternating Direction Implicit (ADI) time discretization (see Paceman and Rachford [19], and Douglas and Gunn [10]) leads to the need to solve multiple tridiagonal systems of equations in each dimension. In computational fluid dynamics (CFD), tridiagonal systems form the core component for solving incompressible fluid flow problems [27] and design of turbomachinery [7], among others. The large number of independent tridiagonal systems, often in multiple dimensions, offer significant parallelization opportunities on modern multi-core and many-core architectures. Recent works such as László et al. [13] demonstrated significant speedups, re-evaluating the well known tridiagonal solver algorithms, Thomas [24], PCR [11], and their combinations.

In this paper we evaluate the parallelization opportunities afforded by tridiagonal systems solver algorithms on modern FPGA hardware devices. The data-flow parallelism targeted in an FPGA provides significant scope to exploit the parallelism inherent in tridiagonal solvers. As such, our underlying goal is to understand the criteria for a given system solver to be amenable to FPGA implementation and uncover the limitations and profitability of such accelerators. Previous work on tridiagonal system solvers for FPGAs utilized both low-level hardware description languages [18], [28], [31] as well as high-level synthesis tools [3], [14], [15], [16], [29]. They demonstrated implementation of standard tridiagonal system solver algorithms (Thomas, PCR, and Spike), evaluating how to best utilize FPGA resources to maximize performance. However, many of these previous works only develop single system solvers in isolation without a design strategy that can be applied for multiple systems and multi-dimensions in general and do not utilize higher-gain optimizations for real-world applications. Some apply application specific optimizations which are not developed as general synthesis techniques. Comparison of performance to traditional architectures such as GPUs are also limited in current literature, minimizing insights into the utility of FPGAs for this class of applications. A key gap is the lack of a unifying design strategy particularly focusing on realistic, non-trivial applications.

In this paper we attempt to bridge this gap with a unifying workflow for designing near-optimal FPGA implementations for these implicit numerical solvers, applied to the solution of real-world multi-dimensional applications. More specifically we make the following contributions:

- We consider the standard tridiagonal solver algorithms together with state-of-the-art FPGA implementations and re-examine the algorithmic trade-offs
required for obtaining optimized, high-throughput solutions for multiple solves in multiple dimensions. We propose a design and optimization strategy for developing FPGA implementations selecting the best designs, based on problem size, dimensionality, number of systems solved and data-flow paths required, including the utilization of High Bandwidth Memory (HBM) on modern devices for combining multiple dimension solves and explicit loops in applications. A key optimization, novel in this area is the batched execution of multiple independent solves on FPGAs, leading to superior performance compared to the state-of-the-art, the current Xilinx tridiagonal solver library.

• Targeting current generation Xilinx FPGAs we implement our designs to produce a new tridiagonal solver library that can be used in the solution of multi-dimensional applications. Using this, we present the optimized design of two non-trivial applications, a 2D and 3D ADI heat diffusion solve, implemented with both single precision (FP32) and double precision (FP64) floating point representations, and a 2D Stochastic-Local Volatility (SLV) model application from the financial computing domain. Given hardware resource constraints, we focus on features of the applications that are amenable for FPGA implementation and optimizations for gaining near-optimal, high throughput performance.

• We develop a predictive analytic model that provides estimates for application runtime giving insights into the profitability of implementing the tridiagonal system solvers on Xilinx FPGAs using our design strategy. The model predicts the runtime performance considering system/batch sizes and optimizations implemented together with memory requirements and operating frequency. Runtime predictions from the model are shown to be within 15% of the achieved runtime on evaluated applications.

• Finally, the runtime, bandwidth, and energy performance of the FPGA implementations on a Xilinx Alveo U280 are compared with a state-of-the-art multi-dimensional tridiagonal solver library for GPUs on the HPC-grade Nvidia V100 GPU.

Results on the U280 FPGA demonstrate competitive performance compared to the best performance achieved for the same application on the GPU using both FP32 and FP64 representations. To our knowledge the extended workflow, new library, predictive model and the superior performance demonstrated for the above applications in this paper present key innovations, advancing the state-of-the-art. We believe our design path provides a promising strategy for use with industrial workloads, particularly from the financial computing domain, significantly reducing the complexity of the development cycle for these platforms.

The rest of the paper is organized as follows: Section 2 presents a brief overview of tridiagonal solver algorithms together with previous work on synthesizing tridiagonal solvers on FPGAs, including the current state-of-the-art. Section 3 presents our proposed design strategy, as a step-by-step methodology, starting from the basic algorithms, down to target FPGA code for the Xilinx Alveo FPGAs. A performance analysis and benchmarking of the FPGA implementations compared to the GPU performance is presented in Section 4. Finally, conclusions are presented in Section 5.

2 Background

Tridiagonal systems arise from the need to solve a system of linear equations as given in equation (1), where

\[ a_i u_{i-1} + b_i u_i + c_i u_{i+1} = d_i, \quad i = 0, 1, ..., N - 1 \]

\[ \begin{bmatrix} b_0 & c_0 & 0 & \cdots & 0 \\ a_1 & b_1 & c_1 & \cdots & 0 \\ 0 & a_2 & b_2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & a_{N-1} & b_{N-1} \end{bmatrix} \begin{bmatrix} u_0 \\ u_1 \\ u_2 \\ \vdots \\ u_{N-1} \end{bmatrix} = \begin{bmatrix} d_0 \\ d_1 \\ d_2 \\ \vdots \\ d_{N-1} \end{bmatrix} \]  

(2)

The solution to such systems of equations is well known. The Thomas algorithm [24] carries out a specialized form of Gaussian elimination providing the least computationally expensive solution, but suffers from a loop carried dependency (see Algo. 1). It has a time complexity of \( O(N) \).

Algorithm 1: thomas(a, b, c, d)

1: \( d_0' \leftarrow d_0 / b_0 \)
2: \( c_0' \leftarrow c_0 / b_0 \)
3: for \( i = 1, 2, ..., N - 1 \) do
4: \( r \leftarrow 1 / (b_i - a_i c_{i-1}') \)
5: \( d_i' \leftarrow r(d_i - a_i d_{i-1}') \)
6: \( c_i' \leftarrow r c_i \)
7: end for
8: for \( i = N - 2, ..., 1, 0 \) do
9: \( d_i \leftarrow d_i' - c_i'd_{i+1} \)
10: end for
11: return \( d \)

In contrast, the PCR algorithm [11] (Algo. 2), operates on a normalized matrix so that \( b_i = 1 \) and then for each matrix row \( i \), subtracts multiples of rows \( i, i+2 \), \( i+2 \), ..., \( 2^{P-1} - 1 \), where \( P \) is the smallest integer such that \( 2^P \geq N \). This leads to each iteration reducing each of the current systems into two systems of half the size (see Fig 1). After \( P \) steps, all of the modified \( a \) and \( c \) coefficients are zero, leaving values for the unknowns \( u_i \). In PCR, the iterations of the inner loop do not depend on each other, which is well suited for traditional multi-core/many-core architectures.
such as CPUs and GPUs allowing multiple threads to be used to solve each tridiagonal system. However, PCR has a complexity of $O(N \log N)$ and is more computationally expensive than the Thomas algorithm, which for an FPGA implementation poses an important consideration, (which we will examine in Section 3) due to the limited availability of resources.

The Spike algorithm [20] decomposes the $A$ matrix, into $p$ partitions of size $m$ to obtain the factorization of $A = DS$ where $D$ is a main diagonal block matrix consisting of tridiagonal matrices $A_1,...,A_p$ and $S$ is the so called spike matrix as given in equation (3), where $A_i V_i = \{0 \ldots 0 B_i\}^T$ and $A_i W_i = \{C_i 0 \ldots 0\}^T$.

$$DS = \begin{bmatrix}
A_1 & & & \\
& A_2 & & \\
& & \ddots & \\
& & & A_p \\
I & W_2 & I & V_2 \\
& & \ddots & \ddots & \ddots \\
& & & W_{p-1} & I & V_{p-1} \\
& & & & W_p & I
\end{bmatrix}$$

The solution to the system then becomes, $DSx = d$ where the system $DY = d$ can be used to obtain $Y$, and $Sx = Y$ to obtain $x$. Since matrix $D$ is a simple collection of $A_i$, each $A_i Y_i = d_i$ can be solved independently. Solving $Sx = Y$ requires only solving a reduced penta-diagonal system (see Wang et al. [26] for a detailed description). The algorithm therefore operates in three steps: factorization, reduced system solve, and back substitution, where the factorization (LU and UL) has a complexity of $O(N)$. The reduced system can be solved directly or indeed can be further reduced to a block diagonal system using the truncated-spike variation that ignores the outer diagonals when $A$ is diagonally dominant. The Spike algorithm is particularly well suited for solving very large systems on traditional architectures.

2.1 Multiple Tridiagonal Systems in 2D/3D

Each of the above algorithms specifies the solution of a single tridiagonal system, which is characteristically a one dimensional problem. However, applications of interest are usually 2 or 3 dimensional, where tridiagonal systems are formed by solving along one of the coordinate axes. This leads to a number of independent systems based on the number of discretization points along the other axis. For example a 3D system with $N_x \times N_y \times N_z$ number of mesh points will have $N_y \times N_z$ number of tridiagonal systems in the first dimension (each system with size $N_x$), $N_x \times N_z$ in the second (each with size $N_y$) and so on. The ADI method, included in the applications we present in this work, repeatedly solve tridiagonal systems along these different axes. Here, the $a_i, b_i, c_i$ and $d_i$ coefficients are calculated for each grid point, in a way that matches the underlying data structure of the application; data is stored contiguously in one row-major (Z is contiguous, Y, X are strided) or more commonly a column-major (X is contiguous, Y and Z are strided) format. This poses a challenge for algorithms that then solve multiple tridiagonal systems simultaneously; coefficients for an individual system will be laid out differently, depending on the direction of the solve. This is especially true on traditional architectures such as CPUs or GPUs [13]. An FPGA design must also carefully consider memory performance when solving such multi-dimensional applications.

2.2 Related Work

Earlier works implementing tridiagonal system solvers on FPGAs such as by Oliveira et al. [18], Warne et al. [28] and Zhang et al. [31] used low-level Hardware Description languages (HDL) such as VHDL or Verilog for implementing the Thomas algorithm. HDLs require extensive hardware knowledge and time/effort in development. These designs were restricted to solving 1D or 1D batched tridiagonal systems, instead of full multi-dimensional applications. However Oliveira et al. [18] pipelined both the forward and backward loops and applied data flow between them and demonstrated the implementation for a smaller $16^2$ mesh based application using only on-chip memory.

With the introduction of High-Level synthesis (HLS) tools, a number of more recent works [14], [15], [16], [29] implemented the Thomas, PCR, and Spike algorithms on FPGA using HLS tools. Many of these works did not demonstrate the solver working on full applications, with the exception of László et al. in 2015 [14] which compared a one factor Black-Scholes option pricing equation using explicit and implicit methods on different architectures such as multi core CPUs, GPUs, and FPGAs. The solution by László et al. in 2015 [14] based on the Thomas algorithm, targets a Xilinx Virtex 7 FPGA and effectively pipelines both forward and backward loops but was not able to apply data flow between these two steps. The authors give estimated resource consumption and runtime using Vivado HLS for both FP32 and FP64 implementations. Comparing the estimated FPGA runtime to a Nvidia K40 GPU shows that the GPU significantly outperforms the FPGA.

Macintosh, et al. in 2014 [16] uses an OpenCL based implementation targeting an Altera Stratix V FPGA using PCR and Spike algorithms. The performance on the FPGA is compared to a CPU implementation on an Nvidia Quadro 4000 GPU. The FPGA performance with PCR is shown to be comparable to that of the GPU, but the Spike algorithm on the FPGA outperforms the GPU. Similarly Macintosh, et al. in 2019 [15] uses OpenCL to develop oclspkt, a library that implements tridiagonal systems solvers targeting FPGAs, GPUs, and CPUs. oclspkt uses the truncated spike algorithm, and as such will not give exact solutions. However it is able to solve tridiagonal systems of any size, taking advantage of interleaved host to device transfer to hide the PCIe latency. The work also develops a Thomas algorithm based solver that handles larger tridiagonal systems, but does not consider pipelining of forward and backward loops. These loops communicate through external memory, further limiting achievable performance. Results show the FPGA (an Altera Arria 10GX on the Bittware A10PL4 board)
performing marginally slower than the GPU (a Nvidia M4000) but providing better energy efficiency.

The Xilinx quantitative finance library [3] provides a PCR based solver, which is a templated implementation for data type, system size steps and vectorization. It must be recompiled for different configurations of the above parameters. The use of PCR means it requires more FPGA resources due to the higher computational intensity of the algorithm. The Xilinx library also implements a Douglas FPGA solver [10] which to our knowledge represents a state-of-the-art application implemented with a multi-dimensional solver on a Xilinx FPGA.

In comparison to above work, the HLS-based synthesis presented in this paper, targets the solution of multiple tridiagonal systems and in multiple dimensions as commonly found in real-world applications. It uses the Thomas algorithm demonstrating that together with techniques such as batching [12] of systems, it provides higher throughput for small and medium sized systems. The Thomas algorithm requires a relatively smaller amount of DSP resources than the more computationally intensive PCR algorithm. For larger systems that do not directly fit in a single FPGA, we develop novel Thomas-Thomas and Thomas-PCR solvers to handle a number of partitioned systems and then a reduced system solve so that it can operate with the available limited on-chip memory of a single FPGA. A further innovation is the use of High Bandwidth Memory (HBM) on modern FPGAs which helps to scale the design to multiple compute units. To our knowledge, the 2D/3D ADI and SLV applications developed in this work, motivated by real-world implicit problems on FPGAs is also novel; SLV being one of the few non-trivial applications using multi-dimensional tridiagonal solvers presented in literature. The Thomas based solver developed in this paper gives higher performance than the current PCR based Xilinx library, as we will show in Section 4. The Thomas algorithm is better suited for obtaining high-throughput when solving batches of tridiagonal systems than PCR. Douglas ADI solver from Xilinx is also based on PCR. Thus, it would be similarly less performant, although implementing a different numerical method, than the ADI solvers in our work. Additionally, the predictive analytic model and the performance comparison with a state-of-the-art GPU based tridiagonal solver library gives a much needed frame of reference for evaluating our FPGA design’s performance, providing insights into the feasibility and profitability of an FPGA design for realistic workloads.

3 FPGA DESIGN

An FPGA use a multiple-instructions, single data (MISD) architecture to implement computation, be it a single kernel or a series of kernels. There is no fixed general purpose architecture that can be exploited using software as a traditional CPU or GPU does. Instead a fixed circuit of the architecture that can be exploited using software as a training process. The overall die consists of a number of these which are called Super Logic Regions (SLR). The U280 has 3 SLRs. Bandwidth within an SLR is extremely high (TB/s) due to the wealth of connections and memory elements, while between SLRs it is limited by the number of silicon connections available. An FPGA board will also include much larger, but slower DDR4 (32 GB on the U280) memory as external memory. Managing the movement of data between these different types of memory is key to achieving high computational performance. The introduction of High-Level Synthesis (HLS) tools has reduced the complexity of FPGA programming, where a high-level programming language such as C++/OpenCL can be used with special directives to target the FPGA. However, getting good performance is still significantly challenging as code needs to be structured to suite the data-flow/pipelined programming style. The key optimizations required to obtain the best performance are transformations enabling pipelining, replication of circuit units (CUs) and tiling to improve locality such that data can be reused by fitting to fast on-chip memory. For a good overview of these techniques we refer the reader to the paper by De Matteis et al. [9] and the Xilinx HLS programming guide [2].

Considering the resources available on an FPGA, a single tridiagonal system solve, using the Thomas algorithm in Algorithm 1, would require 4 multiplications, 1 division and 2 subtractions for the forward path (lines 3-7) and one multiplication and subtraction for the backward path (lines 8-10). However, given that there are dependencies for computing $d^*_l$ and $c^*_l$, each iteration of the forward path loop will have to be executed serially, incurring the full arithmetic pipeline latency. Thus the total latency for solving a single system with the Thomas algorithm would be approximately $l_f \times N + b_f \times N$ clock cycles (assuming $b_f$ cycles is the arithmetic pipeline latency for completing a single iteration of the backward loop). On the other hand, a PCR based single solver implementation would require 2 subtractions, 9 multiplications and 1 division within the inner loop of Algorithm 2. If $l$ is the arithmetic pipeline latency of the inner loop, then the total number of clock cycles for the PCR algorithm, is $(N+l) \times \log N$. Here we assume that the outer loop is executed serially. Given the inner loop iterations are independent, they can be unrolled by some factor $f U = 2, 3, ...$ which will then require $f U \times$ the resources to implement the inner loop. The total clock cycles will then be $(N/f U + l) \times \log N$. The outer loop iterations have a dependency and thus cannot be unrolled.

For the Thomas solver, there are $l_f$ clock cycles between consecutive iterations of a single system solve in the forward path. This can be considered as a dependency distance. As such, we could attempt to solve $l_f$ number of tridiagonal systems to fully utilize the forward path circuit pipeline. This can be done by interleaving the iterations of the forward pass loop of of the Thomas solver such that iteration 1 of system 1 is input followed by iteration 1 of system 2 and so on, per clock cycle, up to iteration 1 of system $l_f$. In fact selecting a group, $g = \text{MAX}(l_f, b_f)$ enables $g$ system solves to be interleaved, saturating the pipeline. If there are
number of total tridiagonal systems to be solved, i.e. a batch size of \( B \), then the total latency with Thomas can be shown to incur a latency given by (4):

\[
(1 + \lceil B/g \rceil) \times gN
\]  

(4)

Thus for large \( B \) the total latency tends to be \( BN \). This is a characteristic of all \( O(N) \) algorithms, which ideally can be pipelined to take input each clock cycle at the cost of differing resource consumption.

For the PCR algorithm, given there are no dependencies between iterations of a single system, solving a batch of \( B \) systems (by matching the inner loop) incurs the latency in (5):

\[
(BN/f_U + l) \times \log N
\]  

(5)

For large \( B \), dividing (5) by (4) gives a factor of \( \log N/f_U \) pointing to the fact that the batched Thomas solver is \( \log N \) times faster than batched PCR, for \( f_U = 1 \). Thus, to match the Thomas solver latency, a batched PCR implementation needs an unroll factor \( f_U = \log N \). However, given that the PCR inner loop has a considerably larger resource requirement, compared to the Thomas solver, on a given FPGA with fixed amount of resources, the batched Thomas solver will always provide better performance. The exception occurs when the system size, \( N \) is large and FPGA on-chip memory becomes the limiting factor. We discuss the design and best algorithms for such cases in Sec 3.1.

Considering a batched solver based on the spike algorithm, assume each system in the batch is of size \( N \). The algorithm creates \( m \) number of blocks and each has \( LU \) and \( UL \) factorization done in parallel, followed by the pentagonal solve and then back-substitution in parallel. This incurs a total latency given by (6):

\[
(1 + \lceil Bm/g + 1 \rceil) \times gN/m + mC
\]  

(6)

The latency for the factorization for each block (first term), is similar to a Thomas forward and backward solve carried out in an interleaved manner. Although the number of cycles spent on the pentagonal reduced system solve is \( BmC \) (assuming a linear latency model) and back substitution is \( BN \) only the latency for first stage of pentagonal solver is added to equation 6 as all three modules are pipelined. Back substitution does not add additional delay between its inputs and outputs. When \( B \) is sufficiently large and stages are pipelined, a latency of \( BN \) is achieved. Again this is due to the spike algorithm having a \( O(N) \) complexity. However, if \( BmC \geq BN \) then data flow must stall for some time decreasing throughput. Considering resource consumption the \( LU/UL \) factorization requires \( 3 \times \) the resources for an equivalent Thomas solver and the pentagonal solver requires additional resources (again more than an equivalent Thomas solver).

Given the lower resource requirements and profitability of the Thomas algorithm, compared to the other algorithms, we first focus on its optimized batched implementation on an FPGA for system sizes that can fit into on-chip memory. As we are interleaving groups of \( g \), the \( a_{i-1}, b_{i-1} \) and \( c_{i-1} \) values needs to be stored in on-chip memory such that they can be used in subsequent \( (i\text{-th}) \) iterations. For a FP32 implementation we have found that a grouping of 32 is sufficient to effectively pipeline the computation (this is 64 for FP64) on the Xilinx Alveo U280. The forward and backward loops operate in opposite directions and thus a First-In-First-Out (FIFO) buffer cannot be used, rather on-chip addressable memory is used for data movement. The forward and backward loops can be made to operate in parallel when batching a number of system solves, using ping-pong buffers (also called double buffers). With this technique, dual port memory is partitioned into two parts, one for the writing process the other for the reading. Once writes (by the forward pass) and reads (backward pass) are completed, read and write locations are swapped. Note that the very first read has to wait till the very first write has completed. Additionally, the technique also doubles the memory requirement compared to using the same memory portion for both read and write. Including the latency for starting the first write to the ping-pong buffer, and writing back the final result to external memory increases the total latency in (4) by \( 2gN \) to give: \( (3 + \lceil B/g \rceil) \times gN \) clock cycles.

The total on-chip memory required for a single Thomas solver interleaving \( g \) systems can be computed based on the need to store the \( a, c, d, c^*, d^* \) and \( u \) vectors, where each consumes \( 2gN \) words in the ping-pong buffers. The total \( 12gN \) requirement with dual port memory can be satisfied with \( 6 \times \) dual port block RAMs (URAM/BRAM) each with a capacity of \( 2gN \). Additionally there is a need to store \( g \) values of the \( i \) and \( i+1 \)th iteration separately, requiring \( 4 \) RAMs with a capacity of \( g \) words.

Data transfer from external memory to on-chip memory plays a crucial part in achieving high performance, especially for multi-dimensional solvers such as the 3D ADI heat diffusion application detailed later in this paper. If we consider a 3D application with systems sizes \( (N) \) of 256 in all three dimensions, then a solve along the \( x \)-dimension will have \( YZ \) (256 \( \times \) 256 in this case) number of systems to be solved, each corresponding to an \( x \)-line system of size 256. Given the data is stored in consecutive memory locations along the \( x \)-lines, good memory throughput can be achieved. However to exploit the full memory bandwidth, a larger number of memory ports needs to be used. For the 512-bit memory ports, on the Alveo U280, it is sufficient to saturate the data-flow pipeline with a width of 256-bits at a 300MHz clock speed, which is our target frequency. This enables us to fetch data sufficient to feed 8 Thomas solvers in parallel. Such a configuration can be viewed as a vectorized Thomas solver. Additionally, the total \( YZ \) number of \( x \)-lines can be set up to be solved in groups \( (g) \) of 32. Here, the 1st Thomas solver circuitry solves the 0th, 8th, 16th and so on, while the 2nd solves 1st, 9th, 17th and so on on \( x \)-lines, and so on. Batches of \( x \)-lines can be solved in such interleaved groups to saturate the data flow pipeline to achieve higher throughput.

In the \( x \)-dimension, the reads from external memory bring in data stored in consecutive memory locations. However, the data fetched belongs to the same line (i.e. same system), thus we need to buffer 8 \( x \)-lines internally and carry out an \( 8 \times 8 \) transpose to feed that to 8 different solvers (see Fig. 2a for an illustration of the issue with a \( 4 \times 4 \) transpose). For solving along the \( y \)-dimension, we fetch each \( XY \) plane to on-chip memory to avoid strided memory accesses and then read along the \( y \)-lines from the on-chip memory (see Fig. 2b). Similarly for solving along the \( z \)-dimension, we read in \( x \)-lines (which are consecutive
in memory) along the z dimension, fetching XZ planes, to on-chip memory. No transpose is required for y- and z-dimension solves as each element corresponds to a different system. Utilizing the HBM available on modern FPGAs, the full vectorized Thomas solver, which can be viewed as a single compute unit (CU), can be instantiated a number of times to obtain further parallel performance. Specific designs for applications with multiple CUs are discussed in Section 4. For a 3D application, the x- and y-dimension solves can be effectively pipelined, storing the resulting XY planes on-chip memory without writing to external memory. However the z-dimension solve requires reading from external memory. As such 2D applications can be further optimized with unrolling. Again we will discuss specific implementations with unrolling in Section 4.

3.1 Larger Systems Solve

Interleaved solving of systems require on-chip memory proportional to the system size, \( N \) and number of groups \( g \). As such the maximum size of the system that can be solved is limited by the FPGA on-chip memory resources. We can split the tridiagonal system into subsystems (or tiles) of size \( M \) where each subsystem can be solved using a modified Thomas solver, where after a forward and backward phase, each unknown is expressed in terms of two unknowns \( u_o \) and \( u_{M-1} \):

\[
a_iu_0 + u_i + c_iu_{M-1} = d_i, \quad i = 1, 2, \ldots, M - 2
\]

This results in a reduced tridiagonal system spread across each sub-domain as can be seen in Fig 3 (as detaited by László et al. [13]). The unknowns at the beginning and end of each subsystem can be solved again using the Thomas algorithm, or indeed PCR. Finally, the result from the reduced system, is substituted back into the individual subsystems (see László et al. [13] which implements a Thomas-PCR solver for GPUs).

The tiled-Thomas-Thomas solver requires additional circuitry implemented to solve the reduced system, but larger systems can be solved. To achieve higher performance, forward and backward phases over tiles can be interleaved. The reduced system size \( N_r \) is double the number of tiles. Solving the reduced system with Thomas requires \( 2gN_r \) clock cycles. This should not exceed the clock cycles taken

\[
(2 + [Bt/g]) \times [N/t]g + g_r \times (2t) \times 2
\]

The second term is for the reduced solve. The \( g_r \) is similar to \( g \), but it is equal to or larger than number of interleaved systems for the reduced solve. It is 32 for FP32 and 64 for FP64 on the U280. Similarly, based on the latency for solving the first phase of the algorithm on a tile, the number of systems to be interleaved is \([32/t]\) for FP32 and \([64/t]\) for FP64. For larger \( B \), we can see that the latency tends to \( Bt[N/t] \). Considering on-chip memory requirements the forward and backward phases of the modified Thomas can be shown to require \( 9 \times 2 \times g/t \times N \) words that can be satisfied by 9 RAMs setup as ping-pong buffers. Here we note that larger \( t \) lead to lower memory requirement. The reduced solve requires much less memory, \( 7 \times 2 \times 2t \times [g/t] \) in the form of 7 ping pong buffers. Furthermore, a FIFO buffer space would be required, equivalent to the maximum clock cycles spent on the reduced system, as we have to flush each point per clock cycle from the backward phase.

The reduced system solve can also be implemented with the PCR algorithm resulting in the latency given in (9).
Again for larger B, this tends to $Bt[N/t]$, however, there is a lower on-chip memory requirement of $(2t + l) \times \log(2t)$ words for each of 3 FIFO buffer, due to the lower latency for reduced system solve in PCR. Since data flow design requires matching performance of solving tiles and the reduced system and as PCR is faster when solving reduced systems, the number of tiles can be increased even for smaller systems, further reducing requirement for on chip memory for the first phase of the algorithm. As such we can conclude that the Thomas-PCR version would result in better performance.

4 Performance

In this section we present performance from our FPGA design strategy for high-throughput tridiagonal system solvers. First, we briefly compare the performance of our library to a current state-of-the-art FPGA tridiagonal solver library from Xilinx [3] which is based on PCR, demonstrating the higher performance gains from a batched Thomas-based solver as predicted by the analytic model developed in Section 3. Batching of systems is key to higher performance. Fig. 4 presents performance of 1D tridiagonal systems of size 128, solved using the Xilinx library (xilinxlib-F1) compared to our Thomas algorithm-based implementation (tridsolvlib) on a range of batch sizes. As discussed in the analytic model, for larger batch sizes the Xilinx library performed significantly slower than the Thomas based solver. Adding further optimizations, such as inner loop unrolling and a FIFO data path to the Xilinx solver (xilinxlib-F2) only marginally improved performance, leaving an order of a magnitude performance gap. We also observed that the PCR-based xilinxlib-F2 implementation consumed higher resources (an example is given in Table 1 for the batch size of 8000 systems).

In the remainder of this section we focus on using our FPGA design strategy. Specifically, we apply it to two representative, non-trivial applications. We investigate both 2D and 3D applications, with both FP32 and FP64 representations. Model predicted resource utilization estimates are used to determine initial design parameters and model predicted runtimes, which we compare to actual runtimes of the applications on a Xilinx Alveo U280. We use Vivado C++ due to ease of use for configurations and support of some C++ constructs compared to OpenCL. However, we note that OpenCL could equally be used to implement the same design. Finally, we compare performance on the FPGA to an NVIDIA Tesla V100 GPU using the tridiagonal solver library, tridsolver implemented by László et al. [13] [1] using its batched version presented by Reguly et al. [22]. This GPU library has been shown [6] to provide matching or better performance than the two current batch tridiagonal solver functions –cusparse<t>gtsv2StridedBatch() and cusparse<t>gtsvInterleacedBatch(), in Nvidia’s cuSPARSE library [4], [25]. Our experiments also confirmed these results for the applications evaluated in this paper. Additionally it features direct support for creating multi-dimensional solvers, whereas cuSPARSE requires data layout transformations, for example in between doing an x-solve and a y-solve to implement multi-dimensional problems. Thus we use tridsolver in our evaluation throughout this paper, but note that cuSPARSE libs would have equally provided the same insights when compared to the FPGA solvers on the U280. Given that previous work has demonstrated GPUs to provide significantly better performance than multi-threaded CPUs [15], we do not compare with CPU runs. Table 2 briefly details the specifications of the FPGA and the GPU systems (both hardware and software) used in our evaluation. The V100 is based on 12nm gate size comparable to the U280’s 16nm gate size. It has a peak bandwidth of 900GB/s, nearly twice that of the U280’s 460GB/s bandwidth.

4.1 ADI Heat Diffusion Application

The first application is an ADI based solve of the heat diffusion equation. The high-level algorithm of the application in 3D is detailed in Algo. 3. The application consists of an iterative loop which starts by calculating the RHS values using a 7-point stencil, followed by calls to the tridiagonal solver for each of two or three dimensions, depending on whether the application is 2D or 3D respectively. The updates from the tridiagonal solver, Tridslv is accumulated to $u$ before the next iteration. For the 3D ADI application, there are three calls to Tridslv. An initial design implements it as a single hardware unit given the data dependencies between the calls. This enables FPGA resource utilization to be maximized by implementing 6 CUs each having 8 Thomas solvers synthesized as a vectorized solver. The RHS calculation, which is a 3D explicit stencil loop, was implemented following techniques in Kamalakannan et al. [12], as a separate module. The intermediate results between CUs and RHS module were written/read to/from

| TABLE 1: Xilinx library performance : 8000 systems of size 128 |
|----------------------|-----------------|-----------------|-----------------|
| Design               | Runtime (ms)    | BW (GB/s)       | DSP URAM BRAM   |
| tridsolvlib          | 0.47            | 43.34           | 218             |
| xilinxlib-F1         | 5.15            | 3.97            | 437             |
| xilinxlib-F2         | 4.32            | 4.73            | 655             |

| TABLE 2: Experimental systems specifications. |
|---------------------------------------------|
| FPGA                        | Xilinx Alveo U280 [30] |
| DSP blocks                  | 8490                  |
| BRAM / URAM                 | 6.6MB (1487 blocks) / 34.5MB (960 blocks) |
| HBM                         | 8GB, 466GB/s, 32 channels |
| DDR4                        | 32GB, 38.4GB/s, in 2 banks |
| Host                        | AMD Ryzen Threadripper PRO 3975WX (32 cores) |
| Design SW                   | Vivado HLS, Vitis 2019.2 |
| GPU                         | Nvidia Tesla V100 PCIe [17] |
| Global Mem.                | 16GB HBM2, 900GB/s |
| Host                        | Intel Xeon Gold 6252 @2.10GHz (48 cores) |
| Compilers, OS              | nvcc CUDA 10.0.130, Debian 9.11 |
Algorithm 3: 3D ADI Heat Application

1: for $i = 0, i < n_{iter}, i + 1 \text{ do}$
2: Calculate RHS : $d = f_{rhs}(u), a = \frac{1}{2} \gamma, b = \gamma, c = -\frac{1}{2} \gamma$
3: Tridslv(x-dim), update $d$
4: Tridslv(y-dim), update $d$
5: Tridslv(z-dim), update $d$
6: $u = u + d$
7: end for

e external memory. The number of CUs is then limited by the available HBM ports but not by any other resource. An improvement on this initial design fuses the generation of independent read and write operations. We introduce two data structures for accumulation in line 6 of Algo 3. But due to limited HBM ports, we had to share single HBM ports with two data structures. This limits the data flow per data structure from/to the HBM2 ports as well as size of data structure, given single HBM port’s capacity is 256MBs. This final design gave the best performance in our evaluations. The full pipeline latency for the design can be shown to be given by (10):

$$L_{adi,3D} = n_{iter} \times \text{MAX}(L_{rhs+xy}, L_z)$$

$$L_{rhs+xy} = (\frac{2xy}{v}) + (2x^2 + 3gx) + (\frac{2xy}{v} + 3gy) +$$
$$[\frac{B}{2NCU}]\frac{xyz}{v}$$

$$L_z = (\frac{2xz}{v} + 3gz) + [\frac{B}{2NCU}]\frac{xyz}{v}$$

Here, $x, y$ and $z$ are the size of systems in each dimension, $NCU$ is the number of CUs implemented on the FPGA and $B$ is the total number of 3D meshes, i.e the number of batches. The first term in (11) accounts for the latency of the 3D stencil computation in RHS which operates over 3 planes. Here we read $xy$ number of mesh points in groups of the vectorization factor $v$. The second term is for Tridslv(x-dim) including latency to transpose the x-lines when reading/writing. Similarly the third term is for Tridslv(y-dim) including the read/write y-lines from the buffered x-lines. The final term is the latency to process $B$ number of meshes using $NCU$ number of CUs. In (12) the first term is for the read/write and solving in the $z$ dimension with Tridslv(z-dim). We take the maximum in (10) because the two modules need to be synchronized, as they are going to swap their read and write location after processing $B/2$ meshes. The vectorization factor $v$ is 8 for our design and $g$ is 32 for FP32 and 64 for FP64. A minor
A similar design can be developed for the 2D ADI Heat diffusion application implemented in both FP32 (a) and FP64 (b) on the Alveo U280 and compares it to execution on the V100 GPU. The design parameters for each are noted in the graphs. Operating frequencies are 292MHz and 288MHz for FP32 and FP64 respectively. In both cases the coefficients $a, b$ and $c$ are internally generated, on the FPGA. This means that only $u$ is read. Performance results demonstrate the FPGA outperforming the GPU particularly for runs with large batch sizes. Additionally the predictive model accuracy is over 85% with large batched predictions being more accurate at over 90%. Inspecting the effective bandwidth on each device as detailed in the top two sub-tables in Table 3 provides insights into the superior performance of the FPGA. The bandwidth is computed by counting the total number of bytes transferred during the execution of each call in Alg. 3, looking at the mesh data accessed and dividing it by the total time taken by each call. On the GPU, we have detailed the achieved bandwidth of the $x$- (Gx) and $y$-dim (Gy) solves. On the FPGA we have detailed the full bandwidth achieved in the pipeline. The $x$-dim bandwidth on the GPU is significantly worse due to the $8 \times 8$ transpose operations. Such lower bandwidths are also confirmed by Lásló et al. [13]. We additionally confirmed the same performance when using cuPARSE’s cusparse<t>gtsv2StridedBatch() library function for the $x$-solve. The higher performance of the FPGA can be attributed to the unrolling of the iterative loop allowing higher bandwidth utilization for the data path and the internal generation of coefficients. The GPU triaxial solver library is not currently setup for such an optimization. Thus, the application writes $a, b, c$ and $u$ to global memory after RHS and intermediate results also written/read between the two Tridslv calls whereas on the FPGA these stay on-chip. Even with modifications to the GPU library to generate coefficients internally which would improve GPU performance, we believe the FPGA results point to a very competitive solution, particularly when batching large meshes that can fit within the resource constraints of the FPGA implementation, for this application.

The first two sub-tables in Table 3 also detail the energy consumption of the 2D runs. The xbtutil utility was used to measure power during FPGA execution, while nvidia-smi was used for the same on the V100. The FPGA on average consumed 75W while the GPU power draw ranged from 50W to 250W. Results indicate that the FPGA energy consumption is approximately $5 \times$ to $6 \times$ lower for

\[
L_{\text{adi,2D}} = \frac{n_{\text{iter}}}{f_U} \times L_{\text{rhs}+xy}
\]

(13)

\[
L_{\text{rhs}+xy} = f_U \times \left[ \left( \frac{2x}{v} \right) + \left( 2v \frac{x}{v} + 3gx \right) + \left( \frac{2xy}{v} + 3gy \right) \right] + \left[ B/N_{CU} \right] \frac{xy}{v}
\]

(14)

Pipeline latency increases with the unroll factor $f_U$, but for large $B$ it results in a higher overall speedup. The size of the FIFO delay buffer is equivalent to the total delay of $B$, $\text{Tridslv}(x\text{-dim})$ and $\text{Tridslv}(y\text{-dim}): 2x/v + 2vx/v + 3gx + 3gy + 2xy/v$.

Fig. 5 details the performance of the 2D ADI Heat diffusion application implemented in both FP32 (a) and FP64 (b) on the Alveo U280 and compares it to execution on the V100 GPU. The design parameters for each are noted in the graphs. Operating frequencies are 292MHz and 288MHz for FP32 and FP64 respectively. In both cases the coefficients $a, b$ and $c$ are internally generated, on the FPGA. This means that only $u$ is read. Performance results demonstrate the FPGA outperforming the GPU particularly for runs with large batch sizes. Additionally the predictive model accuracy is over 85% with large batched predictions being more accurate at over 90%. Inspecting the effective bandwidth on each device as detailed in the top two sub-tables in Table 3 provides insights into the superior performance of the FPGA. The bandwidth is computed by counting the total number of bytes transferred during the execution of each call in Alg. 3, looking at the mesh data accessed and dividing it by the total time taken by each call. On the GPU, we have detailed the achieved bandwidth of the $x$- (Gx) and $y$-dim (Gy) solves. On the FPGA we have detailed the full bandwidth achieved in the pipeline. The $x$-dim bandwidth on the GPU is significantly worse due to the $8 \times 8$ transpose operations. Such lower bandwidths are also confirmed by Lásló et al. [13]. We additionally confirmed the same performance when using cuPARSE’s cusparse<t>gtsv2StridedBatch() library function for the $x$-solve. The higher performance of the FPGA can be attributed to the unrolling of the iterative loop allowing higher bandwidth utilization for the data path and the internal generation of coefficients. The GPU triaxial solver library is not currently setup for such an optimization. Thus, the application writes $a, b, c$ and $u$ to global memory after RHS and intermediate results also written/read between the two Tridslv calls whereas on the FPGA these stay on-chip. Even with modifications to the GPU library to generate coefficients internally which would improve GPU performance, we believe the FPGA results point to a very competitive solution, particularly when batching large meshes that can fit within the resource constraints of the FPGA implementation, for this application.

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this 2D problem. Fig. 5(c) and (d) and the bottom two sub-tables in TABLE 3 detail the performance of the 3D ADI heat diffusion application in FP32 and FP64 respectively. Again we see performance trends similar to the 2D case, however we were only able to run smaller batch sizes due to HBM memory limitations for 3D meshes. On the GPU, again apart from the x-dim solve we observe good achieved bandwidth. On the FPGA the achieved bandwidth is poorer due to no unrolling of the iterative loop as done in the 2D case, where there are 3CUs each unrolled by a factor of 3. The sharing of HBM ports as described in the design of this application limits the data flow per data structure further reducing achieved bandwidth. The energy consumption of the FPGA is 3–4× less than on the GPU.

A Thomas-Thomas based implementation for the 2D ADI-Heat application for larger mesh sizes can be modeled using (15).

\[ L_{x,2D,tiled} = n_{iter} 	imes (L_{rhs+x} + L_y) \]  
\[ L_{rhs+x} = 2 \frac{x}{v} + 2v \frac{x}{v} + \frac{3gx}{v} + 4gt_1 + \frac{Bxy}{v} \]  
\[ L_y = 2y \frac{T_x}{v} + \frac{3gy}{t_2} + 4gt_2 + \frac{Bxy}{v} \]  

In this case, RHS and x-solve can be pipelined but y-solve can’t be pipe-lined together as we are computing “tiles” along the y-dim lines, huge internal memory will be required to transpose the mesh. The explicit stencil computation in RHS does not require tiling as we are not processing very large meshes. If the tile sizes for the Thomas-Thomas solvers are selected to be \( t_1 \) and \( t_2 \) then the reduced system sizes will be \( 2t_1 \times 2t_2 \). Equation (16) accounts for the latency for RHS with x-dimension solve where the first term is stencil latency, second term is the latency for the data path, third is for the modified Thomas solve and fourth is the reduced solve. Similarly (17) given the y-dimension solve latency. Note that here we have used \( T_x \) (this is different to \( t_1 \)) as the tile size for the x-dim data path where we buffer \( T_x \times y \) sized planes. Note also that we have selected the number of interleaved systems and interleaved reduced systems to be equal (i.e. \( g = g_r \) in relation to (8)). The final term in (16) and (17) simply gives the latency for processing a batch of B systems. Replacing the reduced system solve with the PCR algorithm is also possible where then the 4\( gt_1 \) and 4\( gt_2 \) terms in (16) and (17) will become \( \log(2t_1) \times (2t_1 + l) \) and \( \log(2t_2) \times (2t_2 + l) \).

Fig. 6 and TABLE 4 presents the performance of 2D ADI heat diffusion application on large meshes solved using Thomas-PCR and Thomas-Thomas hybrid implementations. Again we compare with the same mesh sizes solved on the GPU. Due to the RHS and Tridslv (x-dim) being pipelined together, the FPGA gets better HBM bandwidth utilization. The GPU also gets good bandwidth utilization where it reaches bandwidth levels similar to batched smaller meshes. The FPGA can be seen to be \( 2 \times \) to \( 3 \times \) more energy efficient than the GPU for the largest mesh sizes.

### 4.2 SLV

The second application we synthesize and evaluate comes from computational finance. It implements a stochastic local volatility (SLV) model, which describes asset price processes, particularly foreign exchange rates [23]. A batched GPU implementation based on a 2nd order finite-difference scheme was developed for this problem using the OPS DSL by Reguly et al. [22]. It is a 2D application implemented in FP64 representation. Its high-level algorithm is detailed in Algo. 4. The application implements a Hunsdorfer-Verwer (HV) method for time integration. The Rannacher smoothing available in the original application has been switched off in our evaluation. The hv_pred* and hv_matrices are explicit loops each using 10 point stencils, requiring a window buffer implementation [12] for data reuse. The 9 kernels in Algo. 4 were implemented as separate hardware modules pipelining the computation within the iterative loop. hv_matrices generates a number of 2D coefficients \( AX, BX, CX, AV, BV, CV \) and 1D coefficient \( EV \) for the
Tridslvs. Coefficients $AX, BX, CX$ then needs to be input to 
(consumed by) Tridslv($x$-dim) kernels and coefficients $AV, BV, CV$ and $EV$ to Tridslv($y$-dim) kernels. Therefore these coefficients are consumed at different stages of 
the pipeline. However other inputs to the Tridslv calls come through the computation of this multi-stage pipeline. Therefore large FIFO delay buffers are required to keep 
synchronization (i.e. avoid pipeline stalling). As such we opt to 
regenerate the above coefficients at separate stages, essentially 
duplicating the circuitry. This results in the generation of 
coefficients $AX, BX, CX$, for the Tridslv($x$-dim), being fused to $hv_{pred0}()$ and $hv_{pred2}()$ and the generating of 
coefficients $AV, BV, CV, EV$, for the Tridslv($y$-dim), being fused to $hv_{pred1}()$ and $hv_{pred3}()$. This results 
in a total of 8 hardware modules, requiring significantly smaller delay buffers than if we implemented the original set of kernels. The performance model for the SLV application is given in (18):

$$L_{slv} = n_{iter}[4 	imes (2x) + 2 	imes (3gx) + 2 	imes (3gy + 2xy) + [B/N_{CU}]xy]$$  \hspace{1cm} (18)$$

Here $g$ is 64 as SLV is in FP64. The first term is the combined input/output latency for the three explicit stencil computations in $hv_{pred}$. The second and third terms account 
for the calls for Tridslv($x$-dim) and Tridslv($y$-dim) calls respectively, including the read/write y-lines from the buffered x-lines. The final term is the latency for processing 
a batch size of $B$ 2D meshes through. The number of CUs, $N_{CU}$ for SLV on the FPGA was 3, given the considerably larger amount of DSP and memory resources required for 
the application, particularly due to its use of FP64 representation. The FIFO delay-buffer size calculation was aided by the Xilinx HLS tools where the exact datapath pipeline latency was estimated to obtain buffer sizes adequate for an implementation.

The motivation for batched solves of multi-dimensional tridiagonal systems primarily comes from financial computing where for example computing prices of financial options and managing of risk by hedging options leads to the need to solve Algo. 4 type applications with different sets of coefficients [22]. Additionally carrying out extensive speculative scenarios required by regulators under various market conditions to evaluate a bank’s exposure means that there are large number of options in the order of thousands to hundreds of thousands to be computed every day. Such a workloads would entail large numbers of roughly identical

PDE problems to be solved which are well suited to be batched together.

Fig. 7 and TABLE 5 details the runtime, bandwidth and energy performance of the SLV application implementation. Only two specific mesh sizes were available from the authors of the original code [22] each was batched up to 3000 batches of 2D meshes for this evaluation. The application is significantly more complex given the additional explicit stencil loops as well as the tridiagonal solvers. The runtimes here were obtained with the FPGA operating at 253.5MHz. As can be seen from the figures, the FPGA in some cases is 
faster than the V100 GPU, but for the largest batch sizes we attempted here, it is 8%-70% slower than the GPU. However the FPGA solution is over 30% more energy efficient for large batch solves over the GPU. The achieved bandwidth on the FPGA is approximately at the same level as the 2D ADI 64FP version. Runtime predictions from the model were also observed to be over 90% accurate for all cases.

Finally, the resource utilization for all the synthesized designs on the Alveo U280 is shown in TABLE 6. Different mesh sizes are supported without re-implementing the FPGA design. For ADI with small mesh sizes, URAM availability is the limiting factor. Thomas-PCR is marginally limited by DSP units and BRAM and did not allow for a more resource intensive design due to routing congestion. The SLV application is very much limited by the available number of DSP units on the FPGA. The implementation has 3CUs where a single SLR unit on the U280 was required for a single CU.

5 Conclusion

We presented a design space exploration for synthesizing optimized high throughput multi-dimension tridiagonal
systems solvers on FPGAs. The main algorithms for direct solution of multiple tridiagonal systems were evaluated in light of the significant parallelization opportunities afforded by this class of solvers, particularly exploitable through the data-flow programming model on FPGAs. We developed a new tridiagonal solver library aimed at implementing high-performance computing applications on Xilinx FPGAs. Key new features of the library include data-flow techniques and optimizations for gaining high throughput with batching multiple system solves, replication of circuitry to carry out multiple solves in a “vectorized” manner and utilization of HBM memory available on modern FPGAs. The best algorithm for the FPGA with batched systems proved to be the Thomas algorithm, even with its loop carried dependencies, due to its simplicity and lower resource consumption. This somewhat subverts the conventional expectation of the more parallel PCR or spike algorithms being the best suited to get higher performance on parallel architectures. Our library, compared to the current state-of-the-art Xilinx tridiagonal library based on the PCR algorithm provided further evidence, where we see the superior performance of our Thomas based solver for larger batch sizes. However, for larger mesh sizes a hybrid Thomas-PCR or Thomas-Thomas solution was required due to the limitations of on-chip memory and demonstrated good performance overall with batched configurations.

Two representative applications (1) a heat diffusion problem based on the ADI method and (2) a stochastic local volatility (SLV) model from the financial computing domain that rely on the solution of multi-dimensional tridiagonal systems were implemented using the new library on a Xilinx Alveo U280 FPGA. As part of the design process a predictive analytic model that estimates the runtime performance of FPGA designs was also developed to assist in design space evaluations. The performance achieved by the FPGA was compared to optimized solutions of the same applications on a modern Nvidia Tesla V100 GPU, showing competitive performance, sometimes even surpassing that of the GPU. This was true for both small and larger mesh problems which enabled creating of longer pipelines keeping intermediate results on FPGA on-chip memory.

Even when runtime is inferior to the GPU, significant energy savings, over 30% for the most complex application (SLV) with large batch sizes, were observed. Considering the motivating real-world scenario for such an application from the financial computing domain, such energy savings point to a significant cost benefit in overall operation. The predictive model provides over 85% accuracy illustrating its significant utility in developing profitable FPGA designs.

The FPGA library, the 2D/3D ADI heat diffusion application and optimized GPU source code developed in this paper are available as open source software at [5]. This code repository also contains results from a Xilinx Alveo U50 FPGA, which was also done as part of this research to investigate the performance and portability of our multi-dimensional tridiagonal solver library. The U50 results also confirms the insights and conclusions from this paper. Future work will explore the use of FPGA hardware from Intel, currently the other major FPGA device vendor, for this class of applications.

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**REFERENCES**

[1] “Tridsolver Library,” July 2020. [https://github.com/OP-DSL/tridsolver.

[2] “Vitis High-Level Synthesis User Guide,” 2020, [https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_2/ug1399-vitis-hls.pdf].

[3] “Vitis Quantitative Finance Library V.2020.2,” 2020, [https://xilinx. github.io/Vitis_Libraries/quantitative_finance/2020.2/].

[4] “CUDA CUSPARSE API Reference,” Oct 2021, [https://docs.nvidia.com/ cuda/cusparse/index.html].

[5] “Tridsolver-FPGA Library,” Oct 2021, [https://github.com/Kamalavasan/Tridsolver-FPGA].

[6] G. D. Balogh, T. Flynn, S. Laizet, G. R. Mudalige, and I. Z. Reguly, “Scalable Many-core Algorithms for Triдиagonal Solvers,” Journal of Computing in Science and Engineering, 2021, (In Press).

[7] T. Brandvik and G. Pullan, “An Accelerated 3D Navier–Stokes Solver for Flows in Turbomachines,” Journal of Turbomachinery, vol. 133, no. 2, 10 2011, 021025. [Online]. Available: [https://doi.org/10.1115/1.4001192]

[8] J. de Fine Licht, A. Kuster, T. D. Matteis, T. Ben-Nun, D. Hofer, and T. Hoefler, “Stencila: Stencil Compiler for Distributed Computing,” Oct 2020, [https://arxiv.org/abs/2010.15218]. [Online]. Available: [https://arxiv.org/abs/2010.15218]

[9] T. De Matteis, J. de Fine Licht, and T. Hoefler, “Fblas: Streaming linear algebra on fp32,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, ser. SC ’20. IEEE Press, 2020.

[10] J. Douglas and J. E. Gunn, “A General Formulation of Alternating Direction Methods,” Numerische Mathematik, vol. 6, no. 1, pp. 426–453, 1964.

[11] W. Gander and G. H. Golub, “Cyclic Reduction—History and Applications,” Scientific computing (Hong Kong, 1997), vol. 9785, 1997.

[12] K. Kamalakkannan, G. R. Mudalige, I. Z. Reguly, and S. A. Fahmy, “High-Level FPGA Accelerator Design for Structured-Mesh-Based Explicit Numerical Solvers,” in 2021 IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2021, pp. 1087–1096.

[13] E. Laszlo, M. Giles, and J. Appleyard, “Manycore Algorithms for Batch Scalar and Block Triangular Solvers,” ACM Transactions on Mathematical Software (TOMS), vol. 42, no. 4, pp. 1–36, 2016.

[14] E. Laszló, Z. Nagy, M. B. Giles, I. Reguly, J. Appleyard, and P. Szolgy, “Analysis of Parallel Processor Architectures for the Solution of the Black-Scholes PDE,” in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 1977–1980.

[15] H. Macintosh, J. Banks, and N. Nelson, “Implementing and Evaluating a Heterogeneous, Scalable, Triangular Linear System Solver with OpenCL to Target FPGAs, GPUs, and CPUs,” Int. J. Reconfigurable Comput., vol. 2019, pp. 3 679 839:1–3 679 839:13, 2019.
[16] H. J. Macintosh, D. J. Warne, N. A. Kelson, J. E. Banks, and T. W. Farrell, “Implementation of Parallel Tridiagonal Solvers for a Heterogeneous Computing Environment,” in Proceedings of the 17th Biennial Computational Techniques and Applications Conference, CTAC-2014, ser. ANZIAM J., J. Sharples and I. L. Bunder, Eds., vol. 56, Feb 2016, pp. C446–C462. [Online]. Available: http://journal.austms.org.au/ojs/index.php/ANZIAMJ/article/view/9371

[17] “NVIDIA V100 Data Sheet,” Nvidia, Jan 2020, https://images.nvidia.com/content/technologies/volta/pdf/volta-v100-datasheet-update-us-1165301-r5.pdf.

[18] F. Oliveira, C. S. Santos, F. A. Castro, and J. C. Alves, “A Custom Processor for a TDMA Solver in a CFD Application,” in Reconfigurable Computing: Architectures, Tools and Applications, R. Woods, K. Compton, C. Bouganis, and P. C. Diniz, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2008, pp. 63–74.

[19] D. W. Peaceman and H. H. Rachford, Jr, “The Numerical Solution of Parabolic and Elliptic Differential Equations,” Journal of the Society for industrial and Applied Mathematics, vol. 3, no. 1, pp. 28–41, 1955.

[20] E. Polizzi and A. H. Sameh, “A Parallel Hybrid Banded System Solver: the SPIKE Algorithm,” Parallel Computing, vol. 32, no. 2, pp. 177–194, 2006, parallel Matrix Algorithms and Applications (PMAA’04).

[21] T. H. Pulliam, “Implicit Solution Methods in Computational Fluid Dynamics,” Applied numerical mathematics, vol. 2, no. 6, pp. 441–474, 1986.

[22] I. Z. Reguly, B. Moore, T. Schmielau, J. du Toit, and G. R. Mudalige, “Batch solution of small PDEs with the OPS DSL,” in High Performance Computing, M. Weiland, G. Juckeland, S. Alam, and H. Jagode, Eds. Cham: Springer International Publishing, 2019, pp. 124–141.

[23] G. Tataru and T. Fisher, “Stochastic Local Volatility,” Quantitative Development Group, Bloomberg Version 1, Feb 5 2010.

[24] L. Thomas, “Elliptic Problems in Linear Differential Equations Over a Network: Watson Scientific Computing Laboratory,” Columbia Univ., NY, 1949.

[25] P. Valero-Lara, I. Martínez-Pérez, R. Sirvent, X. Martorell, and A. J. Peña, “NVIDIA GPUs Scalability to Solve Multiple (Batch) Tridiagonal Systems Implementation of cuThomasBatch,” in Parallel Processing and Applied Mathematics, R. Wyrzykowski, J. Dongarra, E. Deelman, and K. Karczewski, Eds. Cham: Springer International Publishing, 2018, pp. 243–253.

[26] X. Wang, Y. Xu, and W. Xue, “A Hierarchical Tridiagonal System Solver for Heterogenous Supercomputers,” in 2014 5th Workshop on Latest Advances in Scalable Algorithms for Large-Scale Systems, 2014, pp. 69–76.

[27] Y. Wang, M. Baboulin, J. Dongarra, J. Falcou, Y. Fraigneau, and O. Le Meur, “A Parallel Solver for Incompressible Fluid Flows,” Procedia Computer Science, vol. 18, pp. 439–448, 2013, 2013 International Conference on Computational Science.

[28] D. Warne, N. Kelson, and R. Hayward, “Solving Tri-diagonal Linear Systems Using Field Programmable Gate Arrays,” in Proceedings of the 4th International Conference on Computational Methods, Y. Gu and S. Saha, Eds. Australia: Queensland University of Technology, 2012, pp. 1–8. [Online]. Available: https://eprints.qut.edu.au/54894/

[29] D. J. Warne, N. A. Kelson, and R. F. Hayward, “Comparison of High Level FPGA Hardware Design for Solving Tri-diagonal Linear Systems,” Procedia Computer Science, vol. 29, pp. 95–101, 2014, 2014 International Conference on Computational Science. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1877050914001860

[30] Alveo U280 Data Center Accelerator Card Data Sheet, Xilinx Inc., May 2020, v1.3.

[31] W. Zhang, V. Betz, and J. Rose, “Portable and Scalable FPGA-Based Acceleration of a Direct Linear System Solver,” ACM Trans. Reconfigurable Technol. Syst., vol. 5, no. 1, Mar 2012. [Online]. Available: https://doi.org/10.1145/2133352.2133358