C3PU: Cross-Coupling Capacitor Processing Unit Using Analog-Mixed Signal In-Memory Computing for AI Inference

Dima Kilani, Baker Mohammad, Yasmin Halawani, Mohammed F. Tolba and Hani Saleh

System-on-Chip Center (SoCC), Khalifa University, Abu Dhabi, UAE

Abstract—This paper presents a novel cross-coupling capacitor processing unit (C3PU) that supports analog-mixed signal in-memory computing to perform multiply-and-accumulate (MAC) operations. The C3PU consists of a capacitive unit, a CMOS transistor, and a voltage-to-time converter (VTC). The capacitive unit serves as a computational element that holds the multiplier operand and performs multiplication once the multiplicand is applied at the terminal. The multiplicand is the input voltage that is converted to a pulse width signal using a low power VTC. The transistor transfers this multiplication where a voltage level is generated. A demonstrator of 5 × 4 C3PU array that is capable of implementing 4 MAC units is presented. The design has been verified using Monte Carlo simulation in 65 nm technology. The 5 × 4 C3PU consumed energy of 66.4 fJ/MAC at 0.3 V voltage supply with an error of 5.7%. The proposed unit achieves lower energy and occupies a smaller area by 3.4 × and 3.6 ×, respectively, with similar error value when compared to a digital-based 8 × 4-bit fixed point MAC unit. The C3PU has been utilized through an iris flower classification utilizing an artificial neural network which achieved a 90% classification accuracy compared to ideal accuracy of 96.67% using MATLAB.

Index Terms—Analog neural network, cross-coupling capacitor, inference, MAC, in-memory computing.

I. INTRODUCTION

Multiply-and-accumulate (MAC) units are essential building blocks for digital processing units that are used in a multitude of applications, including artificial intelligence (AI) for edge devices, signal/image processing, convolution, and filtering [1]. Recently, research has been focused on AI applications to address complex machine learning problems such as image/speech recognition and language translation [2]. Deep neural networks (DNNs) are widely utilized in such applications since it can achieve high accuracy [3]. However, DNN algorithms are computationally intensive, with large data sets that require high memory bandwidth. This results in memory access bottlenecks that introduce considerable energy and performance challenges. The memory access energy is 1-3 orders of magnitude higher than the compute energy [4]. However, DNNs are approximate in nature, and many AI applications can tolerate lower accuracy [5]. This opens the opportunity for potential tradeoffs between energy efficiency, accuracy, and latency.

One direction to reduce the need for explicit memory access is to utilize in-memory computing (IMC) architectures. It has significant advantages in energy efficiency and throughput compared to traditional computing that is based on von Neumann architecture [6] [7] [8]. Both digital and analog approaches for IMC have been reported in the literature to develop an artificial neural network (ANN). One key component in the ANN is the synaptic memory used for the network’s weight storage. Several weight storage elements are reported and classified in the literature: 1) traditional volatile memory: SRAM [9] and DRAM [10], 2) non-volatile memory (NVM): CMOS-based flash memory [11], and emerging NVM technology such as Resistive RAM (RRAM) [12] and 3) analog-mixed signal circuits using capacitors and transistors [13]. Both SRAM and DRAM are limited to high power devices that are not suitable for duty-cycled edge devices. The flash memory traps the weight charges in the floating gate, which is electrically isolated from the control gate. On the other hand, the RRAM devices such as memristors store the weight as a conductance value. However, memristors suffer from low endurance and sneak path issues which may result in a state disturbance [14]. Capacitors and transistors structures have been demonstrated by IBM as an analog memory to store the weights as charges that control the conductance of the transistors. However, the limitation of this solution is the relatively large and complex biasing circuit that is required to control the charges on the capacitor in addition to the non-linearity due to the variations of the drain-to-source voltage of the transistor. The recent work in [6] employs both 8T-SRAM as a memory and cross-coupling capacitor as an accumulator to perform binary MAC operation using bitwise XNOR gate. To implement an analog MAC operation, this paper develops a novel cross-coupling capacitor (C3) computing, hence, named, the C3 processing unit (C3PU) coupled with a voltage-to-time converter (VTC) circuitry. The C3PU performs multiplication using capacitive coupling and accumulation through the transistor bitline in the array. The main contributions of this paper can be summarized as follows:

- According to the best of the authors’ knowledge, this is the first circuit design that utilizes cross-coupling capacitor for IMC as both a memory and a computational element to perform analog MAC operation.
- The proposed C3PU can be utilized in applications that heavily rely on vector-matrix multiplications, including but not limited to ANN, CNN, and DSP. The design is ideal for applications with fixed coefficients such as pre-trained CNN weights and image compression [8].
- A 5.7 µW low power voltage-to-time (VTC) converter is implemented at the input voltage terminal of the C3PU to generate a modulated pulse width signal. Such cir-
cuit guarantees a linear multiplication operation through CMOS transistor.

- A 5×4 crossbar architecture based on C3PU is designed and simulated in 65nm technology to employ 4 MAC units where each unit performs 5 multiplications and 4 additions. Simulation results show that the energy efficiency of the 5×4 C3PU is 66.4 fJ/MAC at 0.3 V voltage supply with an error compared to computation in MATLAB of 5.7%.

- The proposed C3PU usage has been demonstrated through iris flower classification on a two-layers ANN. The synaptic weights are trained offline and then mapped into capacitance ratio values for the inference phase. The ANN classifier circuit is designed and simulated in 65 nm CMOS technology. It achieves a high inference accuracy of 96.67% obtained from MATLAB.

The rest of this paper is organized as follows. Section II proposes the C3PU circuit design and explains how the MAC operation is performed. Section III discusses the implementation of the MAC operations in a 5×4 C3PU crossbar architecture. Section IV shows an example of C3PU’s potential application targeting iris flower classification using ANN architecture in 65nm technology. Finally, Section V concludes the paper.

II. PROPOSED C3PU CIRCUIT AND OPERATION

The following subsections discuss the operational details of the proposed C3PU. The basic principle of the contribution is based on using a coupling capacitance to transfer the voltage to the transistor’s gate. The generated voltage is linearly proportional to the current passed through the transistor.

A. C3PU Operation

Figure. 1a shows the proposed C3PU circuit that performs in-memory multiplication operation. The C3PU consists of a CMOS transistor and a capacitive unit that includes a cross-coupling capacitor \( C_c \), a capacitor \( C_b \) connected between the gate of the transistor and the ground, and a transistor’s gate capacitor \( C_g \). The modulated input voltage amplitude \( V_{in} \), which is the first multiplication operand, is applied at the terminal of the capacitive unit. The second operand is stored in the capacitive unit as an equivalent capacitance ratio \( X_{eq} = \frac{C_c}{C_c + C_b + C_g} \). The capacitive computational unit multiplies the two operands and generates a voltage \( V_g \) that is a function of \( V_{in} \), \( C_c \), \( C_b \), and \( C_g \) as given in Eq. 1. \( V_g \) is applied to the gate of CMOS transistor producing a drain-source current \( I_{ds} \) as given in Eq. 2 where \( G_m \) is the transistor’s transconductance. Note that \( I_{ds} \) is proportional to the multiplication of its two operands \( V_{in} \) and \( X_{eq} \). Since the multiplication is linear, the transistor must also operate in a linear mode in order to transfer the multiplication correctly to the output in an electrical current form.

\[
V_g = V_{in} \frac{C_c}{C_c + C_b + C_g} \quad (1)
\]

\[
I_{ds} = G_m \times V_g = G_m \times V_{in} \frac{C_c}{C_c + C_b + C_g} \quad (2)
\]

Fig. 1: Proposed C3PU to perform a single multiplication operation by processing the input voltage \( V_{in} \) in the (a) voltage domain and (b) time domain using VTC block.

The value of \( V_g \) determines the operational mode of the transistor and affects its transconductance value and hence its linearity. Figure. 2 depicts the \( I_{ds} \) of the transistor versus \( V_g \) at \( VDD_{C3PU} = 0.3 \) V. As shown in the figure, \( I_{ds} \) is approximately linear only when \( V_g \) is between 0.5 V and 0.8 V with a transconductance slope of 230.13 \( \mu \)S and a mean square error (MSE) of 2.37 pS between the observed and expected ones. The linearity over a small range of \( V_g \) creates some design constraints. First, the input voltage has to be selected within a certain high value range. This means that \( V_{in} \) requires normalization to tolerate the low \( V_{in} \) values resulting in a mapping error. Second, even though \( V_{in} \) is high, the capacitance ratio \( X_{eq} \) should also be high enough to provide a large \( V_g \) value to run the transistor in linear mode.

Fig. 2: \( I_{ds} \) versus \( V_g \) at \( VDD_{C3PU} = 0.3 \) V. The transistor operates either in linear or non-linear mode based on the multiplication output of the two operands.

To overcome the former issues that significantly affect the functionality of the proposed C3PU multiplier, the analog input voltage will be processed in the time domain rather than the voltage domain. This is achieved using a voltage-to-time converter (VTC), as shown in Fig. 1b, by converting the amplitude of analog input \( V_{in} \) into time delay to generate a modulated pulse width signal \( V_{pw} \). This way, the voltage level of \( V_{pw} \) is ensured to be high and having a value equal to the VTC’s supply voltage \( VDD = 1 \) V. Consequently, the transistor will always operate in linear mode giving that \( X_{eq} \) is selected within a specific high range between 0.5 and 0.75 and \( VDD_{C3PU} \) is low with a value of 0.3 V. If \( X_{eq} > 0.75 \), then the value of \( V_g \) will saturate. The resultant \( I_{ds} \) becomes a function of \( V_{pw} \) as shown in Eq. 3 that is linearly proportional to the time delay. The proposed VTC circuit design, as
Fig. 3: (a) Block diagram of the proposed VTC, (b) VTC’s signal flow in the sampling phase, (c) VTC’s signal flow in the evaluation phase.

discussed in section II-B achieves high conversion linearity over a wide range of $V_{in}$. This guarantees that the C3PU performs a valid multiplication between $V_{in}$ and $X_{eq}$ by: a) providing a linear conversion from $V_{in}$ to $V_{pw}$, and b) running the transistor in linear mode.

\[
I_{ds} = G_m \times V_g = G_m \times V_{pw} \frac{C_c}{C_c + C_b + C_g}
\]  

(3)

Presenting the data $V_{in}$ in the time domain has several advantages over the voltage domain, since both time and capacitance scale better with technology. In addition, it has less variations and provides better noise immunity compared to the voltage domain where the signal-to-noise ratio is degraded due to voltage scaling [15].

B. Proposed Voltage-to-Time Converter (VTC)

Figure. 3 shows the block diagram of the proposed VTC circuit design. It consists of a sampling circuit, an inverter, and a current source. To achieve voltage-to-time conversion, the VTC has two operating phases: sampling and evaluation. The basic principle is to transfer the charges from the input to the capacitor during the sampling phase and then discharge this capacitor through a current source during the evaluation phase. A simple inverter is used to transfer the time it takes to discharge the capacitor into a delay. The delay will be linearly proportional to the input voltage.

During the sampling phase, as shown in Fig. 3b, $S_1$ and $S_4$ turn on when the clock $V_{clk}=1$ V and $S_2$ and $S_3$ are off when the inverted clock $V_{clkb}=0$. The capacitor $C_1$ is precharged with a voltage $V_c$ that is equal to the input voltage value $V_{in}$. The capacitor $C_2$ is charged with a voltage $V_x$ that is equal to the supply voltage $V_{DD}$. During the evaluation phase, as shown in Fig. 3c, $S_1$ and $S_4$ turn off when $V_{clk}=0$ and $S_2$ and $S_3$ turn on when $V_{clkb}=1$ V. The node $V_c$ is coupled to $V_x$. In this phase, the functionality of the VTC depends on $V_{in}$. When $V_{in}$ is high, i.e., $V_{in}=V_{DD}$, then $V_c=V_x$ and the initial charge across the capacitors is $Q_s=V_{DD}(C_1+C_2)$. On the other hand, when $V_{in}$ is small, i.e., $V_{in}=0$, the initial charge across the capacitors is $Q_s=V_{in}C_1+V_{DD}C_2$. Due to the potential difference between $C_1$ and $C_2$, the charges are shared among them. Consequently, the current flows from $C_2$ to $C_1$ causing a voltage pump on $V_c$. Then, it starts discharging through the current source $I$ till it reaches the switching point of the inverter $V_{sp}$ resulting in a final charge $Q_f=V_{sp}(C_1+C_2)$. After that, the inverter pulls up the delayed output voltage $V_{out}$. The time it takes to discharge $V_c$ to the inverter’s switching point voltage is referred to as time delay $t_d$. This time delay, given in Eq. 4, depends on four main parameters: voltage values of $V_{DD}$ and $V_{in}$, voltage value of $V_{sp}$, capacitors’ size of $C_1$ and $C_2$, and the average current $I_{avg}$ till it is discharged. The $V_{sp}$ value is set by the aspect ratio of PMOS and NMOS transistors of the inverter ($\frac{W}{L}$) as given in Eq. 5. The $I_{avg}$ value depends on the amount of charges stored in the capacitors, which varies linearly with $V_{in}$ given that $V_{DD}$ is fixed. Thus, $t_d$ has a linear relationship with $V_{in}$.

\[
t_d = \frac{Q_s - Q_f}{I_{avg}} = \frac{C_1V_{in} + C_2V_{DD} - V_{sp}(C_1 + C_2)}{I_{avg}}
\]  

(4)

\[
V_{sp} = \frac{V_{DD} - |V_{thp}| + \sqrt{\frac{2n}{b_p}V_{thn}}}{1 + \sqrt{\frac{2n}{b_p}}}
\]  

(5)

To implement the proposed VTC using CMOS, Fig. 4a shows the detailed circuit diagram. The switches $S_1$ and $S_3$...
are replaced by the pass gates \((M_1, M_2)\) and \((M_5, M_6)\), respectively. The switches \(S_2\) and \(S_4\) are replaced by \(M_3\) and \(M_7\), respectively. The current source is simply implemented using \(M_4\) and controlled by a bias voltage \(V_t\) to operate in the saturation region. The inverter is realized by \(M_8\) and \(M_9\). To generate a pulse width signal \(V_{pw}\), a digital logic block of inverter and AND gate is added. During the sampling phase, when \(V_{clkb}=0\) and \(V_{clk}=1\), \(M_7\) is off, and \(M_1\) is on, so that \(C_2\) is charged to \(VDD\). The pass gate \((M_1, M_2)\) turns on to precharge \(C_1\) with \(V_c=V_{in}\). On the other hand, the pass gate \((M_5, M_6)\) is off, which disconnects the node \(V_c\) from \(V_t\) to eliminate the short circuit current on the delay chain at low voltage levels of \(V_{in}\). At this phase, \(V_{dc}=VDD\), which causes \(V_{out}=0\). During the evaluation phase, when \(V_{clkb}=1\) and \(V_{clk}=0\), the pass gate \((M_5, M_6)\) and \(M_3\) turn on, whereas the pass gate \((M_1, M_2)\) and \(M_7\) turn off. In this phase, \(V_c\) is coupled to \(V_x\) and the charges redistribute between \(C_1\) and \(C_2\). Initially, if \(V_{in}<VDD\), this means that \(V_x<V_t\). As a result, a current flows from \(C_2\) to \(C_1\), making a charge pump on \(V_c\) as shown in Fig. 4b (see gray waveform when \(V_{in}=0.1\) V). On the other hand, if \(V_{in}=VDD\), then \(V_c\) follows \(V_x\) as shown in Fig. 4b when \(V_{in}=1\) V. In both cases, the capacitor current starts discharging through \(M_4\), equating it with the drain-source current of \(M_4\), \(I_{ds4}\). This drops the value of \(V_x\) till it reaches \(V_{sp}\) of the inverter \((M_8, M_9)\). Then, it pulls up \(V_{out}\) that is connected to an inverter chain whose output \(V_{out-b}\) is ANDed with \(V_{clk}\) to generate \(V_{pw}\). Figure. 4b depicts the waveforms of the proposed VTC. Note that the proposed VTC controls the delayed \(V_{out}\) at the rising edge of \(V_{clk}\).

The proposed VTC circuit has been designed, implemented, and simulated in 65 nm industry-standard CMOS technology. The input voltage is set between 0 V to 1 V at \(VDD=1\) V. Both capacitors \(C_{1,2}\) and transistor \(M_4\) sizes are selected to support a minimum time delay of 107 ps at the minimum \(V_{in}\) of 0 V. A metal insulator metal (MIM) capacitors of \(C_3=27\) fF and \(C_6=10\) fF are utilized. The \(M_4\) size of 500 nm/140 nm controlled by its gate voltage of \(V_{in}=0.5\) V provides a current of 14 \(\mu A\). The inverter is carefully sized to provide the desired \(V_{sp}\). Hence, the aspect ratio of \(M_9\) is \(5\times\) the aspect ratio of \(M_8\) such that \(V_{sp}=0.35\) V. Table I summarizes the specifications of the proposed VTC design.

| \(VDD\) (V) | 1 |
| \(V_{in}\) (V) | 0-1 |
| \(C_3\) (fF) | 27 |
| \(C_2\) (fF) | 18 |
| \(W_{1,2,5,6}/L_{1,2,5,6}\) (nm/nm) | 600/60 |
| \(W_{3,7}/L_{3,7}\) (nm/nm) | 200/60 |
| \(W_{4}/L_{4}\) (nm/nm) | 500/140 |
| \(W_{8}/L_{8}\) (nm/nm) | 200/60 |
| \(W_{9}/L_{9}\) (\(\mu m/\mu m\)) | 1/60 |
| \(V_b\) (V) | 0.5 |
| \(V_{sp}\) (V) | 0.35 |

Figure. 5 depicts the modulated pulse width signal \(V_{pw}\) at different \(V_{in}\) values. As shown from the figure, the pulse width varies from 0.260 ns at \(V_{in}=0\) V to 2.3 ns at \(V_{in}=1\) V, resulting in a conversion gain of 2.05 ns/V. Figure. 6 shows the output time delay \(t_{pw}\) from the VTC versus the input voltage observed from the simulation in addition to the expected ones. As depicted from the figure, the time delay is linearly proportional to the input voltage. Note that the VTC is designed to operate in approximate computing architectures for AI applications that are statistical in nature and tolerable to variation and noise [5] [16]. Noise simulation has been carried out to analyze the input-referred noise and the SNR of the VTC at \(V_{in}=1\) V and frequency= 100 MHz. The input noise and signal power averages are obtained by integrating the noise and signal power spectrums over their frequency range. Spice simulation shows that the averaged input referred-noise and signal are 1.425 \(\mu V^2\) and 5.67 \(V^2\) resulting in an SNR value of 65.9 dB. The VTC has a low MSE value of 4.15e\(^{-23}\), low power consumption of 5.7 \(\mu W\), including the clock buffers and a small area of 0.0001 \(mm^2\).

To quantify the impact of mismatch variation on the pulse width value, Monte Carlo Spice simulation is carried out with 200 samples. Figure. 7 shows the effect of mismatch variations...
on the time delay obtained from Monte Carlo simulation at $V_{in}=1$ V. As depicted from the figure, the standard deviation is low such as 0.218 ns from the mean of 2.358 ns at $V_{in}=1$ V. Hence, the ratio of the standard deviation to the mean is approximately 9%. This variation can be reduced by cascading multiple stages of the VTC circuit as shown in Table II. As the number of the VTC stages increases, the variation decreases down to 4.4% for 4-stages. For 4-stages VTC with 200 samples, 3-sigma variations of 13.2% can be covered which is equivalent to 2-sigma variations for 2-stages VTC. Table III shows the comparison between the proposed design and prior works. Although the proposed VTC circuit has a lower conversion gain, the linearity range across $V_{in}$ is improved by $4 \times$ and $5.33 \times$ compared to [17] and [18], respectively. Moreover, for IMC applications where the computation can be performed in a few ns, the pulse width of $V_{pw}$ doesn’t need to be large, and so the conversion gain. The figure of merit (FoM) is developed for the VTC circuit and given in Eq. 6. It indicates accuracy of the VTC in providing conversion gain per power. The VTC’s accuracy is 99.7%, and hence the FoM equals $322 \mu$s/V.W. n t

$$FoM = accuracy \times \frac{Gain}{Power} \quad (6)$$

TABLE II: Variations of the cascaded VTC stages for 200 samples.

| VTC stage number | Mean (ns) | Standard deviation (ns) | Variation (%) |
|------------------|-----------|-------------------------|--------------|
| 1                | 2.04      | 0.188                   | 9.2          |
| 2                | 4.06      | 0.276                   | 6.8          |
| 3                | 6.058     | 0.350                   | 5.8          |
| 4                | 7.98      | 0.351                   | 4.4          |

III. C3PU CROSSBAR ARCHITECTURE FOR IMC APPLICATIONS

To demonstrate the advantage of the proposed design, a crossbar architecture of the C3PU and periphery circuit is designed. Computational crossbars naturally realize highly parallel vector-matrix operations and hence efficiently support high throughput with significant savings compared to the digital counterpart. This efficiency is achieved by performing the MAC operation in the same place where the data is stored.

Therefore, the $5 \times 4$ C3PU crossbar architecture is proposed, as shown in Fig. 8. The transistor source in each C3PU computational element is connected to the supply voltage $V_{DDC3PU}$. It is assumed that the analog input voltages $V_{in,1-5}$ come directly from the sensors. These inputs are converted into modulated pulse width signals $V_{pw,1-5}$ using 5 separate VTCs (discussed in II-B) instead of the need for the ADC as in the traditional design. The $V_{pw,1-5}$ represent the wordlines connected to the C3PU computational block to run it in linear mode. Each current produced by the C3PU is controlled by the multiplication of $V_{pw,1}$ and capacitance ratio $X_{ij}$ ($i$ is the row and $j$ is the column) and then summed by the shared bitline. The resultant currents $I_{1-4}$ represent the complete MAC calculation of each column. The

![Fig. 7: VTC’s histogram mismatch variations at $V_{in}=1$ V. The x-axis represents the delay value and y-axis represents the number of samples. The total number of samples used is 200.](image1)

![TABLE III: Comparison between proposed and prior work.](image2)

| Work | [19] | [17] | [18] | Proposed |
|------|------|------|------|----------|
| Technique | constant | super | starved | sampling |
| Technology (nm) | 65 | 45 | 65 | 65 |
| $V_{DD}$ (V) | 1 | 0.5 | 1 | 1 |
| $V_{in}$ (V) | 0-1 | 0.1-0.5 | 0.2-0.35 | 0-1 |
| Linearity range | high | low | low | high |
| Gain (ns/V) | 0.144 | 101.43 | 3.47 | 2.05 |
| Power ($\mu$W) | 8300 | - | - | 5.7 |
| MSE (s) | - | - | - | $4.15 \times 10^{-23}$ |

![Fig. 8: Proposed $5 \times 4$ C3PU crossbar for MAC operations.](image3)
The value of output voltages depends on two main parameters:
a) time that the current will be accumulated \( t_1 - t_2 \) and b) capacitor size \( C_j \). The time \( t_1 - t_2 \) is usually fixed and "represents the pulse width of the clock. This time is set to be greater than the maximum pulse width of \( V_{pw,i} \). The maximum pulse width of \( V_{pw} \) is approximately 2 ns when the maximum input voltage \( V_{in} = 1 \). Thus, the pulse width of the clock is set to 3 ns to ensure the completion of the computation and accumulation of the currents. In addition, the \( C_j \) size plays an essential role in determining the scaling factor that is required to approximately allow \( V_{1-4} \) to reach the expected output levels. The scaling factor is calculated by dividing the obtained MAC output voltages \( V_{1-4} \) by the expected values, and hence the \( C_j \) size is set. Once the approximate voltages are achieved, the C3PU elements are isolated from the outputs by setting \( V_{clk} = 0 \) to enter the isolation phase. The isolation phase is essential to allow the proper functioning of the VTC and to initialize the output stage of the virtual ground op-amp. The period \( T \), including computation and isolation time taken to operate the MAC calculations is 6 ns. Table IV shows the specifications of the C3PU crossbar architecture. The value of \( C_0 \) has a range between 2.5 fF and 8 fF, and the value of \( C_j \) is fixed with 2.5 fF. Note that the proposed C3PU design targets hardwired fixed functions for AI applications where the weights are fixed. It can be modified to support applications that require programmable weights using emerging memcapacitor [20] [21]. However, this requires control circuits and a tunable voltage to program the capacitance value, which adds power overhead.

### Table IV: 5×4 C3PU crossbar specifications.

| Voltage (V) | Value |
|-------------|-------|
| \( V_{DD} \) (V) | 0.3 |
| \( V_{DD} \) (V) | 1 |
| \( V_{in} \) (V) | 0-1 |
| \( V_{pw} \) (V) | 1 |
| \( t_{pw} \) (ns) | 0-2.3 |
| \( X_e \) | 0.5-0.75 |
| \( V_g \) (V) | 0.5-0.75 |
| \( T \) (ns) | 6 |
| Transistor size (nm/nm) | 500/60 |

The operation of the C3PU crossbar, given in Fig. 8, depends on two-phase functions: computation and isolation. In the computation phase, when the clock signal \( V_{clk} = 1 \), the MAC operation is achieved by multiplying the \( V_{pw,i} \) pulse widths with the capacitance ratios \( \frac{C_{ij}}{C_{ij} + C_{g,ij}} \). Then, the transistors transfer this multiplication into a current that is summed on each bitline. The summed currents are integrated over a time \( t_1 - t_2 \) using a virtual ground current integrator op-amp to provide the outputs as voltage levels \( V_{1-4} \) as given in Eq. 7.

\[
V_j = \frac{1}{C_j} \int_{t_1}^{t_2} I_j \, dt = \frac{1}{C_j} \int_{t_1}^{t_2} \sum_{i=1}^{5} I_{ds,ij}
\]

The 5×4 C3PU crossbar shown in Fig. 8 with the specifications in Table IV is designed and implemented in 65nm technology. The input voltages are fed to the C3PU crossbar for 30 consecutive clock cycles representing the 30 input sets. Each cycle has different sets of input voltage levels that are converted into modulated pulse width signals. Figure 9 shows the input/output time domain waveform of the 5×4 C3PU crossbar for two different input sets. The input and output voltages are validated at the negative edge clock, and the modulated pulse width signals are generated at the positive edge clock. The average computing error in the 5×4 C3PU crossbar is 5.7%. The error is calculated and averaged for 30 input samples by comparing the observed MAC output from simulation with the expected values. Table V demonstrates the error matrix of the C3PU outputs when compared to the expected ones from MATLAB simulation at different input combinations selected from the test set.

The 5×4 C3PU crossbar and the 5 VTC blocks is 26.3 fJ/MAC and 40.1 fJ/MAC, respectively, resulting in total energy efficiency of 66.4 fJ/MAC. Each MAC unit/column includes 5 multiplications and 4 additions. To further increase the number of operations, the crossbar array size can be enlarged. Some
TABLE VI: Evaluation of 5×4 FXP crossbar MAC units with different input and weight resolutions.

| MAC Unit Type | Energy (fJ/MAC) | Error (%) | MSE | Area (µm²/MAC) |
|---------------|-----------------|-----------|-----|----------------|
| 3×3-bit       | 60.9            | 64.7      | 14.64 | 127.7         |
| 4×4-bit       | 107             | 10        | 0.24 | 246.2         |
| 8×4-bit       | 226.2           | 6.52      | 0.099 | 655.8         |
| 8×8-bit       | 526             | 0.74      | 0.002 | 1380.7        |
| C3PU          | 66.4            | 5.7       | 0.082 | 180           |

design constraints need to be considered when increasing the C3PU crossbar size. Adding more rows to the C3PU array increases the accumulated currents, which require a larger capacitor size in the integrator circuit to achieve the desired output voltage. For example, every additional 5 rows demand an additional 300F capacitor. Therefore, there is a tradeoff between the number of rows and the integrator’s capacitor size. Increasing the number of columns is also limited as the line resistance affects the driving signal of the $V_{pw}$. The resistance due to the line connected from the VTCs to the columns increases with the number of columns, and this degrades the pulse width of $V_{pw}$ signal. Simulation results show that the C3PU crossbar with 32 columns will suppress the pulse width of $V_{pw}$ by 10.8%. The maximum number of columns that the C3PU crossbar can afford is 46 with degradation of 13.4% in the pulse width. Another option to accommodate large MAC operations is to duplicate the C3PU arrays similar to memory arrays. For example, multiple C3PU arrays can be placed to increase the number of columns and rows where a repeater can be used instead of the VTC to generate the pulse width signal.

To compare the proposed 5×4 C3PU crossbar, a 5×4 fixed point (FXP) crossbar units have been implemented using ASIC design flow in 65 nm CMOS. Table VI shows the 3×3-bit, 4×4-bit, 8×4-bit, and 8×8-bit FXP crossbars performance compared to the 5×4 C3PU crossbar. The error of the FXP MAC unit is calculated by comparing the observed output from the RTL simulation for each column in the crossbar with the expected ones from MATLAB simulation. The resultant error values are then averaged over 30 input sets. The average error of the C3PU, 5.6%, is comparable to the error percentage produced by the 8×4-bit MAC unit, 6.52%. Furthermore, the MSE values of the C3PU and 8×4-bit MAC crossbars are almost equal with 0.082 and 0.099, respectively. The advantage of the C3PU is the lower energy and area consumption by 3.4× and 3.6×, respectively, compared with the 8×4-bit MAC unit.

Table VII compares the prior and proposed work. The proposed C3PU utilizes an AMS circuit to perform analog MAC with two analog inputs, whereas the work in [22] and [6] uses an AMS circuit to conduct binary MAC with 1-bit×1-bit inputs. Comparing the C3PU with its equivalent digital baseline (8-bit×4-bit) in terms of accuracy, the energy efficiency is improved by 3.4×.

### IV. C3PU Demonstrator for ANN Applications

The advantage of the C3PU is demonstrated by accelerating the MAC operations found in an ANN using iris database [23]. The data set consists of 150 samples divided equally between the three different classes of the iris flower, namely, Setosa, Versicolour, and Virginica. Each sample holds the following features all in cm: sepal length, sepal width, petal length, and petal width. The architecture of the ANN consists of two layers: four nodes for the input layer, each representing one of the input features, followed by three hidden neurons, and lastly, three output neurons for each class. To implement the MAC operations in the ANN, the iris features are considered as the first operands, which are mapped into voltage values, and the weights are considered as second operands that are stored as capacitance ratios in the capacitive unit of the C3PU. A simple linear mapping algorithm is used between the neural weights and capacitance ratios [24].

The training phase is performed offline using MATLAB by dividing the data set between 80% training, and 20% testing. Post-training weights can have values with both positive and negative polarities. Hence, before mapping these weights into capacitance ratio values, they need to be shifted by the minimum weight value $w_{\text{min}}$. After performing the multiplication between the inputs and shifted weights, the effect of the shifting operation must be removed by subtracting the following term from all weights $\sum_{i=1}^{n} IN$, where $IN$ is the input to the hidden/output layer and $n$ is the number of input/hidden nodes. Mapping such operation into C3PU architecture requires adding one column to the hidden and output crossbars to store the $w_{\text{min}}$ value in each layer.

Figure 10 depicts the algorithm flow of the ANN classifier for the iris data set. It has two operational phases: phase 1 and phase 2. In phase 1, when $V_{clk}=1$ and $V_{d}=0$, the inputs are processed in the first layer. In phase 2, when $V_{clk}=0$ and $V_{d}=1$, the outputs from the first layer are taken and processed in the second layer to generate the required output iris classes. In phase 1, the four input features are mapped into four voltage levels $V_{in1-4}$. These voltages are then converted into four pulse width modulated signals $V_{pw1-4}$ using four VTC blocks discussed in section II-B. The bias voltage $V_{bias}$ is added as an input to better fit the ANN model, which is also converted into a pulse width modulated signal $V_{pw5}$. The
$V_{pw1-5}$, first operands, are connected to the $5 \times 4$ weight matrix C3PU as explained previously in Fig. 8. The weights, second operands, in this case, are stored as equivalent capacitance ratios $X_{eq}$ in the C3PU. The output voltages $V_{1-4}$ from the current integrator used at the end of each column in the C3PU weight matrix will act as inputs to the second layer. The current integrator inherently takes care of the scaling factor, which is decided depending on the factor between the shifted output values from a neural network and the output from the C3PU. This is important to compensate for the mapping between the values.

Once $V_{1-4}$ are generated, the classifier switches to phase 2 to process them to the second layer. But before that, the impact of shift operation that is implemented on the weights needs to be removed by subtracting $V_4$ from $V_{1-3}$. Then, the subtracted outputs are passed through the ReLu activation function. In the proposed ANN classifier, the subtraction operation and ReLu function are implemented in the time domain. To achieve such implementation, $V_{1-4}$ are first converted to pulse width modulated signals using VTCs and then passed to the time domain subtractor and ReLu activation function to generate $V_{o-pw1-3}$. These output signals may have small pulse widths due to the subtraction operation which does not correspond to the expected subtraction outputs. Therefore, the pulse widths of the $V_{o-pw1-3}$ are scaled by a constant factor depending on the expected subtraction output from the ANN using MATLAB and observed outcomes from the ANN using C3PU. After that, the scaled pulse width signals $V_{o-pw1-3-s}$ are fed to the $4 \times 4$ C3PU weight matrix. The output voltages from the weight matrix $V_{o1-4}$ are passed to the subtractor and then the softmax function to generate the proper class based on the input features.

Figure 11 shows the detailed circuit design implementation of the time domain subtractor, ReLu activation function, and delay element. Since $V_1$ is subtracted from three variables of $V_{1-3}$, then, each subtraction requires a separate digital circuit. The subtraction output can have a positive or a negative value. The ReLu activation function passes the positive value while assigning the negative value to zero. Such implementation is developed using AND, XOR, and inverter gates, as highlighted in the brown block in Fig. 11. To detect the difference between the pulse widths, the XOR gate is utilized and provides the subtraction output $a_{1-3}$. To determine the sign of the subtraction, $V_{4-pw4}$ is inverted and then ANDed with $V_{(1-3)-pw(1-3)}$ to generate a signal $b_{1-3}$. If any $b_{1-3} = 1$, then the subtraction output is positive, whereas when $b_{1-3} = 0$, the subtraction output is negative. Finally, AND gate is used to pass the positive subtraction output as $V_{o-pw1-3}$ while setting the negative subtraction output to zero. Figure 12 shows the output waveform example of the subtraction and ReLu function when $V_1 > V_4$ and $V_1 < V_4$. When $V_1 > V_4$, the pulse width of $V_{o-pw1}$ is generated whereas it is zero when $V_1 < V_4$. The subtraction output can have a positive or a negative value. The ReLu activation function passes the positive value while
implemented in the digital domain to increase the computing energy efficiency while achieving an acceptable accuracy. The quantization in the time domain may affect the MAC outputs of the 2nd C3PU crossbar. However, since the computation is employed for AI applications, relative results are sufficient for the classification purpose.

After that, the pulse width $T_{o-pw1}$ of the signal $V_{o-pw1}$ is approximately scaled by a factor of 18× based on the subtraction output values between the expected and observed ones. Such a large factor cannot be implemented using inverter delay. Consequently, a VTC circuit is utilized as a delay element to scale the pulse width of the $V_{o-pw1}$ by 18×. To achieve such a scale, the capacitors’ values in the VTC are adjusted ($C_1=50\text{ fF}$ and $C_2=2\text{ fF}$), and the input voltage is set to the supply voltage. The inverted subtraction output $\sim V_{o-pw1}$ is considered as the clock of the VTC. Depending on its pulse width value, the capacitors of $C_1$ and $C_2$ (as discussed in section II-B) are charged to a specific voltage level in the sampling phase. The higher the pulse width of the $\sim V_{o-pw1}$, the higher the voltage level across the capacitors and the longer time it takes to discharge through a current source in the evaluation phase. This means that the delay of the VTC’s output $V_{o-pw1-s}$ is proportional to the pulse width of the $V_{o-pw1}$. The ANN classifier has been designed and simulated in 65 nm CMOS technology with a supply voltage of 1V except the 5×4 and 4×4 weight matrices that operate at a supply voltage of 0.3 V. The input voltages $V_{in1−4}$ have a range of 0 V to 1 V in addition to $V_{bias}=1$ V. The five input voltages are converted into modulated pulse width signals $V_{pw1−5}$ that have pulse widths in the range of 165 ps to 2 ns. The modulated pulse width input signals $V_{o1−4}$ of the second weight matrix have a pulse width in the range of 1.6 ns to 7.5 ns. The pulse width $T_1$ of $V_{clk}$ is set to 3 ns, and the pulse width $T_2$ of $\sim V_{clk−d}$ is set to 9 ns. The proposed ANN classifier using C3PU shown in Fig. 10 achieves an inference accuracy of 90%, whereas the ideal implementation of the ANN classifier in MATLAB has an inference accuracy of 96.67%. The variation of the supply voltage by 5% affects the inference accuracy and reduces it by 3%. Monte Carlo simulation has been carried out to study the mismatch variations on the inference accuracy. Although the MAC outputs’ values from the C3PU crossbars have changed slightly, the inference accuracy remains 90%. This is because the classification does not depend on the exact MAC outputs but rather on its relative values.

V. CONCLUSION

This paper presented an analog-mixed signal MAC unit using cross-coupling capacitor implementation named C3PU. The advantage of utilizing a cross-coupling capacitor for storage and processing element is that it can perform simultaneously as a high density and low energy storage. One operand in the C3PU is stored in the capacitive unit. While the second operand is a modulated pulse width signal using a voltage-to-time converter. The multiplication outputs are transferred to an output current using CMOS transistors and then integrated using the current integrator op-amp. The 5×4 C3PU was developed to run all data simultaneously, realizing fully parallel vector-matrix multiplication in one cycle. The energy consumption of the 5×4 C3PU is 66.4 fJ/MAC at 0.3V voltage supply with an error of 5.7% in 65nm technology. The inference accuracy for the ANN architecture has been evaluated using the proposed C3PU for an iris flower data set achieving a 90% classification accuracy.

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Dima Kilani (S’13-M’21) received her PhD, M.S and B.S degrees in Electrical Engineering and Computer Science from Khalifa University, UAE, in 2019, 2015 and 2013, respectively. Her research focused on low-power mixed signal integrated circuit design including DC-DC power converters targeting high power efficiency. She is currently working as a postdoctoral fellow at the system-on-chip center (SoCC) in Khalifa University where she focuses on power management unit design for power-constrained devices. Dima works as a visiting scholar in Wayne State University, Detroit, MI researching system integration for wearable biomedical devices. She won the best paper session award in TECHCON-SRC in Texas, 2016.

Baker Mohammad (SM’13) earned his Ph.D. from University of Texas at Austin in 2008, his M.S. degree from Arizona State University, Tempe, and BS degree from the University of New Mexico, Albuquerque, all in ECE. He is an associate professor of electronic engineering at Khalifa University, and a consultant for Qualcomm Incorporated. Prior to joining Khalifa University, he was a Senior staff Engineer/Manager at Qualcomm and worked at Intel Corporation. He has over 16 year’s industrial experience in micro processor design with emphasis on memory, low power circuit, and physical design. His research interest includes power efficient computing, high yield embedded memory, emerging technology such as memristor, STT-RAM, and computer architecture, energy harvesting and power management unit.

Yasmin Halawani (S’14-M’20) received her B.S. degree from the University of Sharjah, UAE, in 2012, the M.S. by Research degree in 2014, and the Ph.D. degree in 2019, both from Khalifa University, UAE, and all in Electrical and Electronics Engineering. Her research projects focused on investigating the suitability of emerging memory technologies such as Memristor and STT-RAM for low-power applications. In addition, her research activities included the demonstration of the efficiency in-memory computing (IMC) for both analog and digital domains. She is currently working as a Post-Doctoral Fellow at Khalifa University in the area of memristor-based IMC architectures and artificial intelligence applications.

Mohammed F. Tolba received his B.Sc. in 2014, from Electronics and communications engineering, Fayoum University and M.Sc. in 2018 from Microelectronics System Design (MSD), Nile University. Currently, he is a research associate at SOC, Khalifa University. His research focused on digital design and implementation of deep learning, Convolution Neural Network (CNN), lightweight encryption, low-power approximation techniques, Graphics Processing Unit (GPU) architectures, computer arithmetic, fractional order circuits, Memristor, and chaotic circuits. Mohammed authored or co-authored over 28 journal and conference papers. Received the best paper award in Modern Circuits and Systems Technologies (MOCAST) 2017. In addition to the best master’s Thesis award July 2018.

Hani Saleh (M’12) is an assistant professor of electronic engineering at Khalifa University since 2012. Hani has a total of 19 years of industrial experience in ASIC chip design, microprocessor design, DSP core design, graphics core design and embedded system design. Prior to joining Khalifa University, he worked as a Senior Chip Designer (Technical Lead) at Apple incorporation and he worked for several leading semiconductor companies including Intel (ATOM mobile microprocessor design), AMD (Bobcat mobile microprocessor design), Qualcomm (QDSP DSP core design for mobile SOC’s) and Synopsys (a key member of Synopsys turnkey design group). Hani received a B.S in Electrical Engineering from the University of Jordan, a M.S in Electrical Engineering from the University of Texas at San Antonio, and a Ph.D. degree in Computer Engineering from the University of Texas at Austin. Hani research interest includes DSP algorithms design, DSP hardware design, computer architecture, computer arithmetic, SOC design, ASIC chip design, FPGA design and automatic computer recognition.