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An automated 55 GHz cryogenic Josephson sampling oscilloscope

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A computer-automated superconductive 55 GHz sampling oscilloscope based on 4 kA/cm$^2$, Nb/Nb$_2$O$_5$/Pb edge Josephson junctions is presented. The Josephson sampler chip was flip-chip bonded to a carrier chip with a coplanar transmission line by use of a novel flip-chip bonding machine. A 5.6 ps step pulse was successfully coupled in to the transmission line and 18.5 GHz multiple reflections plus a parasitic oscillation at 43 GHz were observed.

I. INTRODUCTION

For about ten years Josephson sampling oscilloscopes have been used in a wide range of cryogenic experiments to observe electronic signals with microampere amplitude and picosecond rise time. As the result of a collaboration between IBM Research Center, Yorktown Heights and Physics Laboratory I, The Technical University of Denmark we now have a computerized 2-55 GHz sampling oscilloscope with a sensitivity of about 1 μA. The measurement data are stored as sequential files and postprocessing is possible with a variety of programs. The oscilloscope sampling head employs hysteretic superconducting Josephson Junction circuitry operating at 4.2 K for both the sampling gate and the strobe pulse generator. Using a cryogenic sampling head reduces thermal noise at low temperatures; using superconducting materials allows a higher bandwidth in the measurements, since the resistive losses are very low up to the gap frequency of the superconductor (in this case about 700 GHz).

While Josephson samplers are usually integrated on the experimental chip, this procedure only allows measurements on the components on the experimental chip itself. In this work we have made an external connection to the sampler chip by means of the flip-chip bonding technique in order to use the sampler as a multipurpose cryogenic instrument.

Figure 1 shows the 6×6 mm$^2$ silicon sampler chip (SC) connected face to face with a 1×1 in.$^2$ sapphire carrier chip (CC). The surface of the carrier chip has a 1-μm-thick superconductive niobium pattern including the coplanar transmission line (tl) that provides the high frequency connection to the sampler chip.

The 5-20 μm spacing between the sampler chip and the carrier chip, which is typical for the flip-chip bonding technique, makes it possible to obtain much lower inductance leads to the sampling circuit than would be possible using traditional bond wires. This advantage is increasingly important as the signal frequency goes up into the GHz range, since the high inductance of traditional bonding wires leads to a significant parasitic impedance at such high frequencies. For this reason the flip-chip bonding technique is a good alternative to wire bonding for high frequency interconnections.

It should be noticed that hysteretic Josephson junctions were recently fabricated by Virshup et al. using high temperature superconductors. By utilizing such junctions it will be possible to operate superconductive samplers at higher temperatures in the future.

II. THE SAMPLING CIRCUIT

The superconductive oscilloscope utilizes a fast spike-like electrical pulse of approximately 5.5 ps full width at half-maximum (FWHM) which strobes the electrical signal under measurement one point at a time as shown in Fig. 2. The high frequency signal has to be identically repeated many times in order to scan the entire signal, and for this the repetition frequency can be much lower than the signal frequency. We use a 10 kHz repetition rate.

The amplitude of the signal is determined by means of a summing comparator with a threshold level $I_c$. The comparator is fed by the signal $I_{\text{signal}}(t)$, the strobe pulse $I_{\text{strobe}}(t_p)$ occurring at time $t_p$, and a feedback current $I_{\text{fb}}(t_p)$. Because the signal is repeated, the feedback circuit can be made as an integrating counter that will adjust the feedback current $I_{\text{fb}}(t_p)$ so the comparator will switch to its voltage state (at $I=I_c$) with 50% probability. The following threshold condition is then fulfilled at the time $t_p$ of the signal

$$ I_c = I_{\text{signal}}(t_p) + I_{\text{strobe}}(t_p) + I_{\text{fb}}(t_p). \quad (1a) $$

Since the threshold level ($I_c$) as well as strobe amplitude ($I_{\text{strobe}}$) are fixed, the signal can be determined from

$$ I_{\text{signal}}(t_p) = -I_{\text{fb}}(t_p) + \text{const}. \quad (1b) $$

It is important to notice that in this way only one point in the signal is determined when the feedback current has been set by the feedback circuit. After that the position ($t_p$) of the strobe current relative to the signal can be changed and a new amplitude value can be determined. By scanning
FIG. 1. The sampler chip (SC) flip-chip bonded to the top of the carrier chip (CC). The end of the coplanar transmission line (tl) with its three connection pads can be seen to the right of the sampler chip.

the strobe pulse in time relative to the signal the entire high frequency signal will be measured.

Figure 3 shows the current voltage characteristic of a Josephson junction based interferometer, to illustrate how it can be used either as a comparator gate or a pulse generator. In the zero voltage state the current injected into the interferometer is less than the critical current $I_c$. If the current exceeds $I_c$, the junction will switch to the voltage state and stay there until the current is lowered following the quasiparticle curve (QP). In this mode the interferometer works as a threshold detector. In the pulse generator mode, we benefit from the fact that the switching time from the zero voltage state to the voltage state is only a few picoseconds.

The sampler circuit we use is part of a larger scientific chip, SCT-2, developed in 1983 at the IBM Research Center, Yorktown Heights using the Nb/Nb$_2$O$_3$/Pb technology with a junction current density $J_c$ of 4 kA/cm$^2$ and a capacitance to critical current ratio $C'/J_c$ of 2.5 pF/mA. The bandwidth of the sampler is determined by the dynamics of the Josephson junctions together with their embedding circuits and limited to about 55 GHz. In Fig. 4 it is seen that the sampler strobe pulse generator consists of two Josephson junctions (JJ1, JJ2) in the interferometer configuration, plus a third junction (JJ3). This scheme was originally proposed by Faris et al. The strobe pulse starts when the interferometer (JJ1, JJ2) switches to the voltage state. The switch creates a fast rising current ramp that picoseconds later will make the third junction (JJ3) also switch to its voltage state. The junction JJ3 will block the rising current and cause a descending ramp, so that a spike shaped pulse is generated.

The comparator—which acts as the latching sampling gate—is a two junction (JJ4, JJ5) interferometer with the signal, strobe pulse, and feedback currents inductively cou-
SIP-chip bonded to the carrier chip, the input terminals are connected to the high frequency coplanar transmission line. When the SCT-2 chip is flip-chip bonded to the carrier chip, the input terminals are connected to the high frequency coplanar transmission line. As shown in Fig. 4 a step-pulse generator on the SCT-2 chip is connected to the transmission line. In this way it is possible to generate a step pulse that will propagate down the transmission line to the load and subsequently return to the sampling gate to be measured. By using the step-pulse generator in this scheme, the instrument works as a fast and sensitive time domain reflectometer (TDR) where the time difference between the outgoing step pulse and the incoming signal is roughly determined by twice the propagation time for the pulse on the transmission line.

III. THE CONTROL ELECTRONICS

Figure 5 shows the setup that includes the superconductive sampler chip in a cryostat cooled to 4.2 K by means of liquid helium. The cryostat is of the two Dewar vertical type with the outer Dewar for liquid nitrogen at 77 K, and the inner Dewar at liquid helium temperature, 4.2 K. Two liters of liquid He allows for 8 h of operation.

The electronics includes:

* A PC computer with a standard serial RS232 interface connected to a microcomputer system with analog-to-digital (A/D) converters, strobed digital-to-analog (D/A) converters, delay line step-motor control, and a general purpose interface bus (GPIB) parallel interface. The GPIB is connected to the Tektronix (11320) programmable analog oscilloscope which monitors all signals to and from the sampler circuit. The Tektronix oscilloscope also provides the 10 kHz system clock that determines the repetition rate of the signal to be measured.

* 12 bit strobe resettable D/A converters with the output fed into 15 kHz low pass filtered current generators that in turn are connected to the bias lines of the interferometers on the sampler chip.

* ×1000 voltage amplifiers that amplify the voltage across the Josephson junction interferometers. When a Nb/Pb Josephson junction switches to its voltage state the voltage across the junction is only 2.7 mV. The amplifiers are therefore necessary to isolate the Josephson junction interferometers and to provide a voltage level compatible with the subsequent A/D converters and the feedback circuit.

* A feedback circuit based on an integrating counter and a current generator. The time constant of the integrator and the switching probability of the comparator can be chosen independently.

* A HP8080 pulse generator that provides 650 ps FWHM time-synchronized trigger pulses for the sampler strobe pulse generator and the step generator.

* A 1000 ps delay line with a step-motor control allowing a time resolution of ~0.2 ps. The delay-line length (1000 ps) determines the lower measuring frequency of 2.0 GHz. The delay is computer controlled.

* Automatic measurement of the IV curves and critical current versus feedback current for the gates on the sampler chip.

* Automatic setting of the repetition frequency, the monitoring oscilloscope, and the sampler-gates bias currents.

* For a measurement of a high frequency signal the software includes: use of cursors, zoom, digital low pass filtering—smoothing, and a Fourier-transform routine. Data are stored to a disk drive as sequential ASCII files that can be transferred to other types of programs (e.g., spreadsheets).

IV. FLIP-CHIP MOUNTING

As shown in Fig. 1 the superconducting sampler chip (SC) is flip-chip bonded to the larger carrier chip (CC). The CC contains a niobium pattern for connections to the controlling electronics and the coplanar transmission line. The transmission line in turn provides the high frequency connection between the SC and a device under test.
(DUT). The 1×1 in.² CC substrate is of 0.8-mm-thick sapphire. The SC has contact pads for the controlling currents along the edges and the pads for the transmission line at the center of the chip. The edge pads are 100 by 280 μm² and the two pads at the center shown in Fig. 6 are 140 by 140 μm.² In total we connected 22 pads from the SC to the CC. After flip-chip bonding the sampler chip, a DUT chip can be bonded to the three pads at the end of the transmission line.

The contact resistance which needs to be less than about 0.1 Ω depends on the mechanical quality of the interface between the bonding pads and on the materials used. If we simply press the SC and the CC together, the contact resistance is determined by the contact pressure and the nonuniformity of the heights of the carrier chip pads. For this reason soft-metal type contacts were used which allowed the automatic leveling of the contacts by applying pressure. Using this technique the contact resistance was always below 0.1 Ω measured by the two point method.

Commercial systems for aligning and bonding are available but are expensive and are mainly dedicated to semiconductor industry applications. We chose to develop the much simpler flip-chip bonding machine shown in Fig. 7. The setup consists of two parts: (1) a X20 stereo microscope and (2) the machine itself. The carrier chip is held by a vacuum face upwards on a platform which can be moved in the x and y directions and a chuck that moves in the z direction perpendicular to the platform. The carrier chip (CC) is mounted on the platform and the sampler chip (SC) is placed on the chuck. Both chips are held by a vacuum that is controlled by a gate valve with a lever. During bonding the whole setup can be rotated around two axes to allow inspection of the space between the two chips from different sides. Heating of the platform and the carrier chip for soldering is done by a soldering iron inserted into the platform. Bonding can be performed with an accuracy of better than 10 μm.

In early experiments solder bumps were placed on the contact pads of the CC by solder dipping using eutectic Pb/Sn as in Ref. 11. Before the dip soldering the Nb pads were coated with a 2 μm copper layer. The bumps were about 30 μm high before the bonding but shrank to less than 15 μm during bonding. To ease bonding and to reduce the needed pressure the height (typical spread ~3 μm) of the solder bumps could be equalized by pressing a thick plane glass plate onto the pads. The bump deformation could be watched through the glass plate and it was easy to see when all bumps had the same height.

Even though this technique of pressing the SC and CC together worked, it turned out to be not fully reliable during cooldown. To solder the SC and CC together, we changed the procedure for making the contact pads on the CC. Because the original CC was made of sapphire while the SC is on a silicon substrate, soldering cannot be done due to the difference in thermal expansion coefficients (the bonding would crack during cooldown to liquid He temp-
peratures). Therefore 1 x 1 in.\(^2\) substrates were cut out from 0.2 mm Si wafers and used as CCs (thicker wafers should preferably be used to avoid bending and breaking). After this, about 20 µm high copper pads were electrochemically deposited on the CC through a photoresist mask in an acid copper-sulphate solution (20 g crystal, CuSO\(_4\)·5H\(_2\)O, 2.1 ml (95%) H\(_2\)SO\(_4\), 100 ml H\(_2\)O) applying a current density of 30 mA/cm\(^2\) through the photoresist mask. The electroplated layer had a rather rough surface and was not 100% homogeneous. It was smoothed by gently grinding the CC face down on a fine grinding stone (Hard Arkansas Oilstone, HB5). After cleaning, dip soldering was carried out in a low melting point texture, Rose's metal (50% Bi, 25% Sn, 25% Pb), with the melting point of 85–90 °C. This results in sandwich type contacts with equal height and a top layer of solder with a low melting point.

The bonding machine was fitted for soldering with a platform of copper, which is thermally decoupled by a fiberglass plate. Furthermore a hole was drilled in the platform to fit a copper rod that in turn fits into a temperature regulated solder iron. In this way the platform and the CC can be heated up to a controlled temperature. The two chips are first aligned without touching and without heating the platform. When alignment is completed the SC is levitated well above the CC and the solder iron is turned on. After the melting point of the solder is reached, the SC is gently lowered down and pressed onto the CC. The sudden thermal contact causes the solder to solidify instantly and, to avoid further heating of the SC, the sandwich is quickly removed from the bonding machine. This method gives a bonding that stands repeated thermal cycling between 300 and 4.2 K.

V. EXPERIMENTAL RESULTS

Because the soldering procedure using a silicon CC was introduced at a later stage in the project the following data were obtained using sapphire substrates without soldering.

A. A test signal

Figure 8 shows a test signal from the step-pulse generator on the sampler chip itself without connection to the coplanar transmission line. The rise time of this 220 µA signal was 5.6 ps (10% to 90%), and the bandwidth of the instrument can be estimated to be

\[ \frac{1}{\pi/5.6 \text{ ps}} \approx 55 \text{ GHz}. \]

B. The sampler as a TDR instrument

We connected the comparator and the step-pulse generator to a coplanar transmission line with nominally 25 Ω impedance. Before connecting a device to the transmission line, we investigated the quality of the transmission line itself. For this purpose a simple short circuit was placed on the transmission line, 4.0 mm away from the sampling circuit. The measured signal is shown in Fig. 9. Because the transmission line was short circuited, the step pulse was reflected as a negative going pulse at the end of the transmission line end. Adding the negative reflection to the step pulse, the signal amplitude becomes zero when the negatively reflected step returns to the sampler. The amplitude of the main pulse was 45 µA and the time from the foot of the rising part of the pulse to the point where the pulse starts decreasing from its maximum is 52.5 ps. These 52.5 ps are twice the propagation time for the pulse on the transmission line. Some undershoot at the end of the pulse and a tail of damped oscillations with a 23 ps period time can be seen. The rise time of the pulse is about 20 ps, a value much slower than the intrinsic rise time of the step-pulse generator.

VI. DISCUSSION

A. The transmission line

Since the comparator is in parallel with the transmission line, the fast step-generator pulse is divided between...
the comparator and the transmission line. This leads to a
suppressed signal amplitude compared to the test signal, as
shown in Fig. 9. From the slow rise time we conclude that
the impedance of the transmission line is mainly capacitive.
This is not surprising since the sampler chip is only about
10 \mu m above the transmission line and the coplanar trans-
mision line has an open structure. Both effects can be
expected to produce an extra stray capacitance. The stray
capacitance ($C_{SC}$) of the transmission line to the ground
plane of the sampler chip is 1-4 pF [calculated by the area
of the transmission line facing the SC, the 10-15 \mu m spacing
between the chips, and the gap partially filled with SiO
($\varepsilon_r=5$)]. In order to obtain the shorter rise time of about
6 ps which is typical for the step-pulse generator the rela-
tively large stray capacitance of 1-4 pF should have been
reduced. We used coplanar transmission lines because they
are easy to fabricate but a drawback is their open structure.
A smaller stray capacitance could have been obtained ei-
er by using a closed structure transmission line, e.g., by
fabricating a microstrip line with the ground plane facing
the sampler chip or by placing the sampler circuit at the
very edge of the sampler chip.

Figure 10 shows the pulse end and the oscillation in
detail where the data have been low pass filtered by three
point triangular running average. This procedure normally
improves current resolution at the cost of bandwidth, but
in this case, by over sampling the signal, the low pass
filtering does not effectively lower the bandwidth. The inset
in Fig. 10 shows the Fourier transform of the original sig-
na data. Two frequencies are clearly visible; the lower one
at 18.5 GHz which is the result of multiple reflections
between the sampler/transmission line connection, and the
higher one at 43 GHz which corresponds to the 23 ps tail
oscillation. The 23 ps tail of oscillations in Figs. 9 and 10 is
probably due to a resonance between the inductances in the
bonding to the transmission line ($L_{bond}$), combined with
the 1-4 pF stray capacitance of the transmission line to
the sampling circuit. A value for the parasitic inductance
$L_{bond}$ using the flip-chip bonding technique can only be
estimated very roughly from the height of the Pb/Sn
bonding pads on the carrier chip. By assuming that the
signal current is confined to the edges of the contact pads
due to the skin effect we can use $\mu_0/4\pi$ as the intrinsic
inductance. The kinetic inductance of the Cooper pairs\(^ {14}\)
in the superconductor and the geometric inductance of the
contact pads should also be added, but the intrinsic pad
inductance can still be used as an estimate of the lowest value

$$L_{bond} > 2 \times 15 \mu m \times \mu_0/4\pi = 3 \, \mu H.$$ 

These estimates of stray capacitance and parasitic inductance
leads to an estimated $L_{bond}$-$C_{SC,CC}$ time constant of
10-20 ps or greater, in fairly good agreement with the
measured tail oscillation time of 23 ps.

B. Noise

The cryostat is screened by Cu and mu-metal shields
(Vacuumschmelze). Since Josephson junctions are sensitive
to magnetic fields it is essential to have a good mag-
netic shielding. We found for that two concentric mu-metal
rounds plus a cylindrical 8-cm-diam superconductive Pb
shield around the holder for the sampler chip and trans-
mmission line gave good magnetic shielding and long term
stability for the measurement. One drawback of the super-
conductive shield is that the shield itself may trap magnetic
flux and thus disturb the Josephson junctions. Slow cooling
of the sampler chip and shield, however, reduces the ther-
moelectric currents that generate magnetic fields and in
this way the trapped flux can be reduced to an acceptable
level.

Due to the latching nature of the Josephson junctions, noise
conducted via the control lines to the strobe pulse
generator only affects the amplitude of the strobe pulse
slightly. A more severe effect is that the noise alters the
time level of the strobe pulse generator and hence gen-
erates time jitter of the strobe pulse relative to the signal.
Jitter, together with the feedback circuit coupled to a
threshold detector, will impose an ultimate time resolution
that can be understood in the following way. The feedback
circuit is set to a 50% switching probability and if we
consider a signal which is a short pulse, the pulse can only
be detected if more than 50% of the strobe pulses coincide
with it. If the switching probability cannot reach 50% the
feedback circuit will indicate a zero signal. Such as pulse
will never be detected. Assuming a Gaussian distribution
of the strobe jitter relative to the signal we get

$$P_{switch} = 0.5 - erf(x) \quad \text{with} \quad x = \Delta t_{min} / \sigma_{jit},$$
(2a)

where $\Delta t_{min}$ is the minimum detectable pulse width and $\sigma_{jit}$
is the jitter spread. Using a standard table we get

$$\Delta t_{min} \sim 1.36 \sigma_{jit}. \quad (2b)$$
Equation (2b) shows that the jitter imposed time resolution in a system with a threshold detector is slightly larger than the strobe jitter spread. In early experiments the noise was too large, and as a consequence the time resolution was jitter limited to about 10 ps. By introducing cooled attenuators for the trigger lines and by using the same trigger pulse divided for the signal generator and strobe pulse generator trigger, respectively, the time resolution of about 5 ps was reached. In our equipment, it is not possible to obtain a better time resolution than 5 ps because this limit is set by the width of the strobe pulse.

By doing repeated measurements on the signal in Fig. 8 and calculating the spread in the measured signal value $\sigma[l_{\text{signal}}(t_p)]$, a clear correlation between the pulse edge steepness ($\mu$A/ps) and the spread in the measurement was found

$$\sigma[l_{\text{signal}}(t_p)] = 0.5 \mu A + 1.0 \text{ ps} \times \frac{dl_{\text{signal}}(t_p)}{dt}. \quad (3)$$

This means that the spread in a measured signal value is 0.5 $\mu$A if the signal has no time variation and the spread rises in proportion to the time derivative of the signal. Assuming a linear relation between the signal spread and the jitter spread, the jitter spread can be inferred to be 1.0 ps from Eq. (3). Inserting this value into Eq. (2b) the ultimate jitter imposed resolution would be about 1.5 ps. This value is (and should be) well below the 5 ps strobe pulse width, but jitter still deteriorates the accuracy of a measured signal value according to Eq. (3).

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