A High-Stability Regulation Circuit with Adaptive Linear Pole–Zero Tracking Compensation for USB Type-C Interface

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Abstract: We present a high-stability regulation circuit to ensure the safety of a device within a wide range of the back-sink current for a USB Type-C interface application. The proposed adaptive linear pole–zero tracking compensation can linearly compensate for the changes in the back-sink current, thereby adaptively canceling the pole–zero changes caused by the current changes. The simulation results show that the phase margin remains greater than 60°. Meanwhile, the loop bandwidth changes between 45 kHz and 135 kHz, when the current increases from 0 A to 1 A, ensuring excellent loop stability. The high-stability regulation circuit is realized in a standard 180 nm CMOS process with an area of 0.4 mm × 0.6 mm. The chip regulates an output voltage from 4.5 V to 5.5 V with 1 A current capacity and 100 mV maximum dropout voltage with the help of the adaptive linear pole–zero tracking compensation.

Keywords: USB Type-C interface; adaptive linear pole–zero tracking compensation; loop stability

1. Introduction

The USB Type-C interface is significantly advantageous over the conventional data transmission interfaces and has been widely used in various portable electronic devices such as notebooks, desktops and smartphones [1]. The current-limiting switch between the Type-C interface and peripherals is employed to prevent overcurrent, short-circuit or even reverse-current, thus effectively protecting the safety of the host and the device.

Figure 1 shows the schematic structure of a typical USB interface protection circuit. Two NMOS switches MSW1 and MSW2 are connected in series, and the substrate can be prevented from being turned on when the switch is turned off. In practice, MSW1 is used for the current limit protection while MSW2 is employed to protect against the reverse current. The voltage stabilization loop used to control MSW2 is similar to the LDO structure, but the difference from the traditional LDO is that the dropout voltage of the loop needs to be reduced (<100 mV) to avoid the power loss of the switch itself [2–11]. Under such a low dropout voltage, the working state of the MSW2 transistor is approximately in the linear region. It should be noted that according to the protocol requirements of USB3.X, the current flowing through the switch varies from 0 A to several amperes corresponding to the change of the load on the output terminal of the switch, which poses difficulties for the compensation of the loop stability [1].
Due to the large capacitance (microfarad-level) connected to the switch output as the stabilized capacitor for power supply measurement, the output pole appears at a very low frequency when the load current is small. A large capacitance is thus required for conventional Miller compensation, which, however, is unacceptable for a chip application with limited floor space. On the other hand, the traditional equivalent series resistor (ESR) compensation has the problem of zero drift with limited compensation stability [2]. Dynamic pole–zero tracking frequency compensation can compensate the first nondominant pole in multistage op-amps by dynamically generating zeros [3,4]. However, in the conventional pole–zero compensation method, although the tracking MOS transistor works in the saturation region, the zero resistance works in the linear region leading to a continuous change in the impedance, which can further result in a large variation in the relative position of the pole–zero in the full current range. This can have a significant influence on the variation range of the bandwidth, making it unsuitable for the application of a current limiting switch system. In this work, an adaptive linear pole–zero tracking compensation method is proposed by introducing a current detection loop and a constant bandwidth tracking loop. While the loop stability is not affected by the change of the load current, the gain bandwidth of the entire loop is constant at a certain level.

2. Traditional Regulation Circuit with Pole–Zero Tracking Compensation

Figure 2 shows the schematic structure of the circuit design with traditional pole–zero tracking compensation. The regulator loop is composed of a two-stage amplifier, pole–zero tracking voltage generator and output stage. The pole–zero (PZ) dynamic compensation is realized by the output current sensor, PZ tracking voltage generator, Msz and Cc circuits. The current sensor mirrors and tracks the output current and realizes 1/K current scaling by adjusting the mirror ratio of Msbw and Msbw. The drain voltages of Msbw and Msbw are equal through the function of OP1, achieving accurate copying of the current, which is subsequently output through the current mirror composed of Ms2 and Ms2. The current of Ms5 is the output of Ms2 and Ms2 current mirrors. As a result, the Vgs voltage of Ms2 is proportional to the output current. In addition, Ms2 and Cc form a zero, and the gate–source voltages of Msz and Ms are the same, which makes the on-resistance of Msz proportional to the output current. When the output current decreases, the output pole (po) and the Vgs voltage of Msz decrease. With a larger impedance of Msz, the frequency of the zero formed by Msz and Cc is lowered, realizing the tracking compensation of the output pole. The compensated voltage stabilizing loop has only one dominant pole at the output of EA1, which makes the entire loop stable.

Figure 1. Schematic diagram of the USB interface protecting circuit.
From the above analysis, there exist two dominant poles located at $V_{OUT}$ and $EA1$ in the traditional circuit with varying load current. In addition, the $P_o$ at the $V_{OUT}$ terminal will change with the varying load current. For example, with a small output current, $R_L >> R_{MSW2}$ (meanwhile, $R_{MSW1} << R_{MSW2}$), and the output impedance at the $V_{OUT}$ terminal is:

$$R_L = \frac{V_{OUT}}{I_o}$$  \hspace{1cm} (1)

$$P_o = \frac{1}{R_L \times C_L}$$  \hspace{1cm} (2)

The $V_{GS}$ voltage of $MP5$ is calculated as:

$$V_{GS{P5}} = \sqrt{\frac{I_o}{K \times \beta \times \frac{W_{P5}}{L_{P5}}}} + V_{THP}$$  \hspace{1cm} (3)

Since the $V_{GS}$ values of $MRZ$ and $MP5$ are the same, and $MRZ$ is operating in the linear region, the on-resistance of $MRZ$ is:

$$\frac{1}{R_Z} = \frac{W_{RZ}}{K \times \beta \times \frac{V_{OUT}}{L_{RZ}}}$$  \hspace{1cm} (4)

Thus, the zero formed by $MRZ$ and $CC$ can be expressed as:

$$Z_c = \frac{1}{R_Z \times C_C} = \frac{W_{RZ}}{K \times \beta \times \frac{V_{OUT}}{L_{RZ}}} \times \frac{1}{C_C}$$  \hspace{1cm} (5)

The $K$ in Equations (3)–(5) represents the ratio of sensor current, and $W_{MP5}$ and $L_{MP5}$ are the channel width and length of the $MP5$ transistor. The frequency compensation can be achieved by using $Z_c$ to cancel out $P_o$. However, due to the different dependence of $P_o$ (Equation (2)) and $Z_c$ (Equation (5)) on $R_L$, $Z_c$ cannot track the change of $P_o$ well when $R_L$ varies in a large range. This can further result in a large change in bandwidth as well as a deterioration in stability.
3. Proposed Regulation Circuit with Adaptive Linear Pole–Zero Tracking Compensation

To solve the above issue, we propose a regulation circuit with an adaptive linear pole–zero tracking compensation, which is schematically illustrated in Figure 3. The entire circuit includes a two-stage amplifier (AMP STG1 and AMP STG2), buffer stage, output current sensor, adaptive linear PZ tracking voltage generator, output power transistor and load resistor and capacitor. Among these components, the AMP STG1 provides gain and the AMP STG2 provides low output impedance to push the output pole farther from the origin. The output power transistor provides a large current, and the output current sensor can achieve accurate reproduction of the output current. The adaptive linear PZ tracking voltage generator is used to perform the compensation of the output pole making the unity-gain bandwidth (GBW) of the feedback system constant while ensuring stability.

![Figure 3. Proposed structure of regulation circuit with the adaptive linear pole–zero tracking compensation.](image)

Figure 3. Proposed structure of regulation circuit with the adaptive linear pole–zero tracking compensation. (RZ is the equivalent impedance of the NMOS MRZ; I_bias and I_bias1 are bias currents. V_pump is the high-level supply voltage in the USB interface protecting circuit.)

Figure 4 shows the pole–zero distribution of the proposed regulation circuit. There are four poles (P1~P3, Po) and a zero (Zc) in the circuit illustrated in Figure 3.

![Figure 4. The pole–zero distribution of the proposed regulation circuit.](image)

Figure 4. The pole–zero distribution of the proposed regulation circuit.

The four poles can be expressed as:

\[
P_1 = \frac{1}{R_{o1}C_{o1}}
\]

(6)

\[
P_2 = \frac{1}{R_{o3}C_{o2}}
\]

(7)

\[
P_3 = \frac{1}{R_{o3}C_{o3}} = \frac{g_{MNSW}}{C_{o3}}
\]

(8)
\[ P_e = \frac{1}{R_L C_L} \]  

Figure 5 shows the detailed structure of the adaptive linear pole–zero compensation voltage regulation circuit (\(M_{SW1}\) and \(M_{SW2}\) are represented and labeled by \(M_{SW}\) for a better description). The linear pole–zero tracking voltage generator is composed of OP2, \(M_{N5}\) and \(R_s\). The voltage potential at points A and B are clamped to be equal though OP2, which makes the \(V_{DS}\) voltage of \(M_{N5}\) equal to the voltage across \(R_s\), \(V_{DSN5} = V_{RB}\). \(M_{N5}\) can be modulated to work in the linear region through \(V_{RB}\) making \(V_{DSN5} = V_{RB} = V_{\text{drop}}\). The output of OP2 also functions as the gate voltage of both \(M_{RZ}\) and \(M_{N5}\).

Figure 5. The detailed structure of the linear adaptive pole–zero compensation voltage regulation circuit.

From the circuit shown in Figure 5, \(M_{N5}\) is in the linear region, and the drain–source current of \(M_{N5}\) is:

\[ I_{DSN5} = \beta \times \frac{W_{N5}}{L_{N5}} \times (V_{GSN5} - V_{THN}) \times V_{DSN5} \]  

There is a fixed 1/K relationship between the drain–source current of \(M_{N5}\) and the output current due to the current mirror:

\[ I_{DSN5} = \frac{I_o}{K} \]  

From Equations (10) and (11), the \(V_{GS}\) of \(M_{N5}\) transistor is:

\[ V_{GSN5} = \frac{I_o}{K \times \beta \times V_{DSN5} \times \frac{W_{N5}}{L_{N5}}} + V_{THN} \]  

Considering the fact that the \(V_{GS}\) values of \(M_{RZ}\) and \(M_{N5}\) are the same, and both work in the linear region, the on-resistance of \(M_{RZ}\) can be obtained by:

\[ R_z = \frac{1}{K \times \beta \times \frac{W_{RZ}}{L_{RZ}} \times (V_{GSRZ} - V_{THN})} \]  

\[ V_{GSRZ} = V_{GSN5} \]  

From Equations (11)–(14), we can obtain:
The corresponding zero can be obtained from Equation (15):

\[
Z_C = \frac{1}{R_{Z}C_C} = \frac{I_o \times W_{RZ}/L_{RZ}}{W_{NS}/L_{NS}} = \frac{1}{C_C} \times \frac{V_{OUT} \times W_{RZ}/L_{RZ}}{R_L \times W_{NS}/L_{NS}} \times \frac{1}{C_C}
\]  

(16)

Compared to the traditional circuit design, in our proposed circuit design, both \( P_o \) and \( Z_C \) are in a first-order linear relationship to \( R_L \), as indicated by Equations (9) and (16), respectively, realizing the linear tracking and compensation of \( Z_C \) with a different loading current.

4. Simulation and Experimental Test Results

The positions of the poles are the outputs of each stage with \( P_1 \) as the dominant pole and \( P_o \) as the first nondominant pole. \( P_2 \) and \( P_3 \) are far away from \( P_1 \) due to the small equivalent input capacitance and equivalent output impedance, and do not affect the stability of the loop. Then, we can plot the location of the poles of the proposed regulation circuit as shown in Figure 6. From Equations (9) and (16), it can be seen that both \( Z_C \) and \( P_o \) have a first-order linear proportional relationship with \( I_o \). When the load changes, \( Z_C \) can be used to track and compensate for the change of \( P_o \) linearly. Thus, we can obtain a high-stability loop in a wide current range.

**Figure 6.** The location of the poles of the proposed regulation circuit.

Figure 7 shows the continuous change of GBW and the phase margin under different load currents. The current changes from 0 A to 1 A, and the GBW changes from 45 kHz to 135 kHz. The phase margin is greater than 60° in the full current range ensuring excellent loop stability.

**Figure 7.** The simulation results of (a) GBW and (b) phase margin with \( I_o \) from 0 A to 1 A.
The proposed high-stability regulation circuit was designed in a 180 nm CMOS process. The chip micrograph is shown in Figure 8, and the die size is 400 × 600 μm².

**Figure 8.** The chip micrograph.

Figure 9 shows the measured load transient responses when the load changes between 0.2 A and 1 A. From the figure, the output Vo shows undershoot and overshoot voltages of −187.6 mV and 175.4 mV, respectively. The 0.5% settling times are 175 μs and 177 μs, respectively. The test result indicates an enhanced working stability of the entire loop.

**Figure 9.** Measurement output voltage Vo and output current Io waveforms under load transitions between 0.2 A and 1 A.
Finally, we compared the performance that can be achieved by the currently reported compensation methods of voltage stabilisation loops. The comparison is listed in Table 1 in terms of process, dropout voltage, output capacitor and the maximum output current $I_{o}(\text{max})$. From the comparison result, it is found that within the full load range, the bandwidth change of the regulation circuit proposed in this paper is the smallest, the stability of the system is better and a smaller drop voltage can be achieved.

Table 1. Comparison Table.

| Technology (nm) | Ref. [6] | Ref. [9] | Ref. [10] | Ref. [11] | This Work |
|----------------|---------|---------|---------|---------|-----------|
| Power MOS | 180 | 130 | 90 | 180 | 180 |
| Output cap. (μF) | 4.7 | 4 | 1 | 17 | 10 |
| Supply voltage (V) | 1.6–5.5 | >1.15 | 1 | 1.5–3.3 | 4.5–5.5 |
| Quiescent current (μA) | 424 | 50 | 46 | 790 | 100 |
| Output current (A) | 1 | 0.025 | 0.1 | 6 | 2 |
| Dropout voltage (mV) | 200 | >150 | 150 | 110 | 75 |
| GBW range | - | - | - | 26.5–1.48 MHz | 45–135 kHz |
| PM range | 35–95° | - | - | 14.9–61° | 61–80° |
| Area (mm × mm) | 1.4 | 0.049 | 0.0041 | 6.3 | 0.24 |

5. Conclusions

In summary, an adaptive linear pole-zero tracking compensation was proposed in this paper, by changing the tracking transistor from the traditional saturation region to the triode region for a good linear match to the resistance of the zero-adjusting resistor. The frequency change of the zero and the first nondominant pole was linearly consistent. From the simulation and test results, the bandwidth change range was very small within the full load range, due to the high linearity of the zero and the first nondominant pole with the load change. Further delicate circuit design and engineering will shed more light on this issue towards advanced USB Type-C interface applications.

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