A Many-core Machine Model for Designing Algorithms with Minimum Parallelism Overheads

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Abstract

We present a model of multithreaded computation, combining fork-join and single-instruction-multiple-data parallelisms, with an emphasis on estimating parallelism overheads of programs written for modern many-core architectures. We establish a Graham-Brent theorem for this model so as to estimate execution time of programs running on a given number of streaming multiprocessors. We evaluate the benefits of our model with four fundamental algorithms from scientific computing. In each case, our model is used to minimize parallelism overheads by determining an appropriate value range for a given program parameter; moreover experimentation confirms the model’s prediction.

1 Introduction

Designing efficient algorithms targeting implementation on hardware acceleration technologies (multi-core processors, graphics processing units (GPUs), field-programmable gate arrays) creates major challenges for computer scientists. A first difficulty is to define models of computations retaining the computer hardware characteristics that have a dominant impact on program performance. Therefore, in addition to specify the appropriate complexity measures for the algorithms to be analyzed, those models must consider the relevant parameters characterizing the abstract machine executing those algorithms. A second difficulty is, for a given model of computations, to combine its complexity measures so as to determine the “best” algorithm among different algorithmic solutions to a given problem.

In the fork-join concurrency model two complexity measures, the work $T_1$ and the span $T_\infty$, and one machine parameter, the number $P$ of processors, can be combined in results like the Graham-Brent theorem or the Blumofe-Leiserson theorem (Theorems 13 & 14 in [2]) in order to compare algorithm running time estimates. We recall that the Graham-Brent theorem states that the running time $T_P$ on $P$ processors satisfies $T_P \leq T_1/P + T_\infty$. A refinement of this theorem supports the implementation (on multicore architectures) of the parallel performance analyzer Cilkview [10]. In this context, the running time $T_P$ is bounded in expectation by $T_1/P + 2\hat{T}_\infty$, where $\delta$ is a constant (called the span coefficient) and $\hat{T}_\infty$ is the burdened span.

With the pervasive ubiquity of many-core processors, in particular GPUs, it is desirable for models of computations to combine explicitly both task-based parallelism and data-based parallelism. In fact, popular concurrency platforms (CilkPlus [11, 18], CUDA [16, 17] and OpenCL [22]) offer both forms of parallelism, with language constructs specific to each case. Meanwhile, classical models of parallel computations, like the fork-join concurrency model or the PRAM model [21, 5], do not distinguish between task-based and data-based parallelism, which is too simplistic for analyzing algorithms targeting the above concurrency platforms. In addition, the PRAM model fails to retain important features of actual computers related to memory traffic, such as cache complexity [4].

An attempt to integrate memory contention into the PRAM model has been made with the QRQW (Queue Read Queue Write) PRAM, defined in [6] by Gibbons, Matias and Ramachandran. The authors also enhance the Graham-Brent theorem. However, they confine in a single quantity time spent in arithmetic operations and time spent in read/write accesses. We believe that
this unification is not appropriate for recent many-core processors, such as GPUs, for which the ratio between one global memory read/write access and one floating point operation can be in the 100’s.

In a recent paper, Ma, Agrawal and Chamberlain [13] introduce the TMM (Threaded Many-core Memory) model which retains many important characteristics of GPU-type architectures, including several machine parameters such as throughput and coalesced granularity. Moreover, TMM analysis can rank algorithms from slow to fast, given those machine parameters, while their running time estimate on P cores is not based on the Graham-Brent theorem.

Many works, such as [14, 12], targeting code optimization and performance prediction of GPU programs are related to our work. However, these papers do not define an abstract model in support of the analysis of algorithms.

In this paper, we propose a many-core machine model (MMM) which aims at minimizing parallelism overheads of algorithms targeting implementation on GPUs. In the design of this model, we insist on the following features:

- **Two-level DAG programs.** Defined in Section 2 this aspect captures the two levels of parallelism (fork-join and SIMD) of heterogeneous programs (like a CilkPlus program using #pragma simd [15] or a CUDA program with the so-called dynamic parallelism [17]).

- **Parallelism overhead.** We introduce this complexity measure in Section 2.3 with the objective of analyzing communication and synchronization costs.

- **A Graham-Brent theorem.** We combine three complexity measures (work, span and parallelism overhead) and two machine parameters (size of local memory and data transfer throughput) in order to estimate the running time of an MMM program on P streaming multiprocessors. This result is Theorem 1 in Section 2.4.

Our proposed model extends both the fork-join concurrency model and PRAM-based models, with an emphasis on parallelism overheads resulting from communication and synchronization costs.

We sketch below how, in practice, we use this model in order to minimize parallelism overheads of programs targeting GPUs. Consider an MMM program P, that is, an algorithm expressed in the MMM model. Assume that a program parameter s (like the number of threads per thread-block or the amount of data transfer per thread-block) can be arbitrarily chosen within some range S while preserving the specifications of P. Let s0 be a particular value of s which corresponds to an instance P0 of P that, in practice, can be seen as a naive (or simply initial) version of the algorithm.

Assume that, when s varies within S, the work, say W_P(s), does not vary much, that is, W_P(s)/W_P(s0) ∈ Θ(1) hold. Assume also that the parallelism overhead O_P(s) varies more substantially, say O_P(s0)/O_P(s) ∈ Θ(s - s0). Then, we determine a value s_min ∈ S maximizing the ratio O_P(s0)/O_P(s). Next, we use our version of Graham-Brent theorem (more precisely, we use Corollary 1 to check that the upper bound for the running time of P(s_min) is less than that of P(s0). If this holds, we view P(s_min) as a solution of our problem of algorithm optimization (in terms of parallelism overheads).

To demonstrate and evaluate the benefits of our model, and the above optimization strategy, we applied them successfully to four fundamental algorithms in scientific computing, see Sections 3 to 6. These four applications are the univariate polynomial division and multiplication, radix sort and the Euclidean algorithm. Each of them satisfies the hypotheses of the above optimization strategy. Our theoretical analysis, for three of these applications, has led to an optimized implementation reported in [9] and publicly available, while, for the other application, this analysis has explained a posteriori the experimental observations of [19].

2 A many-core machine model

The model of parallel computations presented in this paper aims at capturing communication and synchronization overheads of programs written for modern many-core architectures. One of our objectives is to optimize algorithms by techniques like reducing redundant memory accesses. The reason for this optimization is the fact that, on actual GPUs, global memory latency is approximately 400 to 800 clock cycles, while local memory latency is only a few clock cycles. This memory latency difference, when not properly taken into account, may have a dramatically negative impact on program performance. As mentioned in the introduction, this hardware feature of GPUs cannot be captured by

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1. Our algorithms are implemented in CUDA and publicly available with benchmarking scripts from [http://www.cumodp.org](http://www.cumodp.org).
the well-studied PRAM model. Indeed, any memory access, as well as any integer arithmetic operation, is performed in unit time on a PRAM machine.

This latter, as well as other limitations, have motivated variants of the PRAM model, including our work. Another motivation, mentioned above, is the fact that popular concurrency platforms offer task-based and data-based parallelisms, with language constructs specific to each case.

As specified in Sections 2.1 and 2.2 our many-core machine model (MMM) retains many of the characteristics of modern GPU architectures programming models like CUDA or OpenCL. However, in order to support algorithm analysis with an emphasis on parallelism overheads, as defined in Section 2.3 and 2.4, MMM abstract machines admit a few simplifications and limitations with respect to actual many-core devices.

2.1 Characteristics of the abstract many-core machines

![Figure 1: Overview of a many-core machine program](image)

**Architecture.** An MMM abstract machine possesses an unbounded number of streaming multiprocessors (SMs) which are all identical. Each SM has a finite number of processing cores and a fixed-size local memory. An MMM machine has a two-level memory hierarchy, comprising an unbounded global memory with high latency and low throughput while SMs local memories have low latency and high throughput.

**Programs.** An MMM program is a directed acyclic graph (DAG) whose vertices are kernels (defined hereafter) and edges indicate serial dependencies, similarly to the instruction stream DAGs of the fork-join multithreaded concurrency model. A kernel is an SIMD (single instruction, multiple data) program capable of branches and decomposed into a number of thread-blocks. Each thread-block is executed by a single SM and each SM executes a single thread-block at a time. Similarly to a CUDA program, an MMM program specifies for each kernel the number of thread-blocks and the number of threads per thread-block, following the same extended function-call syntax. Figure 1 depicts the different types of components of an MMM program.

**Scheduling and synchronization.** At run time, an MMM machine schedules thread-blocks (from the same or different kernels) onto SMs, based on the dependencies specified by the edges of the DAG and the hardware resources required by each thread-block. Threads within a thread-block can cooperate with each other via the local memory of the SM running the thread-block. Meanwhile, thread-blocks interact with each other via the global memory. In addition, threads within a thread-block are executed physically in parallel by an SM. Moreover, the programmer cannot make any assumptions on the order in which thread-blocks of a given kernel are mapped to the SMs. Hence, MMM programs run correctly on any fixed number of SMs.

**Memory access policy.** All threads of a given thread-block can access simultaneously any memory cell of the local memory or the global memory: read/write conflicts are handled by the CREW (concurrent read, exclusive write) policy. However, read/write requests to the global memory by two different thread-blocks cannot be executed simultaneously. In case of simultaneous requests, one thread-block is chosen randomly and served first, then the other is served.

For the purpose of analyzing program performance, we define two *machine parameters*:

- **$U$**: Time (expressed in clock cycles) to transfer one machine word between the global memory and the local memory of any SM.
- **$Z$**: Size (expressed in machine words) of the local memory of any SM.

Thus, the quantity $1/U$ is a throughput measure and has the following property. If $\alpha$ and $\beta$ are the numbers of words respectively read and written to the global memory by one thread of a thread-block $B$, then the total time $T_D$ spent in data transfer between the global memory and the local memory of an SM executing $B$ satisfies

$$T_D \leq (\alpha + \beta)U.$$
We observe that, on actual machines, some hardware characteristics may reduce data transfer time (like coalesced accesses to global memory) or the contribution of the latter on the overall running time (like concurrent execution of thread-blocks on the same SM with fast context switching in order to hide data transfer latency). Other hardware characteristics (like partition camping) may increase data transfer time. However, this reduced or increased transfer time will remain in $O(\alpha + \beta)$. Therefore, the fact that MMM machines do not have these hardware characteristics will not lead us to incorrect asymptotic upper bounds when estimating the running time of MMM programs.

Similarly, the local memory size $Z$ unifies different characteristics of an SM and, thus, of a thread-block. Indeed, each of the following quantities is at most equal to $Z$: the number of cores of an SM, the number of threads of a thread-block, the number of words in a data transfer between the global memory and the local memory of an SM.

Relation (1) calls for another comment. One could expect the introduction of a third machine parameter, say $V$, which would be the time to execute one local operation (arithmetic operation, read/write in the local memory), such that, if $\sigma$ is the total number of local operations performed by one thread of a thread-block $B$, then the total time $T_A$ spent in local operations by an SM executing $B$ would satisfy $T_A \leq \sigma V$. Therefore, for the total running time $T$ of the thread-block $B$, we would have

$$T = T_A + T_D \leq \sigma V + (\alpha + \beta)U. \quad (2)$$

Instead of introducing this third machine parameter $V$, we let $V = 1$. In other words, $U$ is the ratio between the time to transfer a machine word and the time to execute a local operation. We assume $U > 1$.

Finally, Relation (2) requires another justification. Indeed, this estimate suggests that, at every clock cycle, every thread is either performing an arithmetic operation or accessing memory. For this to be true, conditional branches responsible for code divergence need to be eliminated by techniques like code replication and the corresponding cost will be captured by the complexity measures (work, span and parallelism overhead) of the MMM model. Since no synchronization occurs between thread blocks, we turn our attention to scheduling.

Scheduling costs. Since an MMM abstract machine has infinitely many SMs and since the kernel DAG defining an MMM program $P$ is assumed to be known when $P$ starts to execute, scheduling $P$’s kernels onto the SMs can be done in time $O(\Gamma)$ where $\Gamma$ is the total length of $P$’s kernel code. Thus, we shall neglect those costs in comparison to the costs of transferring data between SMs’ local memories and the global memory. We also note that assuming that, the kernel DAG is known when $P$ starts to execute, allows us to focus on parallelism overheads resulting from this data transfer. Extending MMM machines to support programs whose instruction stream DAGs unfold dynamically at run time and integrating the resulting scheduling costs as in [10] is left for future work.

Thread block DAG. Since each kernel of the program $P$ decomposes into a finite number of thread-blocks, we map $P$ to a second graph, called the thread block DAG of $P$, whose vertex set $B(P)$ consists of all thread-blocks...
of the kernels of $\mathcal{P}$ and such that $(B_1, B_2)$ is an edge if $B_1$ is a thread-block of a kernel preceding the kernel of the thread-block $B_2$ in $\mathcal{P}$. This second graph defines two important quantities:

$N(\mathcal{P})$: number of vertices in the thread-block DAG of $\mathcal{P}$,

$L(\mathcal{P})$: critical path length (where length of a path is the number of edges in that path) in the thread-block DAG of $\mathcal{P}$.

2.3 Complexity measures for the many-core machine model

Consider an MMM program $\mathcal{P}$ given by its kernel DAG $(K, E)$. Let $K \in \mathcal{K}$ be any kernel of $\mathcal{P}$ and $B$ be any thread-block of $K$. We define the work of $B$, denoted by $W(B)$, as the total number of local operations performed by all threads of $B$. We define the span of $B$, denoted by $S(B)$, as the maximum number of local operations performed by a thread of $B$. Let $\alpha$ and $\beta$ be the maximum numbers of words read and written (from the global memory) by a thread of $B$. Then, we define the overhead of $B$, denoted by $O(B)$, as $(\alpha + \beta)U$. Next, the work (resp. overhead) $W(K)$ (resp. $O(K)$) of the kernel $K$ is the sum of the works (resp. overheads) of its thread-blocks, while the span $S(K)$ of the kernel $K$ is the maximum of the spans of its thread-blocks.

We consider now the entire program $\mathcal{P}$. The work $W(\mathcal{P})$ of $\mathcal{P}$ is defined as the total work of all its kernels

$$W(\mathcal{P}) = \sum_{K \in \mathcal{K}} W(K).$$

Regarding the graph $(K, E)$ as a weighted-vertex graph where the weight of a vertex $K \in \mathcal{K}$ is its span $S(K)$, we define the weight $S(\gamma)$ of any path $\gamma$ from the first executing kernel to the last executing kernel as $S(\gamma) = \sum_{K \in \gamma} S(K)$. Then, we define the span $S(\mathcal{P})$ of the program $\mathcal{P}$ as

$$S(\mathcal{P}) = \max_{\gamma} S(\gamma).$$

Finally, we define the overhead $O(\mathcal{P})$ of the program $\mathcal{P}$ as the total overhead of all its kernels

$$O(\mathcal{P}) = \sum_{K \in \mathcal{K}} O(K).$$

Observe that, according to Mirsky’s theorem [15], the number $\pi$ of parallel steps in $\mathcal{P}$ (i.e. anti-chains in $(K, E)$) is equal to the maximum length of a path in $(K, E)$ from the first executing kernel to the last executing kernel.

2.4 A Graham-Brent theorem with overhead

Theorem 1 We have the following estimate for the running time $T_P$ of the program $\mathcal{P}$ when executed on $\mathcal{P}$ SMs:

$$T_P \leq (N(\mathcal{P})/P + L(\mathcal{P}))C(\mathcal{P})$$

where $C(\mathcal{P}) = \max_{B \in \mathcal{B}(\mathcal{P})} (S(B) + O(B))$.

The proof is similar to that of the original result. One observes that the total number of complete steps (for which $P$ thread-blocks can be scheduled by a greedy scheduler) is at most $N(\mathcal{P})/P$ while the number of incomplete steps is at most $L(\mathcal{P})$. Finally, $C(\mathcal{P})$ is an obvious upper bound for the running time of every step, complete or incomplete.

The proof of the following corollary follows from Theorem 1 and from the fact that costs of scheduling thread-blocks onto SMs are neglected.

Corollary 1 Let $K$ be the maximum number of thread blocks along an anti-chain of the thread-block DAG of $\mathcal{P}$. Then the running time $T_P$ of the program $\mathcal{P}$ satisfies:

$$T_P \leq (N(\mathcal{P})/K + L(\mathcal{P}))C(\mathcal{P})$$

Corollary 1 allows us to estimate the running time of an MMM program as a function of the machine parameters $Z$, $U$ and the thread-block DAG of $\mathcal{P}$. Thus this estimate does not depend on the number of SMs in use to execute $\mathcal{P}$.

3 Polynomial division

Our first application of the MMM deals with univariate polynomial division. One division step, like a Gaussian elimination step, performs a linear combination of two vectors. Hence, the ideas developed in this section would apply to linear algebra and are not specific to polynomial arithmetic.

Let $\mathbb{K}$ be a field and $a, b \in \mathbb{K}[X]$ be univariate polynomials with coefficients in $\mathbb{K}$, with $b \neq 0$. Assume that each arithmetic operation (addition, subtraction, multiplication and division) in $\mathbb{K}$ can be done with a single machine word operation on an MMM machine. Let
n and m be non-negative integers such that we have
\( \deg(a) = n - 1 \) and \( \deg(b) = m - 1 \). Thus, \( n \) and \( m \) are the number of terms (null or not) of \( a \) and \( b \), respectively. Let \( q \) and \( r \) be the quotient and the remainder in the Euclidean division of \( a \) by \( b \). Thus, \( (q, r) \) is a unique couple of univariate polynomials over \( \mathbb{K} \) such that \( a = q \cdot b + r \) and \( \deg(r) < \deg(b) \) both hold.

In Section 3.1 we present a multithreaded algorithm computing \( (q, r) \) on an MMM machine. We call this algorithm naive since it implements the natural idea that, at each division step, each thread computes one coefficient of the next intermediate remainder. In Section 3.2 we propose a second MMM algorithm with the goal of minimizing data transfer. We analyze both algorithms with the complexity measures \(*\) of Section 2.3. In Section 3.3, we compare their running time estimates given by Corollary 1.

3.1 Naive algorithm

In each kernel call, each thread computes one coefficient of an intermediate remainder polynomial by means of one multiplication and one subtraction in the coefficient field \( \mathbb{K} \). Algorithm 1 repeatedly calls the kernel stated in Algorithm 2. The latter performs one division step in parallel. Let \( \ell \) be the number of threads in a thread-block, we note that each kernel uses \( \lceil \frac{\ell}{7} \rceil \) thread-blocks. We observe that each thread of a kernel reads/writes 3 to 5 words\(^4\) in the global memory without storing them in the local memory.

![Figure 2: Naive division: illustration of a thread-block reading coefficients from \( a,b \) and writing to \( r \).](image)

We also notice that Algorithm 1 performs exactly \( n - m + 1 \) consecutive calls to Algorithm 2. Nevertheless, Algorithm 2 works correctly even if, after one division step, the degree of an intermediate remainder drops by more than one. This implementation choice is relevant to dense polynomials, which are our primary interest. In the sparse case, the degree of an intermediate remainder needs to be computed after each division step. Figure 2 shows a division step within a thread-block after running Algorithm 2 once.

**Algorithm 1**: NaivePlainDivisionGPU\( (a,b) \)

**Input**: \( a, b \in \mathbb{K}[X] \) with \( \deg(a) \geq \deg(b) \) that is, \( n - 1 \geq m - 1 \).

**Output**: \( q, r \in \mathbb{K}[X] \) s.t. \( a = q \cdot b + r \) and \( \deg(r) < m - 1 \).

1. Let \( \ell \) be the number of threads in a thread block;
2. Let \( q \) be array of size \( n - m + 1 \) with coefficients in \( \mathbb{K} \);
3. for \( (i = (n - 1) \ldots (m - 1)) \) do
4. \[ \text{NaiveDivKernel} \left( m/\ell, \ell \gg (a, b, q, i, m - 1) \right) \]
5. if \( a[0] == \cdots == a[m - 1] == 0 \) then
6. \[ \text{return} \ [q, 0] \]
7. Compute \( k \), the maximum \( i \) such that \( a[i] \neq 0 \) holds;
8. Let \( r \) be array of size \( k + 1 \) s.t. \( r[i] = a[i] \) for \( 0 \leq i \leq k \);
9. return \( [q, r] \).

**Algorithm 2**: NaiveDivKernel\( (a, b, q, i, d_b) \)

**Input**: \( a, b, q \in \mathbb{K}[X] \), \( d_b = \deg(b) \), \( i \in \mathbb{N} \), \( d_b \leq i \).

1. Let \( \text{blockID, blockDim, threadID} \) be the block id, number of threads per block, thread id respectively;
2. \( j = \text{blockID} \cdot \text{blockDim} + \text{threadID} \);
3. if \( j \leq d_b \) then
4. if \( j == 0 \) then
5. \[ */ \text{writing to global memory} \ /*\]
6. \( q[i - d_b] = (b[d_b])^{-1} \cdot a[i] \);
7. \[ */ \text{updating a in global memory} \ /*\]
8. \( a[j + i - d_b] := b[j] \cdot (b[d_b])^{-1} \cdot a[i] \);

We denote by \( W_1, S_1 \) and \( O_1 \), the work, span and overhead of Algorithm 1 respectively. Since each thread-block performs \( 2 \ell + 1 \) arithmetic operations and each thread makes at most 5 accesses to the global memory, we obtain \( W_1 = (n - m + 1) m (2 \ell + 1) \), \( S_1 = 3 (n - m + 1) \) and \( O_1 = \frac{5 (n - m)}{\ell} m U \). To apply Corollary 1 we shall compute the quantities \( N(P), L(P) \) and \( C(P) \) defined in Section 2. We denote them here by \( N_1, L_1 \) and \( C_1 \), respectively. One can easily check that we have \( N_1 = \frac{(n - m + 1) m}{\ell} \), \( L_1 = n - m + 1 \) and \( C_1 = 3 + 5 U \).
3.2 Optimized algorithm

In each kernel, each thread updates a number of coefficients (instead of just one) of an intermediate remainder polynomial repeatedly during a number of division steps, thus without synchronizing data with other thread-blocks. The motivation of this new scheme is to minimize the amount of data transferred between global and local memories. Similarly to the scheme in Section 3.1, Algorithm 3 repeatedly calls Algorithm 4. Figure 3 shows $s$ division steps within a thread-block after running Algorithm 2 once. More specifically, given an integer $s \geq 1$, Algorithm 4 performs sufficiently many division steps (at most $s$) such that the output polynomial $r$ is either zero or its degree is less than that of $a$ at least by $s$. To this end, each thread-block

- uses $3s$ threads,
- loads the coefficients of $X^d$, $X^{d-1}$, ..., $X^{d-s+1}$ from $a$ (resp. $b$), that we call the $s$-head of $a$ (resp. $b$), where $d$ is the degree of $a$ (resp. $b$), see Lines 3-4,
- loads $2s$ (resp. $3s$) consecutive coefficients of $a$ (resp. $b$), say $X^{d_1}, X^{d_1-1}, ..., X^{d_1-2s+1}$ ($X^{d_2}, X^{d_2-1}, ..., X^{d_2-3s+1}$) for some integer $d_1 > 0$ (resp. $d_2 > 0$) which depends on the thread and thread-block IDs.

![Figure 3: Optimized division: illustration of a thread-block reading coefficients from $a,b$ and writing to $r$.

Since each thread makes at most 9 accesses to the global memory, we obtain $W_s = \frac{(n-m+1) m (9s+1)}{2s^2}$, $S_s = 3(n-m+1)$ and $O_s = \frac{9(n-m+1) m U}{2s^2}$. To apply Corollary 4, we shall compute the quantities $N_\ell(P)$, $L(P)$ and $C(P)$ defined in Section 2. We denote them here by $N_s$, $L_s$ and $C_s$, respectively.

![Algorithm 3: OptimizePlainDivisionGPU($a, b, s$)]

\begin{verbatim}
Input: $a, b \in \mathbb{K}[X]$ with deg($a$) $\geq$ deg($b$) that is, $n-1 \geq m-1$ and $s \in \mathbb{N}$.
Output: $q,r \in \mathbb{K}[X]$ s. t. $a = q \cdot b + r$ and deg($r$) $< m-1$.

1 Let $\ell = 3s$ be the number of threads in a thread-block;
2 Let $q$ be array of size $n-m+1$ with coefficients in $\mathbb{K}$;
3 for ($i = n-1; i \geq m-1; i = i - s$) do
4    \textbf{if} $a[0] = \cdots = a[m-1] = 0$ \textbf{then}
5        \textbf{return} $[q, 0]$;
6    Compute $k$, the maximum $i$ such that $a[i] \neq 0$ holds;
7    Let $r$ be array of size $k+1$. s.t. $r[i] = a[i]$ for $0 \leq i \leq k$;
9    \textbf{return} $[q, r]$;
\end{verbatim}

3.3 Comparison of running time estimates

Before following the algorithm optimization strategy stated in the introduction, we replace $\ell$ and $s$ by $Z/2$ and $Z/7$, respectively, since $2\ell$ or $7s$ coefficients must fit into the local memory, that is, $2\ell \leq Z$ and $7s \leq Z$. Now, we observe that the work ratio $W_1/W_s$ is asymptotically constant:

$$\frac{W_1}{W_s} = \frac{8(Z+1)}{9Z+7},$$  \hspace{1cm} (5)

and $S_1/S_s = 1$. Then, we compute the overhead ratio:

$$\frac{O_1}{O_s} = \frac{20}{441}Z.$$  \hspace{1cm} (6)

We observe that this substantial improvement in data transfer overhead is done at a fairly low expense in terms of work overhead. Next, applying Corollary 1, the
Algorithm 4: OptDivKer\((a, b, q, i, d_b, s)\)

**Input:** \(a, b, q \in \mathbb{K}[X], i \in \mathbb{N}, d_b = \deg(b)\) and \(s \in \mathbb{N}\).

1. Let \(sA, sB, sA, sB\) be local arrays of size \(s, 2s, 3s\) respectively each with coefficients in \(\mathbb{K}\).
2. \(j = \text{blockID} \cdot \text{blockDim} + \text{threadID}; t = \text{threadID};\)
3. /* Reading from global memory */
4. if \(t < s\) then
   5. \(sA[t] = a[i - t]; sBc[t] = b[d_b - t];\)
   6. \(sB[t] = b[d_b - 2s \cdot \text{blockID} - t];\)
5. if \(t \geq s\) then
   6. \(sA[t - s] = a[i - s - 2s \cdot \text{blockID} - t];\)
   7. \(sB[t] = b[d_b - 2s \cdot \text{blockID} - t];\)
7. for \((k = 0; (k < s) \land ((i + k \geq d) \land k = k + 1)\) do
   8. while \((k < s) \land (sAc[k] == 0)\) do
      9. \(k = k + 1;\)
   10. if \(k \geq s\) then
      11. break;
   12. if \(j == 0\) then
      13. /* Writing \(q\) to global memory */
      14. \(q[i - d_b - k] = sAc[k] \cdot b[d_b]^{-1};\)
   15. if \(k \leq t < s\) then
      16. \(sAc[t] = sBc[t - k] \cdot sAc[k] \cdot b[d_b]^{-1};\)
   17. if \(t \geq s\) then
      18. \(sA[t - s] = sB[t - k] \cdot sAc[k] \cdot b[d_b]^{-1};\)
   19. if \(t \geq s\) then
      20. /* Writing back \(a\) to global memory */
      21. \(a[i - s - 2s \cdot \text{blockID} - t] = sA[t - s];\)

This running time estimate of the na"ive and optimized algorithms are bounded over, respectively by \(T_1 = (N_1/K_1 + L_1) \cdot C_1\) with \(K_1 = \frac{n}{7}\) and \(T_s = (N_s/K_s + L_s) \cdot C_s\) with \(K_s = \frac{n}{2^7}\). We compute the ratio \(R = T_1/T_s\), that is,

\[
R = \frac{(3 + 5U) Z}{3(Z + 21U)}.
\]

We observe that \(R\) is larger than 1 if and only if \(Z > 12.6\) holds. The above condition clearly holds on actual GPU architectures. Thus the optimized algorithm (that is for \(s > 1\)) is overall better than the na"ive one (that is for \(s = 1\)). This is verified in practice in [10], where \(s\) is set to 512.

## 4 Radix sort

In [10], the authors present a CUDA implementation of the radix sort algorithm. Assuming that all entries are non-negative integers of bit-size \(c\), this CUDA implementation sorts \(n\) entries by performing \(\frac{c}{2}\) passes where \(s\) is a program parameter. In each pass, each thread-block first loads and sorts its tile using \(s\) iterations of 1-bit split, and write back its \(2^s\)-entry digit histogram and sorted data. Then, it performs a prefix sum over the histogram stored in a column-major order. Finally, each thread-block copies its elements to the correct output position.

Let \(\ell\) be the number of threads per thread-block. Following [10], we assume that each thread deals with \(4\) elements. Then, for each thread-block, \(4\ell\) original elements, \(4\ell\) sorted elements and a \(2^s\)-entry digit histogram must fit into the local memory, hence \(8\ell + 2^s \leq Z\). Thus, the maximum overhead per thread-block is \(9U\) (loading \(4\) elements, writing back \(4\) sorted elements and 1 value of the histogram).

We compute the work, span and overhead, respectively as \(W_s = c \left(\frac{22 + 72 \ell + 12}{4 \ell^2} + \frac{2^s + 20 \ell^2}{16 s \ell^2} + 1\right) n + \frac{c(16 + 192 \ell)}{16 s \ell^2}, S_s = c \left(8 \log_2 \ell + \frac{16}{s \log_2 \ell} + 41 + \frac{54}{\ell}\right), \quad O_s = cU \left(\frac{2}{72 \ell n + 172 \ell^2 n - 1}\right)\).

We view the case \(s = 1\) as a na"ive radix sort algorithm, with work, span and overhead given by \(W_1, S_1, O_1\), respectively. Letting \(n\) escaping to infinity, the work ratio \(W_1/W_s\) is asymptotically equivalent to:

\[
\frac{W_1}{W_s} \sim \frac{104 s \ell^2 + 92 s \ell + 2 s}{88 s \ell^2 + 16 \ell^2 + 20 2^s \ell + 4 s \ell + 48 \ell + 2^s}. \quad (8)
\]

Similarly, the span ratio \(S_1/S_s = \frac{s (24 \log_2 s + 95)}{8 s \ell + 10 (2^s + 41 s + 54)}\) is asymptotically constant, meanwhile the overhead ratio is:

\[
\frac{O_1}{O_s} \sim \frac{s (72 \ell + 34)}{72 \ell + 172 \ell^2}. \quad (9)
\]

We notice that if \(2^s = \Theta(\ell)\) holds, we can reduce the overhead by a factor of \(s\) while increasing the work by a constant factor only. Meanwhile, with \(2^s = \Theta(\ell^2)\), we increase both the work and the overhead by a non-constant factor. In this latter scenario, we could not optimize the na"ive algorithm in any sense.

To apply Corollary [10] we compute the three quantities \(N_s = c \left(\frac{1}{17} + \frac{2^s}{2^s}\right) n, L_s = \frac{5 c}{7}\) and \(C_s = s (41 + 8 \log_2 \ell) + 12 + 9U\). Then, the ratio \(R\) of the running time estimate between the naive algorithm and that for an arbitrary \(s\) is:

\[
R = \frac{(14 \ell + 2) (53 + 8 \log_2 \ell + 9U) s}{(14 \ell + 2^s) (41 s + 8 s \log_2 \ell + 12 + 9U)}.
\]

\(^5\)See the detailed analysis in the form of executable MAPLE worksheet: http://www.csd.uwo.ca/~nxie6/projects/mmm/sorting_overall.mw
We then replace $s$ by $\log_2 \ell$, since we would like to determine whether the overall running time is better or worse in this case. The quotient of the leading terms in $R$ becomes

$$\frac{7 \ell \log_2 \ell (8 \log_2 \ell + 9 U)}{60 \ell \log^2 \ell}.$$ (10)

This ratio is larger than 1 for $\ell < 2^{15.75 U}$, which is realistic. Therefore, letting $2^s = \Theta(\ell)$, the data transfer overhead is reduced by a factor of $s$ and leads to an optimized algorithm. This is consistent with the empirical results of [10].

5 Polynomial multiplication

Let $a$ and $b$ be polynomials as in Section 3 and $f = a \times b$ be their product. Our multiplication algorithm is based on the well-known long multiplication and consists of two phases. During the multiplication phase, every coefficient of $a$ is multiplied with every coefficient of $b$; the resulting products are accumulated in an intermediate array, denoted by $M$. Then, during the addition phase, these accumulated products are added together to form the polynomial $f$.

For this application, the program parameter (as defined in the introduction) is an integer $s > 0$, representing for each thread-block, the number of coefficients of $b$ to be multiplied by a number of coefficients of $a$ in the coefficients multiplication phase, as well as the number of sums per thread in the addition phase. Algorithm 5 is the top level algorithm: it performs the multiplication phase via Algorithm 6 and the addition phase by repeated calls to Algorithm 7.

We denote by $\ell$ the number of threads per thread-block. In multiplication phase, each thread-block reads $s \ell + s - 1$ coefficients of $a$, $s$ coefficients of $b$, computes $s \ell s^2$ products, followed by $\ell s (s - 1)$ of additions. Thus, each thread-block contributes $s \ell$ partial sums to the two-dimensional array $M$, whose format is $x \cdot y$, where $x = \frac{m}{s}$ and $y = n + s - 1$. This multiplication phase, illustrated by Figure 4 loads $s \ell + s - 1$ coefficients of $a$ to guarantee the correctness of the results in $M$.

In the addition phase, the $x$ rows of the auxiliary array $M$ are added pairwise in $\log_2 x$ parallel steps. After each step, the number of rows in $M$ is reduced by half, until we obtain only one row that is, $f = a \times b$. To be more specific, when adding rows $i$ and $j$ (for $i < j$) at a given parallel step, shown in Figure 5 each thread-block loads $s \ell$ elements of $M[i]$ and $M[j]$, respectively, and then adds $M[j]$ to $M[i]$.

![Figure 4: Multiplication phase: illustration of a thread-block reading coefficients from $a, b$ and writing to the auxiliary array $M$.](image)

![Figure 5: Addition phase: illustration of a thread-block reading and writing to the auxiliary array $M$.](image)

**Algorithm 5: PlainMultiplicationGPU(a, b, f, s)**

**Input:** $a, b \in \mathbb{K}[X]$ with $n - 1 := \deg(a)$ and $m - 1 := \deg(b)$ and an integer $s \geq 1$.

**Output:** $f \in \mathbb{K}[X]$ and $f = a \times b$.  
1. $y = n + s - 1$; $x = m/s$;
2. Let $M$ be an array of size $x \cdot y$ with coefficients in $\mathbb{K}$;
3. $\ell$ is the number of threads per block;
4. MulKer $\ll x \cdot y/(s \cdot \ell), \ell \gg (a, b, M, n, m, s)$;
5. for $(i = 0; i \leq \log_2 s; i = i + 1)$ do
6. AddKer $\ll x \cdot y/(2^{i+1} s \cdot \ell), \ell \gg (M, f, y, x, s, i)$;
7. return $f$;

Considering any thread-block of the multiplication phase, we notice that $s$ coefficients of $b$ and $s \ell + s - 1$ coefficients of $a$ are loaded and $s \ell$ results are written back to global memory. Hence $2 s \ell + 2 s - 1$ coefficients must
Algorithm 6: MulKer\(\langle a, b, M, n, m, s \rangle\)

**Input:** \(a, b, M \in \mathbb{K}[X]\) and an integer \(s \geq 1\).

1. \(\ell = \) blockDim; \(t = \) threadIdx;
2. Let \(B'\) and \(A'\) be two local arrays in \(\mathbb{K}\) of size \(s\) and \(\ell \cdot s + s - 1\) respectively;

   ```
   /* copying from local */
   ```

3. \(i = s \cdot \lceil s \cdot j/(n + s - 1) \rceil + t;\)
4. if \(i > m \land t < s\) then

   ```
   B'[t] = b[i];
   ```

5. \(i = s \cdot \lceil j \mod \frac{n + s - 1}{s} \rceil;\)

6. for \(k = 0; k < s; k = k + 1\) do

   ```
   A'[k \cdot \ell + t] = a[i + k \cdot \ell + t];
   ```

7. if \(i - s + t > 0 \land t < s - 1\) then

8. if \(i - s + t \leq 0\) then

9. ```
   M[s \cdot j + e] = h;
   ```

10. ```
   /* writing to global */
   ```

We fit into local memory, that is, we have \(2s \ell + 2s - 1 \leq Z\). Next, we compute the work, span and parallelism overhead, respectively as \(W_s = (2m - \frac{1}{2})(n + s - 1)\), \(S_s = 2s^2 + s \log_2 \frac{m}{s} - s\) and \(O_s = \frac{(n + s - 1)(5m + 2m - 3s^2)}{s^2 \ell}\).

We also obtain the quantities characterizing the thread block DAG that are required in order to apply Corollary 1.

\[N_s = \frac{(n + s - 1)(5m + 2m - 3s^2)}{s^2 \ell}, \quad L_s = \log_2 \frac{m}{s} + 1, \quad C_s = 2s - 1 + 2U(s + 1).\]

We set \(s = 1\) in Algorithm 5 and view it as a “naive algorithm.” The work ratio \(W_1/W_s = \frac{n}{n + s - 1}\), is asymptotically constant as \(n\) escapes to infinity. The span ratio \(S_1/S_s = \frac{s \log_2 \frac{m}{s} + 2s - 1}{s \log_2 \frac{m}{s} + 2s - 1}\) shows that \(S_s\) grows asymptotically with \(s\). The parallelism overhead ratio, letting \(m = n:\)

\[
\frac{O_1}{O_s} = \frac{n s^2 (7n - 3)}{(n + s - 1)(5n s + 2n - 3s^2)}. \tag{11}
\]

We observe that, as \(n\) escape to infinity, this latter ratio is asymptotically equivalent to \(s\). Applying Corollary 1, let \(R\) be the ratio of the running time estimate between the naive algorithm and that for an arbitrary \(s\). We obtain

\[
R = \frac{(n \log_2 n + 3n - 1)(1 + 4U)}{(n \log_2 \frac{m}{s} + 3n - s)(2U s + 2U + 2s^2 - s)} \tag{12}
\]

which is essentially \(\frac{2 \log_2 n}{s \log_2 (n/s)}\). This latter ratio is smaller than 1, such that the “initial” algorithm (that is for \(s = 1\)) performs better. This also indicates that increasing \(s\) makes the algorithm performance worse. In practice shown in Table 1, setting \(s = 4\) performs best, while with larger \(s\), the running time becomes slower, which is coherent with our theoretical analysis.

6 The Euclidean algorithm for polynomials

Let \(a\) and \(b\) be polynomials as defined in Section 3. In Section 6.1, we present a simple multithreaded algorithm that computes \(\text{GCD}(a, b)\) on an \(\text{MMM}\) machine. We call it naive (like Algorithm 1) as this algorithm also performs one division step within one kernel. In Section 6.2, we describe another algorithm on an \(\text{MMM}\) machine that reduces the overhead of data transfer by performing several division steps within one kernel. Finally, in Section 6.3, we compare those two algorithms by means of Corollary 1. A detailed analysis in the form of executable MAPLE worksheet is available at [1](http://www.csd.uwo.ca/~nxie6/projects/mmm/euclidean_overall.mw).
6.1 Naive algorithm

Algorithm 8 computes GCD(a, b). Similarly to the naive division of Algorithm 1, it calls a kernel (stated as Algorithm 2) that completes one division step. The former algorithm calls the latter one at most \( n + m - 2 \) times. Algorithm 6 is the same as Algorithm 2 except that it checks the current degrees of both \( a \) and \( b \) so as to decide which one takes the role of the divisor, and then it completes a division step. To do so, we use an array \( st \) of length 2 to store the degrees of \( a \) and \( b \) during each division step. The fact that the degree of an intermediate remainder may be dropped by more than 1 is taken into account, so that Algorithm 9 works correctly even if the GCD is computed before \( n + m - 2 \) kernel calls. After \( n + m - 2 \) division steps, either \( a \) or \( b \) becomes zero or constant. Algorithm 8 returns the other polynomial as GCD. Figure 6 shows one Euclidean division step within a thread-block after running Algorithm 9 once.

![Figure 6: Naive Euclidean: illustration of a thread-block reading coefficients from \( a,b \) and writing to \( g \).](image)

We denote by \( \ell \) the number of threads per thread-block. We compute the work, span and overhead, respectively as \( W_1 = \frac{m}{2}(\ell + \ell + \ell - 1) \), \( S_1 = 3(m + n - 2) \) and \( O_1 = \frac{5mU(n+\ell+1)}{\ell} \). To apply Corollary 1, one can easily check that those three quantities are \( N_1 = \frac{m(n+\ell+1)}{\ell} \), \( L_1 = m + n - 2 \) and \( C_1 = 3 + 5U \).

6.2 Optimized algorithm

In each kernel, thread-blocks collectively perform at most \( s \) division steps, instead of one, and update \( s \) coefficients from both \( a \) and \( b \). After a division step, the degree of the dividend polynomial is decreased by at least one, and then in the next division step, coefficients from the divisor polynomial are adjusted by one or more shift operations. Thus, we need \( 2s \) coefficients from both \( a \) and \( b \) to be sure that after \( s \) division steps we correctly have \( s \) coefficients of both \( a \) and \( b \). Since the consecutive thread-blocks have \( s \) common coefficients of both \( a \) and \( b \), the number of thread-blocks is \( \min(\frac{\deg(a)+1}{s}, \frac{\deg(b)+1}{s}) \). A thread-block also needs \( s \)-head coefficients of both \( a \) and \( b \) to run \( s \) division steps. Thus, each thread-block uses \( 3s \) threads (like Algorithm 1). Algorithm 10 is our top level optimized algorithm for computing GCD(a, b). Figure 7 shows \( s \) Euclidean division steps within a thread-block after running the kernel Algorithm 11 once.

![Figure 7: Optimized Euclidean: illustration of a thread-block reading coefficients from \( a,b \) and writing to \( g^a,g^b \).](image)


\textbf{Algorithm 9:} NaivePlainGcdKernel\(a, b, \text{st}\)

\textbf{Input:} \(a, b \in \mathbb{K}[X]\) and \(\text{st}\) stores the current degree of \(a\) and \(b\).
\begin{algorithmic}[1]
  \State \(j = \text{blockID-blockDim + threadID};\)
  \If {\(\text{st}[0] \geq \text{st}[1] > 0 \land j < \text{st}[1]\)}
  \State \(k = j + \text{st}[0] - \text{st}[1];\)
  \State \(a[k] = a[k] - b[j] \cdot a[\text{st}[0]] \cdot b[\text{st}[1]]^{-1};\)
  \EndIf
  \While {\((\text{st}[0] \geq 0) \land (a[\text{st}[0]] = 0)\)}
  \State \(\text{st}[0] = \text{st}[0] - 1;\)
  \EndWhile
  \EndIf
  \ElseIf {\(0 < \text{st}[0] < \text{st}[1] \land j < \text{st}[0]\)}
  \State \(k = j + \text{st}[1] - \text{st}[0];\)
  \State \(b[k] = b[k] - a[j] \cdot a[\text{st}[1]] \cdot a[\text{st}[0]]^{-1};\)
  \EndIf
  \While {\((\text{st}[1] \geq 0) \land (b[\text{st}[1]] = 0)\)}
  \State \(\text{st}[1] = \text{st}[1] - 1;\)
  \EndWhile
\end{algorithmic}

three quantities are \(N_s = \frac{mn}{2} + \frac{m}{2}, L_s = \frac{n}{2} + \frac{m}{2}\) and \(C_s = 3s + 8U\).

\textbf{Algorithm 10:} OptimizedPlainGcdGPU\(a, b, s\)

\textbf{Input:} \(a, b \in \mathbb{K}[X]\) with \(\text{deg}(a) \geq \text{deg}(b)\) that is, \(n - 1 \geq m - 1\) and an integer \(s > 1\).
\textbf{Output:} \(g \in \mathbb{K}[X], \text{ s.t. } g = \text{GCD}(a, b)\).
\begin{algorithmic}[1]
  \State \(\ell = 3s\) be the number of threads in a thread block;
  \For {\(i = 0; i < n + m - 2; i = i + s\)}
  \State \(\text{OptGcdKernel}[\llfloor \frac{m}{s}\rrfloor, \ell] \\ll (a, b, s, \text{st});\)
  \EndFor
  \If {\(a\) is a zero or constant polynomial}
  \State Compute \(k_0\) the maximum \(i\) s.t. \(b[i] \neq 0\) holds;
  \State Compute \(k_0\) the maximum \(i\) s.t. \(a[i] \neq 0\) holds;
  \State Compute \(k_a\) the maximum \(i\) s.t. \(a[i] \neq 0\) holds;
  \EndIf
  \State Let \(g\) be array of size \(k_b + 1\) with coefficients in \(\mathbb{K}\) s.t. \(g[i] = b[i]\) for \(0 \leq i \leq k_b;\)
  \State Let \(g\) be array of size \(k_a + 1\) with coefficients in \(\mathbb{K}\) s.t. \(g[i] = a[i]\) for \(0 \leq i \leq k_a;\)
\end{algorithmic}

\begin{equation}
\frac{O_1}{O_s} = \frac{5}{48} \frac{Z}{(2n + 2 + Z)} \frac{Z}{6n + Z}.
\end{equation}

We see that the parallelism overhead improvement is done at a fairly low expense in terms of work overhead. Applying Corollary \(1\) we denote the running time estimate ratio \(R\) of the naive algorithm over the optimized one, that is,

\begin{equation}
R = \frac{(6n - 2 + Z)(3 + 5U)}{(18n + Z)(Z + 16U)}.
\end{equation}

When \(n\) escapes to infinity, the ratio \(R\) is equivalent to

\begin{equation}
\frac{(3 + 5U)}{3(Z + 16U)}.
\end{equation}

We observe that this ratio is larger than 1 if and only if \(Z > 9.6\) holds. This condition clearly holds and the optimized algorithm is overall better. This is verified in practice \(9\), where \(s\) is set to 256, also shown in Table \(2\).

\section{Conclusion}

We have presented a model of multithreaded computation combining the fork-join and SIMD parallelisms, with an emphasis on estimating parallelism overheads, so as to reduce communication and synchronization costs in GPU programs.

Four applications illustrated the effectiveness of our model. In each case, we determined a range of values for a program parameter in order to optimize the corresponding algorithm in terms of parallelism overheads. Experimentation validated the model prediction.

Our order of magnitude estimates for the program parameter of radix sort \(19\) agrees with the empirical results of that paper.

For the Euclidean algorithm, our running time estimates match those obtained with the Systolic VLSI Array Model \(3\). Moreover, our CUDA code \(9\) implementing this optimized Euclidean algorithm runs in linear time w.r.t. to the input polynomials degree, up to degree 10,000.

For polynomial multiplication, our theoretical analysis implies that the program parameter \(s\) must be as small as possible. In practice, we could vary this parameter between 2 and 32 and we found that the optimal value was 4. Since certain hardware features are
not integrated into the model, we found that the model prediction was also useful in that case.

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Algorithm 11: OptGcdKer\((a, b, s)\)

Input: \(a, b \in \mathbb{K}[X]\), an integer \(s > 1\) and \(st[]\) stores the current degree of \(a\) and \(b\).

1. Let \(sA, sB, sA, sB\) be local arrays of size \(s, 2s, 2s\) respectively with coefficients in \(\mathbb{K}\);
2. local integers \(u = v = w = e = 0\);
3. \(j = \text{blockID} + \text{blockDim} + \text{threadID} = \text{threadID}\);

/* copying from global memory */

4. \(t < s\) then
5. \(sA[t] = a[st[0] - t];\)
6. \(sB[t] = b[st[1] - t];\)

7. \(t \geq s\) then
8. \(sA[t - s] = a[st[0] - s \text{ blockID} - t]\)
9. \(sB[t - s] = b[st[1] - s \text{ blockID} - t];\)

10. for \((k = 0; k < s; k = k + 1)\) do
11. if \((st[0] \geq st[1] \land st[1] \geq 0)\) then
12. if \((u + t < s) \land (v + t < s)\) then
13. \(sA[u + t] = sB[v + t] \cdot sA[u] \cdot sB[v]^{-1};\)
14. \(sA[u + t] = sA[w + t - s] \cdot sA[u] \cdot sB[v]^{-1};\)
15. \(sB[e + t - s] \cdot sA[u] \cdot sB[v]^{-1};\)
16. \(t = 0\) then
17. \(sA[u + 1] = w + 1;\)
18. \(st[0] = st[0] - 1;\)
19. if \((st[1] \geq st[0]) \land (st[0] \geq 0)\) then
20. if \((u + t < s) \land (v + t < s)\) then
21. \(sB[v + t] = sA[u + t] \cdot sB[v];\)
22. \(sB[v + t] = sA[u + t] \cdot sB[v]^{-1};\)
23. \(sB[e + t - s] = sA[w + t - s] \cdot sB[v] \cdot sA[u]^{-1};\)
24. \(t = 0\) then
25. \(sB[u] = 0\) do
26. \(sB[u] = 0\) do
27. \(v = v + 1;\)
28. \(e = e + 1;\)
29. \(st[1] = st[1] - 1;\)
30. Update \(st[]\) array with the new degree of \(a\) and \(b\);