Design of a power efficient self-adaptive LVDS driver

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Abstract: A self-adaptive technique is presented for a low voltage differential signaling (LVDS) driver. By combining a high speed voltage detection circuit and drive capability control loop, the proposed architecture can adapt to the changes of output load and operating frequency automatically. This makes the driver suitable for using in field programmable gate array (FPGA), where load and frequency variation is large. Compared to previously reported LVDS drivers with fixed drive capability, the proposed driver eliminates power wasting under small load and low frequency condition. A prototype chip has been fabricated in 130 nm CMOS technology. Test results show the proposed driver improves maximum bit rate to 2.2 Gb/s and reduces power consumption by 48% compared to previously reported works with fixed drive capability.

Keywords: self-adaptive, power efficient, LVDS

Classification: Integrated circuits

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1 Introduction

With the rapid growth in battery powered mobile systems, there exists increasing demand on low power transceivers. Low voltage differential signaling (LVDS) [1, 2] standard offers low power consumption and high speed transmission at the same time.

Fig. 1 shows three LVDS driver architectures discussed in previously reported works, the double current source (DCS) architecture is shown in Fig. 1(a). DCS has two current sources M4 and M5. Switch transistors M2 and M3 control the direction of current flows through the termination resistor, therefore generate “1” or “0” at the receiving end. DCS architecture has smaller load on the previous stage and larger headroom voltage. But in DCS, only the current of one branch can be delivered to the load, therefore half of the power consumption is wasted. Switchable current source (SCS) [3] architecture eliminates power wasting in DCS by only turning on the current source which provides load current through S1 and S2 in Fig. 1(b), but switch S1 and S2 will introduce extra jitter in SCS. Bridged switched...
current source (BSCS) [4, 5] architecture shown in Fig. 1(c) eliminates power wasting in DCS by using four switch transistors M2–M5. BSCS architecture has smaller jitter compared to SCS, the disadvantage of BSCS is small voltage headroom due to the cascode topology.

Ideally, for DCS, SCS and BSCS drivers which adopt current-mode structures [6, 7], differential voltage at the receiving end is constant as long as the current flows through the termination resistor is fixed. Actually, differential voltage changes significantly with the changes of chip packaging, electro-static discharge (ESD) structure [8], receiver circuit architecture and printed circuit board (PCB) trace parameters. Fig. 2 shows the output load of an LVDS driver with BSCS architecture in a practical application, only part of the constant current $I_B$ generated by current source M6 flows through the termination resistor, the rest of the current is used to charge and discharge the load capacitance which is composed of $C_L$, $C_P$, $C_C$, $C_T$ and $C_R$. Therefore, to maintain differential voltage constant, extra-current has to be provided by the driver to charge and discharge the load capacitance, Pre-emphasis technique [9, 10] can provide the extra-current at the beginning of each transition, but the current provided by pre-emphasis circuit is fixed, while load capacitance varies over a wide range. For example, Capacitor $C_R$ in Fig. 2 ranges from 2 pF [11] to 10 pF [12] in FPGA applications since FPGA is always used as glue logic to connect various chips together in a system. And in FPGA, there exists extra load capacitance represented by $C_S$ because IO module of FPGA integrates different types of drivers and receivers to support different IO standards [13]. Besides, the impedance of the capacitor varies with frequency, thus more current is required under high-speed condition. Therefore, to guarantee the minimum differential voltage required by the receiver. Drive current of the traditional LVDS driver is set to meet the maximum load capacitance and maximum operating frequency. Therefore the power is wasted when load capacitance is small and operating frequency is low.

In this paper, a self-adaptive LVDS driver is presented. By automatically adjusting drive current, the proposed driver can adapt to the changes of output load and operating frequency, therefore eliminates power wasting under small load and low frequency condition.
2 Circuit design

2.1 Architecture

The main idea of the proposed self-adaptive LVDS driver is to monitor the voltage of output signal and control the current source digitally, a simple way to realize this idea is by adopting A/D converter.

Fig. 3 shows the architecture of a 1-bit Flash A/D converter. For an LVDS driver with maximum bit rate up to 2.2 Gb/s, period of the output differential signal is less than 910 ps. The self-adaptive loop needs to detect whether the high voltage of output differential signal exceeds the reference voltage. But the duration when output signal exceeds reference voltage can be very short. For A/D converter, to detect signal changes in such small duration requires high sampling rate. For example, in order to detect the high voltage of output signal within the duration equals to 1/8 of the output period, at least 8.8 GS/s sampling rate is required. This requires a frequency multiplier block in the design, and such high frequency operations results in extra power consumption. In this paper, a new method is proposed. Instead of converting the voltage of output signal continuously, only the point when output voltage exceeds \( V_{ref} \) is detected, which triggers subsequent operations to control drive capability. Fig. 4 shows the detailed architecture of the proposed self-adaptive LVDS driver. Signal \( V_{inp} \) and \( V_{inn} \) are a pair of differential signals generated from \( V_{in} \), which drive switch transistors M2 to M5. The frequency divider (FD) unit generates a divide-by-sixteen signal \( FDIV \) from \( V_{in} \). \( FDIV \) drives the clock port of a 6-bit adder and the reset port of a D Flip-Flop (DFF). Here the
6-bit adder actually performs increment by one or decrement by one depends on the ‘Add/Sub’ signal in each FDIV cycle. The delay module in Fig. 4 is used to maintain enough hold time for the 6-bit adder.

The size of current sources CS0 to CS5 is arranged in a binary form, therefore the current of CS1 is twice that of CS0, and the current of CS5 is 32 times that of CS0. By this way, the adjustment range and precision can be guaranteed at the same time through only six current sources.

Fig. 5 shows timing relationship of signals $V_{in}$, FDIV, VC, DFF and CTRL[5:0] in self-adaptive control logic. When FDIV is high, signal DFF.Q is reset to ‘0’. When FDIV is low, and a positive edge is detected on clock port of the DFF, DFF.Q is set to ‘1’. The high speed comparator compares the voltage of output signal $V_{outp}$ and reference signal $V_{ref}$, if $V_{outp}$ exceeds $V_{ref}$, the comparator will generate a high level signal, therefore DFF will detect a positive edge on clock port, and signal DFF.Q will be ‘1’, at the rising edge of FDIV, the 6-bit adder performs decrement by one operation, and DFF.Q is reset to ‘0’ as shown in Fig. 5(a). This reduces drive current by $I_B$.

On the contrary, if $V_{outp}$ does not exceed $V_{ref}$, signal DFF.Q will be ‘0’ when FDIV is low, at the rising edge of FDIV, the 6-bit adder will perform increment by one operation. Therefore increase drive current by $I_B$, and this operation will repeat at each rising edge of FDIV until the drive current is large enough to make $V_{outp}$ exceeds $V_{ref}$.

In our design, reference voltage $V_{ref}$ is set to 1.4 V, therefore drive capability is adjusted to make high voltage of differential signals $V_{outp}$ and $V_{outn}$ equal to
1.415 V, high voltage of output signal is a little larger than $V_{\text{ref}}$ because of the limited gain and bandwidth of comparator I1. At the same time, feedback loop consists of $R1$, $R2$, $I2$ and $M1$ keeps the common mode voltage equals to 1.25 V, therefore keeps the low voltage of $V_{\text{outp}}$ and $V_{\text{outn}}$ equal to 1.085 V.

At each rising edge of $FDIV$, the output of the DFF is reset to zero. At the same time, the 6-bit adder perform increment or decrement operation according to the output of DFF, to maintain enough hold time on ‘Add/Sub’ port of the adder, a delay cell is inserted on signal path of $DFF_\cdot Q$.

### 2.2 Current source

Fig. 6 shows the detailed structure of current sources CS0 to CS5. On and OFF status of the current sources are controlled by signal $CTRL[5:0]$.

![Fig. 6. Current sources.](image)

For example, when $CTRL[5]$ is ‘1’, gate voltage of CS5 equals to the bias voltage $V_{\text{bias}}$, thus CS5 is turned on and provide $32I_B$ drive current. When $CTRL[5]$ is ‘0’, gate voltage of CS5 equals to VDD, which turns off the current source.

By this way, the drive current is adjusted in every 16 transitions of the LVDS driver. Providing maximum current of $63I_B$ and minimum current of $I_B$. The 6-bit adder has an overflow protection circuit to stop increment operation when $CTRL[5:0]$ equals to $2\cdot b11111$, and a underflow protection circuit to stop decrement operation when $CTRL[5:0]$ equals to $2\cdot b000001$.

### 3 Experimental results

The proposed self-adaptive LVDS driver was fabricated in a 130 nm CMOS process. Fig. 7 shows the layout and test platform.

Fig. 8 shows measured eye diagram of the proposed LVDS driver at 1.8 Gb/s bit rate with 1 pF load capacitance, differential voltage is 330 mV with self-adaptive technology, while differential voltage is 420 mV when self-adaptive function is
Fig. 7. (a) Chip layout of the proposed LVDS driver (b) Test platform.

Fig. 8. Eye diagram of the proposed self-adaptive LVDS driver at 1.8 Gb/s.

Fig. 9. Eye diagram of the proposed self-adaptive LVDS driver at 400 Mb/s.
disabled for the same driver. Fig. 9 shows measured eye diagram of the proposed LVDS driver at 400 Mb/s bit rate with 1 pF load capacitance. With self-adaptive technology, differential voltage keeps constant, but without self-adaptive technology, differential voltage changes from 420 mV to 600 mV when bit rate is reduced from 1.8 Gb/s to 400 Mb/s.

Fig. 9. Measured eye diagram of the proposed LVDS driver at 400 Mb/s bit rate with 1 pF load capacitance.

Fig. 10 shows test results of the proposed driver under different conditions. Power consumption under different loads with self-adaptive technology are represented by three curves marked as ‘Self-adaptive@1 pF load’, ‘Self-adaptive@5 pF load’ and ‘Self-adaptive@10 pF load’. While power consumption under different loads without self-adaptive technology are represented by three curves marked as ‘Without self-adaptive@1 pF load’, ‘Without self-adaptive@5 pF load’ and ‘Without self-adaptive@10 pF load’. Power consumption results of reference [3], reference [4] and reference [14] are represented by data points marked as ‘Ref. [3]’, ‘Ref. [4]@1 pF’, ‘Ref. [4]@5 pF’ and ‘Ref. [14]@5 pF’. Since self-adaptive technology reduces drive current and keeps differential voltage constant at lower bit rate, power consumption with self-adaptive is lower compared to the same driver when self-adaptive function is disabled. At 400 Mb/s bit rate, power consumption is reduced by 46%, 35% and 30% at 1 pF, 5 pF and 10 pF load capacitance respectively.

Table I summarizes comparison results with a previously reported LVDS driver [4] and an LVDS driver implemented in commercial FPGA device [14]. Power results of the LVDS driver in commercial FPGA device is achieved by the tool ‘Power Estimator’ from Xilinx.

At 400 Mb/s, power consumption of the proposed driver with 5 pF load capacitance is 5.8 mW, while power consumption of reference [4] is 8.5 mW under same condition, with 10 pF load capacitance, power consumption of the proposed driver is 14 mW, while power consumption of reference [14] is 27 mW under same
condition. The proposed driver reduces power consumption by 31% and 48% compared to reference [4] and [14] respectively.

| Reference | Ref. [4] | This work | This work | Ref. [4] | This work | This work |
|-----------|----------|-----------|-----------|----------|-----------|-----------|
| Architecture | BSCS | Self-adaptive | Without self-adaptive | BSCS | Self-adaptive | Without self-adaptive |
| Technology | 180 nm | 130 nm | 130 nm | 180 nm | 130 nm | 130 nm |
| Bit Rate | 400 Mb/s | 400 Mb/s | 400 Mb/s | 1.8 Gb/s | 1.8 Gb/s | 1.8 Gb/s |
| Capacitance | 5 pF | 5 pF | 5 pF | 1 pF | 1 pF | 1 pF |
| Power | 8.5 mW | 5.8 mW | 8.9 mW | 11.6 mW | 11.3 mW | 15.1 mW |

Reference Ref. [14] This work This work Ref. [14] This work This work
Architecture BSCS Self-adaptive Without self-adaptive BSCS Self-adaptive Without self-adaptive
Technology 90 nm 130 nm 130 nm 90 nm 130 nm 130 nm
Bit Rate 400 Mb/s 400 Mb/s 400 Mb/s 1 Gb/s 1 Gb/s 1 Gb/s
Capacitance 10 pF 10 pF 10 pF 10 pF 10 pF 10 pF
Power 27 mW 14 mW 20 mW 28 mW 21 mW 24 mW

Under high speed condition, the proposed driver can provide more current to charge and discharge the output capacitive load, therefore maintains differential voltage large enough to meet the requirements of the receiver, the maximum bit rate of the proposed driver is improved to 2.2 Gb/s compared to reference [4] and [14] with 1.8 Gb/s and 1 Gb/s maximum bit rate respectively.

4 Conclusion

A self-adaptive LVDS driver is presented and implemented in a 130 nm CMOS technology. Instead of providing a constant drive current under different conditions, the proposed driver can adjust drive current according to the changes of output load and operating frequency automatically, therefore eliminates power wasting under small load and low frequency condition. Test results show the proposed driver reduces power consumption by 48% and improves maximum bit rate to 2.2 Gb/s compared to previously reported LVDS drivers with fixed drive capability.