2-1 Switched-current multi-stage noise-shaping delta–sigma modulator with a digital noise-cancellation circuit

Leenendra Chowdary Gunnam\textsuperscript{1,2}, Guo-Ming Sung\textsuperscript{1,3} \& Lei-Wen Weng\textsuperscript{1}

\textsuperscript{1}Electrical Engineering, National Taipei University of Technology, 1, Sec. 3, Zhongxiao E. Road, Taipei 10608, Taiwan
\textsuperscript{2}Electronics and Communication Engineering, Sasi Institute of Technology and Engineering, Tadepalligudem 534101, Andhra Pradesh, India
\textsuperscript{3}Research and Development Centre for Smart Textile Technology, National Taipei University of Technology, 1, Sec. 3, Zhongxiao E. Road, Taipei 10608, Taiwan

E-mail: gmsung@ntut.edu.tw

Abstract: This study focuses on the design of a 2-1 switched-current (SI) multi-stage noise-shaping delta–sigma modulator with a digital noise-cancellation circuit. The noise-cancellation circuit is designed by employing various algorithms for designing the logic circuits and constructing a delay block with an inverter and a transmission gate. It can eliminate the higher-order quantisation noise from the first stage of the modulator completely. In the proposed differential current-mode sample-and-hold circuit, low-input impedances are presented with feedback and width-length adjustment in SI feedback memory cell, a coupled differential replicate with the common-mode feed-forward (CMFF) circuit is used to stabilise the common-mode bias voltage at input terminal, and a differential cross-connected CMFF circuit is utilised to fix the bias voltages. Post-layout simulations reveal that the simulated signal-to-noise-and-distortion ratio (SNDR) was 90.4 dB and the effective number of bit (ENOB) was 14.73 bits. Measurements show that the SNDR was 59.13 dB and the ENOB was 9.53 bits at a sampling rate of 10.24 MHz, an oversampling ratio of 256, and a signal bandwidth of 20 kHz. This design has a power requirement of 12.99 mW from a supply voltage of 1.8 V and occupies a core area of 0.14 mm\textsuperscript{2}.

1 Introduction

Delta–sigma modulation (DSM) is a promising digital processing technique used in modern electronic applications such as sensor interface circuits, frequency synthesizers, biomedical instrumentation, and motor controllers [1–3]. The DSM entails the reshaping of an analogue signal into a multibit digital word in the time domain by using a quantiser with a high signal quality. To maintain a high signal quality, that is, a high signal-to-noise-and-distortion ratio (SNDR), a delta–sigma modulator uses oversampling and noise shaping to eliminate the quantisation noise from the required signal band [4]. In general, the SNDR of a DSM can be improved to ~60 + 3 dB/octave by using an nth-order noise-shaping modulator. Higher-order modulators can be developed using either single-loop or multi-loop architectures. When strong signals occur at the input of a single-loop DSM of an order higher than two, the system becomes unstable [5].

This instability in high-order DSM can be avoided by constructing lower-order modulators in cascade. This arrangement is called multi-stage noise-shaping (MASH); the advantage of this arrangement is that the lower-order modulators are more stable; hence, the overall system remains stable. Moreover, cascade architectures are less sensitive to analogue circuit imperfections, namely limited op-amp gain and bandwidth mismatch caused by gain errors, because they depend on the precise matching of the transfer functions of intermediate delta–sigma stages [6]. To overcome the mismatch problem, a higher-order modulator is employed in the primary stage, so that any leak through of its noise has a less effect compared with that of a first-order primary modulator [7]. In this paper, a third-order modulator was implemented using a second-order modulator in the primary stage and a first-order modulator in the secondary stage. This approach exhibits superior tone performance and less band noise because the noise can be cancelled in the second-order modulation.

Furthermore, the MASH architecture acquires signals from different stages and cancels the lower-order quantisation noise from the earlier stage of a DSM by using a noise elimination network called the digital noise-cancellation circuit (DNCC) [8]. The analogue variations in multiple paths of the DSM can be compensated for by choosing the even and odd adaptive filter coefficients in the DNCC [9]. Digital correction of noise from the earlier stage has been investigated using offline [10] and online adaptive methods [11–14]. An online ‘blind’ calibration technique requires no reference and operates directly on the digital output during conversion; however, this technique requires a band-limited spectrum of the unknown input signal [15]. For this design, we propose various algorithms for the logic circuits and employ a simplified delay block in a DNCC to cancel the noise errors from the earlier stage and generate a third-order noise-shaping output. The aim of this paper was to design a simple, reliable, and inexpensive DNCC to cancel the second-order noise from the primary stage and generate a third-order noise-shaping output for the secondary stage.

In the following section, the design of a 2-1 switched-current (SI) MASH DSM and the optimal parameters are described. Section 3 elucidates the circuit implementation of the proposed 2-1 SI MASH DSM and its relational circuits. Considerations for designing the DNCC by using those proposed algorithms are presented in Section 4. Simulation and measurement results are presented in Section 5, and conclusions are drawn in Section 6.

2 2-1 MASH delta–sigma modulator

We use a second-order modulator in the primary stage and a first-order modulator in the secondary stage, as shown in Fig. 1; this design provides low band noise and absolute stability because of the lower-order modulators. The signal transfer function (STF) and the quantisation noise transfer function (NTF) of each modulator depend on the analogue scaling coefficients. These coefficients are selected in order that minimum quantisation noise, superior signal levels in the transition, and physically realisable blocks such as integrators and digital-to-analogue convertors (DACs) could be obtained [16, 17]. The analogue scaling coefficients of the modulator are listed in Table 1.
2.1 Primary stage

The primary stage of the 2-1 MASH DSM comprises of two discrete-time integrators, two 1 bit DACs, and a 1 bit quantiser; this stage forms a second-order modulator. The output swing of each integrator depends on the input level and gain of the integrator. Furthermore, each integrator exhibits some non-ideal characteristics such as integrator leakage and mismatch between the coefficients, producing noise and distortion in the fundamental frequency at the output of the integrator. The output of the first integrator drives the second integrator; this output depends on the gain of the first integrator. The second integrator produces more attenuation. Thus, the overall modulator performance is poor because of overloading. The aforementioned discussion indicates that the first integrator plays a paramount role in the performance of the modulator.

To obtain high performance, an integrator must be insensitive to the sampling frequency. This can be accomplished using an SI integrator, which provides an area reduction of ∼72% compared with a switched-capacitor (SC) integrator [18]. The rise time of the SI feedback memory cell (FMC) is ∼4.5 ns, whereas that of the traditional first generation (FG) SI MC is ∼16 ns. Clearly, the operating speed of the SI FMC is 70% greater than that of the traditional FG SI MC [19], if the errors due to the quantisation of 1 bit quantiser are $Q_1(z)$ and $Q_2(z)$ in the primary stage and secondary stage, respectively. The STF and NTF of the primary stage are expressed as follows:

$$Y_1(z) = STF_1 \cdot X(z) + NTF_1 \cdot Q_1(z)$$

where

$$STF_1 = \frac{a_1 a_2 z^{-2}}{1 + (a_2 b_2 - 2) z^{-1} + (1 + a_1 a_2 b_1 - a_1 b_2) z^{-2}}$$

$$NTF_1 = \frac{(1 - z^{-1})^2}{1 + (a_2 b_2 - 2) z^{-1} + (1 + a_1 a_2 b_1 - a_1 b_2) z^{-2}}$$

From Table 1, (1) can be rewritten as

$$Y_1(z) = \frac{1}{1 - 1.5z^{-1} + 0.75z^{-2}} \times [0.25z^{-2} \times X(z) + (1 - z^{-1})^2 \times Q_1(z)]$$

(4)

2.2 Secondary stage

The secondary stage of the 2-1 MASH DSM comprises of a discrete-time integrator, a 1 bit DAC, and a 1 bit quantiser; this stage forms a first-order modulator. The STF and NTF of the secondary stage are expressed as follows:

$$Y_2(z) = STF_2 \cdot Y_1(z) - Q_1(z) + NTF_2 \cdot Q_2(z)$$

(5)

where

$$STF_2 = \frac{a_3 z^{-1}}{1 + (a_3 b_3 - 1) z^{-1}}$$

(6)

$$NTF_2 = \frac{1 - z^{-1}}{1 + (a_3 b_3 - 1) z^{-1}}$$

(7)

From Table 1, (5) can be rewritten as

$$Y_2(z) = z^{-1} [Y_1(z) - Q_1(z)] + (1 - z^{-1}) \cdot Q_2(z)$$

(8)

3 Circuit implementation of 2-1 SI MASH DSM

As displayed in Fig. 1, a 2-1 SI MASH DSM consists of three integrators, three current-mode DACs, two 1 bit current-mode quantisers, a non-overlapping clock generator, and a bias current generator. Fig. 2 shows the modified SI integrator circuit with a delay unit ($z^{-1}$), which is completed with two non-overlapping clocks $\phi_1$ and $\phi_2$ and two current-mode sample-and-hold (SH) circuits $SH_1$ and $SH_2$. 

![Block diagram of the proposed 2-1 MASH delta–sigma modulator](image-url)
3.1 Current-mode SH circuit

As shown in Fig. 2, the modified current-mode SH circuit is composed of a differential SI FMC, a coupled differential replicate (CDR) with common-mode feed-forward (CMFF) circuit, and a differential cross-connected CMFF circuit. The proposed SI FMC is used to ensure low-input impedance and small transmission error [19]. Furthermore, the CDR with CMFF is utilised to make a compensation for the error of current mirror, which is caused by either the difference of the drain voltage or the process variation [20] or that the cross-connected CMFF circuit is used to correct the bias voltage at input terminal. That is, the bias voltage of input terminal is deviated from the feedback voltage of DAC. Furthermore, two capacitors, $C_1$ and $C_2$, and two metal–oxide–semiconductor field-effect transistors (MOSFETs), $M_{AA}$ and $M_{BB}$, are added to stabilise the bias voltage and to provide the stable bias current.

In the common-mode operation, both complementary MOS (CMOS) switches are open [20, 21]. The node A at the right-hand side is connected to that at the left-hand side of the cross-connected CMFF circuit, and so does node B. This arrangement guarantees

![Fig. 2 Modified current-mode SH circuit with two FMCs, a CDR CMFF circuit, and a cross-connect CMFF circuit](image)

![Fig. 3 1 bit Cascode current-mode DAC with two switches](image)

![Fig. 4 1 bit Differential current-mode quantiser, which includes two current comparators $M_{21}$–$M_{24}$ and $M_{31}$–$M_{34}$ and two inverters $M_{11}$–$M_{12}$ and $M_{41}$–$M_{42}$](image)

![Fig. 5 Adopted DNCC](image)

![Fig. 6 Modified DNCC](image)

![Fig. 7 Simplified unit delay circuit using inverters and transmission gates](image)
the stability of bias voltage at the input terminal. In the differential-mode operation, a positive small-signal current $i_+$ occurs at $M_1$ with an input current of $i_{in+}$ and a negative small-signal current $-i_-$ occurs at $M_{12}$ with another input current of $i_{in-}$. Then, the bias current of $M_{11}$ is increased to $I_{B} + i_+$. By passing it through the current mirror pair, $M_{11}$ and $M_{12}$, the bias current of $M_{12}$ is changed to $I_{B} + i_-$ and $I_{B} - i_-$. Consequently, the output current of the positive terminal $i_{out+}$ is roughly $2 \times i_+$. In the same manner, the output current of negative terminal $i_{out-}$ is about $-2 \times i_-$.  

### 3.2 1 bit Cascode current-mode DAC circuit

Fig. 3 presents a 1 bit cascade current-mode DAC with two switches, $D_1$ and $D_2$, which are controlled with thermometer codes. When the switch $D_1$ is turned on, the output current $i_{out}$ flows outside the DAC with a bias current $I_{DA}$, so that $i_{out} = I_{DA}$, whereas when the switch $D_2$ is turned on, the output current $i_{out}$ flows inside the DAC, so that $i_{out} = -I_{DA}$. The bias current $I_{DA}$ is controlled with a bias voltage $V_b$. The advantages of this DAC circuit are the high-current swing and the ability to equalise the output current using the thermometer code. Notably, width $W$ and length $L$ of a MOSFET must be as low as possible to minimise the chip size and the power consumption by lowering the bias current.

### 3.3 1 bit Differential current-mode quantiser

Fig. 4 shows a 1 bit differential current-mode quantiser, which is composed of two current comparators, $M_{21}$–$M_{24}$ and $M_{31}$–$M_{34}$, and two inverters, $M_{11}$–$M_{12}$ and $M_{41}$–$M_{42}$. Notify that both input terminals, $i_{in+}$ and $i_{in-}$, are connected to sources of $M_{21}$, $M_{22}$, $M_{31}$, and $M_{32}$ to have a low-input resistance. If a positive input current $+i_m$ flows into the first current comparators $M_{21}$–$M_{24}$, then the source voltage of $M_{22}$ will be enlarged and a positive voltage will occur at output node $V_{out+}$. In the meantime, a negative voltage is generated at output node $V_{out-N}$. The functions of the inverter, $M_{41}$ and $M_{42}$, are utilised to have an optimal output swing from $V_{SS} (=0 V)$ to $V_{DD} (=1.8 V)$. If the reset switch is turned on, both output voltages will be equal. Thus, the differential output voltage is roughly zero. If the Reset switch is turned off, the quantiser will work successfully.

### 4 Digital NCC

A 2-1 MASH DSM provides a second-order NTF (NTF$_1$) in the primary stage [$Y_1(z)$] and a first-order NTF (NTF$_2$) in the second stage [$Y_2(z)$]. By deploying a suitable DNCC, we can obtain a third-order NTF from the secondary stage and eliminate the second-order NTF from the primary stage of the 2-1 DSM, as shown in Fig. 5.

Through digital signal processing, the DNCC converts the two outputs of the 2-1 MASH DSM into a single output digital word having a third-order output with a third-order NTF. The output digital word should have the number and characteristics of the

### Table 2 Output digital word, $S_0$–$S_1$, of logic circuit in 2's complement form

| Items | Inputs | $F$ | $G$ | Output/frequencies | $S_0$ | $S_2$ | $S_4$ | $S_6$ | 2's Complement representation |
|-------|--------|-----|-----|--------------------|-------|-------|-------|-------|-----------------------------|
| 1     | 1      | 1   | 1   | 1                   | 1     | 1     | 1     | 1     | 1                           |
| 2     | -1     | -1  | -1  | -1                 | 0     | -1/2  | 1     | 1     | 1                           |
| 3     | -1     | -1  | 1   | -1                 | 1     | 0     | 1     | 1     | 1                           |
| 4     | -1     | -1  | -1  | 1                  | 0     | -9/2  | 1     | 1     | 1                           |
| 5     | -1     | -1  | -1  | -1                | 0     | -1/2  | 1     | 1     | 1                           |
| 6     | -1     | -1  | -1  | 1                | 16    | 15/1  | 0     | 0     | 1                           |
| 7     | -1     | 1   | -1  | -1                | -8    | -9/2  | 1     | 1     | 1                           |
| 8     | -1     | 1   | -1  | -1                | 0     | -3/2  | 1     | 1     | 1                           |
| 9     | -1     | 1   | -1  | -1                | 8     | 5/2   | 0     | 0     | 0                           |
| 10    | -1     | 1   | 1   | -1                | 16    | 13/1  | 0     | 0     | 1                           |
| 11    | -1     | 1   | 1   | -1                | -8    | -1/2  | 1     | 1     | 1                           |
| 12    | -1     | 1   | 1   | -1                | 0     | -3/2  | 1     | 1     | 1                           |
| 13    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 14    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 15    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 16    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 17    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 18    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 19    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 20    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 21    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 22    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 23    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 24    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 25    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 26    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 27    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 28    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 29    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 30    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 31    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |
| 32    | -1     | 1   | 1   | -1                | 3     | 8     | 11/2  | 0     | 0                           |

330  IET Circuits Devices Syst., 2019, Vol. 13 Iss. 3, pp. 327-336
This is an open access article published by the IET under the Creative Commons Attribution-TypeNonCommercial License (http://creativecommons.org/licenses/by-nc/3.0/)

[4](http://creativecommons.org/licenses/by-nc/3.0/)
Table 3 Value G with respect to three inputs: C, D, and E

| Items | C | D | E | G |
|-------|---|---|---|---|
| 1     | −1| −1| −1| 0 |
| 8     | 1 | 1 | 1 | 0 |
| 9     | −1| −1| −1| 0 |
| 16    | 1 | 1 | 1 | 0 |
| 17    | −1| −1| −1| 0 |
| 24    | 1 | 1 | 1 | 0 |
| 25    | −1| −1| −1| 0 |
| 32    | 1 | 1 | 1 | 0 |

where \(d_1, d_2, H_1(z), \) and \(H_2(z)\) can be expressed with 1.0, 4 (\(= a(z)^{-1}\)), \(z^2\), and \((1-z^{-1})^2\), respectively. From (4) and (8), \(Y(z)\) becomes

\[
Y(z) = z^{-3}X(z) + 4(1 - z^{-1})Q2(z)
\]

Equation (10) clearly shows that the output of the DNCC has a third-order noise function; moreover, it eliminates noise \(Q2(z)\) from the first stage. Equation (9) can be rewritten as

\[
Y(z) = (2z^{-1} - z^{-3})Y_1(z) + (4 - 8z^{-1} + 4z^{-3})Y_2(z) = 2A - B + 4C - 8D + 4E
\]

where \(A, B, C, D, \) and \(E\) are \(z^{-2}Y_1(z), z^{-3}Y_1(z), Y_2(z), z^{-1}Y_2(z), \) and \(z^{-2}Y_2(z)\), respectively.

As shown in (11), the DNCC can be implemented using a logic circuit and delay blocks; each delay block provides one-unit delay \((z^{-1})\), as shown in Fig. 6. This one-unit delay can be produced with the help of a non-overlapping clock by using inverters and transmission gates, as shown in Fig. 7, to switch the signal. The logic circuit produces an output digital numeral between \(-19\) and \(+19\). The input-output relationship is not a one-to-one function, and its numerical distribution is not uniform. This output value of logic circuit is a function of inputs such as \(A, B, C, D, \) and \(E\), and is represented as a 6 bit digital word from \(S_1\) to \(S_6\) in 2’s complement form. \(S_6\) is the most significant bit and \(S_1\) is the least significant bit of the output digital word.

Table 2 illustrates that each digital bit is influenced by the inputs, except \(S_1\) because its value is always 1 for any combination of the input. For example, if \(A = 1, B = 1, C = -1, D = 1, \) and \(E = -1\), then \(Y = (2A - B) + (4C - 8D + 4E) = -15\) and its 2’s complement value \((S_6 - S_1) = 011001\) (item 27 in Table 2).

Implementing (11) requires at least four sets of components of a 6 bit full adder, four 6 bit multipliers, five 6 bit registers, and five transmission gates, as shown in Fig. 7, to switch the signal. The logic circuit produces an output digital numeral between \(-19\) and \(+19\). The input-output relationship is not a one-to-one function, and its numerical distribution is not uniform. This output value of logic circuit is a function of inputs such as \(A, B, C, D, \) and \(E\), and is represented as a 6 bit digital word from \(S_1\) to \(S_6\) in 2’s complement form. \(S_6\) is the most significant bit and \(S_1\) is the least significant bit of the output digital word.

Table 2 illustrates that each digital bit is influenced by the inputs, except \(S_1\) because its value is always 1 for any combination of the input. For example, if \(A = 1, B = 1, C = -1, D = 1, \) and \(E = -1\), then \(Y = (2A - B) + (4C - 8D + 4E) = -15\) and its 2’s complement value \((S_6 - S_1) = 011001\) (item 27 in Table 2).

Implementing (11) requires at least four sets of components of a 6 bit full adder, four 6 bit multipliers, five 6 bit registers, and five transmission gates, as shown in Fig. 7, to switch the signal. The logic circuit produces an output digital numeral between \(-19\) and \(+19\). The input-output relationship is not a one-to-one function, and its numerical distribution is not uniform. This output value of logic circuit is a function of inputs such as \(A, B, C, D, \) and \(E\), and is represented as a 6 bit digital word from \(S_1\) to \(S_6\) in 2’s complement form. \(S_6\) is the most significant bit and \(S_1\) is the least significant bit of the output digital word.

Table 2 illustrates that each digital bit is influenced by the inputs, except \(S_1\) because its value is always 1 for any combination of the input. For example, if \(A = 1, B = 1, C = -1, D = 1, \) and \(E = -1\), then \(Y = (2A - B) + (4C - 8D + 4E) = -15\) and its 2’s complement value \((S_6 - S_1) = 011001\) (item 27 in Table 2).

Implementing (11) requires at least four sets of components of a 6 bit full adder, four 6 bit multipliers, five 6 bit registers, and five transmission gates, as shown in Fig. 7, to switch the signal. The logic circuit produces an output digital numeral between \(-19\) and \(+19\). The input-output relationship is not a one-to-one function, and its numerical distribution is not uniform. This output value of logic circuit is a function of inputs such as \(A, B, C, D, \) and \(E\), and is represented as a 6 bit digital word from \(S_1\) to \(S_6\) in 2’s complement form. \(S_6\) is the most significant bit and \(S_1\) is the least significant bit of the output digital word.
$S_6$ is influenced by three inputs, $A$, $D$, and $G$. If $G = 0$, then $S_6 = \bar{A}$. If not, $S_6 = D$.

### 4.2 $S_5$ algorithm and logic circuit

Fig. 10 illustrates the determination of the $S_5$ value using the $S_5$ algorithm. Table 5 illustrates that the output bit $S_5$ is affected by the input $A$ and value $G$.

**Table 5** Output bit $S_5$ with respect to the input $A$ and value $G$

| Items | $A$ | $A$ | $G$ | $S_5$ |
|-------|-----|-----|-----|-------|
| 1     | -1  | 1   | 0   | 1     |
| 8     | -1  | 1   | 0   | 1     |
| 9     | -1  | 1   | 0   | 1     |
| 16    | -1  | 1   | 0   | 1     |
| 17    | 1   | -1  | 0   | 0     |
| 24    | 1   | -1  | 0   | 0     |
| 25    | 1   | -1  | 0   | 0     |
| 32    | 1   | -1  | 0   | 0     |
| 2     | 1   | -1  | 8   | 0     |
| 3     | 1   | -1  | -16| 1     |
| 4     | 1   | -1  | -8 | 1     |
| 5     | 1   | -1  | 8  | 0     |
| 6     | 1   | -1  | 16 | 0     |
| 7     | 1   | -1  | -8 | 1     |
| 10    | 1   | -1  | 8  | 0     |
| 11    | 1   | -1  | -16| 1     |
| 12    | 1   | -1  | -8 | 1     |
| 13    | 1   | -1  | 8  | 0     |
| 14    | 1   | -1  | 16 | 0     |
| 15    | 1   | -1  | -8 | 1     |
| 18    | -1  | -1  | 8  | 0     |
| 19    | -1  | -1  | -16| 1     |
| 20    | -1  | -1  | -8 | 1     |
| 21    | -1  | -1  | 8  | 0     |
| 22    | -1  | -1  | 16 | 0     |
| 23    | -1  | -1  | -8 | 1     |
| 26    | -1  | -1  | 8  | 0     |
| 27    | -1  | -1  | -16| 1     |
| 28    | -1  | -1  | -8 | 1     |
| 29    | -1  | -1  | 8  | 0     |
| 30    | -1  | -1  | 16 | 0     |
| 31    | -1  | -1  | -8 | 1     |

$S_5$ is the complement of $A$. By contrast, if the value of $G$ is not equal to 0, the value of $S_5$ depends on the values of $A$ and $G$. Moreover, if the value of $A$ is equal to 1 and the value of $G$ is equal to 8, the $S_5$ is equal to 0. By the way, the $S_5$ is equal to 1 if the value of $G$ is not equal to 8. Furthermore, if the value of $A$ is not equal to 1 and the value of $G$ is equal to $-8$, then $S_5$ becomes 1. Conversely, $S_5$ changes into 0 if the value of $G$ is not equal to $-8$, as shown in Fig. 10. Fig. 11 shows the logic circuit to implement the $S_5$ algorithm.

### 4.3 $S_4$ algorithm and logic circuit

Figs. 12 and 13 illustrate the $S_4$ algorithm and its corresponding logic circuit, respectively. Table 6 illustrates that the output bit $S_4$ is influenced by the inputs, $A$, $C$, $E$, and value $G$. If the value of $G$ is not equal to 0 and $A$ is equal to 1, the value of $S_4$ is equal to an exclusive OR operation of $C$ and $E$. The $S_4$ value is equal to an XNOR operation of $C$ and $E$ when $G$ is not equal to 0 and $A$ is not equal to 1, as shown in Fig. 12. Fig. 13 shows the logic circuit to implement the $S_4$ algorithm.

### 4.4 $S_1$, $S_2$, and $S_3$ algorithms

As shown in Table 2, the value of $S_3$ is the complement of $A$, $S_3 = \bar{A}$, the value of $S_2$ is the complement of $B$, $S_2 = \bar{B}$, and the value of $S_1$ is fixed to 1. Fig. 14 shows the logic circuit to implement the $S_1$, $S_2$, and $S_3$ algorithms.
5 Simulated and measured results

Fig. 15 illustrates the magnitude plot for $Q_1(z)$ before and after implementation of the DNCC using MATLAB software. The slope of $Q_1(z)$ was almost 0 dB/decade after implementation of the circuit [$Q_1(z)$ is cancelled in $Y(z)$], whereas it was 40 dB/decade before implementation of the circuit [$Q_1(z)$ in $Y_1(z)$]. Fig. 16 illustrates the magnitude plot of $Q_2(z)$. Before implementation of the DNCC, $Q_2(z)$ had a slope of 20 dB/decade (i.e. first-order noise), whereas, after implementation, the slope was 60 dB/decade (third-order noise); these results indicate an improvement in the bandwidth.

Fig. 17 illustrates the pre-layout simulation of the input–output waveforms of the DNCC implemented using the proposed

Table 6 Output bit $S_4$ with respect to the inputs: $A$, $C$, $E$, and value $G$

| Items | $A$ | $C$ | $E$ | $G$ | $S_4$ |
|-------|-----|-----|-----|-----|-------|
| 1     | 1   | 1   | 1   | 0   | 1     |
| 2     | −1  | −1  | −1  | −1  | 0     |
| 3     | 1   | 1   | −1  | −1  | 0     |
| 4     | −1  | −1  | −1  | −1  | 0     |
| 5     | 1   | −1  | −1  | −1  | 0     |
| 6     | −1  | −1  | −1  | −1  | 0     |
| 7     | −1  | −1  | −1  | −1  | 0     |
| 8     | 1   | −1  | −1  | 0   | 1     |
| 9     | −1  | −1  | 1   | 0   | 1     |
| 10    | 1   | 1   | 1   | −1  | 1     |
| 11    | −1  | −1  | −1  | 1   | 0     |
| 12    | 1   | 1   | −1  | −1  | 1     |
| 13    | −1  | −1  | 1   | −1  | 1     |
| 14    | 1   | 1   | 1   | −1  | 1     |
| 15    | −1  | −1  | 1   | 1   | 0     |
| 16    | 1   | 1   | 1   | −1  | 1     |
| 17    | −1  | −1  | 1   | 1   | 0     |
| 18    | 1   | −1  | 1   | −1  | 0     |
| 19    | −1  | −1  | 1   | −1  | 0     |
| 20    | 1   | 1   | 1   | 1   | 0     |
| 21    | −1  | −1  | 1   | 1   | 0     |
| 22    | 1   | 1   | 1   | 1   | 0     |
| 23    | −1  | −1  | 1   | 1   | 0     |
| 24    | 1   | 1   | 1   | 1   | 0     |
| 25    | −1  | −1  | 1   | 1   | 0     |
| 26    | 1   | 1   | 1   | 1   | 0     |
| 27    | −1  | −1  | 1   | 1   | 0     |
| 28    | 1   | −1  | 1   | 1   | 0     |
| 29    | −1  | −1  | 1   | 1   | 0     |
| 30    | 1   | 1   | 1   | 1   | 0     |
| 31    | −1  | −1  | 1   | 1   | 0     |

This is an open access article published by the IET under the Creative Commons Attribution -NonCommercial License (http://creativecommons.org/licenses/by-nc/3.0/)
algorithms and logic circuits. For certain inputs such as $A = +1$, $B = +1$, $C = -1$, $D = +1$, and $E = -1$, $Y = (2A - B) + (4C - 8D + 4E) = -15$, and its 2’s complement value ($S_6$–$S_1$) was 110,001 at the digital output code, as shown in Fig. 17 (item 27 in Table 2).

We used Laker layout software to complete the circuit layout of the 2-1 SI MASH DSM with the DNCC, as shown in Fig. 18. The clock frequency and oversampling ratio (OSR) were 10.24 MHz and 256, respectively. The chip was implemented using a Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm 1P6M CMOS process, and the layout area was estimated to be 0.980 × 0.903 mm$^2$ including pads; the power dissipation of the chip was roughly 12.99 mW. Fig. 19 shows the chip microphotograph of the proposed 2-1 SI MASH DSM with DNCC. Moreover, the SNDR and the effective number of bits (ENOBs) were 90.4 dB and 14.73, respectively, as shown in Fig. 20. The post-layout simulations of SNDR and ENOB values are presented in Table 7. All simulated ENOBs are larger than 14 bits in spite of process variation.
Fig. 21 shows the measured platform including 9 V battery, device under test (DUT) printed circuit board (PCB), ultra-low distortion function generator (SRS DS360), synthesised signal generator (Anritsu MG3642A), digital signal analyser-oscilloscope (Keysight DSAV134A), logic analyser (Agilent 16902B), and LabVIEW software. The signal generator provides a sampling frequency of 20 MHz, the ultra-low distortion function generator generates a differential input sine wave, and the oscilloscope is used not only to display the output waveform in the time domain, but also to proceed the fast Fourier transform analysis in the frequency domain. Finally, the digital output code will be captured by logic analyser and be sent to LabVIEW software to calculate the SNDR and ENOB. Notify that the power regulators of bias circuit (bias power), a digital circuit (digital power), and an analogue circuit (anologue power) are separated to be prevented from power interference in DUT PCB. By the way, the battery is considered to have a stable power supply.

In general, the proposed 2-1 SI MASH DSM is integrated with DNCC and fabricated in a chip not only to improve the DSM performance, but also to reduce the chip area. However, we find that the DSM performance is affected by DNCC in SNDR measurement. To remedy this problem, the measurement is completed with two chips. One is used to measure the SNDR of DSM; the other is used to verify the function of the designed DNCC. Fig. 22 shows the measured PCB of the proposed DSM with DNCC. The input sine wave is fed to the chip 1 to measure the SNDR of DSM and a 6 bit digital output word can be read from chip 2. The reason why we select two chips is that the analogue DSM is affected by the proposed DNCC and the guard ring is too thin to isolate the analogue circuit from the digital circuit. Furthermore, we find that the bias voltage at the input terminal will be changed with DAC feedback. Thus, a cross-connected CMFF circuit is able to stabilise the common-mode bias voltage at the input terminal, as shown in Fig. 2.

Fig. 23 presents the measured 65535-point power spectrum density (PSD) of the proposed 2-1 SI MASH DSM with DNCC at an input current of 14 μA, a signal frequency of 10 kHz, a signal bandwidth of 20 kHz, and an OSR of 256. At the sampling frequency of 10.24 MHz, the proposed SI DSM with DNCC yields an SNDR of 56.74 dB, which indicates that the ENOB is ∼9.13 bits at a control voltage $V_{b1}$ of 0.8 V, a first bias voltage $V_{b2}$ of 0.25 V, a second bias voltage $V_{b3}$ of 1.05 V, and a third bias voltage $V_{b3}$ of 1.4 V. By the way, an SNDR of 59.13 dB, which indicates that the ENOB is ∼9.53 bits, is achieved with a signal frequency of 15 kHz. According to the simulated SNDR of 134.9 dB for DNCC, the difference between simulated signal-to-noise ratio (SNR) and measured SNR is due to analogy circuit. Process variation, thermal noise, and time delay are the dominant variations in DSM circuit. The modified current-mode SH circuit and simplified unit delay circuit are used to improve the resolution of analogue-to-digital converter.

A performance summary and comparison with other MASH DSMs are presented in Table 8, which demonstrates the simulated and measured properties of the proposed DSM developed herein. Here, the figure-of-merit (FoM) is defined as follows [21]:

$$FoM = \frac{power}{2BW (\text{conversion step})}$$ (13)

The performance comparison in Table 8 displays that the signal bandwidth, sampling frequency, simulated SNRs, power consumption, and core area of the proposed 2-1 SI MASH DSM with DNCC are better than those in [20, 22]. The simulated and measured FoMs of this paper are 11.95 and 439.27 pJ/step, respectively, and are significantly improved by the modified current-mode SH circuit with cross-connected CMFF circuit. That is, the simulated FoM of 11.95 pJ/step and the measured FoM of 439.27 pJ/step are superior to those in [22–24]. The proposed 2-1 SI MASH DSM with DNCC demonstrates a competitive FoM at the Nyquist frequency compared with the similar SI design up-to-date [22–24]. In comparison with switched-capacitor (SC) and

![Fig. 23 Measured PSD of the proposed 2-1 SI MASH DSM with DNCC](image)

| Table 7 | Post-layout simulated SNDR value of each process variation |
| Corners | TT | FF | SS | SF | FS |
| SNDR, dB | 90.4 | 88.3 | 93.6 | 87.1 | 95.3 |
| ENOB, bits | 14.73 | 14.38 | 15.26 | 14.17 | 15.54 |

| Table 8 | Performance summary and contrast with other SI MASH delta–sigma modulators |
| reference (year) | [22] (2004) | [23] (2006) | [24] (2016) | [20] (2017) | this work (2018) |
| technology, μm | 0.8 | 0.18 | 0.18 | 0.18 | 0.18 |
| supply voltage, V | 3.3 | 1.8 | 1.8 | 1.8 | 1.8 |
| sampling category | SI | SI | SI | SI | SI |
| signal bandwidth, kHz | 8 | 5 | 20 | 20 | 20 |
| sampling frequency, MHz | 2.048 | 0.64 | 10.24 | 10.24 | 10.24 |
| simulated SNR, dB | — | 50.6 | 65.57 | 84.85 | 90.4 |
| measured SNR, dB | 54 | — | 60.87 | 64.4 | 59.13 |
| simulated ENOB, bits | — | 8.11 | 10.6 | 13.78 | 14.73 |
| measured ENOB, bits | 8.68 | — | 9.82 | 10.39 | 9.53 |
| power, mW | 18 | 0.18 | 18.82 | 18.80 | 12.99 |
| core area, mm² | 0.45 | 0.77 | 0.30 | 0.30 | 0.146 |
| simulated FoM, pJ/conv | — | 65.15 | 303.14 | 32.9 | 11.95 |
| measured FoM, pJ/conv | 2742.9 | — | 520.53 | 357.6 | 439.27 |
continuous-time categories [25, 26], the SI technique performs with high power consumption and large FoM. Those disadvantages limit its performance significantly. Fortunately, this paper occupies less chip space because that the DNCC is implemented using the proposed algorithms and the SI integrators. Notify that this paper suffers from the process variation, thermal noise, and time delay. This is the reason why we have a high post-layout simulated ENOB of 14.73 bits, whereas a low-measured ENOB of 9.53 bits is achieved in the designed chip. The ENOB decrement results in a huge difference between simulated FoM and measured FoM.

6 Conclusion

In this paper, we present many novel algorithms to implement the designed DNCC for a 2:1 SI MASH DSM by using a TSMC 0.18 μm 1P6M CMOS process. The post-layout simulation shows that the SNDR was 90.4 dB and the ENOB was 14.73 at a sampling rate of 10.24 MHz, an OSR of 256, and a signal bandwidth of 20 kHz. Finally, the power dissipation was 12.99 mW with a supply voltage of 1.8 V, and the core area was roughly 0.146 mm² without pads. This paper occupies less chip space using the proposed algorithms and the SI integrators. Notify that the performance has significantly improved by the modified current-mode SH circuit with cross-connected CMFF circuit. Measurements reveal that the SNDR and ENOB are 59.13 dB and 9.53 bits, respectively. This paper suffers from the process variation and thermal noise. Table 8 summarises the performance and compares the performance of our design with other MASH DSMs. The simulated SNR and chip area of the proposed design are superior to those of previously published designs.

7 Acknowledgments

The authors thank the Ministry of Science and Technology, R.O.C., Taiwan, for financially supporting this research under Contract no. MOST 106-2221-E-027-075. They are grateful to the Chip Implementation Center, Taiwan, for fabricating the test chip. We acknowledge Wallace Academic Editing for editing this paper.

8 References

[1] Ohnhäuser, F.: ‘Analog-digital converters for industrial applications including an introduction to digital-analog converters’ (Springer, New York City, USA, 2015)
[2] Bourdopoulos, G.I.: ‘Delta–sigma modulators: modeling, design, and applications’ (Imperial College Press, London, UK, 2003)
[3] Kozak, M.K.I.: ‘Oversampled delta–sigma modulators: analysis, applications and novel topologies’ (Springer US, New York City, USA, 2003)
[4] Pavan, S., Schreier, R., Temes, G.C.: ‘Understanding delta–sigma data converters’ (Wiley, New Jersey, USA, 2016)
[5] Carusone, T.C., Johns, D., Martin, K.: ‘Analog integrated circuit design’ (John Wiley & Sons, New Jersey, USA, 2001)
[6] Gaggl, R.: ‘Delta–sigma A/D-converters: practical design for communication systems’ (Springer Series in Advanced Microelectronics, New York City, USA, 2013)
[7] Fernández, R.R., Hidalgo, F.M., Pérez-Verdú, B.: ‘CMOS cascade sigma–delta modulators for sensors and telecom: error analysis and practical design’ (Springer Science & Business Media, New York City, USA, 2011)
[8] Hosseini, K., Kennedy, M.P.: ‘Minimizing spurious tones in digital delta–sigma modulators’ (Springer Science & Business Media, New York City, USA, 2011)
[9] Kiss, P., Silva, J., Wiesbauer, A., et al.: ‘Adaptive digital correction of analog errors in MASH ADCs. II. Correction using test-signal injection’, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., 2000, 47,(7), pp. 629–638
[10] Cauwenberghs, G., Temes, G.C.: ‘Adaptive calibration of multiple quantization oversampled A/D converters’. Proc. Int. Symp. Circuits and Systems, Atlanta, GA, USA, May 1996, pp. 512–515
[11] Yang, Y., Schreier, R., Temes, G.C., et al.: ‘On-line adaptive digital correction of dual-quantization delta–sigma modulators’, Electron. Lett., 1992, 28,(16), pp. 1511–1513
[12] Abdennadher, S., Kaei, S., Temes, G.C., et al.: ‘Adaptive self-calibrating delta–sigma modulators’, Electron. Lett., 1992, 28,(14), pp. 1288–1289
[13] Wiesbauer, A., Temes, G.C.: ‘Adaptive digital compensation of analog circuit imperfections for cascaded sigma–delta modulators’. Proc. 30th Asilomar Conf. Signals, Systems and Computers, Pacific Grove, CA, USA, November 1996, pp. 1073–1077
[14] Cauwenberghs, G.: ‘Blind on-line digital calibration of multi-stage Nyquist-rate and oversampled A/D converters’. Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'98), Monterey, CA, 1998, vol. I, pp. 1–4
[15] Cauwenberghs, G., Temes, G.C.: ‘Adaptive digital correction of analog errors in MASH ADCs – part I: off-line and blind on-line calibration’, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., 2000, 47,(6), pp. 621–628
[16] Silva, J., Moon, U., Steenegaard, J., et al.: ‘Wideband low distortion delta–sigma ADC topology’, IET Electron. Lett., 2001, 37,(12), pp. 737–738
[17] Marker-Viluums, N., Jorgensen, I.H.H., Bruun, E.: ‘Low power continuous-time delta–sigma ADC with current output DAC’. Proc. 2015 European Conf. Circuit Theory and Design (ECCDT), Trondheim, Norway, August 2015, pp. 1–4
[18] Sung, G.M., Yu, C.P., Yao, D.A.: ‘A comparison of second-order sigma–delta modulator between switched-capacitor and switched-current techniques’. Proc. 2008 IEEE Asia Pacific Conf. Circuits and Systems (APCCAS), Macao, China, November 2008, pp. 1172–1175
[19] Sung, G.M., Yao, D.A., Chang, K.H., et al.: ‘A second-order sigma–delta modulator with switched-current memory cell for closed-loop motor control system’. Proc. 37th IEEE Power Electronics Specialists Conf., Jeju, Korea, June 2006, pp. 1–5
[20] Sung, G.M., Gunnam, L.C., Lin, W.S., et al.: ‘A third-order multibit switched-current delta–sigma modulator with switched-capacitor flash ADC and IDWA’. IEEE Trans. Electron., 2017, E100-C,(8), pp. 1–10
[21] Chae, Y., Han, G.: ‘Low voltage, low power, inverter-based switched-capacitor delta–sigma modulator’, IEEE J. Solid-State Circuits, 2009, 44,(2), pp. 458–472
[22] Loulou, M., Dallet, D., Masmoudi, N., et al.: ‘A 3.3 V, 10 bins, clock-feedthrough compensated switched-current second order sigma–delta modulator’, Analog Integr. Circuits Signal Process., 2008, 54,(1), pp. 81–87
[23] Cheng, C.J., Lee, S.Y.: ‘A low-voltage adaptive switched-current SDF for bio-acquisition microsystems’. Proc. IEEE Int. Symp. Circuits and Systems, Island of Kos, Greece, May 2006, pp. 341–344
[24] Sung, G.M., Lin, W.S., Yu, C.P.: ‘Third-order switched-current delta–sigma modulator with ADC and IDWA’. Proc. Int. Symp. Computer, Consumer and Control (IS3C), Xi’an, China, July 2016, pp. 323–326
[25] Chang, C.L., Wu, J.T.: ‘A V 1000 dB dynamic range 24-kHz bandwidth delta–sigma modulator’. Proc. IEEE Int. Symp. Circuits and Systems (ISCAS 2013), Beijing, China, May 2013, pp. 813–816
[26] Xu, Y., Zhang, Z., Chi, R., et al.: ‘A 5.20 MHz BW reconfigurable quadrature bandpass CT ΔΣ ADC with antipole-splitting opamp and digital IQ calibration’, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2016, 24,(1), pp. 243–255