Power Loss Investigation of Si-SiC Hybrid Switches in a Modular Multilevel Converter System

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Abstract. To reduce the power loss in a modular multilevel converter (MMC), hybrid switches with different combinations of Si-IGBT, SiC-MOSFET, Si-FRD and SiC-SBD in parallel or anti-parallel are comparatively investigated. By comparing the power losses in MMC submodule (SM) bridge arm switching devices, one bridge arm of a SM is replaced with a different switch configuration, while the other remains in the conventional Si-IGBT and FRD configuration. $I_{tot} - E_{sw}$ and $I - V$ curves are obtained for four switch configurations through SIMETRIX, and brought to SIMULINK simulation over longer time scales to account for the variable switch operating condition. Along with the simulation and experimental results, the loss differences under different switch configurations are verified, obtaining the optimal switch configuration at last, which is instructive for the selection of MMC SM in the future.

1. Introduction

Modular multilevel converter (MMC) has become the first choice for Voltage Source Converter-High Voltage Direct Current (VSC-HVDC) due to its low control difficulty, low loss, high output voltage waveform quality, and strong grid fault handling capability[1]. However, device failures and relatively high power loss remain as concerns. Indeed, customer demand for efficiency and reliability has put pressing requirement on manufacturers to keep improving device performance[2].

Silicon Insulated Gate Bipolar Transistor (Si IGBT) together with anti-paralleled Fast Recovery Diode (FRD) is the conventional switch configuration widely used in power electronic converters, but bipolar devices usually bring about large switching losses while the conduction loss only reduces slowly as the current reduces. A Silicon- Silicon Carbide (Si-SiC) hybrid switch, Hys-F in figure 1, was proposed with the purpose to reduce the switching loss without increasing the conduction loss[5-6]. Separate IGBT and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) gate driving was recommended for zero-voltage switching of the IGBT[6]. SiC- Schottky Barrier Diode (SBD) was later used as the freewheeling diode (Hys-S) to avoid large reverse recovery current ($I_{rr}$) in the FRD[4]. Care should be taken to prevent the body-diode in the MOSFET from being turned on.

The potential benefit of the hybridization very much depends on the operating condition of the switch. So far, most studies have focussed on fixed conditions. For instance, an optimum switching sequence would be valid for a certain current level. As a result, intended applications have been mainly DC-DC converters. This paper aims to evaluate the benefit in an MMC submodule (SM) where the switch
operating point is constantly changing. For the reason to become clear later, the evaluation should consider the interactions between the devices included in the combined switch configuration. This study demonstrates an evaluation process using the SEMITRIX software to account for the device level physics. The results are then scaled up to evaluate a relatively large MMC system. In addition to intra-cycle variations, variation of the switch operating point can also occur over longer time scales in grid applications.

The hybrid switches considered in this study consist of similarly rated Si-IGBT, SiC-MOSFET and SiC-SBD. It is assumed that the MMC SM is of a half-bridge configuration as shown in figure 1. In a standard design, each of the two arm switches will consist of several IGBTs in parallel and PiN diodes in anti-parallel. In order to clearly show the effect of device hybridization, only the upper arm will be replaced by these four switch configurations[7].

![Figure 1. The switch configurations in MMC SM. (a) MMC half-bridge SM (b) Conventional switch: IGBT and PiN diode in anti-parallel (c)Mixed switch: IGBT and SiC SBD in anti-parallel (d) Hys-F: IGBT, SiC MOSFET and PiN diode in anti-parallel (e) Hys-S: IGBT, SiC MOSFET and SiC SBD in anti-parallel.](image)

### 2. Switch configurations setup in MMC system

The SM upper arm switch will be considered to have one of the hybrid configurations shown in figure 1. It is assumed here that the MMC works in the inverter mode with parameters listed in Table 1.

| Parameter                        | Value                                      |
|----------------------------------|--------------------------------------------|
| Pole-pole dc voltage             | 5kV                                        |
| Grid voltage                     | 2.75kV line-to-line, 50Hz                  |
| MMC active power                 | 1.9MW                                      |
| Grid side inductance             | 8.1mH                                      |
| Grid side resistance             | 0.2Ω                                       |
| Arm inductance                   | 8.1mH                                      |
| Arm resistance                   | 0.1Ω                                       |
| Rated SM capacitance             | 3mF                                        |
| Number of SMs                    | 20 per arm                                 |
| SM capacitance dc voltage        | 500V                                       |

This investigation chooses for the IGBT and MOSFET to turn on simultaneously, providing dual channels for \(I_{TE}\) (if any) of the diode and reduce current overshoot. Then at turn-off the IGBT is 1.5\(\mu\)s ahead of the MOSFET and this includes most of the IGBT tail current time but will not increase too much of the MOSFET’s conduction loss. The fixed switching coordination is shown in figure 2.
Figure 4 shows the waveforms of the arm current going through the SM switches. The current of the active switch in the upper bridge arm is in general less than the lower arm current in the inverter mode of operation, however, the diodes just behave in opposite. Corresponding to this, one can configure different switches for the bridge arms in the SM to minimize the total loss. From the I-V curves in figure 3, it can be seen that the MOSFET tends to have lower conduction loss than IGBT in the low current range.

In simulation, models of a 1200V/50A Si-IGBT RGS50TSX2HR without FRD and a 1200V/31A SiC-MOSFET SCT3080KL as well as two 1200V/40A SiC-SBD SCS240KE2 are built. The current rating of the SBDs is 80 A, relatively large compared with SiC-MOSFET, to prevent the body diode from turning on. These form a single hybrid switch block as shown in figure 1(e). The relatively low amperes of all the fundamental devices are due to the limitation in the SIMETRIX software. The conventional switch is also modelled in SIMETRIX, with two 50 A IGBTs RGS50TSX2DHR with FRD to form a building block as figure 1(b). Meanwhile, the lower arm is kept as Si-IGBT and Si-PiN Diode, and the upper arm uses these four switch configurations shown in figure 1(b)-(e) to compare the power changes, respectively.

As shown in figure 4, the positive and negative peak values of the bridge arm current are 400 A and -150 A, respectively. Therefore, appropriate number of building blocks is used to reach the same total current rating. Therefore, in this investigation SIMETRIX is used to build a double pulse model for the switch building block and extract its switching and conduction characteristics first. Keep the upper and lower arms unchanged respectively, and increase the charging time to obtain different output current where the forward and reverse $I_{sat} - E_{sw}$ curves of arm switches can be obtained through equation (1) further. Sending the data into SIMULINK system to calculate the switching loss based on the block numbers. With SIMETRIX DC Sweep, obtain the forward and reverse $I-V$ curves of each switch configuration at 150°C, because the temperature has a great effect on voltage drop, and use equation (2)-(3) to calculate the conduction loss.

\[ E_{sw} = \int_0^t P(t) \cdot dt = \int_0^t V(t) \cdot I(t) \cdot dt \]  
\[ V_f = a_1 \cdot I^n(t) + \cdots + a_n \cdot I^l(t) \]  
\[ E_{con} = \int_0^t V_f(t) \cdot I(t) \cdot dt = \int_0^t V_f[I(t)] \cdot I(t) \cdot dt \]
3. Results and discussions

Different configurations for SM bridge arm can indeed bring about a significant losses reduction (shown in Table 2), and the Hys-S can bring about the lowest power loss, around 12% loss reducing than conventional switch.

Table 2. Power loss results in simulation.

|            | Switch         | FWD   | $P_{\text{tot}}$(W) | Percentage |
|------------|----------------|-------|---------------------|------------|
| Conv.      | IGBT          | FRD   | 96                  | 100%       |
| Mixed      | IGBT          | SBD   | 86                  | 90%        |
| Hys-F      | SiC MOS+IGBT  | FRD   | 102                 | 106%       |
| Hys-S      | SiC MOS+IGBT  | SBD   | 84                  | 88%        |

Actually the main part in power loss is the conduction loss due to its low switching frequency of single SM. The loss reduction of mixed switch is mainly due to the replacement of FRD by SiC-SBD, which greatly reduces the $I_{\text{rr}}$ loss. Hys-F’s conduction loss and turn-off loss are slightly reduced, but the total loss is higher since FRD in IGBT is as its main reverse diodes. Both the conduction and $I_{\text{rr}}$ losses of Hys-S have been greatly reduced, becoming the lowest loss category among these four configurations.

To test the effectiveness of the Hys-S switch in switching loss reducing, a double-pulse test platform was built. As shown in figure 5, a signal generator is used to input gate signals with a 1.5μs off-delay of IGBT in lower bridge, and SiC-SBD is used as an anti-parallel diode. The results are compared with conventional switch.

In the experiment at 500V DC link voltage, the current distribution of each switching device under different bridge currents was obtained. Figure 6 shows the turn-off current of each switching device, and the solid and long dashed lines indicate the current waveforms of lower bridge with a 1.5μs turn-
off delay for MOSFET. That is to say, IGBT is turned off at zero voltage, which also saves most of the switching losses. Figure 7 shows the $I_{rr}$ in upper bridge, and $I_{rr}$ overshoots in short dashed and dot-dashed lines are much larger than the other two lines, which can be solved by the Hys-S proposed in this article.

![Figure 6. Comparison of turn-off current.](image1)

![Figure 7. Comparison of $I_{rr}$.](image2)

Figure 6. Comparison of turn-off current.

Figure 7. Comparison of $I_{rr}$.

Figure 8 represents the loss comparison of two switches at different currents. Taking 31A total current as an example, the turn-off loss in lower bridge for Hys-S is reduced by 11.4% compared with conventional switch, and the $I_{rr}$ loss is reduced by 57.6%, and total switching and $I_{rr}$ losses are reduced by 15.3%. Conduction losses can be calculated by the production of conduction current and on-state voltage drop, and these are the main reason for power electronic devices’ losses in MMC system due to its low switching frequency.

![Figure 8. Energy loss comparison.](image3)

Figure 8. Energy loss comparison.

4. Conclusions

In order to reduce the semiconductor power loss in MMC based on an actual operating condition, where the losses caused by conventional switch in SM are very large, a Hys-S switch is proposed in this paper which is composed of SiC-MOSFET, Si-IGBT, and SiC-SBD, reducing its conduction and switching losses. Among the four investigated configurations, there is no benefit when only Si-IGBT exchanged to SiC-MOSFET and Si-IGBT cross-switch because of low switching frequency in MMC and high reverse recovery losses from PiN diode, however, SiC-SBD has great superiority in reducing reverse recovery losses. The proposed switch including SiC-MOSFET and SiC-SBD shows the lowest total power loss, a 12% reduction compared to that of the conventional IGBT and FRD, which benefits the efficiency improvement of the MMC systems. This paper has guiding significance for the semiconductor devices’ selection of MMC SM in the future.
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