Inference Latency Prediction at the Edge

ZHOUJIN LI, University of Southern California, USA
MARCO PAOLIERI, University of Southern California, USA
LEANA GOLUBCHIK, University of Southern California, USA

With the growing workload of inference tasks on mobile devices, state-of-the-art neural architectures (NAs) are typically designed through Neural Architecture Search (NAS) to identify NAs with good tradeoffs between accuracy and efficiency (e.g., latency). Since measuring latency of a huge set of candidate architectures during NAS is not scalable, approaches are needed for predicting end-to-end inference latency on mobile devices. Such predictions are challenging due to hardware heterogeneity, optimizations applied by ML frameworks, and diversity of neural architectures. Motivated by these challenges, in this paper, we first quantitatively assess characteristics of neural architectures and mobile devices that have significant effects on inference latency. Based on this assessment, we propose a latency prediction framework which addresses these challenges by developing operation-wise latency predictors, under a variety of settings and a number hardware devices, with multi-core CPUs and GPUs, achieving high accuracy in end-to-end latency prediction, as shown by our comprehensive evaluations. To illustrate that our approach does not require expensive data collection, we also show that accurate predictions can be achieved on real-world NAs using only small amounts of profiling data.

CCS Concepts:
- General and reference → Performance: Empirical studies;
- Computing methodologies → Neural networks;
- Human-centered computing → Mobile devices.

Additional Key Words and Phrases: neural networks, NAS, latency, prediction, mobile, GPU, CPU

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1 INTRODUCTION

Due to significant breakthroughs in machine learning (ML), inference tasks using neural networks are being deployed to an increasing number of edge devices (e.g., smartphones, smartwatches, tablets), largely for computer vision and natural language tasks. In comparison with powerful cloud servers, edge devices have limited resources, which restricts the choice of deployed neural architectures (NAs).

In such a limited resource setting, state-of-the-art neural architectures [25, 49, 50] are typically designed through Neural Architecture Search (NAS) [64] by searching for an architecture with a good trade-off between accuracy and efficiency. For example, recent works [49, 59] propose to optimize accuracy under constraints on efficiency metrics (e.g., latency) that are measured directly on a target platform. However, neural architectures exhibit distinct performance characteristics across platforms [51], and it is impractical to measure end-to-end latency of every architecture on all possible platforms during model search. As an alternative to direct measurements, existing...
approaches for evaluating the efficiency of a neural architecture can be categorized as those using: (1) Proxy metrics [50, 65] (e.g., FLOPs), which are usually platform-independent and cannot accurately reflect the actual performance due to the diversity of platforms [39, 51]. (2) Lookup tables [7, 11, 56], which are collected for pre-defined building blocks in the search space, but cannot cover every possible configuration in a potentially huge search space and require comprehensive measurements on each platform. (3) Prediction models [2, 8, 12], which broadly rely on machine learning techniques (e.g., MLPs) and have the potential to predict the performance of any configuration in the search space. However, it is difficult to build accurate prediction models for efficiency metrics on mobile devices due to the following challenges.

(1) Hardware heterogeneity: Existing prediction models mainly focus on cloud servers [2, 14, 15, 32] where Nvidia GPUs dominate the market for ML workloads; instead, the heterogeneity of mobile CPUs and GPUs makes performance prediction more difficult. In particular, inference tasks are frequently performed on mobile devices using CPUs [57], due to the support of a broader set of available operations (e.g., Channel Shuffle [63] is currently unavailable on the TensorFlow-Lite GPU Delegate [34]). Modern mobile CPUs typically use the ARM big.LITTLE architecture, which consists of heterogeneous core clusters, e.g., high-performance cores and high-efficiency cores [55]; when an inference task takes advantage of this multi-core architecture, the schedule of threads on different cores has a significant impact on performance (Section 3.1.1). In addition, multi-core speedups on a given device can vary for different neural architectures; for instance, MobileNet (with width multiplier of 0.75) and ResNet18 (with width scale of 0.25) achieve comparable inference latency (28.4 ms and 28.1 ms, respectively) on Pixel 4 with one medium core, but differ by 24.6% with three medium cores (11.8 ms and 14.7 ms, respectively). Therefore, it is necessary to evaluate prediction approaches using heterogeneous hardware resources, in particular on multi-core CPUs; this is not taken into consideration by existing works on latency prediction for mobile CPUs [37, 62].

(2) ML framework optimizations: Modern ML frameworks introduce optimizations that can significantly accelerate inference tasks. For example, operator fusion [42] reduces overhead in the invocation of OpenCL kernels on GPUs; our tests show that disabling OpenCL kernel fusion in TensorFlow Lite (TFLite) [17] can lead to an average 22% performance degradation over 102 real-world NAs on PowerVR GE8320 (Section 3.2.1). Similarly, the choice of algorithms used to implement each operation can considerably affect inference performance; e.g., TFLite uses the faster Winograd [33] algorithm for some (but not all) convolution layers on GPUs. Existing works on latency estimation for mobile GPUs [3, 4] do not consider such optimizations (which are specific to ML frameworks) but predict inference latency only from the architecture of the neural network.

(3) Neural architecture diversity: During the exploration of the search space by NAS algorithms, the properties of neural architectures (e.g., the number of operations and their latency) can vary considerably; in addition, novel architectures are proposed by manual design [25, 39, 63], prompting the definition of new NAS search spaces. Existing ML-based performance prediction models use training and test datasets with very similar neural architectures [2, 3, 48], or with a small set of popular architectures [6, 15, 21]; in contrast, practical applicability of performance prediction to NAS requires accuracy on a large set of diverse neural architectures.

Motivated by the above-stated challenges, in this paper, we first quantitatively assess characteristics of neural architectures and mobile devices that have significant effects on inference latency. Based on this assessment, we develop a framework to predict latency of inference tasks on mobile CPUs and GPUs using machine learning models as well as carry out a comprehensive evaluation study to demonstrate the accuracy of the proposed approach. Our approach predicts inference latency using ML models trained to estimate latency of neural architecture components as “building blocks” of end-to-end latency. A per-component approach provides learning efficiency (i.e., models
can be trained quickly from small datasets), in contrast with complex learning models [2, 12, 14] predicting latency from graphs of tensor operations (including parameters of all operations).

Our prediction framework allows us to address several shortcomings in existing literature. We develop a training dataset that is representative of real-world neural architectures but provides broader coverage of possible neural architectures, leading to better generalizability. In addition, while existing works [37, 62] study the performance of mobile CPUs on a single core, our dataset includes measurements over a broader set of practical scenarios, e.g., choices of CPU cores and use of data representations (floating-point or integer quantization); our prediction models allow NAS approaches to account for realistic scenarios, leading to better estimation of inference latency on mobile devices. Also differently from previous work [62], which builds black-box models to estimate effects of ML framework optimizations, we expose important principles from open-source ML framework, which enables accurate estimation of GPU kernels without deploying candidate neural architectures on actual devices.

Thus, the main contributions of our work are as follows.

- By collecting measurements for 102 state-of-the-art neural architectures from 25 papers on 4 mainstream mobile platforms (or SoCs), based on quantitative evidence, we identify aspects of hardware and ML frameworks which substantially affect the latency of inference tasks on mobile devices. For mobile CPUs, we expose performance characteristics under various settings, including multithreading over ARM heterogeneous core clusters and quantization with lower-bit representations (Section 3.1). On mobile GPUs, we categorize two types of optimization strategies due to ML framework compilation: kernel fusion and kernel selection (Section 3.2). As a representative example, we expose the principles of both strategies in TFLite, and empirically evaluate resulting speedups to highlight their impact on inference latency.

- Based on the results of our performance study, we develop a framework for estimating end-to-end inference latency on mobile devices by composing accurate latency predictions of individual NA components (Section 4.2). To address hardware heterogeneity, we profile execution times of neural architectures under various settings of multi-core and data representations, and train ML models to predict performance under each setting. For ML framework optimizations, we are able to deduce the OpenCL kernels that are selected on mobile GPUs, without the need for deploying and compiling the target neural architecture on the actual hardware (Section 4.1). By conducting one-time training data collection on each device, we are able to utilize learning-based models to accurately predict latency of inference tasks under various settings of mobile CPUs and GPUs, which can be used by existing NAS techniques to evaluate inference latency without access to actual hardware.

- We build a synthetic dataset of 1000 neural architectures sampled from a NAS space covering a majority of configurations for common operations and building blocks (Section 4.3). For each neural architecture, we comprehensively measure latency under 72 scenarios across 4 mainstream mobile platforms, including the combination of multiple cores and the utilization of integer representations after quantization. In addition to accurate latency prediction, this provides insight to (i) NA developers for how to build efficient neural architectures and (ii) mobile developers for how to choose suitable optimizations for running inference tasks.

- To evaluate how our approach addresses the aforementioned challenges, in addition to the default setting of NAS (Section 5.1), we show that our predicting framework also achieves accurate estimations under hardware heterogeneity (Section 5.2), neural architecture diversity (Section 5.3), and ML framework optimizations (Section 5.4). To address the concerns of the cost of training data collection [37], we evaluate accuracy of predictions with limited amounts
of training data, using multiple ML methods (Section 5.5). Our results highlight that, when trained with sufficient data of 1000 synthetic neural architectures, more powerful ML methods can achieve accurate predictions for neural architectures with similar characteristics to the training data (e.g., by using GBDT [13], 2.4% average error when using one large CPU core and 6.3% when using GPUs); with limited training data of only 30 neural architectures, the linear approach of Lasso [52] can generalize well to real-world neural architectures, even when their characteristics differ from training data (e.g., 6.9% average error for CPUs with one large core, and 9.1% for GPUs).

2 BACKGROUND: NEURAL ARCHITECTURES ON MOBILE DEVICES

As illustrated in Fig. 1, the lifecycle of neural architecture development and deployment on mobile devices consists of (1) designing and training a neural network model on cloud servers, and (2) deploying the model on a target mobile device where it is executed, i.e., where inference tasks are performed on CPU cores or GPU.

State-of-the-art neural architectures are developed by both manual design [23, 26, 39] and NAS [25, 46, 49, 50]. Due to scarce computing and memory resources, neural architectures intended for inference tasks on mobile devices are designed not only to maximize prediction accuracy, but also to satisfy performance constraints such as end-to-end latency and memory consumption. To achieve these goals, model quantization [31, 41] is frequently applied: fixed-width integers are used to represent the model parameters and to perform computations with low precision, reducing memory requirements and computation times (as shown in Section 3.1.2).

After the identified neural architecture is trained on cloud servers, it is stored as a model file, which can be distributed to heterogeneous mobile platforms for inference tasks. For instance, in TFLite, a neural architecture is described as a computational graph, where each node represents an operation and each edge represents the flow of intermediate results between operations; the complete computational graph is included in the .tflite model file.

A mobile device can be equipped with multiple hardware accelerators to serve inference tasks (e.g., CPU, GPU, DSP and Edge TPU are available on Pixel 4). To be executed on different hardware, the model is "compiled" to select an optimized CPU implementation or a platform-specific GPU kernel for each operation of the computational graph. Notably, the same operation can be executed using different algorithms on different devices; for example, the TFLite GPU Delegate can select different kernels for convolution operations on Adreno GPUs vs. Mali GPUs (as detailed in Section 3.2.2). In addition, the computational graph can be optimized during model compilation; for instance, two consecutive operations can be “fused” and executed with a single GPU kernel (as detailed in Section 3.2.1). Eventually, a compiled model is executed on the target hardware: on GPUs, kernels...
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Device | Platform | CPU Cores | GPU |
---|---|---|---|
Google Pixel 4 | Snapdragon 855 | Large: 1x Kryo 485 Prime (2.84 GHz) Medium: 3x Kryo 485 Gold (2.32 GHz) Small: 4x Kryo 485 Silver (1.8 GHz) | Adreno 640 |
Xiaomi Mi 8 SE | Snapdragon 710 | Large: 2x Kryo 360 Gold (2.2 GHz) Small: 6x Kryo 360 Silver (1.7 GHz) | Adreno 616 |
Samsung Galaxy S10 | Exynos 9820 | Large: 2x M4 Cheetah (2.73 GHz) Medium: 2x Cortex-A75 (2.31 GHz) Small: 4x Cortex-A55 (1.95 GHz) | Mali G76 |
Samsung Galaxy A03s | Helio P35 | Large: 4x Cortex-A53 (2.3 GHz) Small: 4x Cortex-A53 (1.8 GHz) | PowerVR GE8320 |

Table 1. Mobile Platforms in Our Study

are dispatched to a command queue for execution; on CPUs, operations are executed sequentially, while multithreading is used only to accelerate the execution of individual operations on multiple cores (as detailed in Section 3.1.1).

3 PERFORMANCE CHARACTERISTICS OF INFERENCE ON MOBILE DEVICES

In this section, we present the results of our empirical study on the performance of state-of-the-art neural architectures on mobile platforms; in particular, we analyze thread scheduling and model quantization in multicore mobile CPUs (Section 3.1), and kernel fusion and selection in mobile GPUs (Section 3.2), evaluating their impact on inference latency. The insight gained here will be used in Section 4 to develop our latency prediction framework.

3.1 Performance Characteristics of Mobile CPUs

3.1.1 Effects of Multithreading. Modern mobile platforms typically adopt the ARM big.LITTLE architecture, which allows multiple types of CPU cores to be integrated on the same system; each group of homogeneous cores is operated as a “core cluster” running at the same clock speed. The “big cores” with higher clock speed can handle computationally intensive tasks, while the “LITTLE cores” with lower clock speed can reduce power consumption. Table 1 lists the core clusters of the 4 SoCs in our study, providing a range of mobile device hardware. For example, Snapdragon 855 uses three clock domains for prime, gold and silver core clusters, respectively: tasks with high priority are usually scheduled on prime and gold cores for higher performance, while non-urgent tasks are scheduled on silver cores to reduce energy consumption.

An inference task can be accelerated with multithreading over multiple cores. Fig. 2 uses boxplots to depict end-to-end latency of 102 state-of-the-art neural architectures (details of these neural architectures are reported in Appendix A) on Snapdragon 855, Snapdragon 710, Exynos 9820, and Helio P35 platforms for different multicore configurations; in these experiments, we use a number of threads equal to the number of cores and specify CPU affinity for each thread to schedule on a specific core. In Fig. 2 (and in the rest of the paper) boxplots indicate 1st quartile, median, and 3rd quartile of the data; whiskers extend for 1.5x the interquartile range; points outside of whiskers are denoted as outliers. For clarity of presentation, in Fig. 2 we omit some outliers with substantially higher latency (<4% of data points per configuration); due to lack of space, complete data are reported in Fig. 26 of the Appendix. Counterintuitively, using multiple heterogeneous cores can result in performance degradation: for example, on Snapdragon 855 (Fig. 2a), the combination of a medium core and a small core exhibits worse performance (on average) than a medium core; on Exynos 9820 (Fig. 2c), the combination of a large core and a small core is slower than a large core. After inspecting the source code of TFLite and of its library Ruy for CPU execution [18, 19], we attribute
this performance degradation to: (1) the overhead of multi-threading across different clusters of CPU cores (e.g., large and small cores), and (2) the approach used to distribute work, which is split equally among the number of available threads; with heterogeneous CPU cores, threads assigned to slower cores can become the stragglers.

For multithreading with homogeneous cores in Fig. 2, we observe a sublinear speedup with respect to the number of cores. Fig. 3 shows the speedup of different operation types with respect to the number of homogeneous cores. We observe that convolution, depthwise convolution and fully-connected operations achieve sublinear speedups as the number of threads increases. However, performance improvements on the remaining operations are negligible, due to the lack of support for parallel execution of these operations in the current TFLite implementation.
3.1.2 Effects of Quantization. On mobile devices with limited power and computing resources, neural architectures can be converted into lower-precision representations (e.g., 16-bit floating point or 8-bit integers) to reduce memory utilization and computational demand, without substantial accuracy loss. We focus on the approach of integer-arithmetic-only inference [31] available in TFLite, where both weights and activations are represented as 8-bit integers during inference.

Fig. 4 compares inference latency using an 8-bit integer representation and a floating point representation. Similarly to Fig. 2, we omit outliers (only of a couple of points) for better visualization, and report complete data in Fig. 27 of the Appendix. As can be seen, quantization shows a distinct speedup on various combinations of cores on all devices.

Fig. 5 depicts performance improvement of each type of operation after quantization. On all devices, most operations achieve significant speedup when using 8-bit integers; however, padding and element-wise operations show performance degradation after quantization. For example, the average latency of element-wise operations is increased to 2.55x and 2.60x on Snapdragon 855 and Exynos 9820 respectively. Previous work [31, 41] suggests that this degradation is due to the overhead of matching quantization ranges (i.e., the scale) of all inputs of quantized operations (e.g., element-wise addition).

Insight 2. Quantization can reduce latency and memory utilization of a model, significantly improving the performance of inference tasks on mobile CPUs. However, quantization can cause performance degradation for some operations due to the cost of scaling its inputs.

3.2 Performance Characteristics of Mobile GPUs

3.2.1 Effects of Kernel Fusion. Kernel fusion has been broadly adopted to reduce the overhead of dispatching kernels [62]. We analyzed the implementation of kernel fusion available in TFLite [16],...
which we report in the Appendix (Algorithm C.1); two consecutive operations of the computational graph are fused when (1) the first operation has only one output tensor, (2) the second operation is the only operation in the graph using this output tensor, (3) uses this output tensor as its first input and produces a single output, and (4) has a compatible type.

Fig. 6a illustrates the difference in number of OpenCL kernels observed when kernel fusion is enabled: kernel fusion results in a reduction in the number of kernels of over 45% for these state-of-the-art neural architectures. Fig. 6b shows the performance improvements from kernel fusion on four mobile devices; the outliers (only a couple of data points) are removed to improve visualization. We observe 1.22x speedup of the average end-to-end latency over all the neural architectures on four mobile devices, due to a reduction in the cost of kernel dispatching.
Insight 3. By substantially reducing the number of operation kernels, kernel fusion can improve the performance of inference tasks on mobile GPUs. However, only element-wise operations provide substantial performance improvements; effect on other operations is negligible.

3.2.2 Effects of Kernel Selection. Machine learning frameworks can use different optimized algorithms to implement operations of the computational graph. For example, Algorithm C.2 summarizes the criteria used by TFlite to enable the use of the Winograd algorithm for convolution operations: when the input tensor and kernel size of a convolution operation both satisfy certain criteria (defined by the \texttt{CheckWinograd} function), the kernel of Winograd will be selected for the operation. Fig. 8 shows the performance improvement from using Winograd kernels in state-of-the-art neural architectures; the application of Winograd kernels results in performance improvements up to 1.32x for PowerVR GE8320 and 1.26x for Mali G76.

Notably, kernel selection is hardware-dependent. We observe that none of these neural architectures obtains performance improvements on Adreno 640 or Adreno 616, because the requirements for applying Winograd algorithm on Adreno GPUs are stricter than Mali and PowerVR GPUs in current TFLite implementation. For example, Table 2 presents three convolution operations in ResNet16, which all have only one convolution group, kernel size 3x3 and stride 1. For convolution (1), src_depth and dst_depth fail to satisfy the conditions for Adreno GPUs (Line 15), but meet the requirements for Mali and PowerVR GPUs (Line 19). For convolution (2), total_tiles is too small for Adreno 600-level GPUs (Line 22), but large enough for Mali and PowerVR GPUs (Line 26). Convolution (3) cannot be implemented using the Winograd algorithm in either GPU because of the small total_tiles (Line 26).

Another operation allowing optimized implementations is grouped convolution, which consists of three stages: (1) splitting the input tensor over channel size, (2) performing a convolution on each resulting tensor (i.e., on each group), and (3) concatenating all output tensors. A naive
implementation of grouped convolution uses an independent convolution kernel for each group, and two kernels for the split and concatenation operations. TFLite supports an optimized implementation of grouped_convolution_2d using only one kernel. Fig. 9 illustrates the performance improvement of the optimized grouped_convolution_2d kernel over a naive implementation; we observe substantial improvements, e.g., 2.96x speedup for RegNetX004 on PowerVR GE8320.

**Insight 4.** Framework-dependent optimizations have significant impact on the performance of inference tasks. In TFLite, convolution operations with certain shapes of input tensors and kernel sizes can use the Winograd algorithm to accelerate the execution; grouped convolution can make use of an optimized implementation to achieve considerable performance improvement. Therefore, for an accurate performance prediction model, it is important to understand which kernels are executed during inference.

### 4 METHODOLOGY

Given a model file (e.g., a .tflite file of TFLite) generated on a cloud server (e.g., during NAS), we aim at accurately predicting the end-to-end latency over different mobile CPUs and GPUs, without deploying the neural architecture on the actual mobile devices; this framework includes the following steps: (1) from an input model file, we first extract the information of the operations on the computational graph, which are the execution units on mobile CPUs; (2) for mobile GPUs, we deduce (without using the mobile device) the actual kernels executed after kernel fusion and kernel selection (Section 4.1); (3) for each operation type (e.g., convolution, fully-connected), we use ML models to predict its inference latency on the target device from the operation parameters (e.g., input shape, number of channels, Section 4.2); (4) end-to-end latency is estimated as the sum of predicted operation latencies plus the additional latency due to ML framework overhead. To train the ML models and to evaluate our approach, we collect latency measurements on a synthetic dataset including 1000 neural architectures from a NAS space (Section 4.3), which we will make publicly available to help further research on mobile performance.

#### 4.1 Kernel Deduction

From the model file, we are able to extract the computational graph of the target neural architecture, which includes information on all operations as well as the data flow between operations. As discussed in Section 3.1.1, these operations are sequentially executed on mobile CPUs and multiple threads can collaborate on the computation of each operation. Hence, for each type of operation and each CPU core combination, we train a machine learning model to predict inference latency.

However, when using mobile GPUs, operations of the computational graph can be fused (Section 3.2.1) or implemented with optimized algorithms (Section 3.2.2); since our measurements
illustrate that kernel fusion and kernel selection have substantial effects on performance, identifying which kernels are actually executed for a given computational graph and target device is critical to obtaining accurate latency predictions. To avoid the cost of deploying the neural architectures on the physical device (which is impractical for NAS with a huge number of candidate neural architectures), we deduce the kernels executed on a device by simulating the process of kernel fusion and kernel selection, according the principles elicited from the implementation of TFLite. Specifically, to predict latency on mobile GPUs, we first fuse kernels according to the rules presented in Section 3.2.1; then, we use the rules presented in Section 3.2.2 to select a kernel among {Conv2D, Winograd, GroupedConv2D} based on the parameters of each convolution operation (e.g., input size, output size, kernel size) and the target device.

4.2 Prediction Models

For each neural architecture, after obtaining the computational graph (and applying kernel fusion/selection estimation for mobile GPUs), we predict the latency of each operation from its configuration parameters. We use parameters that define the shape of an operation augmented with features associated with both memory access cost (e.g., size of input/output data, parameters) and computational cost (e.g., FLOPs). Feature space details are given in the Appendix in Table 3.

Formally, given feature vectors \( x_i \in \mathcal{X} \) of an operation of the computational graph and corresponding latencies \( y_i \in \mathcal{Y} \) measured on a specific device, for \( i = 1 \ldots, N \), where \( N \) is the size of the training dataset\(^2\), our goal is to train a prediction model \( f \) minimizing the mean absolute percentage error (MAPE) \( L_{MAPE} = \frac{1}{N} \sum_{i=1}^{N} \left| \frac{f(x_i) - y_i}{y_i} \right| \). Since input features can be of different magnitudes, we standardize each feature \( j \) based on its mean \( \mu_j = (\sum_{i=1}^{N} x_{i,j}) / N \) and standard deviation \( \sigma_j = \sqrt{\frac{\sum_{i=1}^{N} (x_{i,j} - \mu_j)^2}{N}} \) in the training set, i.e., \( \hat{x}_{i,j} = (x_{i,j} - \mu_j) / \sigma_j \) for all \( 1 \leq i \leq N \), and we minimize the mean square percentage error based on standardized feature vectors \( \hat{x}_i \) and latencies \( y_i \), \( \forall 1 \leq i \leq N \): \( f^* = \min_f \frac{1}{N} \sum_{i=1}^{N} \left| \frac{f(\hat{x}_i) - y_i}{y_i} \right|^2 \). To develop a prediction model, we consider the following representative ML approaches [40] adopted in the literature [3, 4, 15, 32, 62]; as will be shown in our evaluations (Section 5.4), properly accounting for characteristics we identified as significant to end-to-end latency (Section 3.2), results in similar prediction accuracy across these ML approaches.

\[ Lasso. \] We first consider a linear model \( f(x) = w^T x \) and estimate the optimal weights \( w^* \) as

\[
w^* = \min_w \frac{1}{N} \sum_{i=1}^{N} \left| w^T \hat{x}_i - y_i \right|^2 + \alpha \|w\|_1 \quad \text{subject to} \; w \geq 0.
\]

An L1 regularization term with hyperparameter \( \alpha \) is included to control model complexity and to favor a sparse solution. We use grid search in \([10^{-5}, 10^2]\) to find the best \( \alpha \). Since each input feature \( \hat{x}_{i,j} \) is positively correlated with latency, we constrain weights \( w_{i,j} \) to be nonnegative (Eq. (1)).

\[ Random \; Forest (RF). \] An RF model includes multiple decision trees to reduce overfitting of a single decision tree. We tune hyperparameters including the number of decision trees (1 to 10) and the minimum number of samples to split an internal node (2 to 50) using 5-fold cross-validation.

\[ Gradient-Boosted \; Decision \; Trees \; (GBDT). \] GBDT generates decision trees with gradient boosting on multiple stages. We tune hyperparameters including the number of gradient boosting stages (1 to 200) and the number of examples required to split a node (2 to 7) using 5-fold cross-validation.

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\(^2\)Technically, each operation has a different training set size, but for clarity of presentation, we use \( N \) as a generic size.
Fig. 10. Difference between End-to-end Latency and Sum of Operation-wise/Kernel-wise Latency for State-of-the-art Neural Architectures

(a) CPUs
(b) GPUs

Fig. 11. Latency Breakdown of State-of-the-art Neural Architectures

(a) Snapdragon 855 (Adreno 640)
(b) Exynos 9820 (Mali G76)

Multi-Layer Perceptron (MLP). An MLP consists of multiple layers of fully-connected layers. We tune the hyperparameters for the number of layers from 1 to 6 and the number of neurons in each layer from \{64, 128, 256, 512\}. Similarly to previous work [15], we use ReLU activations after each layer and the Adam optimizer with learning rate from \{5 \times 10^{-3}, 5 \times 10^{-4}, 5 \times 10^{-5}\}, and weight decay from \{10^{-3}, 10^{-4}, 10^{-5}\}. We use 20% of training data as the validation set, and stop training after no improvement on the validation error over 50 epochs.

After predicting execution latency of each operation on CPU cores or on the GPU, we account for additional latency due to overhead and data transfers in TFLite; as shown in Fig. 10, the sum of the latencies measured for all operations is consistently lower than the measured end-to-end latency, especially on GPUs (Fig. 10b). Since the difference fluctuates around a constant value for all neural architectures on a specific GPU, we use the average difference between end-to-end latencies and operation-wise latencies in the training dataset to estimate this additional latency $T_{\text{overhead}}$.

Formally, for a neural architecture with the set of operations $C$, we predict end-to-end latency as $T_{\text{overhead}} + \sum_{c \in C} f_{c}^{*}(\hat{x}_{c})$ where $f_{c}^{*}$ is the latency predictor trained from measurements of operations with the same type as $c$.

4.3 Synthetic Dataset

Next, we present our synthetic dataset consisting of neural architectures from a NAS space, which covers a broad range of operations and building blocks in recent work. We first introduce the technique used to profile each operation, and then we describe the design of the NAS space.

4.3.1 Profiling Kernel Latency. For mobile CPUs, we utilize TFLite Model Benchmark Tool [20] to measure the latency of each operation. However, the tool currently provides no official interface to profile kernels on mobile GPUs. As a solution, we record the timestamps of each OpenCL kernel by enabling profiling information collection at the OpenCL command queue. To reduce the overhead of recording timestamps, we dispatch the same kernel multiple times (specifically, 256) and record only the timestamps for the first and last events, thus amortizing profiling overhead.
Fig. 12. Design of the NAS Space for Synthetic Dataset

Fig. 11 display the average latency breakdown for 102 state-of-the-art neural architectures. As can be seen, convolution and depthwise convolution operations account for a significant proportion of the end-to-end latency. In addition, we observe that, for the same set of neural architectures in our dataset, Winograd kernels are applied on Mali G76 but not on Adreno 640, because the selection of kernels is dependent on the hardware platform, as discussed in Section 3.2.2.

4.3.2 NAS Space for Sampling Neural Architectures. Fig. 11 highlights the importance of studying the performance of convolution and depthwise convolution operations. Consequently, we design a search space to effectively sample various configurations of these operations for the purpose of understanding their performance characteristics. As illustrated in Fig. 12, synthetic neural architectures of our NAS space use a sequence of 9 blocks halving input width/height after blocks 1, 3, 5, 7, 9; then a convolution with kernel size 1x1 and fully-connected layer produce a output vector of 1000 dimension. The type and parameters of each building block are selected uniformly at random as:

1. A convolution layer (with kernel size 3x3, 5x5 or 7x7, optionally group size $k$, $1 \leq k \leq 16$).
2. Depthwise separable convolution [26] (with kernel size 3x3, 5x5 or 7x7).
3. Linear bottleneck [46] (with kernel size 3x3, 5x5 or 7x7, expansion rate 1, 3 or 6, optionally including Squeeze-and-Excite as [25]).
4. Average or maximum pooling layer (with pooling size 1x1 or 3x3).
5. A split layer (with number of splits 2, 3 or 4), followed by element-wise operations performed on each output tensor, and a concatenation layer which merges all output tensors.

Due to the limited memory and computing resources on mobile devices, we sample the output channel sizes of these building blocks (identified as $C_1$ to $C_9$) with the following constraints: 

- $\{C_1, ..., C_5\}$ are uniformly sampled from $[8, 80]$;
- $\{C_6, ..., C_9\}$ are uniformly sampled from $[80, 400]$; $C_{10}$ is uniformly sampled from $[1200, 1800]$.

We adopt a synthetic dataset including 1000 neural architectures sampled from this NAS space. For each neural architecture, we collect training measurements on 4 mobile platforms in Table 1, for a total of 72 scenarios, covering (1) combinations of homogeneous or heterogeneous cores, (2) 32-bit floating point and 8-bit integer representations, and (3) mobile GPUs from different manufacturers. Fig. 13 illustrate the latency breakdown for neural architectures in our synthetic dataset; the latency distribution over different operations is similar to state-of-the-art neural architectures in Fig. 11.

5 RESULTS

This section presents a comprehensive evaluation of our latency prediction framework across a broad range of scenarios: first, we present results on the default setting of NAS (Section 5.1), and then we evaluate the impact of hardware heterogeneity (Section 5.2), neural architecture diversity (Section 5.3), and ML framework optimizations (Section 5.4). In addition, to address a common criticism of cost of training data collection, we present results using a small number of training examples and a simple linear model (Section 5.5).

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$^3$When presenting the percentage of end-to-end latency, we include the results of NAs that may not have all type of operations; e.g., depthwise convolution operations only appear in 58 NAs, so its median across 102 NAs is zero.
5.1 Default Setting: Evaluation on Neural Architectures from NAS Space

We first test our framework in a common scenario of applying our latency prediction model during NAS: we sample test neural architectures (the candidate architectures during NAS) and the training neural architectures (the profiling architectures to train our latency prediction model) uniformly at random from the same search space (Section 4.3.2). These sampled neural architectures constitute our synthetic dataset of 1000 samples. Here, 900 of these are used for training and 100 for testing.

Fig. 14 presents average (across 4 platforms) MAPE under different ML approaches when predicting end-to-end latency, as well as latency of the 4 operation types accounting for most of end-to-end latency (convolution, depthwise convolution, mean, pooling); due to lack of space, MAPE of each platform is reported in Table 5 of the Appendix. Based on the latency breakdown of synthetic neural architectures on CPUs and GPUs (Fig. 13), convolution operations typically account for the largest proportion of end-to-end latency; consequently, prediction error of convolution dominates the error of end-to-end latency prediction for all four ML approaches on both CPUs and GPUs. For example, Lasso has a large MAPE (60.9%) on mean operations on CPU, while its MAPE for end-to-end latency is only 11.7%, because, as shown in Fig. 14a, 75% of mean operations contribute to less than 4.9% of the end-to-end latency (on the platforms in Fig. 13).

As can be seen, in our default setting, all nonlinear ML approaches (RF, GDBT, MLP) achieve comparable accuracy on end-to-end latency predictions, with average MAPE across four platforms below 3.2% for CPU predictions and below 6.7% for GPU predictions; Lasso achieves less accurate predictions (11.7% on CPUs and 11.0% on GPUs), because its linear model cannot represent nonlinear relationships between latency and operation features, as identified by previous work [51, 62].

5.2 Case Study: Hardware Heterogeneity

Next, we evaluate our prediction framework under hardware heterogeneity, including scenarios with different CPU core combinations and with both floating-point and integer representations. We select GBDT as a representative ML approach in this section, since it shows comparable or slightly better predictions than RF and MLP in the case of a large CPU core (Fig. 14a).

Fig. 15 illustrates GBDT predictions of end-to-end latency for various core combinations; for clarity of presentation, we omit some outliers (<9% data points for 1 large and 2 medium cores of
Fig. 15. GBDT Predictions of End-to-end Latency using Multiple CPU Cores (Synthetic Neural Architectures)

Fig. 16. Predictions of GBDT on GPUs (Synthetic Neural Architectures)

Exynos 9820, and <4% data points for all other configurations), and report plots with all data points in the Appendix (Fig. 30). We observe that an increasing number of homogeneous cores typically leads to higher prediction errors. Using more cores can result in larger measurement variance, due to background jobs running on mobile devices (e.g., camera, sensors, and networking services); measurement variance can impair the quality of profiling results and thus affect prediction accuracy. For example, from the results on Snapdragon 710 shown in Fig. 15d, the MAPE on 6 small cores (5.2% for floating-point and 6.4% for integer quantization) is significantly higher than on 1 small core (2.0% and 3.2%, respectively), due to the substantial interference of background jobs when an inference task attempts to make use of all the efficient cores on the device. (Additional supporting data is included in Fig. 32 in the Appendix.) Overall, GBDT achieves accurate predictions across all platforms: the worst MAPE for homogeneous cores is 10.5% on Exynos 9820, 5.8% on Snapdragon 855, 6.0% on Helio P35, and 6.4% on Snapdragon 710.

Note that using heterogeneous cores results in even higher variability of latency measurements due to inter-cluster communication [55]. In addition, as explained in Section 3.1.1, operations without multithreading implementations can be scheduled on arbitrary cores, complicating prediction accuracy; for example, when using 1 large and 1 medium core on Snapdragon 855, prediction errors (MAPEs of 3.9% for floating-point and 5.5% for integer quantization) are higher with respect to using 2 medium cores (3.2% and 3.9%, respectively).

Fig. 16 presents predictions of GBDT on multiple GPUs. For convolution operations, we split the results of Conv2D and Winograd kernels in Fig. 16a because separate latency predictors are trained for each kernel; no Winograd kernel is used on Adreno 640 and 616 due to the rules of
5.3 Case Study: Neural Architecture Diversity

Next, we evaluate our framework under diverse neural architectures: we consider a scenario where training data include only a small number of neural architectures sampled at the early stages of NAS, while test data are high-accuracy neural architectures generated at the end of NAS. In our evaluation, we use 1000 synthetic neural architectures as training data and 102 real-world neural architectures (from existing literature) as test data. The two sets of neural architectures have different distributions (i.e., we introduce a dataset shift): we observe that the latency of convolution operations in real-world neural architectures is generally lower than in synthetic neural architectures. Fig. 17a shows percentage of end-to-end latency attributed to convolution operations (split by range) on Helio P35 (with a single large core): convolutions greater than 500 ms dominate end-to-end latency in our synthetic neural architectures, while faster convolutions are more important in real-world neural architectures.

Fig. 18a shows the average MAPE across four devices for the real-world neural architectures on CPUs. For most ML approaches trained on synthetic neural architectures, prediction errors are higher for real-world neural architectures than synthetic neural architectures (Fig. 14), which are generated from the same distribution as the training data. The only exception is Lasso, which has better performance on real-world neural architectures, achieving the lowest end-to-end MAPE on CPUs (5.7%). We attribute this anomaly to the better accuracy of Lasso predictions on fast operations (< 500 ms) due to higher weights assigned to faster operations (in Eq. (1)), which we observe in both synthetic and real-world architectures (Fig. 17b); since real-world architectures include a larger proportion of fast operations, average accuracy is better on this test set.

Fig. 18b presents predictions on mobile GPUs. We observe that, for some small real-world neural architectures, the overhead of TFLite is significant. Since the overhead has high runtime variability (in particular, on PowerVR GE8320 and Mali G76), it can affect the accuracy of end-to-end latency predictions, especially for neural architectures with low latency, such as MobileNets.
5.4 Case Study: ML Framework Optimizations

Next, we illustrate the improvements of GPU predictions resulting from accounting for ML framework optimizations such as kernel fusion and kernel selection.

Kernel Fusion. In Section 3.2.1, we show that kernel fusion considerably reduces the number of kernels and leads to improvements in end-to-end latency. Fig. 19a shows that, after applying our algorithm (Algorithm C.1 detailed in the Appendix) for estimating which kernels will be fused by TFLite (Section 3.2.1), we obtain a number of kernels close to actual measurements collected on 102 real-world neural architectures. Figs. 19b and 19c illustrate that we obtain substantial error reduction in end-to-end latency prediction with respect to ML models which do not consider kernel fusion (labeled as “w/o Fusion”).

Kernel Selection. As introduced in Section 3.2.2, a convolution operation in the computational graph can be evaluated by TFLite using different kernel implementations compatible with the target device and convolution parameters. We deduce the actual kernels selected by TFLite for convolution operations (specifically, Conv2D and Winograd) and train separate predictors for each (since they have different performance characteristics). Fig. 20a shows the considerable error reduction achieved by accounting for kernel selection on PowerVR GE8320, for real-world neural architectures that support Winograd kernels; Fig. 20b confirms that this reduction is due to more accurate predictions of the latency of Winograd kernels.

5.5 Case Study: Limited Training Data

The high cost of collecting sufficient training data is a common criticism of ML approaches to predict latency of neural architectures during NAS [37]. In this section, we study the effects of training set size on different ML approaches, illustrating the benefits of a simple model when training data is limited.

5.5.1 Comparison of ML Approaches. Figs. 21 and 22 show prediction errors of different ML approaches for varying training set sizes $N_{Train}$, on synthetic neural architectures (presented in
Section 5.1) and real-world neural architectures (presented in Section 5.3), respectively (errors are average MAPE across 4 platforms; MAPEs for each platform are reported in Tables 4 and 5 in the Appendix). Predictions of Lasso are less sensitive to the size of training data, while other more complex approaches achieve lower error when the training set size is increased from 30 to 900. Notably, MLP achieves lower prediction errors with a smaller training set of size 30. This is due to severe prediction errors on concatenation/split operations: on Pixel 4 (one large CPU core), MAPEs on concatenation/split operations are 56.7%, 1400.4% and 1068.7%, after training on 30, 100 and 900 neural architectures, respectively; due to lack of space, more detailed data is in the Appendix (Fig. 33). This anomaly is due to the very small amount of training data (only 5, 25 and 312 concatenation/split operations from training data of 30, 100 and 900 neural architectures, respectively). Instead, for convolution operations we have sufficient data and the prediction errors are 7.8%, 5.1% and 4.6% with training set of size 30, 100 and 900, respectively, on the same platform.

Notably, for real-world neural architectures, using only 30 training examples, Lasso considerably outperforms other ML approaches on CPUs with a large core (Fig. 22a), with the average MAPE of 6.9% across four platforms. As pointed out by prior work [37], the cost of profiling only 30 neural architectures on each target device is negligible compared to the time-consuming process of NAS.

5.5.2 Predictions of Lasso on Limited Training Data. Next, we thoroughly evaluate the predictions of Lasso with limited training set size (i.e., 30 neural architectures) on real-world neural architectures, across a broad range of scenarios with hardware heterogeneity.

Fig. 23 displays the predictions of Lasso on real-world neural architectures, across various combinations of cores and data representations; for clarity of presentation, we omit some outliers (<4% data points per configuration), and report plots with all data points in the Appendix (Fig. 31). Generally, the trend of prediction errors for homogeneous and heterogeneous clusters are similar to the results in Fig. 15. The maximum MAPE for combinations of homogeneous cores is 22.9% on Exynos 9820, 13.5% on Snapdragon 855, 9.6% on Helio P35, and 10.9% on Snapdragon 710. We believe the large prediction errors on Exynos 9820 are due to the variance of measurements collected with many small efficient cores, which can affect the quality of training data for this limited dataset. By adding more training data, MAPEs can be reduced to less than 14.8%.
Most existing work aims at latency predictions of training or inference tasks on cloud GPUs \cite{2,14,15,21,32} or edge GPUs \cite{3,4}, where Nvidia GPUs dominate the market for ML workloads. However, the heterogeneity of mobile platforms makes performance prediction more difficult, particularly when using heterogeneous cores. Our paper studies multiple mainstream hardware heterogeneity.

**6 RELATED WORK**

**Hardware heterogeneity.** Most existing work aims at latency predictions of training or inference tasks on cloud GPUs \cite{2,14,15,21,32} or edge GPUs \cite{3,4}, where Nvidia GPUs dominate the market for ML workloads. However, the heterogeneity of mobile platforms makes performance prediction more difficult, particularly when using heterogeneous cores. Our paper studies multiple mainstream

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**Inference Latency Prediction at the Edge**

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mobile devices from different manufacturers, and tackles hardware heterogeneity across these platforms. Recent works [8, 37, 62] focus on performance predictions of mobile CPUs, but only limited to a single core with floating-point computations. Instead, our work evaluates inference latency of mobile CPUs across a broad range of realistic scenarios, including the utilization of multiple heterogeneous CPU cores, and both floating point and integer data representations.

**ML Framework Optimizations.** The majority of existing work [8, 15, 21, 32] proposes to predict latency based on the features extracted from neural architectures and hardware, but neglects the effects of ML framework optimizations. As identified by our results, accounting for these optimizations results in significant improvements of the predictions for real-world neural architectures across multiple ML approaches. Since ML framework optimizations cannot be analyzed on Nvidia cloud and edge GPUs (cuDNN is not open-source [10]), recent work [62] proposes a black-box approach to learn their policies (i.e., the algorithms for kernel fusion). In contrast, on mobile platforms, ML frameworks (e.g., TFLite) use open-source algorithms and OpenCL kernels to support a broad range of heterogeneous GPUs; we highlight their optimizations, accurately inferring the actual kernels used after compilation without deploying and compiling NN models on actual devices.

**Prediction Approaches.** Existing works [2, 12, 14] adopt ML approaches to predict end-to-end latency of neural architectures by encoding the entire neural architecture as a single vector of input features; this approach, however, requires complicated ML techniques as well as large amounts of training data. In contrast, we make latency predictions for each component of the neural architecture, allowing simple ML approaches that require less training data and are easier to interpret (e.g., in the case of Lasso) for understanding and development. Similarly to our work, component-wise approaches are used by [8, 62] for latency prediction on mobile devices, but only limited to a single core for CPUs; ML framework optimizations are considered only by [62] but with a black-box approach. Analytical performance models also exist in the literature, accounting for the computational cost of operations [43] and memory access traffic of GEMM-based convolution [36, 38], but these works only target Nvidia cloud GPUs and their models do not account for the diverse hardware accelerators of mobile platforms, nor for optimizations applied by ML frameworks.

7 CONCLUSIONS

Using measurements collected on 4 mobile devices for a number of neural architectures (1000 synthetic NAS architectures and 102 real-world architectures), we showed the impact of different factors on inference latency, including optimizations applied by ML frameworks for mobile GPUs (kernel fusion and kernel selection), scheduling over heterogeneous subsets of CPU cores and integer representations after quantization, often neglected by related work. Based on this experimental evaluation, we proposed an approach to estimate end-to-end inference latency by training ML models to predict latency of each component type of neural architectures. Our approach can accurately predict latency of novel neural architectures on a given device using limited profiling data (e.g., from 30 architectures); notably, we achieve good accuracy also when the test dataset has different characteristics from training data, a common scenario in NAS. In future work, we plan to extend our evaluation and prediction approach to other efficiency metrics (e.g., power consumption) and to different classes of specialized hardware accelerators for inference tasks (e.g., Apple Neural Engine).

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A DETAILS OF THE REAL-WORLD NEURAL ARCHITECTURES

In this appendix, we include details of the 102 state-of-the-art neural architectures used in our evaluation. Due to the limited resources available on mobile devices, we restricted our selection to neural architectures with up to 18 million parameters, and in particular to the architectures proposed (by manual design or NAS) in the following 25 articles: BagNet [5], BN-Inception [30], DenseNet [28], DiracNetV2 [61], DLA [60], EfficientNet [50], FBNNet [56], FD-MobileNet [44], GhostNet [22], HarDNet [9], HRNet [53], MnasNet [49], MobileNet [26], MobileNetV2 [46], MobileNetV3 [25], PeleeNet [54], PreResNet [24], ProxylessNAS [8], RegNet [45], ResNet [23], ResNeXt [58], SE-ResNet/SE-PreResNet [27], SPNASNet [47], SqueezeNet/SqueezeResNet [29], VoVNet [35].

The TensorFlow implementations of these neural architectures are in [1], which also provides pre-trained parameters as well as the Top-1 and Top-5 test errors on the ImageNet-1K dataset. For each architecture, we first generated a TensorFlow model and then converted it to a .tflite model file (using either floating-point or 8-bit integers) that can be compiled for each mobile platform.

Fig. 25 illustrates the range of model sizes and end-to-end latencies of these real-world neural architectures (on Adreno 640). Table 3 presents a summary of the operations that can be found in these architectures; for each operation, we provide the list of parameters used as input features to train our latency predictors.

| Operation / Kernel   | Features                                                                 |
|----------------------|--------------------------------------------------------------------------|
| Conv2D, DepthwiseConv2D | Input height (width), input channel, output height (width), stride, kernel height (width), filters, input size, output size, kernel size, FLOPs |
| GroupedConv2D        | Input height (width), input channel, output height (width), stride, kernel height (width), filters, input size, output size, kernel size, group number, FLOPs |
| FullyConnected       | Input channel, filters, parameter size, FLOPs                            |
| Mean                 | Input height (width), input channel, kernel height (width), input size, FLOPs |
| Concat, Split        | Input height (width), input channel, kernel height (width), output channel, input size, output size |
| Pooling              | Input height (width), input channel, input height (width), stride, kernel height (width), input size, output size, FLOPs |
| Padding              | Input height (width), input channel, output height (width), padding size, output size |
| Element-wise         | Input height (width), input channel, input size                            |

Table 3. Feature Space for Each Category of Operations

B SUPPLEMENTARY DATA

In this appendix, we include supplementary data from our measurements and prediction results. This data is provided here for completeness, e.g., to include the full set of outliers that were omitted.
in some of the figures of the main text due to lack of space and for clarity of presentation. Fig. 26 depicts end-to-end latency of state-of-the-art neural architectures on 4 platforms for different multi-core configurations, including the outliers omitted in Fig. 2 for clarity of presentation (Section 3.1.1). Fig. 27 depicts the speedup from quantization, including the small set of outliers omitted in Fig. 4.
Fig. 29. Effects of Kernel Fusion on Operation-wise Latency

Tables 4 and 5 report the complete MAPEs of end-to-end latency predictions on each hardware platform, for synthetic and real-world neural architectures, respectively, across different ML approaches, with varying training set sizes. This detailed data corresponds to the results in Figs. 21 and 22 in the main text where these errors were averaged across hardware platforms. For predictions on different CPU core combinations and with both floating-point and integer representations, Fig. 30 shows the end-to-end latency predictions of GBDT for synthetic neural architectures on various core combinations, including the small set of outliers omitted in Fig. 15 (Section 5.2); Fig. 31 presents the end-to-end latency predictions of Lasso for real-world neural architectures on various core combinations, including the small set of outliers omitted in Fig. 23 (Section 5.5.2). Fig. 32 depicts the coefficient of variation with multi-core on different platforms, to illustrate larger measurement variance when using multiple cores (Section 5.2). Fig. 33 shows the prediction errors of MLP with different training set sizes, to support the explanation of the lower prediction errors of MLP with a smaller training set of size 30 (Section 5.5.1).

C DETAILS OF KERNEL FUSION AND KERNEL SELECTION IN TFLITE

Algorithm C.1 presents the implementation details of kernel fusion in TFLite: two operations of the computational graph are fused when (1) the first operation has only one output tensor (Line 5), (2)
| Approach | Training Size | Snapdragon 855 | Exynos 9820 | Snapdragon 710 | Helio P35 |
|----------|---------------|----------------|-------------|----------------|-----------|
|          |               | CPU       | GPU       | CPU       | GPU       | CPU       | GPU       |
| Lasso    | 30            | 12.84%    | 17.95%    | 9.08%     | 10.29%    | 8.85%     | 14.15%    |
|          | 100           | 12.93%    | 18.71%    | 8.87%     | 10.23%    | 8.72%     | 14.46%    |
|          | 900           | 13.26%    | 16.36%    | 8.90%     | 9.63%     | 9.33%     | 12.67%    |
| RF       | 30            | 10.71%    | 13.68%    | 13.52%    | 9.99%     | 11.83%    | 12.97%    |
|          | 100           | 6.20%     | 9.43%     | 4.90%     | 8.58%     | 6.13%     | 11.47%    |
|          | 900           | 2.83%     | 7.33%     | 2.82%     | 8.34%     | 2.29%     | 8.30%     |
| GBDT     | 30            | 7.91%     | 12.52%    | 7.76%     | 9.59%     | 7.10%     | 15.97%    |
|          | 100           | 3.97%     | 9.77%     | 4.36%     | 8.59%     | 4.73%     | 12.29%    |
|          | 900           | 2.12%     | 7.60%     | 1.92%     | 8.41%     | 2.01%     | 6.56%     |
| MLP      | 30            | 9.11%     | 10.02%    | 7.94%     | 8.55%     | 8.21%     | 10.12%    |
|          | 100           | 4.03%     | 9.17%     | 3.84%     | 9.01%     | 3.07%     | 9.28%     |
|          | 900           | 2.30%     | 6.37%     | 2.44%     | 8.19%     | 2.03%     | 6.35%     |

Table 4. End-to-end Predictions on Synthetic Neural Architectures (CPU Stands For a Large Core)

Fig. 31. Predictions of Lasso on End-to-end Latency with Multiple CPU Cores (Real-world Neural Architectures)

the second operation is the only operation in the graph using this output tensor (Line 14), (3) the second operation uses this output tensor as its first input and produces a single output (Line 21), and (4) the next operation has a compatible type (Line 23).

Algorithm C.2 summarizes the criteria used by TFlite to enable the use of the Winograd algorithm for convolution operations: when the input tensor and kernel size of a convolution operation both...
| Approach | Training Size | Snapdragon 855 | Exynos 9820 | Snapdragon 710 | Helio P35 |
|----------|---------------|----------------|-------------|----------------|-----------|
|          |               | CPU  | GPU   | CPU  | GPU   | CPU  | GPU   | CPU  | GPU   | CPU  | GPU   | CPU  | GPU   |
| Lasso    | 30            | 9.77% | 12.04% | 5.83% | 12.68% | 6.40% | 4.78% | 5.51% | 6.79% |
|          | 100           | 8.23% | 14.41% | 4.85% | 11.77% | 7.08% | 5.21% | 4.87% | 6.51% |
|          | 900           | 7.29% | 12.10% | 5.24% | 12.28% | 5.27% | 4.59% | 4.65% | 6.06% |
| RF       | 30            | 14.79% | 14.77% | 20.15% | 13.23% | 14.37% | 7.99% | 18.86% | 6.81% |
|          | 100           | 11.67% | 9.94% | 10.85% | 11.24% | 9.10% | 5.72% | 10.26% | 7.19% |
|          | 900           | 7.43% | 7.24% | 8.01% | 11.39% | 5.02% | 5.60% | 5.71% | 6.01% |
| GBDT     | 30            | 12.20% | 12.13% | 16.57% | 12.50% | 11.92% | 9.03% | 16.11% | 6.92% |
|          | 100           | 12.32% | 7.83% | 10.28% | 12.32% | 7.38% | 5.24% | 10.19% | 6.44% |
|          | 900           | 6.38% | 6.68% | 7.86% | 11.87% | 4.79% | 4.15% | 4.80% | 5.86% |
| MLP      | 30            | 14.87% | 7.79% | 13.18% | 9.94% | 11.35% | 8.52% | 13.01% | 7.03% |
|          | 100           | 18.31% | 9.05% | 16.61% | 10.51% | 12.35% | 10.37% | 12.25% | 7.91% |
|          | 900           | 14.48% | 7.59% | 14.23% | 11.06% | 16.59% | 11.06% | 10.22% | 7.08% |

Table 5. End-to-end Predictions on Real-world Neural Architectures (CPU Stands For a Large Core)

Fig. 32. Coefficient of Variance for 100 Test Synthetic Neural Architectures

satisfy certain hardware-dependent criteria (i.e., CheckWinograd), the kernel of Winograd is selected for the operation.
Algorithm C.1. Kernel Fusion in TFLite GPU Delegate

Mergenodes(nodes)
1 read	ensors = []
2 for cur_node in nodes
3 for dst	ensor in cur_node.dst_tensors
4 ready	ensors.insert(dst	ensor)
5 if cur_node.dst	ensors.size() != 1
6 continue
7 candidate_nodes = []
8 candidate	ensor_index = 0
9 for next_node in nodes
10 for k = 0 to next_node.src	ensors.size() - 1
11 if next_node.src	ensors[k] == cur_node.dst	ensors[0]
12 candidate	ensor_index = k
13 candidate_nodes.insert(next_node)
14 if candidate	ensors.size() != 1 or candidate	ensor_index != 0
15 continue
16 next_node = candidate_nodes[0]
17 if next_node.src	ensors[0] ∈ ready	ensors and isLinkable(next_node)
18 Merge(cur_node, next_node)
19 nodes.remove(cur_node)
20 return nodes

IsLinkable(node)
21 if node.output	ensors.size() != 1
22 return False
23 if node.type ∈ [ACTIVATION, COPY, ADD, SUB, MUL, DIV, EXP, LOG, SQRT, SQUARE, ABS, NEG, POW, EQUAL, GREATER, LESS, MAXIMUM, MINIMUM]
24 return True
25 return False

Fig. 33. Predictions of MLP on Snapdragon 855 CPU (One Large Core)
Algorithm C.2. Kernel Selection for Convolution Operations in TFLite GPU Delegate

```
SELECTCONV2DKERNEL(gpu_info, op_info)
1   If CheckGroupedConv2D(gpu_info, op_info)
2     return Kernel(GroupedConv2D, gpu_info, op_info)
3   Else if CheckWinograd(gpu_info, op_info)
4     return Kernel(Winograd, gpu_info, op_info)
5   Else return Kernel(Conv2D, gpu_info, op_info)

CHECKGROUPEDCONV2D(gpu_info, op_info)
6   src_group_size = op_info.input_channel
7   dst_group_size = op_info.output_channel / op_info.group
8   If op_info.group ≠ 1 and src_group_size % 4 == 0 and dst_group_size % 4 == 0
9     return True
10   return False

CHECKWINOGRAD(gpu_info, op_info)
11  If op_info.group ≠ 1 or op_info.kernel_shape ≠ 3x3 or op_info.stride ≠ 1
12     return False
13  src_depth = ⌈op_info.input_channel/4⌉
14  dst_depth = ⌈op_info.output_channel/4⌉
15  If gpu_info.type == Adreno and (src_depth < 32 or dst_depth < 32)
16     return False
17  Else if gpu_info.type == AMD and (src_depth < 16 or dst_depth < 8)
18     return False
19  Else if src_depth < 16 or dst_depth < 16
20     return False
21  total_tiles = ⌈op_info.output_height/4⌉ * ⌈op_info.output_width/4⌉
22  If gpu_info.type == Adreno6xx and total_tiles < 128
23     return False
24  Else if gpu_info.type == Adreno and total_tiles < 64
25     return False
26  Else if total_tiles < 32
27     return False
28  return True
```