Influence of silicon wafer surface roughness on semiconductor device characteristics

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The surface roughness of silicon wafer is one of the most important issues that degrade characteristics of semiconductor devices. The importance of spatial roughness frequency as an influential parameter has been pointed. In this research, the effect of roughness frequency on MOSFET characteristics was studied using samples with different roughness for frequency. From the obtained results, it was found that roughness with a low spatial wavelength affects electron mobility and gate insulating film reliability such as $E_{bd}$, $Q_{bd}$ and SILC.

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1. Introduction

The surface roughness of silicon wafer is one of the most important issues in semiconductor devices that degrade some electrical characteristics. For instance, it is known that the mobility of the electron and hole is affected by impurities in silicon,1,2 temperature,2,3 crystal plane orientation of the silicon surface,4,5 and crystal orientation,6 but it is also known for MOSFETs that the mobility is affected by the roughness of the interface between the semiconductor substrate and the gate dielectric film. It has been reported that the mobility of MOSFETs on silicon wafer changes by various cleaning conditions or gate oxidation conditions.9,12,13 There are various reports about the methods of improving mobility, such as the use of strained Si.10 It has been reported that atomic order flattening of the silicon surface by Ar annealing in a highly clean ambient and radical oxidation using microwave-excited plasma at the gate insulator formation process has the effect of flattening the Si–SiO2 interface and improving the mobility of the electron and hole.5,11 In addition, the gate dielectric film reliability of MOS capacitors on silicon wafer also depends on the surface roughness controlled by cleaning conditions or gate oxidation conditions.9,12,13 There are various reports on the method of improving gate dielectric film reliability, such as the use of Xe/H2 plasma flattening,14 and it has been reported that atomic order flattening of silicon surface annealing in a highly clean Ar ambient and radical oxidation at the gate insulator formation process is effective in improving gate dielectric film reliability.15–18 The atomic order flattening technology has been proven to improve sub-threshold swing factors (S-factor),15 I/f noise,11,12,19 random telegraph noise (RTN)20,21 and stress induced leakage current (SILC).22 It has been reported that the roughness of the silicon surface affects device characteristics not only in devices using SiO2 gate oxide film but also in devices using high-k gate insulating films such as HION.23 Therefore, reduction of the surface roughness of the silicon wafer is an important issue in both current and future semiconductor devices.

Fig. 1. Process flow of wafers for fabricating MOSFETs.

The silicon wafer engineering processes which affect roughness are not only cleaning and annealing but also mirror polishing.24–26 Conventionally, the surface roughness was mainly indicated by the index of roughness height such as arithmetical mean height (Ra or $S_a$), root mean square ($R_q$ or $S_q$), maximum roughness ($R_z$ or $S_z$), and so on. However, it has been pointed out that the roughness spatial frequency or spatial wavelength is also important.18,27 In this research, the four kinds of wafers with variable average roughness and spatial frequency from the same ingot were prepared by controlling cleaning and mirror polishing conditions, and some semiconductor device characteristics fabricated on these wafers were measured and compared. This paper is the extended version of a recently published conference paper at the 2019 International Workshop on Dielectric Thin Films for Future Electron Devices (IWDTF). In this paper, detailed discussions of the results of electron mobility, $E_{bd}$, $Q_{bd}$ and SILC have been newly added.

2. Experimental methods

The silicon wafers used in these experiments were manufactured by slicing a 200 mm diameter Czochralski (Cz) grown boron-doped silicon ingot with (100) growth direction. The resistivities of wafers were 52.0–53.2 Ω cm. Figure 1 shows process flow of wafers for fabricating MOSFETs. By controlling polishing and cleaning conditions, the silicon wafers with different surface roughness were prepared. In addition, some silicon wafers were atomically flattened by Ar...
annealing in ultra clean ambient.\(^{28}\) The annealing time was 1 h at 1000 °C. Surface roughness of each silicon wafer was evaluated with an atomic force microscope (AFM) and white light interferometer to evaluate both the small region and large region. Figure \(2\) shows \(1 \times 1 \mu m^2\) AFM images of each wafer surfaces. AFM image consists of 512 \(\times\) 256 pixels. In the case of 3D areal surface texture, root mean square plane roughness (\(S_q\)) can be described as follows:

\[
S_q = \sqrt{\frac{1}{A} \int_A \int A Z(x, y) dx dy}
\]

where \(A\) is the definition area and \(Z\) is the height. After annealing, \(S_q\) values of AFM images became approximately 0.05 nm. Comparing the A condition and B condition of the as-polished wafer, \(S_q\) value of B condition was rougher than that of the A condition. Figure \(3\) shows \(4.4 \times 4.4 \, \text{mm}^2\) white light interferometer images of each wafer surfaces. The white light interferometer image consists of 1024 \(\times\) 1024 pixels. Comparing the A condition and B condition, the \(S_q\) values of the A condition were larger than that of the B condition, and it is found that Ar annealing has no impact on the long-range roughness which is detected by the white light interferometer.

The silicon wafer surface has concaves and convexes with various spatial wavelengths ranging from the distance between atoms to the size of the wafer. Equivalently, each spatial wavelength of silicon wafer surface roughness can be described by the power spectral density. The power spectral density can be described as follows:\(^{29}\)

\[
F(k) = \sum_{n=0}^{N-1} Z_n \exp\left(\frac{-i2\pi kn}{N}\right) \\
\times (k = 0, 1, 2, \ldots, N-1) \\
\times P(k) = \frac{2\pi d}{N} |F(k)|^2
\]

where \(Z_n\) is the \(n\)th profile data, \(N\) is the number of data in the \(X\) direction or the \(XY\) direction, \(d\) is the sampling interval, and \(P(k)\) is the power spectral density at the spatial frequency \(f = k (N-1) d\). AFM has a horizontal resolution of about 10 nm, however AFM cannot measure a wide area. A white light interferometer can measure a wide area, but the horizontal resolution is about 4 \(\mu m\). Therefore, the results of roughness analysis from the small spatial wavelength to the wide spatial wavelength need to be discussed for both conditions.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
 & A condition & B condition \\
\hline
As polished & \begin{tabular}{c}
\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure2.png}
\caption{(Color online) \(1 \times 1 \mu m^2\) AFM images of each wafer surfaces. The annealing time is 1 h at 1000 °C.}
\end{figure}
\end{tabular} & \begin{tabular}{c}
\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure3.png}
\caption{(Color online) White light interferometer images of each wafer surface. The A condition is rougher than the B condition. Ar annealing has no impact on the roughness which is detected by the white light interferometer.}
\end{figure}
\end{tabular} \\
\hline
Ar anneal & \begin{tabular}{c}
\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure2.png}
\caption{(Color online) \(1 \times 1 \mu m^2\) AFM images of each wafer surfaces. The annealing time is 1 h at 1000 °C.}
\end{figure}
\end{tabular} & \begin{tabular}{c}
\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure3.png}
\caption{(Color online) White light interferometer images of each wafer surface. The A condition is rougher than the B condition. Ar annealing has no impact on the roughness which is detected by the white light interferometer.}
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\end{table}
AFM and white light interferometer. Figure 4(a) shows the $P(k)$ of each $10 \times 10 \mu m^2$ AFM images. The $X$ axis indicates the spatial wavelength, and the $Y$ axis indicates amplitude intensity at each spatial wavelength. Roughness of the spatial wavelength range shorter than 300 nm was lower in the A condition than the B condition, and the roughness in the spatial wavelength range shorter than 300 nm was reduced by Ar annealing. Figure 4(b) shows the $P(k)$ of each white light interferometer image. The roughness of the spatial wavelength range of 30 $\mu m$ or more of the A condition was higher than that of the B condition, and the roughness of this wavelength range was not affected by Ar annealing.

3. Results and discussion

Figure 6 shows electron mobility characteristics at $-30, 0$ and $20 \degree C$ as functions of the effective electric field ($E_{\text{eff}}$) in MOSFETs samples with a gate width of 50 $\mu m$, length of 50 $\mu m$ and oxide thickness of approximately 5 nm. The electron mobility of Ar anneal-flattening wafer in the $E_{\text{eff}}$ range of 0.3–0.5 MV is higher than that of the wafer without annealing. Without Ar anneal-flattening case, the electron mobility of the A condition in the $E_{\text{eff}}$ range of 0.3–0.5 MV is higher than the B condition. This suggests that a spatial wavelength range less than 300 nm of roughness affects electron mobility degradation. The difference of electron mobility is clearly observed at low temperatures. This is caused by phonon scattering decreasing at low temperatures and then, surface roughness scattering becomes apparent. In past research, it has been reported that mobility degradation due to surface roughness scattering occurs in the high $E_{\text{eff}}$ region. However, in this research, the difference in electron mobility due to surface roughness scattering occurs in the middle $E_{\text{eff}}$ region, and there is no difference in the high $E_{\text{eff}}$ region. Similar cases have been reported in Si-Strained.
**p-type Si (100), Resistivity = 52.0-53.2 Ω cm**

**Isolation**
- Ar Anneal : Kr/O₂ radical oxidation
- As Polished : Wet Oxidation
- NSG deposition : 300 nm

**Active region patterning**
- Lithography
- NSG etching by buffered HF

**Channel stop layer & well formation**
- Kr/O₂ radical oxidation : 6 nm
- B implantation

**Activation Annealing**
- 900°C N₂ Anneal 30min.

**Sacrificial oxidation**
- DHF & H₂-UPW rinse

**Gate Insulator formation**
- Ar Anneal : Kr/O₂ radical oxidation : 5 nm
- As polished : Wet Oxidation : 5 nm

**Gate electrode formation**
- Doped-Poly-Si deposition : 150 nm
- Lithography
- Doped poly-Si etching
- DHF Cleaning

**Source/Drain junction formation**
- Lithography
- As⁺ implantation
- SPM-UPW rinse
- 900°C N₂ Anneal 30min.

**Re-oxidation**
- Kr/O₂ radical oxidation : 6 nm

**Interlayer formation**
- NSG deposition : 300nm

**H₂ sintering**
- H₂ : 10%, 400°C 30min

**Contact formation**
- Lithography
- NSG Etching
- SPM Cleaning

**Metallization**
- Al Vapor deposition
- Lithography
- Wet Etching
- Resist removal wet chemical

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**Fig. 5.** (Color online) (a) Experimental flow and (b) schematic structure of fabricated MOSFET.

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**Fig. 6.** Electron mobility characteristics as a function of the effective electric field ($E_{eff}$). $E_{eff}$ with the Ar anneal-flattening higher than that of the wafer without annealing. $E_{eff}$ of the A condition is higher than the B condition. The difference in electron mobility is clearly observed at low temperatures.
MOSFETs. Therefore, the influence of electron mobility due to surface roughness scattering needs to be reexamined.

Figure 7 shows the Weibull plot on the gate oxide film breakdown electric field intensity ($E_{bd}$) of the MOS capacitor with an area of $1 \times 10^{-4}$ cm$^2$. $E_{bd}$ of the Ar anneal-flattening wafer is approximately 1 MV cm$^{-1}$ better than that of the wafer without annealing. This indicates that there are many local spots that induce electric field concentration on the as-polished wafer surface compared with the Ar anneal-flattening wafer, and it is considered that the spatial wavelength of local spots is less than 300 nm.

Figure 8 shows the Weibull plot of the charge to breakdown ($Q_{bd}$) of MOS capacitors with an area of $1 \times 10^{-4}$ cm$^2$ for the Ar anneal-flattening wafer and as-polished wafer. The charge was injected by applying a constant current with a current density of 0.2 A cm$^{-2}$. $Q_{bd}$ of the Ar anneal-flattening wafers is approximately 10 times larger than that of wafers without annealing. Comparing the as-polished levels of the A condition and B condition, $Q_{bd}$ of the A condition is twice as good as the B condition. In the $Q_{bd}$ characteristic, $Q_{bd}$ of the A condition is smaller than that of the B condition although the spatial wavelength range of 30 μm or more of the A condition is worse than the B condition. However, the roughness of the spatial wavelength range smaller than 300 nm was lower in the A condition than the B condition, and the roughness in the spatial wavelength range shorter than 300 nm was reduced by Ar annealing. From results of roughness evaluations and $Q_{bd}$ measurements, it is considered that the roughness of spatial wavelengths of 30 μm or more does not affect $Q_{bd}$, but roughness of spatial wavelengths of 300 nm or less affects $Q_{bd}$. This result indicates that there are many local spots that induce electric field concentration on the as-polished wafer surface especially the B condition wafer as compared with the Ar anneal-flattening wafer, and it is suggested that the size of the local spots is less than 300 nm. In addition, $Q_{bd}$ of the A condition of the Ar anneal-flattening wafer is better than the B condition of the Ar anneal-flattening wafer. This is assumed to be attributed to other origins that affect $Q_{bd}$, such as the difference of the crystalline of the silicon wafer surface which is induced in each silicon wafer polishing condition. To clarify the mechanism, it requires a more detailed investigation.

Figure 9 shows the gate current density as a function of injected charge density ($Q$) of the MOS capacitor with an area of $1 \times 10^{-4}$ cm$^2$ at the electric field is 9.0 MV cm$^{-1}$. The charge was injected by applying a constant current with a current density of 10 μA cm$^{-2}$. In order to measure the increase of SILC due to the injection of stress charge, gate voltage–gate current was measured before and after the injection of stress charge. After the charge injection, the leakage current with Ar anneal-flattening are smaller than those without flattening, regardless the oxide thickness. This means the SILC can be suppressed by the Ar anneal-flattening. Without the flattening case, SILC of the B condition is larger than that of the A condition for all charge injections although the roughness of the B condition is smaller than that of the A condition in the long spatial wavelength region and the oxide of the B condition is thicker than that of the A condition. The differences in SILC suggest that the electric field concentration is caused by the wavelength range less than 300 nm of roughness, and SILC is degraded. On the other hand, SILC of the A condition at an injected charge density of 0.1(C cm$^{-2}$) or less is better than that of the B condition even with Ar anneal-flattening. It is therefore...
considered that other origins affect SILC, such as the difference of crystalline of silicon wafer surface which is induced in each polishing condition. However, in order to clarify the mechanism, it is necessary to investigate both the crystalline of the silicon wafer and the detailed electrical characteristics of MOSFETs.

4. Conclusions
Electron mobility and gate oxide film reliability such as $E_{bd}$, $Q_{bd}$ and SILC with the Ar anneal-flattening are better than that of the wafer without annealing. Electron mobility, $Q_{bd}$ and SILC of the A condition are better than those of the B condition although the roughness of the A condition in the long wavelength region is larger than those of the B condition. These suggest that the roughness with a narrow pitch is more important in electron mobility and gate oxide film reliability. The difference between the A condition and the B condition is assumed to be due to differences in silicon wafer manufacturing processes, but clarification of the mechanism requires more detailed investigation.

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Fig. 9. The gate current density as a function of injected charge density after the charge injection. The leakage current with Ar anneal-flattening is smaller than those without flattening.