A High Step-up Sextuple Voltage Boosting 13S-13L Inverter with Fewer Switch Count

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ABSTRACT In this work, a high step-up sextuple voltage boosting 13 switches – 13 level inverter (SVB-13S-13LI) structure was proposed through a pulse width modulation technique with selective harmonic elimination. This topology can deliver six times of voltage boosting capability. A single voltage source, 13 switches, two diodes, and three capacitors are utilized to obtain the objective of this research. This work carried out various tests on the proposed topology to find efficiency, voltage stress, total standing voltage, and voltage gain. The detailed comparative study of existing inverter topologies is tabulated to prove the proposed topology has a better performance. The main feature of this topology is six times voltage boosting, a minimum number of switches, less voltage stress, and a self-balanced floating capacitor. Further to isolate or eliminate the undesired low order harmonics the particle swarm optimization-based SHEPWM Technique is used. For proving the above-mentioned merits, the simulation was carried out using MATLAB SIMULINK and their corresponding THD results are compared with different Modulation indexes. Also, experimental results are validated by the FPGA SPARTAN 6E controller and their cost function [CF] for the unit price ($) are compared with the state-of-art literature 13-level inverters.

INDEX TERMS 13S-13L inverter, switched capacitor, SHE PWM technique, power losses, voltage – boosting ability.

I. INTRODUCTION

To promote adoptable of the conventional variable voltage-frequency as an efficient model, the process of DC-AC power conversion plays a vital role. Among many conventional methods, a multilevel inverter (MLIs) is well-known and widely deployed across most power-consuming applications. That demands include flexible AC transmission systems or renewable energy resources and high voltage transmission or variable frequency drives on several standard voltages [1]. Conventional MLIs topologies in the literature and listed as 1. Neutral-Point-Clamped MLI 2. Cascade H-Bridge MLI 3. Diode-clamped MLI 4. Flying capacitor MLI [FC-MLI] is expressed from [2]. In PV applications, SCMLIs can achieve advantageous features like voltage boosting, capacitor voltage self-balancing, grid compatible distortion-free waveform, and reduction in filter size [3]. In [4], [7] though the peak inverse voltage of the switches is low, more switching devices are needed even for low voltage gain. In [5], six times voltage boosting is achievable, but the rating of the switches is high which also limits the charging of the capacitor when the modulation index is low. SCMLIs introduced [6], incorporation of typical H-bridge with switched capacitor demands more semiconductor devices. In addition to that, the capacitor voltage balancing becomes difficult which also increases the cost function. In [8], though high voltage gain is attained with less number of switches, the topology suffers from high TSV and high rating capacitors. To meet the above challenges by implementing a multilevel inverter with the switched capacitor (MLI-SCs) and to get a boosting ability, it is to be designed in such a way that it hosts a smaller transformer (or) inductor than by using the SCMLI. The challenge of implementing T-type topology based on SCs is its high unreliability for High-voltage application and its back-end H-bridge [HB] generates a negative voltage level [9].

The maximum output voltage endured must use the four-power semiconductor switch on the HB [10]. Fig. 1 depicts the block diagram of the SHE technique for the multilevel inverter. By making a series-parallel input voltage source in SCs get a grid of the necessity of the exterior
boosting circuit that makes the circuit simpler [11], [12]. From the literature study, it is clear that if the output level has been attempted to increase, that consequently makes the circuit more complex and becomes costlier to implement.

Thus, various studies were done in the literature that is significantly involved in minimizing the usage of components such as voltage sources, power semiconductor switches, and switched capacitors. For example, 13-Level - MLIs [13], comprising of 4 DC sources and 10 switches. A kite structure of ML’s is developed in [14] to reduce the number of sources. A K-Type SC-MLIs presented in [15] required a single DC source, four capacitors, and 14 switching devices. Yet, the voltage boosting the ability of underlying switches, the generated total blocking voltage [TBV], the complex designing of the gate driving circuit, and the charge for each level remain as significant challenges. To address the challenges, the 13-Level ML’s have been put forth. A 13- level ML Topology has been designed with only 10 switch counts comprising four capacitors and four diodes with a boosting ability of six which makes it cost-effective. To obtain better output voltage and the maximum total stored energy in the 4 capacitors and requires two more switch counts [16]. The author proposed in [17], use an H-bridge in the back end of the inverter. So, the output voltage level not be varied flexibly. A new SSC unit is proposed but it also needs two more additional isolated DC sources and if the levels are increased and the SSC switched capacitor based inverter and it requires three more switches to generate thirteen levels without any additional circuits and sensors. From the literature study, it is clear that if the output level has been attempted to increase, that consequently makes the circuit more complex and becomes costlier to implement. A new SSC unit is proposed but it also needs two more additional isolated DC sources and if the levels are increased and the SSC switched capacitor based inverter and it requires three more switches to generate thirteen levels without any additional circuits and sensors. The circuit description, modes of operation of the 13- level proposed SCs MLI, and Level shifted modulation index was discussed in section II. The optimization of SHE-PWM with PSO implemented in the proposed topology has been discussed in Section III. In section IV detailed comparisons with recent topologies are tabulated with different criteria. The power loss is analyzed in Section V. Section VI portrays the result discussion. Finally, in the VII section conclusion portion is concluded.

II. 13S-13L INVERTER TOPOLOGY

A. CIRCUIT EXPLANATION

Fig. 2 depicts the 13- level multilevel structure with a switched capacitor. It comprises 13 switch counts, two diodes (D1 and D2), three capacitors (C1-C3), and four complementary switches (S1, S2, S3, and S4). V_{ab} is the output of the inverter obtained from the source voltage V_{dc}.

This topology comprises three sections, left end is the source voltage along with thrice times of voltage boosting (S1, S2, S1', S2', C1, C2, and source voltage V_{dc}) is obtained from the voltage Trippler section. The Middle section is generating another three times voltage boosting with help of a single floating capacitor (S3, S4, S5, S6, S7, and S8 & C6). Four switches (S3, S6' & S8, S8') are integrated and form the polarity changer section (H- Bridge). To obtain a constant dc voltage without any charging issues the C1, C2 are assumed as large μF and ignore ON-state
resistance (R_{ON}) and the frontward voltage drop across the switching components. \( V_{dc} \) and 3\( V_{dc} \) are the voltage flowing through the capacitors (\( C_1, C_2 \) and \( C_3 \) is maintained without requiring any additional circuit. Low voltage stress (\( V_{dc} \)) has occurred across each component.

**B. OPERATING PRINCIPLE AND SC VOLTAGE BALANCING**

For an inductive load, the current flow path is represented in Fig. 3 as per the switching Table I respectively. Every cycle of operations has completed the 17 operating states in the proposed topology. The entry “1” for ON state and “0” for OFF state is indicated in the switching table. In the voltage tripler section, the capacitors \( C_1, C_2 \) are coupled to the source voltage in parallel to charge each capacitor to the maximum rating of \( V_{dc} \). These two capacitors discharged to the load along with the source voltage in a rating of 3\( V_{dc} \). In this section, each capacitor can charge through the connection of source voltage parallel at the same time another capacitor can discharge to the load through the connection of series along with source \( V_{dc} \). Particularly in the states of (a) & (d) from Fig 3. The capacitors \( C_1 \) & \( C_2 \) are charged by integrating the source \( V_{dc} \) to the parallel. Similarly, in the states of (b), (c), & (f), the connected capacitors are discharged along with the source. It aims to refill the capacitor with more energy paucity thereby recuperating the voltage.

\( V_{ab}=0 \): During this state as shown in Fig. 3g, voltage Tripler circuit (3\( V_{dc} \)) is charged the floating capacitor (\( C_3 \)) by discharging \( C_1 \) and \( C_2 \) along with source voltage. i.e., 3 \( V_{dc} \) in capacitor \( C_3 \). Hence zero voltage flows to the load.

\( V_{dc}=V_{dc} \): The state explains the capacitors \( C_1 \) & \( C_2 \) are charged with help of source voltage simultaneously the obtained load voltage is \( V_{dc} \) through the power semiconductor devices (\( S_{dc}^{1}, S_{1} \) and \( S_{2}, S_{4}, S_{5} \) and \( S_{6}^{1} \)) in ON state position. Similarly, for a negative mode of operation switches \( S_{1}, S_{4}, S_{5} \), and \( S_{9} \) are triggered. The positive mode of operation. as shown in Fig 3(a).

\( V_{dc}=2V_{dc} \): During this state 2-3, by turning ON the switch as per Table I the 2\( V_{dc} \) is obtained in the load.

\( V_{dc}=3V_{dc} \): During this state 4, the source voltage is coupled in series with storing devices such as capacitors \( C_2 \) - \( C_1 \) to charge the floating capacitor and supply the load voltage. So the capacitor \( C_3 \) is in parallel with input voltage source \( V_{dc} \) when \( S_1, S_4, S_6, S_7 \) are ON so, the total amplitude of state 4 is 3\( V_{dc} \) generated.

\( V_{dc}=4V_{dc} \): During this state 5, the capacitors \( C_2 \) & \( C_1 \) are joined with parallel, and capacitor \( C_3 \) is in series with dc source when \( S_1, S_2, S_4, S_6 \), \( S_7 \) are ON so, the received amplitude is 4\( V_{dc} \) on the load side.

\( V_{ab}=5V_{dc} \): During this state 6-7, the SCs are in redundancy. When \( S_1, S_3, S_5, S_6, S_7 \) are turned ON so, the total amplitude of state 6-7 is 5\( V_{dc} \) generated.

\( V_{ab}=6V_{dc} \): During this state 8, all capacitors \( C_1, C_2, C_3 \) are discharged to the load by the connection of series. When \( S_1, S_2, S_4, S_7, S_9 \) are ON so, the total amplitude of state 6 is 6\( V_{dc} \) generated.

**C. MODULATION INDEX**

In MLIs, the switches ON and OFF control is done by the PWM technique. For this purpose, a Phase Disposition (PD)
TABLE I
SWITCHING STATE OF PROPOSED 13-LEVEL INVERTER

| States | Voltage Tripler circuit | Switches | Capacitors | Vbus | Vab |
|--------|-------------------------|----------|------------|------|-----|
| S1     | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | C1 | C2 | C3          |
| 1      | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | C | C | -     | Vdc | Vdc | |
| 2      | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | D | C | -     | 2Vdc | 2Vdc | |
| 3      | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | C | D | -     | 2Vdc | 2Vdc | |
| 4      | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | D | D | C     | 3Vdc | 3Vdc | |
| 5      | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | C | D | C     | Vdc  | 4Vdc | |
| 6      | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | D | C | D     | 2Vdc | 5Vdc | |
| 7      | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | C | D | D     | 2Vdc | 5Vdc | |
| 8      | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | D | D | D     | 3Vdc | 6Vdc | |
| 9      | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | D | C | D     | 3Vdc | 0    | |
| 10     | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | C | C     | -     | Vdc  | -Vdc |
| 11     | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | C | D     | -2Vdc | -2Vdc | |
| 12     | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | D | C     | -2Vdc | -2Vdc | |
| 13     | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | D | D     | -3Vdc | -3Vdc | |
| 14     | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | C | D | C     | -Vdc  | -4Vdc | |
| 15     | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | C | D | D     | -2Vdc | -5Vdc | |
| 16     | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D | C | D     | -2Vdc | -5Vdc | |
| 17     | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D | D | D     | -3Vdc | -6Vdc | |

FIGURE 4. Level shifted PWM technique for 13 L and corresponding on state switches.

level-shifted multicarrier (PD-LS-PWM) PWM is recommended to improve the output voltage quality. In the PD, all carrier signals are in phase and the level is shifted. In the middle of the carrier signal, zero references are placed as shown in Fig. 4. It is also suitable for lower switching frequency and higher switching frequency. Generally, for the several levels are higher, then the low switching frequency is recommended and for several levels is lower, the high switching frequency is recommended. In [8] is accepted for the modulation technique of the proposed 13 level MLIs inverter topology. Fig. 4 comprises a sinusoidal reference signal and the six triangular carriers ($V_{c1}$-$V_{c6}$) of the same frequency 2.5 kHz is compared with semi sinusoidal reference 50 Hz. The redundant states [20], is presenting a power-sharing is equally among the capacitor $C_1$ and $C_2$ in the symmetrical charging/discharging.

III. SHE-PWM MODULATION FOR THE PROPOSED INVERTER

The process of selective harmonics elimination plays a significant role to address lower total harmonics distortion (THD) in the voltage ($V_{ab}$) waveform of the multilevel inverter. This inverter is designed to reject the harmonics...
which are low order in each level. The mathematical expression of the voltage \( V_{ab} \) waveform can be expressed as

Fourier series is

\[
V_o = a_o + \sum_{i=0}^{n} a_n \cos \left( \frac{2\pi nf}{T} \right) + b_n \sin \left( \frac{2\pi nf}{T} \right) \tag{1}
\]

For quarter-wave symmetry \( a_o = 0 \) and \( a_n = 0 \), the even-order harmonics were canceled.

Fourier series expression that to express the output phase voltage were given by,

\[
V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n \omega t) \tag{2}
\]

From the above Equation (2), the expressed term of instantaneous voltage \( V_{ab} \) is as

\[
V_o(t) = \sum_{i=1,3,5,..} b_n \sin(n \omega t) \tag{3}
\]

Fig. 5. Shows the odd notches per quarter cycle of order harmonics from a fewer range of modulation index.

\[
b_n = 4V \left[ \frac{\sum_{k=1}^{m} (-1)^k \cos(n \omega t)}{\pi} \right] \tag{5}
\]

Where \( m \) is odd

\[
M = \text{number of edges/ notches per quarter cycle}
\]

In the proposed topology, the eliminating five categories of lower order harmonics in the waveforms by finding six firing angle \( S \) i.e., \( S-1 \) in the waveform of output voltage. For thirteen-level inverter topology, 3\(^{rd}\), 5\(^{th}\), 7\(^{th}\), 9\(^{th}\), 11\(^{th}\) harmonic order output voltage waveform has been picked for harmonic elimination. Equation (6) is used to find the firing angle \( \theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \theta_6 \) that was calculated by the relationship

\[
\begin{align*}
0 &< \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6 < \frac{\pi}{2} \\
V_n &= \frac{4V}{\pi} \left[ \cos(n \theta_1) - \cos(n \theta_2) + \cos(n \theta_3) - \cos(n \theta_4) \right. \\
&\left. + \cos(n \theta_5) - \cos(n \theta_6) + \ldots \cos(n \theta_k) \right] \tag{6}
\end{align*}
\]

In the output voltage waveform, 3\(^{rd}\) harmonics \( (n=3) \), 5\(^{th}\) harmonics \( (n=5) \), 7\(^{th}\) harmonics \( (n=7) \), and so on were eliminated.

\[
V_1 = \frac{4V}{\pi} \left[ \cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) - \cos(\theta_4) \right] \\
V_3 = \frac{4V}{3\pi} \left[ \cos(3\theta_1) - \cos(3\theta_2) + \ldots + \cos(3\theta_j) - \cos(3\theta_k) \right] \\
V_5 = \frac{4V}{5\pi} \left[ \cos(5\theta_1) - \cos(5\theta_2) + \ldots + \cos(5\theta_j) - \cos(5\theta_k) \right] \\
V_7 = \frac{4V}{7\pi} \left[ \cos(7\theta_1) - \cos(7\theta_2) + \ldots + \cos(7\theta_j) - \cos(7\theta_k) \right] \\
V_9 = \frac{4V}{9\pi} \left[ \cos(9\theta_1) - \cos(9\theta_2) + \ldots + \cos(9\theta_j) - \cos(9\theta_k) \right] \\
V_{11} = \frac{4V}{11\pi} \left[ \cos(11\theta_1) - \cos(11\theta_2) + \ldots + \cos(11\theta_j) - \cos(11\theta_k) \right] 
\]

To diminish the 3\(^{rd}\), 5\(^{th}\), 7\(^{th}\), 9\(^{th}\), and 11\(^{th}\) harmonics in outputs, the corresponding voltage has set to zero, and meanwhile (8) was employed to vary the modulation index from 0 to 1, to obtain the required angle through the inverter linear range while,

\[
V_1 = \frac{4V}{\pi} \left[ \cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) - \cos(\theta_4) \right] \\
V_3 = \frac{4V}{3\pi} \left[ \cos(3\theta_1) - \cos(3\theta_2) + \ldots + \cos(3\theta_j) - \cos(3\theta_k) \right] \\
V_5 = \frac{4V}{5\pi} \left[ \cos(5\theta_1) - \cos(5\theta_2) + \ldots + \cos(5\theta_j) - \cos(5\theta_k) \right] \\
V_7 = \frac{4V}{7\pi} \left[ \cos(7\theta_1) - \cos(7\theta_2) + \ldots + \cos(7\theta_j) - \cos(7\theta_k) \right] \\
V_9 = \frac{4V}{9\pi} \left[ \cos(9\theta_1) - \cos(9\theta_2) + \ldots + \cos(9\theta_j) - \cos(9\theta_k) \right] \\
V_{11} = \frac{4V}{11\pi} \left[ \cos(11\theta_1) - \cos(11\theta_2) + \ldots + \cos(11\theta_j) - \cos(11\theta_k) \right] 
\]

\[
M = \frac{V_1}{n} \tag{8}
\]

As of now, the proposed work eliminates all the undesired low order harmonics from a fewer range of modulation index has been one of the significant contributions of SHEPWM. The main impartial is to become fundamental at the anticipated level for every modulation index.

\[
\theta_i = \frac{1}{C} \times \left[ M - \left( \frac{V_1}{kV_s} \right) + \left( \frac{V_3}{kV_s} \right) + \left( \frac{V_5}{kV_s} \right) + \left( \frac{V_7}{kV_s} \right) + \left( \frac{V_9}{kV_s} \right) + \left( \frac{V_{11}}{kV_s} \right) \right] \tag{9}
\]
For a 13-level inverter, six optimized switching angles are $\theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \theta_6$ calculated by using the above fitness function (9). A feasible modulation index with the least THD was computed by multiplying the error 1/e with its 1% of the limit. In the experimental setup, the variable modulation index was varied from 0 to 1 range with a step change of 0.01 along with the generated switching angle. The inertia weight has been varied from 0.9 to 0.4 ranges with an acceleration factor of 2. The variable of the objective function has been randomized. In a ring topology [25], the $P_{best}$ has been generalized by as much iteration by updating their velocity and angle.

The motive of the PSO algorithm is to guide the direction that paves the maximum utility. The best particle position is achieved by deploying an experiential learning model that learns from the utility gained by each particle due to its respective movement in search space. In every iteration, the particle velocity and dimension are getting updated by the following equations.

$$V_{(m,n)} = (W \times V_{(m,n)}) + C_1 \times r_1 \times (P_{best} - X_{(m,n)}) + C_2 \times r_1 \times (G_{best} - X_{(m,n)})$$

$$X_{(m,n)} = X_{(m,n)} + V_{(m,n)}$$

$$w = w_{max} - \frac{w_{max} - w_{min}}{Total \ number \ of \ iterations} \times current \ iteration$$

IV. COMPARISON WITH OTHER RECENT SCMLI TOPOLOGIES

The proposed cost-effective yet robust 13-level optimal MLIs was designed to generate a peak 13-level of AC output voltage efficiently. In Table II, recent topologies have been compared with the proposed model. In this proposed 13-level SCIs, it is seen that the maximum voltage of all operating switches has not exceeded three times the maximum load voltage.

In [17], [18], the four-switch count on the HB and 2 switches count in [19] have to suffer from the peak load voltage. It requires two switches count series-coupled with half-rating [3Vsw] for High-voltage applications. The proposed 13-level inverter topology is a symmetrical circuit comprised of a single DC source of $V_{dc}$= 60V. For inverter configuration, the prime parameter is Total standing voltage (TSV). It is the summation of the absolute blocking voltage (maximum) across every switching device, while the same voltage stress occurs in the complementary switch count. The cost function of the 13S-13L inverter is compared to other 13-Level MLIs, which are shown in Table III.

The proposed 13S-13L level inverter topology is a symmetrical circuit comprised of a single DC source of $V_{dc}$= 60V. For inverter configuration, the prime parameter is TSV. It is the summation of the absolute voltage (MVB) across through every switching device, while the same voltage stress occurs in the complementary switch count. The Cost function of the 13S-13L inverter is compared to other 13-Level MLIs, the voltage stress across the switches has been computed by [10], [19] – [23] as follows

Complementary switches, $S_1, S_2, S_3, S_4, S_5, S_6$

$$V_{S_1} = V_{S_2} = V_{S_3}$$

$$V_{S_4} = V_{S_5} = V_{S_6}$$

Complementary switches, $S_7, S_8, S_9$

$$V_{S_7} = V_{S_8}$$

Switches, $S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$

$$V_{S_1} = V_{S_2} = V_{S_3}$$

$$V_{S_4} = V_{S_5} = V_{S_6}$$

$$V_{S_7} = V_{S_8}$$

$$V_{S_9}$$

$TSV_{p.u.} = \frac{13}{V_{dc}} \sum_{y=1}^{13} V_{y}$

Therefore, substitute (13)– (15) in (16) and get

$$= 2(V_{S_1} + V_{S_2}) + (V_{S_3} + V_{S_4} + V_{S_5} + V_{S_6} + V_{S_7} + V_{S_8}) + 2(V_{S_5} + V_{S_9})$$

$$= (2 + 1) + 3 + 3 + 3 + 3 + 3 + 2(3 + 3)$$

$$= 4 + 15 + 12$$

$$TSV = 31V_{dc}$$

The TSV of the proposed system is 31Vdc and the TSV_{p.u.} is calculated by,

$$TSV_{p.u.} = \frac{TSV}{V_{o, peak}} = \frac{31V_{dc}}{6V_{dc}}$$

$$= 5.167 \mu F$$

The Voltage Gain=

$$\frac{V_{o, peak}}{V_{dc}} = 6$$

$$CF = N_{sw} + N_d + N_e + N_w + TSV_{pu} + TCD_{avg}$$

It is to be noted that the input voltage considered in the entire simulation and experimental hardware is 60 V and its corresponding recorded output is about 360 V. The capacitor $C_1$ and $C_2$ is 820 $\mu F$, which stores the energy of about 60 V whereas the capacitor $C_3$ as 1200 $\mu F$ that stores about 180 V are shown in Table IV. The simulation and hardware results are compared in terms of total harmonics distortion (THD) value of various modulation indexes are shown in Fig. 7 & 8.
TABLE II
COMPARISON OF PROPOSED TOPOLOGY WITH OTHER MLIS

| Topology | \( N_{\text{switches}} \) | \( N_{\text{sources}} \) | \( N_{\text{capacitors}} \) | \( N_{\text{diode}} \) | \( \text{PIV,} \text{p.u.} \) | \( N_{\text{level}} \) | \( \text{TSV,} \text{p.u.} \) | Voltage Gain | Capacitor Balancing | Voltage boosting Ability |
|----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|
| NPC      | 16             | 1              | 8              | 56             | 2              | 21             | 44             | -              | Additional Circuits Required for >3-Level | No              |
| FC       | 16             | 1              | 31             | -              | 6              | 21             | 44             | -              | No additional Circuit Required        | No              |
| 14       | 14             | 2              | 2              | -              | 6              | 13             | 39             | 2              | Self-Balancing            | Yes             |
| 15       | 14             | 1              | 4              | -              | 6              | 13             | 6.0             | 1.5            | Self-Balancing            | Yes             |
| 16       | 10             | 1              | 4              | 4              | 3              | 13             | 5.5             | 6              | Self-Balancing            | Yes             |
| 17       | 10             | 1              | 5              | 10             | 6              | 13             | 6.0             | 6              | Self-Balancing            | Yes             |
| 18       | 19             | 1              | 5              | -              | 6              | 13             | 6.84            | 6              | Self-Balancing            | Yes             |
| 19       | 8              | 1              | 3              | 3              | 4              | 9              | 5.75            | 4              | Self-Balancing            | Yes             |
| 20       | 13             | 1              | 3              | 2              | 3              | 13             | 5.5             | 6              | Self-Balancing            | Yes             |
| 21       | 12             | 1              | 3              | 4              | 3              | 13             | 6.0             | 6              | Self-Balancing            | Yes             |
| Proposed | 13             | 1              | 3              | 2              | 3              | 13             | 5.16            | 6              | Self-Balancing            | Yes             |

\( N_{\text{switches}} \) - No. of Switches, \( N_{\text{sources}} \) - No. of Sources, \( N_{\text{capacitors}} \) - No of Capacitor, \( \text{PIV,} \text{p.u.} \) - Peak Inverse Voltage, \( N_{\text{level}} \) - No. of Levels, \( \text{TSV,} \text{p.u.} \) - Total Standing Voltage & \( VG \) - Voltage Gain.

FIGURE 6. Components comparison with recent ML’s a. \( N_{s} \), b. \( N_{SDC} \), c. \( N_{c} \), d. \( N_{d} \), e. PIV/LEVEL, f. \( N_{L} \), g. TSV.
V. ANALYSIS OF LOSSES

Generally, three losses are associated with the Multilevel Inverter i.e. a) conduction loss b) Switching loss c) Blocking loss is calculated based on [27]. Based upon the Table I the switches are triggered so each switch is changing from ON to OFF and OFF to ON. Minimum losses are occurred due to this operation. Based upon the various states as shown in Table I the switches are conducted by turning ON the position (0 to ±6Vdc). In the blocking mode, a minimum leakage current is generated and this quantity is very less because this loss occurred when switching components in OFF condition.

From the above definition, the efficiency of the inverter is only based upon the losses which are combined with conduction and switching losses. So the total losses are calculated as

\[ P_{\text{total}} = P_{\text{switching}} + P_{\text{conduction}} \]  \hspace{1cm} (20)

A. CONDUCTION LOSSES

13S-13L inverter topology \( S_1 - S_9 \) \& \( S_1' - S_9' \) are the unidirectional switches. Based upon the switching pattern with carrier signal frequency the instantaneous conduction losses have occurred.

In the current path, the switches and diodes are in ON-state that period is used to determine the conduction losses by the follow equation

\[ P_{L, \text{con}}(t) = P_{L, \text{switch}}(t) + P_{L, \text{diode}}(t) \]  \hspace{1cm} (21)

\[ P_{L, \text{con}}(t) = \left[ V_T + R_T I_0(t) \right] + \left[ V_d + R_d I_p(t) \right] I_p(t) \]  \hspace{1cm} (22)

Where, \( V_T \& V_d \) - Threshold voltage of the semiconductor switches and diodes

\( R_T \& R_d \) - Diode Resistance in ON-State and switch having an equivalent series resistance of the capacitor.

\( I_p \) - Output current at peak value \( I_p \)

\( \beta \) - Constant

B. SWITCHING LOSSES

Based upon the carrier frequency these losses are calculated with individual devices. After calculating the individual losses the total switching loss is determined by adding all switching components of the inverter topology.

The individual switch losses are calculated by applying a general approximation method.

Turn - ON switching loss is calculated as

\[ P_{\text{SW,ON},n} = \int_0^{t_{\text{ON}}} v(t) i(t) dt \]  \hspace{1cm} (24)

\[ = \frac{t_{\text{ON}}}{7} \left[ (t-t_{\text{ON}}) - v_s,n I \right] \]  \hspace{1cm} (25)

Turn-OFF switching loss is calculated as

\[ = \frac{v_s,n H_{\text{OFF}}}{7} \]  \hspace{1cm} (26)

Where

\( v_{s,n} \) - Standing voltage of switches

\( I \) - Current flowing through switches

\( t_{\text{ON}} \& t_{\text{OFF}} \) - ON state and OFF state of switches

To calculate the switching losses of each switch by

\[ P_{L, \text{SW},n} = f_s \left( P_{\text{SW,ON},n} + P_{\text{SW,OFF},n} \right) \]  \hspace{1cm} (27)

\[ = \frac{v_{s,n}(t_{\text{ON}} + t_{\text{OFF}}) f_s}{7} \]
After calculating the total losses of the inverter the efficiency is determined as follows,

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$  \hspace{1cm} (28)$$

Compare to existing topologies minimum switch counts are used to design the proposed 13S-13L topology. So minimum losses have occurred.

The energy stored in the capacitor is mainly due to the variation of the voltage drop, so a suitable selection of capacitor value is given in sec.5.c.

The THD value for different 13- level inverters was discussed in Table VI for the modulation index of 0.9, [15] have the THD value of 19.56%, and [16] have the THD value of 17.34%, and remaining THD values were given in Table VI.

### TABLE IV

| Magnitudes          | Simulation | Experiment |
|---------------------|------------|------------|
| Source Voltage (V_{in}) | 60 V       | 60 V       |
| Load Voltage (V_{L})  | 360 V      | 360 V      |
| Carrier’s frequency  | 2.5 kHz    | 2.5 kHz    |
| Reference signal     | 50 Hz      | 50 Hz      |
| Capacitors           | C_{1} & C_{2} = 820 \mu F, 60V and C_{1} = 1200 \mu F, 180V | C_{1} & C_{2} = 820 \mu F, 60V and C_{1} = 1200 \mu F, 180V |
| Switches             | MOSFET     | N-MOSFET-4* |
|                      |            | IRFB4410PBF |
|                      |            | 9* IXFQ60N50P3 |
| Diodes               | D_{1}, D_{2} | MBR30100CT |
| Load                 | R = 50 \Omega, L = 30 mH | R-L Load bank |

C. SELECTION OF OPTIMAL CAPACITOR VALUE

The longest discharge time (LDT) for one full cycle of the fundamental output voltage, V_{ab} is shown in Fig. 5, which is considered to find the switched capacitor’s C_{1}, C_{2} and C_{3} optimal value.

The energy released by the switched capacitor C_{3} during LDT is computed by

$$Q_{c3} = 2 \times \int_{t_4}^{T} i_o(t) dt$$  \hspace{1cm} (29)$$

The output current (I_{ab}) for R load in the LDT period can be given by

$$i_o(t) = \frac{4V}{R_L} for t_4 \leq t \leq t_5 , i_o(t) = \frac{5V}{R_L} for t_5 \leq t \leq t_6$$ and

$$i_o(t) = \frac{6V}{R_L} for t_6 \leq t \leq \frac{T}{4}$$  \hspace{1cm} (30)$$

The fundamental frequency scheme is employed to find the expressions for the time t_4, t_5, and t_6, which are

$$t_4 = \sin^{-1}\left(\frac{7}{12} \times \frac{1}{2\pi f}\right) , t_5 = \sin^{-1}\left(\frac{9}{12} \times \frac{1}{2\pi f}\right)$$ and

$$t_6 = \sin^{-1}\left(\frac{11}{12} \times \frac{1}{2\pi f}\right)$$  \hspace{1cm} (31)$$

Using (29) - (31), we obtain

$$Q_{c3} = \frac{10V_{dc}}{2\pi f R_L}$$  \hspace{1cm} (32)$$

The switched capacitor’s C_{3} optimal value can be decided by

$$C_{3, opt} \geq \frac{Q_{c3}}{p \times V}$$  \hspace{1cm} (33)$$

Based on (32) and (33)

$$C_{3, opt} \geq \frac{10}{2\pi f \times R_L \times p}$$  \hspace{1cm} (34)$$

The energy released by the switched capacitors C_{1} and C_{2} in the LDT period can be computed by

$$Q_{c1} and Q_{c2} = 2 \times \int_{t_4}^{T} i_o(t) dt$$  \hspace{1cm} (35)$$

Based on (30) and (31), Q_{c1} and Q_{c2} is expressed as

$$Q_{c1} and Q_{c2} = \frac{5V}{2\pi f \times R_L}$$  \hspace{1cm} (36)$$

Based on (33) and (36), the optimal value of capacitance (C_{1, opt} and C_{2, opt}) could be found by

$$C_{1, opt} and C_{2, opt} \geq \frac{5}{2\pi f \times R_L \times p}$$  \hspace{1cm} (37)$$

Where p stands for the maximum permissible capacitor ripple voltage in percent, R_L stands for Resistive load, f stands for the fundamental frequency. Fig. 7(a&b) shows the possible optimal values of C_{1}, C_{2}, and C_{3} for different R loads.

**FIGURE 7.** Variation in optimal capacitor C_{1, opt}, C_{2, opt} and C_{3, opt} with Resistive Load (R Load) for different ripple in capacitor voltage.

For RL load, the output current (I_{ab}) can be expressed as

$$I_{ab} = \frac{V_{dc}}{2\pi f R_L}$$  \hspace{1cm} (38)$$

$$I_{ab} = \frac{V_{dc}}{2\pi f R_L}$$  \hspace{1cm} (39)$$

$$I_{ab} = \frac{V_{dc}}{2\pi f R_L}$$  \hspace{1cm} (40)$$

$$I_{ab} = \frac{V_{dc}}{2\pi f R_L}$$  \hspace{1cm} (41)$$
\[ i_a(t) = I_{o,max} \sin(o_1 - \varphi) \]  \hspace{1cm} (38)

Where \( \varphi \) is the phase angle between the fundamental output voltage (\( V_{ab} \)) and current (\( I_{ab} \))

From the equation (29), (31), and (38), we get \( Q_{c3} \) as

\[ Q_{c3} = \frac{2}{\pi} \int_{0}^{T} I_{o,max} \sin(o_1 - \varphi) dt \]

\[ Q_{c3} = \frac{I_{o,max}}{2\pi f} \left[ \cos(0.63 - \varphi) - \sin(\varphi) \right] \]  \hspace{1cm} (39)

From (33) and (39),

\[ C_{3,\text{opt}} \geq \frac{I_{o,max}}{2\pi f \times V \times p} \left[ \cos(0.63 - \varphi) - \sin(\varphi) \right] \]  \hspace{1cm} (40)

From (30), (35) and (38) we get \( Q_{c1} \) and \( Q_{c2} \)

\[ Q_{c1} \text{ and } Q_{c2} = \frac{2}{\pi} \int_{0}^{T} I_{o,max} \sin(o_1 - \varphi) dt \]  \hspace{1cm} (41)

\[ C_{1,\text{opt}} \text{ and } C_{2,\text{opt}} \geq \frac{I_{o,max}}{2\pi f \times V \times p} \left[ \cos(1.16 - \varphi) - \sin(\varphi) \right] \]  \hspace{1cm} (42)

Compared to [20] – [24], the 13S-13L inverter gives a low ripple value for capacitors \( C_1 \), \( C_2 \) and \( C_3 \). The \( C_1 \) and \( C_2 \) have a ripple of 1.33% and \( C_3 \) has ripple of 1.66% which is evaluated from simulation results shown in Fig. 8(c, d, e).

VI. RESULTS AND DISCUSSION

The simulation results are presented for 13S-13L inverter in Fig. 8. The \( V_{ab} \) and \( I_{ab} \) for RL load (\( R=50 \Omega \) and \( L=60 \text{ mH} \)) are 360 V and 5.6 A respectively as shown in Fig. 8a. For R load (\( R=50 \Omega \)), the \( I_{ab} \) is 6.9 A as shown in Fig. 8b. The simulated capacitor waveforms are shown in Fig. 8(c, d, e) for the modulation index of 0.95. For both RL load and R load, \( V_{ab} \) and \( I_{ab} \) for different modulation indexes are shown in Fig. 8f. THD without optimization for various modulation indexes is shown in Fig.9.

To demonstrate the significance and contribution in the proposed 13S-13L multilevel inverter, a less complex and efficient model has been built, studied, and evaluated. Discrete N-channel MOSFET 4* IRFP240PBF and 9* IXFH18N60X is used to design the proposed model that operates with an input voltage of 60 V. The PSO optimized selective harmonic elimination has been implemented by using an FPGA controller of SPARTAN 6E, where the carrier frequency is about 2.5 kHz and reference frequency or base frequency of 50 Hz.
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FIGURE 8. Simulation results for modulation index 0.95. a. $V_{ab}$ and $I_{ab}$ with RL load (50 Ω and $L=60$ mH), b. $V_{ab}$ and $I_{ab}$ with R load (50 Ω), c, d, e. capacitor voltage and current waveforms, f. $V_{ab}$ and $I_{ab}$ for different modulation index and different load condition.

FIGURE 9. Shown as the THD value for without optimization. a. MI=0.9 b. MI=0.75 c. MI=0.35.

TABLE V
FIRING ANGLE FOR DIFFERENT MODULATION INDEX

| Harmonic Order up to 3 | N | $\alpha_1$ (deg.) | $\alpha_2$ (deg.) | $\alpha_3$ (deg.) | $\alpha_4$ (deg.) | $\alpha_5$ (deg.) | $\alpha_6$ (deg.) |
|------------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| MI=0.9                 | 13| 4.91              | 16.65             | 28.47             | 41.28             | 58.85             | 87.21             |
| MI=0.75               | 9 | 9.20              | 14.20             | 32.20             | 39.60             | -                 | -                 |
| MI=0.35               | 7 | 11.33             | 18.34             | 35.60             | -                 | -                 | -                 |

For SHE, the generated six firing angles are given to microcontroller FPGA SPARTAN 6E to vary the angle of the carrier signal which results in low THD is given in Table V. After using the optimized angles, the THD has been reduced as shown in Fig. 10. The optimized switching angle versus modulation index plot is shown in Fig.11a and the plot for variation of harmonics versus modulation index is shown in Fig. 10b. The six-firing angle helps to minimize the THD significantly. The proposed 13-level inverter is loaded with Resistive Inductive load while R=50 Ω & L=60 mH are demonstrated in Table IV. It shows the $V_{ab}$ of 360 V, $I_{ab}$ of 5.6 A, and then capacitance-voltage of $C_1$, $C_2$, and $C_3$ are

FIGURE 10. Shows THD with PSO optimized firing angle for a. MI=0.9 b. MI=0.75 c. MI=0.35.

FIGURE 11. (a) Optimized switching angles (Vs) modulation index (b) Variation of harmonics (Vs) modulation index for 0.75.

TABLE VI
COMPARISON OF THD WITH OTHER 13-LEVEL INVERTER

| Topology | Total Harmonics Distortion |
|----------|----------------------------|
| 15       | 19.56%                     |
| 16       | 17.34%                     |
| 17       | 13.45%                     |
| 20       | 15.87%                     |
| 21       | 16.89%                     |
| Proposed | 6.12%                      |
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Figure 12. Shows (a). Hardware prototype (b). Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω and L=60 mH) RL Load, (c). Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω) R Load, (d) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω and L=60 mH) RL Load after 0.04sec. R is decreased to 30 Ω, (e). Capacitor Voltages $V_{c1}$, $V_{c2}$ and $V_{c3}$ (f). Ripple voltage of capacitor $V_{c1}$, $V_{c2}$ & $V_{c3}$ (g) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=30 Ω) R Load after 0.04sec. No load after 0.10sec. R is increased to 50 Ω and L=60 mH is added, (h) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω and L=60 mH) RL Load after 0.04sec. Inductor is removed, (i) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=30 Ω and L=60 mH) RL Load after 0.04sec. No load after 0.10sec. R is increased to 50 Ω, (j) zoomed $V_{ab}$, $I_{ab}$ with (R=50 Ω) after 0.04sec. 50 mH inductor is added, (k),(l) THD spectrum without optimization for M. I=0.9 and 0.75 with 50 Hz.
Figure 13. Shows (a) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω and L=60 mH) RL Load, (b) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω) R Load, (c) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω) R Load after 0.04sec. No Load after 0.10sec. inductor is added to 60 mH, (d) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=30 Ω and L=60 mH) RL Load after 0.04sec. R is increased, (e) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=30 Ω) R Load after 0.04sec. R is increased to 50 Ω, (f) Hardware Results showing $V_{ab}$ and $I_{ab}$ with (R=50 Ω) R Load after 0.04sec. No Load after 0.10sec. R is decreased to 30 Ω, (g) zoomed output $V_{ab}$ and $I_{ab}$ with (R=50 Ω and L=60 mH) RL Load after 0.04sec. inductor is removed for Modulation index=0.75. (h) & (i). shows THD with PSO Optimized Firing Angle for M. I= 0.9 and 0.75.

Figure 14. (a). Shown as the voltage stress across each switch (b) current stress across each switch.
recorded while the voltage of capacitor C1 and C2 was 60 V and then C3 was 180 V respectively. The ripple voltage of capacitor Vc1, Vc2, and Vc3 are shown in Fig. 12f with modulation index 0.9. Initially, the Lab is 5.3 A for the R-L Load R=50 Ω and L=60 mH, after 0.04s resistance value is reduced to 30 Ω and the current is 7.7 A for the modulation index 0.9. Initially, the Lab clocks around 5.3 A for the RL Load R=50 Ω and L=60 mH for about 0.04 sec, and thereafter the inductance is removed are shown in Fig. 12h. The experimental waveform is exhibited in Fig. 12 and the proposed topology was validated by the FPGA SPARTAN 6E controller. For the modulation index of 0.75 and Vab of 180 V results are shown in Fig. 13a and the voltage of the capacitor remains unchanged, so C1 and C2 is 60 V and the capacitor C3 is 180 V are shown in Fig. 13c. The load magnitudes like voltage and current waveforms and the capacitor voltage in the modulation index range of 0.9 and 0.75 are depicted in Fig. 12 and 13 respectively. The voltage stress of each switch is shown as in Fig. 14a of Switch S1, S1 and S2, S2 is 100 V, and their remaining switch S3-S6 is 300 V. Fig. 14b presents the current stress of switches S1, S1, S2, S2 are 2.8 A, S2 is 1.3 A and S3-S6 are 3.5 A. After finding the six-firing angle through the FPGA SPARTAN 6E controller and noting the THD value shown in Fig. 13 (h & i). As compared to another 13-level inverter [17], [20], [21], the proposed model has a better THD value as illustrated in Table VI. The TSV is clearly shown in Table II and also cost comparison with other recent 13-level inverter are discussed in Table III. Further, the switching losses and conduction losses for switches and diodes are explained in sec. V. A thermal model is built with the help of PLECS, and the simulated peak efficiency is 97.5% of the proposed topology at 2 kW. For the topology [20] is 95.9%, for the topology [21] is 96.7% and for the topology [22] is 95.5%. The proposed topology gives better efficiency than other recent 13-level inverters.

6. Conclusion

An efficient and novel sextuple voltage boosting 13-level multilevel has been presented in this paper. The proposed topology has been designed as simplistic with a minimum of 13 switch counts, three capacitors, and two diodes with a single DC source. The SHE with PSO is employed to obtain six firing angles to minimize the lower order harmonics that cause lower THD value as the literature suggests. One of the prominent and key contributions of the model is the switched capacitor voltage could be effectively balanced by a simple series/parallel combination without any additional circuit/sensor. The Proposed 13-Level inverter has been well analyzed and studied with various multicarrier PWM and the optimal PWM was recommended in Table IV. Finally, the prominence of the proposed 13-level inverter was well established through the above-mentioned methods in terms of low THD.

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