Suppressing Voltage Spikes of MOSFET in H-Bridge Inverter Circuit

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Abstract: Power electronics devices are made from semiconductor switches such as thyristors, MOSFETs, and diodes, along with passive elements of inductors, capacitors, and resistors, and integrated circuits. They are heavily used in power processing for applications in computing, communication, medical electronics, appliance control, and as converters in high power DC and AC transmission in what is now called harmonized AC/DC networks. A converter’s operation is described as a periodic sequencing of different modes of operation corresponding to different topologies interfaced to filters made of passive elements. The performance of converters has improved considerably using high switching frequency, which leads to a significant improvement in a power converter’s performance. However, the high dv/dt through a fast-switching transient of the MOSFET is associated with parasitic components generating oscillations and voltage spikes having adverse effects on the operation of complementary switches, thereby affecting the safe operation of the power devices. In this paper, the MOSFET gate-driver circuit performance is improved to suppress the H-Bridge inverter’s voltage spikes. The proposed technique is a simple improvement to the gate driver based on the IR2112 driver (IC) by adding a capacitor to attenuate the effect of parasitic components and the freewheeling current, suppressing the negative voltage spikes. This paper’s main contribution is to improve the gate driver circuit’s capability for suppressing the voltage spikes in the H-Bridge inverter. The improved gate driver circuit is validated experimentally and is compared with the conventional gate driver. The experimental results show that the proposed technique can effectively suppress the MOSFET’s voltage spikes and oscillations.

Keywords: H-Bridge inverter; voltage spikes; power switches; gate driving circuit

1. Introduction

Producing high-quality output waveforms from Multilevel Inverter (MLI) has been challenging for researchers working in the area. The high-quality output results from reduced switching losses in the power semiconductors and for improving output waveform [1–4]. With the rapid development of the power transistor industry, fast switching
frequency speed has greatly increased. Although higher switching frequency guarantees quality output, it increases switching losses. However, by applying high switching speed, the parasitic parameters such as parasitic capacitance and inductance with the PCB traces become crucial factors that mainly affect the power transistors’ performance. Therefore, it is important to analyze these parasitic components’ effect and calculate the loss of the MOSFET accurately. One has to engage in a tradeoff between the two situations when it comes to implementing power converters. On the other hand, H-Bridge inverters have suffered from voltage spikes in their output signals. These spikes have undesirable effects such as phonetic noise and harmonic heating losses, semiconductors switching power losses, and mechanical vibrations [5,6]. On the other hand, the parasitic inductance can boost the voltage overshoot, leading to total harmonic distortion. It is important to eliminate the parasitic resonance to improve the H-Bridge converter’s performance and mitigate the effect of the total harmonic distortion [7]. A root locus technique has been used with an RC snubber circuit design in Reference [8] for a double pulse circuit of the SiC MOSFET by ignoring the parasitic inductance source. Simultaneous switching of these devices can generate a high voltage spike and high dv/dt at the inverters’ output terminal. This high voltage spike may easily damage the power switches. In practical operation of H-Bridge converter during ON/OFF transient of one MOSFET under fast switching conditions will produce voltage spikes on its complementary MOSFET [9–14]. Several techniques have been used to suppress the effect of voltage spikes [15,16]. Reference [17] proposed controlled gate resistance to mitigate the voltage spikes. However, it needs to use feedback control, which leads to a relative time delay. A level shift circuit is proposed in Reference [18] to produce a negative gate voltage to suppress the positive gate spikes; however, this negative gate voltage considers a risk to damage the MOSFET. In [19–23], Snubber circuits have been utilized with semiconductor devices to absorb the high dv/dt energy and reduce harmonic spikes. The voltage spikes will increase due to the reverse load current by increasing the load current [24]. Developing a gate driver of SiC MOSFET will eliminate the gate-source voltage spike. A series of capacitors have been connected to the gate of a MOSFET transistor by an auxiliary transistor to absorb the negative voltage spike when the complementary power transistor is turned off [25]. In [26], a new active driver circuit is proposed for the MOSFET transistor to absorb the effect of turn-off spikes and oscillation. Another technique is proposed to reduce positive voltage spikes by using an auxiliary transistor for controlling JFET. However, this technique cannot mitigate negative voltage spikes [27]. The soft gate technique and active driver-controlled circuit are presented in Reference [28]. A novel technique for the driver gate controller to suppress the negative voltage spikes is introduced in Reference [29]. In the turn off state and due to the voltage rising across the MOSFET, charging current stream via its parasitic capacitance leads to inducing positive voltage spikes at the gate. If the voltage of these spikes overrun gate threshold voltage, the high side of the MOSFET could be falsely triggering. The gate impedance monitoring method has been used to decrease the gate voltage spikes in order to provide a low impedance path by added external gate-source capacitance [30,31].

This paper presents a new design to suppress the voltage spikes by improving the MOSFET gate driver circuit in the H-Bridge circuit based on the integrated circuit IR2112. The performance of the proposed technique has been evaluated experimentally.

2. H-Bridge Inverter

The H-Bridge inverter is the most common inverter used to convert DC to AC, as shown in Figure 1. Two power switches in a complementary manner are used in each leg of the H-Bridge circuit, which can be controlled (ON/OFF) using modulation signals such as Sinusoidal Pulse Width Modulation (SPWM) or Selective Harmonic Elimination (SHE) technique [32,33]. Each H-Bridge topology unit can generate three-level output voltages, +Vdc, 0, and −Vdc.
Operating Principle

In power switching applications, switching losses at most are dependent on switching speed. Thus, the switching characteristic is the most important in the high-power switching application. In addition, a voltage spike is a very significant issue that affects the performance of the power inverter adversely, and it is presented and addressed in this paper using the proposed approach to design and improved high-performance gate drive circuits based on the gate driver IR2112 for high-efficiency and high-power, switching applications using a power MOSFET and IGBT.

3. Proposed Technique

Figure 2 shows the circuit diagram of the half-bridge circuit with driver IR2112, which drives the power transistors. This integrated circuit has a high-performance and high voltage driver for power switches with two independent channels for high side and low side output. By adding an external bootstrap capacitor (CBOOT) and bootstrap diode (DBOOT), the driver provides a high switching speed [34]. The High Side Floating Voltage (VS) of the IR2112 driver is already connected to the output via the upper transistor source (Q1). When the low side channel (LO) is turned ON, the lower MOSFET (Q2) will be ON, and the high side (HO) turned OFF, the upper MOSFET (Q1) will be OFF. In this case, the VS pin will get connected to the ground via a lower transistor (Q2). The CBOOT capacitor starts charging up via the DBOOT from the VCC source, as shown in Figure 3. [35]. The highest voltage charges from CBOOT are dependent on the voltage value of the VCC source. The equivalent schematic of the MOSFET parasitic components in a half-bridge circuit is shown in Figure 4.
This circuit’s biggest issue is the negative voltage spike existent at the switching device source during the OFF state that causes load current flow suddenly in the low-side freewheeling diode. This negative spike can defect the gate driver’s output because it directly affects the source VS pin of the driver or PWM control IC and might pull some of the internal circuitry significantly below ground, as shown in Figure 5. The other problem caused by the negative voltage transient is developing an over-voltage condition across the bootstrap capacitor. Given the fast-rising drain-source voltage, the parasitic capacitances
of a MOSFET cause a negative voltage spike during switching transitions and may result in spurious turn-on if it exceeds the threshold voltage. When the upper MOSFET turns ON, the current flow between the drain and source leads to induce the parasitic capacitor \( C_{dg} \) in the lower MOSFET, and it will motivate the gate-source capacitor \( C_{gs} \) to charge up. Therefore, it will push up the lower MOSFET’s gate voltage and generate a positive pseudo pulse. On the other side, when the lower MOSFET is turned ON, and the upper switch is turned OFF, a negative pseudo voltage will generate between the lower MOSFET gate and source, as shown in Figure 6 [36].

Figure 5. VS signal and negative spike at turn off condition.

Figure 6. Cont.
When the power source Vcc of the driver is referenced to the ground, the maximum voltage that can build on the CBoot capacitor is the sum of Vcc and the amplitude of the negative voltage at VS pin. Figure 7 illustrates the waveforms of the high-side MOSFET during the OFF state. The negative voltage spike's amplitude is proportional to the parasitic inductances and the turn-off speed, di/dt. Sum of Cgs and Cgd, called Miller capacitance. The biggest problem is when the VS goes below ground significantly, and therefore, the gate drive suffers damage.

Figure 7. Voltage spike during turned OFF state of the upper MOSFET.
4. Proposed Design to Suppress Voltage Spikes

The proposed design is used to reduce \( \frac{dv}{dt} \) at the power switches’ transition and suppress the voltage spikes from the output voltage signal. The gate driver circuit is based on the integrated circuit IR2112. The driver connects to the H-Bridge inverter’s power transistor via three terminals: \( Ho_\) gate signal of the upper transistor, \( Lo_\) gate signal of the lower transistor, and \( VS \) feedback signal between the source of the top transistor and the drain of the lower transistor.

When the upper MOSFET is turned OFF and the lower MOSFET is turned ON, the \( VS \) pin connection will be connected to the ground via a lower transistor. Therefore, most of the load current (freewheel current) will flow suddenly through the lower MOSFET’s internal diode. Hence, a negative voltage spike will appear at \( VS \)-pin, as shown in Figure 8. This negative spike will develop across the \( C_{BOOT} \) capacitor, reaching maximum amplitude as the sum of VCC source and the negative spike’s amplitude. At the same time, part of the load current will flow through the parasitic gate-source capacitance \( C_{gs} \) of the lower transistor \( Q_2 \), which leads to charge the capacitor \( C_{gs} \). In this case, the gate voltage will push up and generate another harmful gate-source spurious voltage pulse. The voltage spikes issue has occurred during the transient process of the complementary switches of the H-Bridge inverter. The voltage spikes’ value depends on the source voltage and ON time of the duty cycle.

![Figure 8. Load current direction and negative spike at the turn off condition.](image)

To give the mathematical modeling of the voltage spikes and oscillation conditions, the turn off process of the MOSFET has been analyzed depending on Figure 9. An ideal MOSFET transistor consists of a gate-drain capacitance \( (C_{gd}) \), drain-source capacitance \( (C_{ds}) \), gate-source capacitance \( (C_{gs}) \), and internal diode with the parasitic inductance \( (L_D, L_S) \). However, \( R_g \) is the gate driver resistance. During turn-off condition of the MOSFET, \( C_{gs} \) capacitance starts discharge via \( R_g \) resistance, leading to decreased gate-source voltage \( V_{gs} \).
Figure 9. Equivalent circuit of the MOSFET transistor.

Therefore, the pseudo-gate-source voltage of the MOSFET can be based on Reference [25]:

\[ i_{C_{gs}} = C_{gs} \frac{dV_{C_{gs}}}{dt} \]  
(1)

\[ i_{C_{dg}} = C_{dg} \frac{dV_{C_{dg}}}{dt} \]  
(2)

\[ V_s = V_{C_{gs}} + V_{C_{dg}} \]  
(3)

where: \( C_{gs}, C_{dg}, C_{ds} \) MOSFET parasitic capacitance; \( V_{C_{gs}} \) is the maximum charge value of the \( C_{gs} \) capacitor, and \( V_{C_{dg}} \) is the maximum charge value of the \( C_{ds} \) capacitor.

\[ V_{C_{gs}(max)} = \frac{V_s}{1 + C_{gs}/C_{dg}} \]  
(4)

While the drain current \( i_d \) starts falling, the load current moves out to the freewheeling diode (FWD), as illustrated in Equations (5) and (6). Additional to the voltage spikes, the drain current \( i_d \) composes oscillation due to the parasitic components of the MOSFET in the power loop at turn-off operation [26].

\[ i_d = g_m (V_{gs} - V_{th}) \]  
(5)

\[ \frac{di_d}{dt} = g_m \frac{dV_{gs}}{dt} \]  
(6)

where: \( i_d \) is the drain current; \( g_m \) is the transconductance.

These issues of voltage spikes will affect the MOSFET through their gate signals. The spikes’ entrance into the circuit may lead to the failure of the switches and damage to the IC driver. Besides, these spikes will show up on the output voltage waveform of the inverter. They may create more problems to the load in the form of electromagnet interference and harmonic-related heating effects.

To tackle the issue of a negative voltage spike, a new capacitor CA is added to the driver IR2112 between VS-pin and the ground to absorb these spikes effectively, as shown in Figure 10. This capacitor’s main objective is to suppress the negative voltage spike,
which appears at VS pin of IR2112, to improve the output voltage signal’s quality and reduce voltage spikes.

![Proposed design to remove the voltage spikes.](image)

Figure 10. Proposed design to remove the voltage spikes.

This capacitor CA provides a low impedance loop to the reverse load current during the transient condition of the upper transistor, leading to suppressing the voltage spikes. At OFF state (when Q1 is OFF), VS pin is connected to the ground via Q2. However, at the ON state (Q1 is ON), the voltage of VS equals the DC source’s voltage, and the voltage-time of this point depends on the duty cycle of PWM. The equivalent circuit of the proposed scheme at the turn off state is shown in Figure 11. Therefore, the new capacitor CA value can be calculated depending on the DC voltage source and ton of the duty cycle.

![The equivalent circuit of the proposed capacitor with the MOSFET parasitic parameters.](image)

Figure 11. The equivalent circuit of the proposed capacitor with the MOSFET parasitic parameters.

According to Kirchhoff’s voltage law (KVL) gives:

\[ V_{LD} + V_{LS} + V_{Cds} = V_S \]  
\[ LD \frac{di}{dt} + LS \frac{di}{dt} + \frac{1}{C_{ds}} \int idt = V_S \]  
\[ (LD + LS) \frac{di}{dt} + \frac{1}{C_{ds}} \int idt = V_S \]
Applying a Laplace transform and solving the differential equation,

\[ S(LD + LS)I(S) + \frac{1}{SC_{ds}}I(S) = V_S(S) \]  

(10)

\[ S^2[(LD + LS)C_{ds} + 1]I(S) = V_S(S) \]  

(11)

\[ V_S = \frac{1}{C_A} \int idt \]  

(12)

\[ C_A = \frac{1}{V_S} \int_{t_1}^{t_2} idt, \ t = t_{on} \]  

(13)

where:

- \( t_1 \) and \( t_2 \) is the ON time at the period time of PWM;
- \( LD \) is the Internal Drain Inductance;
- \( LS \) is the Internal Source Inductance;
- \( CA \) is the external capacitor;
- \( V_S \) is the voltage at VS pin.

\[ t_{1,2} = \frac{\alpha_1}{f_s \times 360} \]  

(14)

where: \( f_s \) is the switching frequency.

5. Experimental Verification

The proposed gate driver circuit was implemented and tested for the H-Bridge inverter, where the inductive load was utilized to verify the proposed design’s effectiveness for the suppression of the voltage spike and oscillation, as shown in Figure 12. In the experimental prototype, MOSFET IRF640 and IC driver IR2112 were used. An Arduino Uno board was used to generate PWM. The experimental parameters of the design circuit are listed in Table 1.

![Figure 12. The hardware setup of a proposed H-Bridge inverter circuit.](image)

Table 1. The experimental parameters.

| Parameter          | Value         |
|--------------------|---------------|
| DC voltage         | 12 V          |
| Switching frequency| 50 Hz & 10 kHz|
| Load inductance    | 100 µH        |
| Load Resistance    | 100 Ω         |
| Gate resistor R    | 10 Ω          |
6. Experimental Results

A 50 Hz and 10 kHz switching frequency was used to operate the inverter circuit to address the effect of negative voltage spikes and the oscillation of the H-Bridge inverter of renewable energy application.

6.1. 50 Hz Switching Results

Figure 13 shows the negative spike at VS pin in a conventional gate drive circuit before using the proposed design. It can be seen that the voltage of the negative spike at V-Spike is 2.5 V.

![Figure 13](image_url)

**Figure 13.** The voltage spike at VS pin for a conventional gate driver circuit, switching frequency $f_s = 50$ Hz.

The gate-source voltage and the drain-source voltage signals for a conventional gate drive circuit and the proposed driver circuit are shown in Figures 14 and 15. Comparing the results of Figures 14 and 15, after improving the driver circuit, the oscillation and the voltage spike amplitude have been mitigated from 10.40 V to 1.50 V.

![Figure 14](image_url)

**Figure 14.** Gate-source and drain-source voltage of the conventional drive circuit for switching frequency $f_s = 50$ Hz.
Figure 15. Gate-source and drain-source voltage signal after improved the drive circuit or switching frequency $f_s = 50$ Hz.

### 6.2. 10 KHz Switching Frequency

By using 10 kHz as a switching frequency for the H-Bridge DC to AC inverter, Figure 16 shows the signal at VS pin during OFF state for conventional gate drive.

Figure 16 shows that the negative voltage spike at switching frequency 10 kHz is less than when the switching frequency is 50 Hz with 2.22 V and 2.50 V, respectively. The gate-source voltage $V_{gs}$ and drain-source voltage $V_{ds}$ waveform are shown in Figure 17 under switching frequency $f_s = 10$ kHz. The voltage spike is raised to 13 V with high oscillation for the drain-source voltage. By increasing the switching frequency, the voltage spikes and the overshoot oscillation are increased on drain-source voltage $U_{ds}$. However, the negative voltage spike at VS pin is decreased when the switching frequency increases.
The experimental prototype in Figure 10 has been utilized to verify the proposed scheme’s effect for the output voltage waveform of the H-Bridge inverter. Figure 18 illustrates the output voltage waveform with the conventional gate driver circuit before improving the driver. The output voltage signal is affected by the positive and negative voltage spikes, which lead to more issues for power transistors and the load system.

On the other hand, the proposed scheme’s performance for mitigating the voltage spikes of the output voltage waveform of the H-Bridge is presented in Figure 19. In the proposed design, both the positive and negative voltage spikes have been removed from the output voltage signal to a considerably good level.
Figure 19. The experimental results of the proposed design for the H-Bridge output voltage waveform.

7. Comparison of MOSFET Gate Driver Techniques for Suppressing Voltage Spikes

A comparison with different methods is presented in References [13–17] to show the proposed scheme’s advantage. These techniques can improve the performance on some sides. However, they all have some disadvantages in other aspects. Table 2 illustrates the comparison between different techniques for the capability of suppressing voltage spikes. This paper’s proposed method has superior characteristics compared to other gate drivers in terms of the voltage spikes suppression capability and the simplicity in design.

| Reference | Proposed Technique | Suppressing of Positive Voltage Spike | Suppressing of Negative Voltage Spike |
|-----------|--------------------|--------------------------------------|--------------------------------------|
| [9]       | A new gate drive based on adjustment of magnetic bead’s | No                                   | Yes                                  |
| [18]      | RCD level-shifter for bridge-leg configuration | Yes                                  | No                                   |
| [25]      | A passive triggered transistor with a series capacitor to suppress the negative voltage spikes | Yes                                  | Yes                                  |
| [26]      | Active Gate Driver for MOSFET to Suppress Turn-Off Spike and Oscillation | No                                   | Yes                                  |
| The proposed | Improvement of gate driver circuit for MOSFET | Yes                                  | Yes                                  |

8. Conclusions

A gate driver circuit for the H-Bridge inverter based on the integrated circuit IR2112 was proposed to suppress the voltage spikes. The proposed gate driver circuit’s performance and efficiency have been validated and tested experimentally by leading IRF640 MOSFET on the H-Bridge DC-AC inverter at a switching frequency of 50 Hz and 10 kHz. The design has been efficient in reducing pins’ impact on the inverter circuit’s output; however, unavoidable parasitic components impacted its ability to demonstrate its effectiveness in eliminating the voltage spikes. The findings of this research can be applied in renewable electronics. Moreover, such results are suitable for running the solar source-operated induction motors used in electric vehicles.
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