A Low Power Pre-Setting Based Sub-Radix-2 Approximation for Multi-bit/cycle SAR ADCs

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ABSTRACT A pre-setting based sub-radix-2 approximation technique for multi-bit/cycle successive-approximation-register (SAR) analog to digital converters (ADCs) is proposed in this paper. The proposed approximation technique enhances the conversion speed and relieves the power hungry reference voltage buffer. The sub-radix-2 approximation only adjusts the weights of original binary DAC array without introducing additional unit capacitors and leading to reduced silicon area and power consumption. An adder based encoding circuit is proposed, with negligible power and silicon area overhead. Furthermore, the non-ideal DNL/INL, which are caused by incomplete DAC settling, are characterized and analysed in this paper. The peak DNL/INL values are symmetrically located at 1/4 and 3/4 of full scale. With the presence of sub-radix-2 approximation, the peak INL/DNL could be significantly reduced. The simulation results show the better performance of sub-radix-2 approximation than binary approximation. Designed in CMOS 40nm technology, it could keep a higher (>9.5-bit) effective number of bits (ENOB) with short settling time of DAC buffer, and boost the sampling rate equivalently.

INDEX TERMS 2b/cycle, ADCs, non-binary, SAR, sub-radix-2.

I. INTRODUCTION
The development of high-speed communication and data acquisition requires the ADCs to obtain higher resolution and higher speed while keeping low power consumption. The trend of 802.11 standards is towards higher bandwidth (80∼160MHz for 802.11ac) and higher SNR requirement. It has been proven that successive approximation register (SAR) ADCs have better power efficiency for certain ADC resolutions [1]–[6]. However, the state-of-the-art single channel 10-bit SAR ADC [6] is approaching the speed limitation, which operates at 240MS/s with speed-enhanced redundant conversion in 28nm CMOS. To achieve higher sampling rate in SAR ADCs, 2-bit/cycle structure are widely used [8]–[10]. For the conventional binary approximation 2b/cycle ADCs [8], the conversion rate is limited by accuracy, without error tolerant scheme. A non-binary 2b/cycle solution is reported in [9], resulting in 1GS/s 7-bit single- channel ADC without interlaving. However, an extra redundant range of 10 LSBs was added into the entire DAC. A similar redundancy technique could be found in a 1bit/cycle SAR ADC in [2]. Another redundancy technique for 2b/cycle SAR ADC with time domain quantization was presented in [14].

This paper proposes a sub-radix-2 approximation technique for 2b/cycle SAR ADCs, which needs no extra redundant unit capacitors. The DAC size is maintained as same as the binary approximation scheme, only the weights of each branch are changed with redundancy embedded. The non-binary digital outputs are converted to binary code by adders based low power encoding circuit. The remainder of the paper is divided into four sections. Section II briefly introduces the first-order model of incomplete DAC settling in 2b/cycle SAR ADC. In Section III, the sub-radix-2 approximation of 2b/cycle SAR ADC is described. The simulation results are given in Section IV. Finally the conclusion is drawn in Section V.

II. MODELLING OF INCOMPLETE DAC SETTLING
For conventional binary-weighted SAR ADCs, the DAC settling of each cycle must satisfy the accuracy requirement.
Otherwise, the conversion error occurs. For a 10-bit 2b/cycle SAR ADC, shown in Fig. 1. The DAC settling of \(i\)-th branch should meet the condition:

\[
V_{REF} \cdot e^{-\frac{t_{set}}{\tau}} \cdot \frac{C_i}{C_{DAC}} < \frac{1}{2} \text{LSB}_{10\text{-bit}},
\]

where \(\tau\) is the time constant of DAC buffer, \(V_{REF}\) is the reference voltage, \(t_{set}\) is the time allocated for DAC settling, \(C_i\) is the capacitance of \(i\)-th branch and \(C_{DAC}\) is the total DAC capacitance. The time constant \(\tau\) equals switch on-resistance multiply DAC branch capacitance. Here, it is assumed that the time constant \(\tau\) of DAC buffer driving from 0 to \(V_{REF}\) is the same as that from \(V_{REF}\) to 0 for all DAC branches (without mismatch). For the binary DAC settling of \(i\)-th conversion, the \(t_{set}\) should satisfy that

\[
t_{set} > \ln\left(\frac{C_i}{C_{DAC}} \cdot 2^{11}\right) \cdot \tau.
\]

By adopting sub-radix-2 searching algorithm, the settling accuracy requirement could be reduced substantially. Suppose that the settling redundant ratio of \(i\)-th comparison is \(r_i\), then if

\[
V_{REF} \cdot e^{-\frac{t_{set}}{\tau}} \cdot \frac{C_i}{C_{DAC}} < r_i V_{REF+}, \quad i = 1, 2, \ldots,
\]

no settling error occurs [11]. Then, the \(t_{set}\) needs to satisfy

\[
t_{set} > \ln\left(\frac{C_i}{C_{DAC}} \cdot \frac{1}{r_i}\right) \cdot \tau
\]

where \(r_i\) is the redundant ratio of \(i\)-th conversion. In addition, since the settling accuracy requirement is much reduced. Therefore, the bandwidth of the reference voltage buffer could be smaller, resulting in lower power consumption.

### III. SUB-RADIX-2 APPROXIMATION FOR A 2B/CYCLE SAR ADC

The block diagram of the proposed 2b/cycle SAR ADC with sub-radix-2 DAC arrays is shown in Fig. 2. Only two capacitive DACs (CDACs) array are adopted due to first-stage interpolated pre-amplifier A2. Further, there is a second-stage interpolated comparator (C2 or C4) between every two adjacent pre-amplifiers (A1, A2 or A2, A3) to increase the resolution by 2 bits. During the first five conversion cycles, the dynamic comparators Co2 and Co4 are powered down, and only activated in the last cycle. Similarly, the comparators Co1, Co3, Co5 are powered down at last cycle. Therefore, only 3 dynamic comparators are activated.

![FIGURE 1. Illustration of first-order DAC settling model of 2b/cycle SAR ADC.](image1)

![FIGURE 2. The architecture of the 2b/cycle SAR ADC, including sub-radix-2 DAC array, interpolated pre-amplifier and comparators.](image2)
FIGURE 3. Illustration of the non-binary 2b/cycle approximation algorithm architecture.

in each cycle without extra power wasted. The two-stage interpolation reduces the resolution of the CDACs by 2 bits. Compared to binary approximation [12], one more conversion cycle is required. In Fig. 2, the branch ratio of the DAC array is $C_1:C_{1r}:C_2:C_{2r}:C_3:C_{3r}:C_4:C_{4r}:C_5 = 64:56:20:18:6:5:2:1:1$. Basically, $C_i$ ($i = 1, 2, 3, 4, 5$) is used for threshold pre-setting, while $C_{ir}$ ($i = 1, 2, 3, 4$) contributes the redundant values. To describe the operation of the proposed sub-radix-2 approximation scheme, one example with an input of 550.5 LSBs is illustrated in Fig. 3. The threshold values indicated in blue are generated by CDACs, while the threshold values in red at the last cycle are generated by interpolation of dynamic comparators $Co2$ and $Co4$ (Fig. 2). From Fig. 3, it also can be seen that the redundant value from MSB to LSB conversion are 64 LSBs, 16 LSBs, 8 LSBs, 8 LSBs, 0 LSBs and 0 LSBs, respectively. The redundant values are generated by the switching of the DAC array, which will be illustrated in Fig. 4. Overall, one conversion includes six cycles with 2 bits solved in each cycle. Therefore, a set of 12-bit sub-radix-2 code is produced in one data conversion.

TABLE 1. Equivalent weights of sub-radix-2 DAC.

| Output Bits Per Cycle | Settled Capacitance | Weights (8-bit resolution) | Weights (10-bit resolution) |
|-----------------------|---------------------|---------------------------|-----------------------------|
| $D_{n+1}D_n$ ($k=10, 8, 6, 4$) | $C_r, C_{ir}$ | $(C+2C_r)$ | $4*(C+2C_r)$ |
| $10$ | $C, C_{ir}$ | $(C+C_{ir})$ | $4*(C+C_{ir})$ |
| $01$ | $C_{ir}$ | $C_{ir}$ | $4*C_{ir}$ |

TABLE 2. Relation between non-binary bits and binary weights.

| Non-Binary Bit | Sum of Binary Weights |
|----------------|-----------------------|
| $D11$ | $256+128+64+32$ |
| $D10$ | $128+64+32$ |
| $D9$ | $128+16+8$ |
| $D8$ | $64+8$ |
| $D7$ | $32+8+4$ |
| $D6$ | $16+4$ |
| $D5$ | $8+4$ |
| $D4$ | $4$ |
| $D3$ | $8$ |
| $D2$ | $4$ |
| $D1$ | $2$ |
| $D0$ | $1$ |

defined as

$$r_i = \frac{R_i}{S_i/4} \quad (6)$$

Therefore, the redundant ratios of the first four non-binary cycles are 25%, 20%, 33.3%, 50%, respectively.

To elaborate the sub-radix-2 switching operation further, Fig. 4 shows the single-ended switching procedure of one conversion. The sampling phase is illustrated in Fig. 4(a). All the bottom plates of CDACs are connected to input during the sampling. Before the MSB comparison (Fig. 4(b)), the threshold of CDAC1 is set to $3/4V_{FS}$ (by connecting one $C_1$ to 0 and others reset to 1), while the threshold of CDAC2 is set to $1/4V_{FS}$ (by connecting one $C_1$ to 1 and others reset to 0). Briefly, the CDAC1 searches from the top 1024 LSB, while the CDAC2 searches from the bottom 0 LSB. Both CDACs approximate the targeted input (550.5 LSB). According to the MSB comparison results “011” ($D_{11}D_{10} = 10$), one $C_1$ and $C_{1r}$ are connected to 1 and the other $C_{ir}$ connected to 0 as described in Table 1. To create a redundant range, the $C_1$ in CDAC1 is switched back to 1 and one $C_{1r}$ is switched to 0. Also in CDAC2, one $C_{ir}$ is connected to 1. Simultaneously, the $C_2$ is set to 0 in CDAC1 (1 in CDAC2) to create thresholds for MSB-1 comparison (Fig. 4(c)). The comparisons are repeated in similar ways (Fig. 4(d), Fig. 4(e), Fig. 4(f)) until LSB comparison. Fig. 4(g) shows the operation of LSB comparison, where the last two bits are generated by interpolated comparators. In Fig. 4(g), voltage difference settled between CDAC1 and CDAC2 is
one LSB_{8-bit} (1/256V_{FS}). At the output of pre-amplifiers, the thresholds of interpolated dynamic comparator Co2 and Co4 are 3/1024V_{FS} and 1/1024V_{FS} within one LSB_{8-bit} respectively. All of the offsets of pre-amplifiers and comparators are calibrated separately in the background to prevent the deterioration of system linearity [12].

IV. LOW-COST ENCODING CIRCUIT FOR SUB-RADIX-2 APPROXIMATION

To map the redundant output codes to binary codes, a low-cost sub-radix-2 encoding circuit for multi-bit/cycle conversion is proposed. The corresponding encoding mapping is listed in Table 2, where each non-binary weight is represented as a sum of binary weights. Different from [9], [10], no offset is required for the redundant digital output. Since most of the redundant values are set as a power of 2, it is straightforward to realize encoder by only adders instead of complex arithmetical units [13]. Fig. 5 shows the schematic of encoding circuit, which converts the redundant 12 bits raw data (D_{12} to D_{0}) to 10 bits binary code (B_{9} to B_{0}). The bits C_i' and C_i'' are the carry bits of bit-i (i = 0~9), and they are connected by labels in Fig. 5. The encoder is built with only 13 full adders (FA), 12 half adders (HF) and 1 OR gate. Overall, the proposed non-binary searching technique for 2b/cycle SAR ADC consumes less power and has low silicon area overhead. At a sampling rate of 400MS/s, the simulated power consumption is less than 0.15mW. And the propagation delay is less than 1 ns. Moreover, the redundant weight in
V. SIMULATION RESULTS

A. BEHAVIOURAL MODEL SIMULATIONS

To demonstrate the proposed sub-radix-2 approximation algorithm, the model of the approximation is built with DAC settling behaviour included. The incomplete DAC settling of binary 2b/cycle SAR ADC is also presented for comparison. By setting time $t_{\text{set}} = 7\tau$ and $t_{\text{set}} = 3\tau$ respectively, the DNL/INL of traditional 2b/cycle SAR ADC are plotted in Fig. 6. The settling requirement of 10-bit resolution is met by setting $t_{\text{set}}$ as $7\tau$, therefore, the DNL/INL show acceptable peak values of 0.24/0.24 LSBs. However, the DNL/INL degrade to 12.7/12.7 LSBs with $t_{\text{set}}$ reduced to be $3\tau$. Fig. 7 shows the DNL/INL of proposed sub-radix-2 2b/cycle SAR ADC. It can be seen that the peak DNL maintains a low value of 0.26/0.26 LSBs with $t_{\text{set}} = 3\tau$, which proves the settling error tolerance capability of sub-radix-2 approximation. In addition, with different number
of τ, the peak DNL and INL are shown in Fig. 8. Within the tolerable error range of sub-radix-2 approximation algorithm, the peak DNL/INL only has a slightly drop. Regarding the effect of incomplete settling on dynamic performances, the SFDR and SNDR of traditional 2b/cycle SAR ADC are only 64.9 dB and 49.9 dB with $t_{\text{set}} = 3\tau$, respectively, which are shown Fig. 9 (a). On the contrary, Fig. 9 (b) shows that for sub-radix-2 2b/cycle SAR ADC the SFDR and SNDR are 85.1 dB and 61.6 dB, respectively, which achieves an ENOB of 9.94-bit. The SFDR and SNDR versus different number of time constant are depicted in Fig. 10. The sub-radix-2 approximation could keep the ENOB above 9.59-bit with settling time $t_{\text{set}} > 2\tau$. However, for binary approximation the $t_{\text{set}}$ needs to be larger than $5\tau$ to keep the ENOB above 9.9-bit.

B. TRANSISTOR LEVEL LAYOUT SIMULATIONS

A fabricated design example of binary 2b/cycle SAR ADC was reported in [12], where the interpolated pre-amplifiers and comparators have been verified except the proposed...
sub-radix-2 approximation algorithm in this work. To evaluate the conversion rate improvement, the post-layout simulation based comparison between traditional and the sub-radix-2 2b/cycle SAR ADCs is depicted. The layout of the proposed SAR ADC is shown in Fig. 11, which is revised radix-2 2b/cycle SAR ADCs is depicted. The layout of the simulation based comparison between traditional and the sub-radix-2 approximation algorithm in this work. To verify the linearity, the SFDR versus input frequency at different corners and temperatures at 400MS/s is shown in Fig. 13. In addition, the ENOB versus 10 Monte-Carlo (MC) simulations, which includes local mismatch of transistors, resistors and capacitors, are shown in Fig. 14. In the above MC simulations, TRAN noise option is turned on. The ENOB versus supply voltage VDD variation is shown in Fig. 15. The performance summary and comparison between the state-of-the-art 2b/cycle SAR ADCs and the proposed sub-radix-2 SAR ADC is listed in Table 3.

VI. CONCLUSION
A sub-radix-2 approximation algorithm for 2b/cycle SAR ADC is proposed in this paper. The sub-radix-2 approximation only introduces one more DAC branch and adders based encoding circuit. The additional power consumption and silicon area of the hardware overhead are negligible. The non-ideal DNL and INL curves are characterized with the presence of incomplete DAC settling. It is proved that the sub-radix-2 could tolerate the incomplete DAC settling error and improve the DNL and INL significantly. Equivalently, the sub-radix-2 approximation could boost the conversion speed by 33% for a 300MS/s 10-bit 2b/cycle SAR ADC.

REFERENCES
[1] G.-Y. Huang, S.-J. Chang, Y.-Z. Lin, C.-C. Liu, and C.-P. Huang, “A 10b 200 MS/s 0.82 mW SAR ADC in 40 nm CMOS,” in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Nov. 2013, pp. 289–292.
[2] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang, C.-H. Huang, L. Bu, and C.-C. Tsai, “A 10b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2010, pp. 386–387.
[3] Y. Shen, Z. Zhu, S. Liu, and Y. Yang, “A reconfigurable 10-to-12-b 80-to-200 MS/s bandwidth scalable SAR ADC,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 1, pp. 51–60, Jan. 2018.
[4] L. Kull, T. Toifl, M. Schmutz, P. A. Francesc, C. Menolfi, M. Brandli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, “A 3.1 mW 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS,” IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3049–3058, Dec. 2013.
[5] D. Li, Z. Zhu, R. Ding, and Y. Yang, “A 1.4-mW 10-bit 150-MS/s SAR ADC with nonbinary split capacitive DAC in 65-nm CMOS,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 11, pp. 1524–1528, Nov. 2018.
[6] J. H. Tsai, “A 0.003 mm² 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction an correlated-reversed switching,” IEEE J. Solid-State Circuits, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.
[7] Z. Cao, S. Yan, and Y. Li, “A 32 mW 1.25 GS/s 6b 2b-step SAR ADC in 0.13 µm CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 542–634.
[8] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, “A 3.8 mW 8b 1 GS/s 2b/cycle interleave SAR ADC with compact DAC structure,” in Proc. Symp. VLSI Circuits (VLSIC), Jun. 2012, pp. 86–87.
[9] H.-K. Hong, W. Kim, S.-J. Park, M. Choi, H.-J. Park, and S.-T. Ryu, “A 7b 1GS/s 7.2 mW nonbinary 2b/cycle SAR ADC with register-to-DAC direct control,” in Proc. IEEE Custom Integr. Circuits Conf., Sep. 2012, pp. 1–4.
[10] H.-K. Hong, H.-W. Kang, B. Sung, C.-H. Lee, M. Choi, H.-J. Park, and S.-T. Ryu, “An 8.6 ENOB 900MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2013, pp. 470–471.
[11] L. Qiu, K. Tang, Y. Zheng, and L. Siek, “A flexible-weighted nonbinary searching technique for high-speed SAR-ADCs,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2808–2812, Aug. 2016.

TABLE 3. Comparison with state-of-the-art works and summary.

|               | [10]  | [15]  | [12]  | This Work* |
|---------------|------|------|------|------------|
| Architecture  | 2b/cycle SAR | 2b/cycle SAR | 2b/cycle SAR | 2b/cycle SAR |
| Technology (nm) | 45   | 45   | 40   | 40         |
| Supply voltage (V) | 1.2  | 1.25 | 1.2  | 1.2        |
| Power (mW)     | 10.8 | 7.2  | 5.8  | 6          |
| Sampling Rate (MS/s) | 900 | 1000 | 300  | 400        |
| Resolution     | 9    | 7    | 10   | 10         |
| ENOB(bit)      | 8.2  | 6.62 | 8.3  | 9.5        |
| FOM@Nyquist (fJ/conv-step) | 40.8 | 73   | 61.3 | 20.7       |
| Area (mm²)     | 0.082| 0.016| 0.032| 0.034      |

* Simulation results.
[12] L. Qiu, K. Wang, K. Tang, L. Siek, and Y. Zheng, “A 10-bit 300 MS/s 5.8 mW SAR ADC with two-stage interpolation for PET imaging,” *IEEE Sensors J.*, vol. 18, no. 5, pp. 2006–2014, Mar. 2018.

[13] F. Kuttner, “A 1.2 V 10b 20MSample/s non-binary successive approximation ADC in 0.13 μm CMOS,” in *Proc. IEEE Int. Solid-State Circuits Conference. Dig. Tech. Papers*, Feb. 2002, pp. 176–177.

[14] L. Qiu, C. Yang, K. Wang, and Y. Zheng, “A high-speed 2-bit/cycle SAR ADC with time-domain quantization.” *IEEE Trans. Very Large Scale Intege (TVLSI) Syst.*, vol. 296, no. 10, pp. 2175–2179, 2018.

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