Quantum transport properties of industrial $^{28}\text{Si}/^{28}\text{SiO}_2$

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We investigate the structural and quantum transport properties of isotopically enriched $^{28}\text{Si}/^{28}\text{SiO}_2$ stacks deposited on 300 mm Si wafers in an industrial CMOS fab. Highly uniform films are obtained with an isotopic purity greater than 99.92%. Hall-bar transistors with an equivalent oxide thickness of 17 nm are fabricated in an academic cleanroom. A critical density for conduction of $1.75 \times 10^{11} \text{ cm}^{-2}$ and a peak mobility of 9800 cm$^2$/Vs are measured at a temperature of 1.7 K. The $^{28}\text{Si}/^{28}\text{SiO}_2$ interface is characterized by a roughness of $\Delta = 0.4$ nm and a correlation length of $\Lambda = 3.4$ nm. An upper bound for valley splitting energy of 480 $\mu$eV is estimated at an effective electric field of 9.5 MV/m. These results support the use of wafer-scale $^{28}\text{Si}/^{28}\text{SiO}_2$ as a promising material platform to manufacture industrial spin qubits.

Enrichment of the spin-zero $^{28}\text{Si}$ isotope drastically reduces spin-bath decoherence in silicon [1,2] and has enabled solid state spin qubits with extremely long coherence [3,4] and high control fidelity [5–7]. The limited availability of isotopically enriched $^{28}\text{Si}$ in industrially adopted forms [8], however, was previously thought to be a major bottleneck to leverage CMOS technology for manufacturing qubits with the quality and in the large numbers required for fault tolerant quantum computation [9,10]. Recently, isotopically enriched silane ($^{28}\text{SiH}_4$) has been employed in a pre-industrial CMOS facility to deposit high quality $^{28}\text{Si}$ epi-wafers [11]. Crucially, an industrial supply of $^{28}\text{SiH}_4$ has been established and silicon quantum dots were fabricated on a wafer-scale $^{28}\text{Si}/^{28}\text{SiO}_2$ stack grown in an industrial manufacturing CMOS fab [12]. In these quantum dots, a single-electron spin lifetime of 2.8 ms was obtained at a temperature of 1.1 K and weak charge noise was measured, pointing to a promising material platform for qubit operation at elevated temperatures.

Studies devoted to $^{28}\text{Si}$ quantum dots, however, tend to discuss only marginally the structural properties of the originating $^{28}\text{Si}/^{28}\text{SiO}_2$ material stack and the electrical transport in the associated two-dimensional electron gas (2DEG). In this paper we provide structural characterization of the same industrial $^{28}\text{Si}$ wafer used for quantum dots in Ref. [12] and assess the disorder properties of the critical $^{28}\text{Si}/^{28}\text{SiO}_2$ interface. By investigating the quantum transport properties of Hall-bar transistors, we extract key material metrics such as carrier mobility, critical density, interface roughness, interface correlation length, and valley splitting energy. Electron mobility is typically used as a figure of merit to assess the quality of the semiconductor/oxide interface. However, peak mobility is measured at high electron density, where screening effects are relevant [15,16]. The critical density, instead, indicates the minimum density required to establish metallic conduction by overcoming electron trapping at the oxide interface. As such, the critical density is a complementary metric to the mobility and characterizes the interface disorder at low densities, where quantum devices typically operate. Overall, large mobility and small critical density indicate material uniformity and low disorder at the confining interfaces. These properties are beneficial for obtaining reproducible quantum dots at intended locations on the substrate. Valley splitting quantifies the energetic separation between the ground state used for computation and the lowest excited state. A sharp flat interface is required to achieve large splitting energy, which is beneficial for qubit operation [15,16]. The results reported in this work indicate a low disorder environment at the $^{28}\text{Si}/^{28}\text{SiO}_2$ interface and potential to achieve large valley splitting, supporting the industrial integration of spin qubits on wafer-scale $^{28}\text{Si}$.

The schematics in Fig. 1 illustrate the key steps in the supply chain of isotopically enriched precursors for wafer-scale epitaxial growth of $^{28}\text{Si}$. A silicon-tetrafluoride gas ($\text{SiF}_4$) with natural abundance of $^{28}\text{Si}$ of 92.23% is isotopically enriched in $^{28}\text{Si}$ to a concentration greater than 99.92% by centrifuge separation. The $^{28}\text{SiF}_4$, with a residual $^{28}\text{Si}$ concentration of 0.08%, is then reduced to obtain high purity $^{28}\text{SiH}_4$. $^{28}\text{SiH}_4$ gas cylinders have been installed for use in a state-of-the-art chemical vapour deposition tool of a 300 mm fabrication line to deposit $^{28}\text{Si}$ epilayers. Maintaining the chemical purity of gas precursors throughout the supply chain is crucial to obtain a low-disorder $^{28}\text{Si}/^{28}\text{SiO}_2$ stack. The growth process starts with the deposition of 1 $\mu$m of intrinsic natural Si.
on a high-resistivity 300 mm Si(100) wafer followed by a 100-nm-thick intrinsic $^{28}\text{Si}$ epilayer. The wafer is then thermally processed at high temperature for the formation of a high quality 10-nm-thick $^{28}\text{SiO}_2$ layer.

In Fig. 1 we compare morphology and composition of the grown stack at the center and the edge of the 300 mm wafer. No difference in surface or interface roughness, composition, and purity could be observed across the wafer, indicating a uniform film deposition. Atomic force microscopy shows a uniform and near defect-free surface with a root mean square surface roughness of 0.2 nm. Secondary ion mass spectroscopy of isotopes $^{28}\text{Si}$, $^{29}\text{Si}$, and $^{30}\text{Si}$ shows a high purity film with a residual concentration of non-zero-spin nuclei $^{29}\text{Si}$ reduced from 4.76% in the Si buffer to 0.08% in the purified epilayer, demonstrating that the precursor purity has been preserved during the deposition process. The concentration of common background contaminants C and O is below the detection limit of $4 \times 10^{17}$ cm$^{-3}$ and $1 \times 10^{18}$ cm$^{-3}$, respectively. High-resolution transmission electron microscopy shows that no dislocations or stacking faults are visible in the epilayer. Moreover, the $^{28}\text{Si}/^{28}\text{SiO}_2$ interface is flat down to 1-2 atomic layers over distances ($\approx 200$ nm) that are larger than the typical size of Si quantum dot spin qubits. The sharpness of the interface, the negligible density of defects in the lattice, and the associated electron diffraction pattern highlight the film quality and the good control over the growth process attained in a manufacturing CMOS fab.

Moving on to device fabrication, Fig. 2(a) shows schematics and optical micrograph of a MOS transistor shaped in a Hall-bar geometry to investigate the magnetotransport properties of the 2DEG at the $^{28}\text{Si}/^{28}\text{SiO}_2$ interface. The device was fabricated in an academic cleanroom environment, starting from coupon-sized samples diced from the original $^{28}\text{Si}/^{28}\text{SiO}_2$ 300 mm wafer. We employ e-beam lithography and lift-off additive techniques to resemble the process flow used to fabricate quantum dots as in Ref. [12]. Highly doped n$^{++}$ regions are obtained by P-ion implantation followed by 30 s of activation anneal at 1000°C in N$_2$ environment. Multiple ohmic contacts are deposited on the implant regions by e-beam evaporation of Al. An additional Al$_2$O$_3$ layer was deposited by atomic layer deposition at 300°C, so that the $^{28}\text{Si}/^{28}\text{SiO}_2$ interface undergoes similar processing as in the fabrication of multi-layer gate-defined qubits [12]. The resulting dielectric stack has an equivalent oxide thickness (EOT) of 17 nm. A Ti/Pd top gate is deposited to define a Hall-bar geometry with a 100-µm-wide and 500-µm-long central region. The last processing step is a forming gas anneal at 400°C to reduce the damage induced by e-beam lithography [14] [17].

The electrical characterization of the device was performed at a temperature of 1.7 K using standard four-terminal low frequency lock-in techniques with a constant source-drain excitation voltage of 1 mV. Longitudi-
experimental capacitance $C = e \frac{dn}{dV_g} = 0.19 \, \mu F/cm^2$ matches within 5% the expected value for the given EOT. Upon multiple sweeps of $V_g$, no hysteresis is observed and the same values of $V_{t0}$ and $C$ are measured, indicating a stable potential landscape at the oxide interface.

The experimental and theoretically calculated density-dependent mobility curves are shown in Fig. 2(d). Above a critical density, required to establish metallic conduction in the 2DEG, the mobility rises sharply due to screening from charged impurity Coulomb scattering [18–21]. A peak mobility of 9800 cm$^2$/Vs is reached at $n = 1.13 \times 10^{12}$ cm$^{-2}$, corresponding to a mean free path of 120 nm. Beyond, the mobility drops due to surface roughness scattering at the $^{28}$Si/$^{28}$SiO$_2$ interface [18–20] 21. The calculated scattering-limited mobility takes into account a scattering charge density at the semiconductor/oxide interface and an exponential autocorrelation function form of the interface roughness [13, 20] 21. A good match is obtained for a scattering charge density of $4.65 \times 10^{10}$ cm$^{-2}$, an interface roughness of $\Delta = 0.4$ nm, and an interface correlation length of $\Lambda = 3.4$ nm. $\Delta$ describes the interface root-mean-square height fluctuations, $\Lambda$ is the lateral distance over which the fluctuations are correlated. The interface roughness is compatible with the morphology investigation by transmission electron microscopy reported in Fig. 1.

The critical density is extracted from a percolation fit of the density-dependent conductivity (Fig. 2(e)) $\sigma_{xx} \sim (n - n_p)^p$ [13, 14], where $n_p$, $p$ are the percolation transition density and exponent, respectively. By fixing $p = 1.31$, as expected in a 2D system, we estimate $n_p = 1.75 \times 10^{11}$ cm$^{-2}$ at $T = 1.7$ K. Previous studies have shown that $n_p$ decreases with decreasing temperature [13, 14], therefore the obtained value of $1.75 \times 10^{11}$ cm$^{-2}$ sets an upper bound for the critical density in the temperature regime at which qubits are typically operated ($T \leq 100$ mK).

Both the mobility and critical density obtained in wafer-scale isotopically enriched $^{28}$Si/$^{28}$SiO$_2$ stack are qualitatively comparable to the values previously reported for high-mobility Si MOSFETs at low temperatures [13, 14, 17, 22, 23] (see Table I). In drawing a meaningful comparison with the data reported in the literature, the reader should consider samples with similar EOT and device process flow. In fact, the mobility is known to be higher in devices with thicker oxide [18–24] and degrades upon device exposure to electron-beam [14, 17].

Transport characterization at high magnetic field (Fig. 3) allows the measurement of effective mass $m^*$ and quantum lifetime $\tau_{q}$, from which we estimate an upper bound for the valley splitting energy and the $g$-factor. In Fig. 3(a) we report the longitudinal magnetoresistivity at a density $n = 1.05 \times 10^{12}$ cm$^{-2}$ which corresponds to an effective electric field of 9.5 MV/m. Shubnikov-de Haas (SdH) oscillations are observed, with minima

![Figure 2. (a) Schematics of the Hall-bar device fabrication, starting from the 300 mm $^{28}$SiO$_2$/$^{28}$Si(100) stack followed by coupon-size processing. The optical micrograph of the final device shows the multi-terminal geometry used for Hall measurements. (b) Source-drain current $I_{SD}$ measured as a function of top gate voltage $V_g$ at $T = 1.7$ K. (c) Linear relationship between 2DEG Hall density $n$ and top gate voltage $V_g$. (d) Channel mobility $\mu$ measured as a function of $n$ (black) and corresponding calculation (red) including scattering from charged impurities and from interface roughness. (e) 2DEG conductivity in the low density range (black) and fit to percolation theory (red).](image-url)
aligned to quantum Hall plateaus in $R_{xy}$. SdH oscillations start at $B_{eff} = 1$ T and spin degeneracy is resolved at $B_S = 4.3$ T, corresponding to the even filling factor $\nu = 10$. Figure 3(b) shows the filling factor progression against $1/B$. High mobility and density allow to resolve filling factors up to $\nu = 36$, with fourfold periodicity at low magnetic field due to spin and valley degeneracy and twofold periodicity beyond $B_S$. We do not observe odd filling factors, indicating that twofold valley degeneracy is not resolved under these measurement conditions. From the linear filling factor progression we extract a density $n_{SdH} = 1.06 \times 10^{12}$ cm$^{-2}$. The agreement between the Hall density $n$ and $n_{SdH}$ indicates that only one high-mobility subband contributes to electrical transport, confirming the high quality $^{28}$Si epitaxy.

The transverse effective mass $m^*$ of the high mobility carriers is calculated from the damping of the SdH oscillations with increasing temperature, described by the relation [25,28]

$$ \frac{\Delta \rho_{xx}(T, B)}{\Delta \rho_{xx}(T_0, B)} = \frac{T \sinh \chi_0}{T_0 \sinh \chi}, $$

where $\Delta \rho_{xx}$ is the SdH oscillation amplitude after polynomial background subtraction, $\chi = 2\pi^2 k_B T/\hbar \omega_c$, $\chi_0 = \chi(T_0 = 1.7$ K), $\omega_c = eB/m^*$ is the cyclotron frequency, $\hbar$ is the Planck constant, and $k_B$ the Boltzmann constant. Figure 3(d) shows the temperature dependence of the oscillation amplitude at $B = 3.18$ K, before spin-splitting, normalized to the amplitude at $T_0 = 1.7$ K. By fitting the data to Eq. 4 we obtain an effective mass of $m^* = 0.19m_e$, where $m_e$ is the free-electron mass, and a transport lifetime $\tau_t = \mu m^*/e = 1.06$ ps. The $m^*$ value is in agreement with measurements performed on natural Si [29] and corresponds to the expected value obtained from band structure calculations neglecting many-body effects [13].

Once the effective mass is measured, the quantum lifetime $\tau_q$ can be determined from the SdH oscillation envelope at $T_0$, using the relation [25, 28]

$$ \Delta \rho_{xx}(T_0, B) \sim \sqrt{B} \frac{\chi_0}{\sinh \chi_0} \exp \left( -\frac{\pi}{\omega_c \tau_q} \right). $$

Figure 3. (a) Longitudinal ($\rho_{xx}$, purple) and transverse ($R_{xy}$, black) resistivity at $n = 1.05 \times 10^{12}$ cm$^{-2}$ and $T = 1.7$ K. The arrows indicate the magnetic field at which SdH oscillations and Zeeman spin-splitting are resolved. (b) Linear relationship between the filling factors $\nu$ and the inverse of magnetic field $B$. The solid line is the linear fit from which $n_{SdH}$ is calculated. (c) Temperature dependence of the SdH oscillations amplitude in the range $T = 1.7\text{–}3.1$ K, after polynomial background subtraction. (d) $\Delta \rho_{xx}$ at $B = 3.18$ T as a function of $T$, normalised at the value at $T = 1.7$ K. The solid line is the fit used to extract $m^*$. (e) Dingle plot at $T = 1.7$ K, considering the 8 most resolved oscillation maxima. The solid line is the linear fit used to extract $\tau_q$.

The Dingle plot of Fig. 3(e) reports the fit from which we extract $\tau_q = 0.69$ ps. The obtained $\tau_q$ implies a Landau level broadening of $\Gamma \approx \hbar/2\tau_q = 480$ $\mu$eV, which sets an upper bound to valley splitting at the investigated...
density (electric field) and magnetic field. For comparison, a valley splitting energy of 275 µeV was measured in $^{28}$Si quantum dots fabricated on the same wafer in an academic environment \[12\]. The electron $g$-factor is evaluated by considering that the onset of spin-splitting at $B_2$ implies a Zeeman energy $g\mu_B B_2 \simeq \Gamma$, where $\mu_B$ is the Bohr magneton. From this, a $g$-factor of $g = 1.92 \pm 0.07$ is estimated, which is close to the expected single-particle value of $g = 2$.

In conclusion, we investigated the structural and quantum transport properties of isotopically enriched $^{28}$Si/$^{28}$SiO$_2$ stacks deposited on 300 mm wafers in an industrial CMOS fab. The material characterization shows that the level of control achieved in the growth process results in a uniform deposition with high purity epilayers and a sharp semiconductor/oxide interface. Detailed quantum transport characterization of Hall-bar devices fabricated in an academic cleanroom points to a high-quality $^{28}$Si/$^{28}$SiO$_2$ interface, promising for hosting spin qubits. Mobility and critical density for these stacks are among the best reported for equivalent oxide thicknesses, with the potential to achieve large valley splitting. Disorder at the critical semiconductor/oxide interface is expected to further decrease by processing the entire gate stack in the high volume manufacturing environment, because an advanced process control is attainable and e-beam induced damage is avoided.

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