A Novel Method of Solving Linear Programs with an Analog Circuit

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Abstract—We present the design of an analog circuit which solves linear programming (LP) problems. In particular, the steady-state circuit voltages are the components of the LP optimal solution. The paper shows how to construct the circuit and provides a proof of equivalence between the circuit and the LP problem. The proposed method is used to implement a LP-based Model Predictive Controller by using an analog circuit. Simulative and experimental results show the effectiveness of the proposed approach.

I. INTRODUCTION

Analog circuits for solving optimization problems have been extensively studied in the past [1], [2], [3]. Our renewed interests stems from Model Predictive Control (MPC) [4], [5]. In MPC at each sampling time, starting at the current state, an open-loop optimal control problem is solved over a finite horizon. The optimal command signal is applied over a shifted horizon. The optimal solution relies on a dynamic model of the process only during the following sampling interval. At the next time step a new optimal control problem based on new measurements of the state is solved over a shifted horizon. The optimal solution depends on a dynamic model of the process only during the following sampling interval. The optimal solution relies on a dynamic model of the process only during the following sampling interval. The optimal solution depends on a dynamic model of the process only during the following sampling interval.

We present the design of an analog circuit whose steady state voltages are the LP optimizers. Thevenin Theorem is used to prove that the proposed design yields a passive circuit. Passivity and KKT conditions of a tailored Quadratic Program are used to prove that the analog circuit solves the associated LP. The proposed analog circuit can be used to repeatedly solve LPs with varying rhs and therefore is limited to problems where the matrices $A_{ineq}$ and $A_{eq}$ contain only small integer values. An extended version of the circuit includes multiport DC-DC transformer and can represent arbitrary matrices $A_{ineq}$ and $A_{eq}$. Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchoff’s laws) are used to prove that the circuit converges to the solution of the optimization problem. This work had limited practical impact due to difficulties in implementing the circuit, and especially in implementing the multiport DC-DC transformer.

In later work, Chua [6] showed a different and more practical way to realize the multiport DC-DC transformer using operational amplifiers. In subsequent works, Chua [3], [7] and Hopfield [2] proposed circuits to solve non-linear optimization problem of the form

$$\min_x f(x) \quad \text{s.t.} \quad g_j(x) \leq 0, \quad j = 1 \ldots m \quad (2)$$

where $x \in \mathbb{R}^n$ is vector of optimization variables, $f(x)$ is the cost function and $g_j(x)$ are the $m$ constraint functions. The LP (1) was solved as a special case of problem (2) [3], [2]. The circuits proposed by Chua, Hopfield and coauthors model the Karush-Kuhn-Tucker (KKT) conditions by representing primal variables as capacitor voltages and dual variables as currents. The dual variables are driven by the inequality constraint violations using high gain amplifiers. The circuit is constructed in a way that capacitors are charged with a current proportional to the gradient of the Lagrangian

II. PREVIOUS WORKS

A. Optimization problems and electrical networks

Consider the linear programming (LP) problem

$$\min_{V=[v_1,\ldots,v_n]} c^T V \quad \text{s.t.} \quad A_{eq} V = b_{eq} \quad (1b)$$

$$A_{ineq} V \leq b_{ineq} \quad (1c)$$

where $[v_1,\ldots,v_n]$ are the optimization variables, $A_{ineq}$ and $A_{eq}$ are matrices, and $c$, $b_{eq}$ and $b_{ineq}$ are column vectors.

The monogram by J. Dennis [1] from 1959 presents an analog electrical network for solving the LP (1). In Dennis’s work the primal and dual optimization variables are represented by the circuit currents and voltages, respectively. A basic version of Dennis’s circuit consists of resistors, current sources, voltage sources and diodes. In this circuit each entry of matrices $A_{ineq}$ and $A_{eq}$ is equal to number of wires that are connected to a common node. Therefore, this circuit is limited to problems where the matrices $A_{ineq}$ and $A_{eq}$ contain only integer values. An extended version of the circuit includes multiport DC-DC transformer and can represent arbitrary matrices $A_{ineq}$ and $A_{eq}$. Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchoff’s laws) are used to prove that the circuit converges to the solution of the optimization problem. This work had limited practical impact due to difficulties in implementing the circuit, and especially in implementing the multiport DC-DC transformer.

The paper is organized as follows. Existing literature is discussed in section II. We show how to construct an analog circuit from a given LP in section III. Section IV proves the equivalence between the LP and the circuit. Simulative and experimental results show the effectiveness of the approach in section V. Concluding remarks are presented in section VI.

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of problem (2)
\[
\frac{\partial x_i}{\partial t} = -\left[ \frac{\partial f(x)}{\partial x_i} + \sum_{j=1}^{m} I_j \frac{\partial g_j(x)}{\partial x_i} \right]
\]

where \( \frac{\partial x_i}{\partial t} \) is the capacitor voltage derivative and \( I_j \) is the current corresponding to the \( j \)-th dual variable. The derivatives \( \frac{\partial f}{\partial x_i} \) and \( \frac{\partial g_j}{\partial x_i} \) are implemented by using combinations of analog electrical devices [8]. When the circuit reaches an equilibrium, the capacitor charge is constant (\( \frac{\partial x_i}{\partial t} = 0 \)) and equation (3) becomes one of the KKT conditions. The authors prove that their circuit always reaches an equilibrium and equation (3) becomes one of the KKT conditions. The approach since the circuit can be intuitively mapped to the KKT equations. However, the time required for the capacitors to reach an equilibrium is non-negligible. This might be the reason for relatively large settling time reported to be "tens of milliseconds" for those circuits in [3].

B. Applying analog circuits to MPC problems

The analog computing era declined before the widespread use of Model Predictive Control. For this reason, the study of analog circuits to implement MPC problems has never been pursued. In [9] fast analog PI controllers are implemented on an Anadigm’s Field Programmable Analog Array (FPAA) device [10] for an application involving fast chemical microreactor. The analog circuit designed in [9] has a computation time faster than a digital controller implementing the PI controller. The article briefly proposes to use FPAA for MPC without specifying details. To the best of authors knowledge, no further work has been published in this direction.

III. ELECTRIC CIRCUIT FOR SOLVING LINEAR OPTIMIZATION PROBLEM

Without loss of generality, we assume that \( A_{ineq}, A_{eq} \) and \( c \) have non-negative entries. Any LP may be transformed into this form by using a three-step procedure. First, defining a new negative and positive variable for each original variable \( V^- + V^+ = 0 \), second splitting \( A_{ineq}, A_{eq} \) and \( c \) into positive and negative parts (\( A_{ineq} = A^{+}_{ineq} - A^{-}_{ineq}, A_{eq} = A^{+}_{eq} - A^{-}_{eq} \) and \( c = c^+ - c^- \)), and third replacing \( A_{ineq}V, A_{eq}V \) and \( c^TV \) with \( A^{+}_{ineq}V^+ - A^{-}_{ineq}V^-, A^{+}_{eq}V^+ - A^{-}_{eq}V^- \) and \( c^+T V^+ - c^-T V^- \), respectively.

In the beginning of this section we present the basic building blocks which will be lately used to create a circuit that solves problem (1). The first basic block enforces equality constraints of the form (1e). The second building block enforces inequality constraints of the form (1f). The last basic block implements the cost function.

A. Equality constraint

Consider the circuit depicted in Fig. 1. In this circuit \( n \) wires are connected to a common node. We call this node \( \alpha \), its potential is \( U \) and the current that exits this node is \( I \). Kirchhoff’s current law (KCL) implies
\[
\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I,
\]

where \( V_k \) is the potential of node \( k \), \( R_k \) is the resistance between node \( k \) and the node \( \alpha \). Equation (4) can be written as an equality constraint on potentials \( V_k \):
\[
\sum_{k=1}^{n} \frac{1}{R_k} V_k = I + U \sum_{k=1}^{n} \frac{1}{R_k}.
\]

If we can set the right hand side (rhs) of (5) to any desired value \( b \), then (5) enforces an equality constraint on a linear combinations of \( V_k \). Therefore every equality constraint (1e) can be implemented with a circuit which enforces (5) and implements
\[
U = \frac{b - I}{\sum_{k=1}^{n} \frac{R_k}{R_k}}.
\]

Equation (6) together with (5) yields
\[
\begin{bmatrix}
\frac{1}{R_1} & \cdots & \frac{1}{R_n}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
\vdots \\
V_n
\end{bmatrix} = b.
\]

and the circuit implementing (7) is shown in Fig. 2.

Remak 1: In the circuit in Fig. 2 the negative resistance \( -\sum_{k=1}^{n} \frac{1}{R_k} \) can be realized by using operational amplifiers.

B. Inequality constraint

Consider the circuit shown in Fig. 3. Similarly to the equality constraint circuit, \( n \) wires are connected to a common node \( \alpha \). Its potential is \( U \) and the current exiting this node is \( I \). Kirchhoff’s current law (KCL) implies
\[
\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I.
\]
An ideal diode connects node $\alpha$ to node $\beta$. The potential of node $\beta$ is $U'$. The diode enforces $U \leq U'$. In Fig. 5 the voltage $U'$ can be computed as follows

$$U' = \frac{b - I}{\sum_{k=1}^{n} \frac{1}{R_k}} \geq U.$$  \hfill (9)

Equation (9) and $U \leq U'$ yield

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k} \leq I + U' \sum_{k=1}^{n} \frac{1}{R_k} = b.$$ \hfill (10)

Which can be compactly rewritten as

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \\ ... \\ V_n \end{bmatrix} \leq b,$$ \hfill (11)

with the diode enforcing

$$I \geq 0,$$ \hfill (12a)

$$I(U - U') = 0.$$ \hfill (12b)

By using (9) and rearranging some terms, equation (12b) can be rewritten as:

$$I \left( \sum_{k=1}^{n} \frac{1}{R_k} \right) U - b + I = 0.$$ \hfill (13)

C. Cost function

Consider the circuit in Fig. 4. In this circuit the potential of node $\alpha$ is equal to $U_{\text{cost}}$ and the current that exits the node is $I_{\text{cost}}$. From (5) we have

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I_{\text{cost}} + U_{\text{cost}} \sum_{k=1}^{n} \frac{1}{R_k} \triangleq J.$$ \hfill (14)

where $c = [1/R_1 \ldots 1/R_n]$ and $J$ is the cost function.

This part of the circuit implements the minimization of the cost function. When $U_{\text{cost}}$ is set to a low value, the voltages $V_k$ are driven to a direction which leads the objective function value $J$ to approach the $U_{\text{cost}}$ value. However, the cost $J$ is different from $U_{\text{cost}}$ because the current $I_{\text{cost}}$ is not zero. A detailed explanation on this part of the circuit will be presented later in section IV-C.

D. Connecting the basic circuits

This section presents how to construct the circuit that solves a general LP. We construct the conductance matrix $G \in \mathbb{R}^{(m+1) \times n}$ as

$$G \triangleq \begin{bmatrix} c^T \\ A \end{bmatrix} = \begin{bmatrix} c^T \\ A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix}$$ \hfill (15)

and denote $G_{ij}$ the $i, j$ element of $G$. For a given LP (1) the $R_{ij}$ resistor is defined as

$$R_{ij} = \frac{1}{G_{ij}}, \ i = 0, \ldots m, \ j = 1, \ldots, n$$ \hfill (16)

where the first row of $G$ (corresponding to $c^T$) is indexed by 0.

Consider the circuit shown in Fig. 5. The circuit is shown using a compact notation where each resistor $R_{ij}$ is represented by a dot, vertical wires represent variables nodes with potentials $V_1 \ldots V_n$ and horizontal wires represent constraint nodes. If $G_{ij} = 0$ then no resistor is present in the corresponding dot. This circuit is constructed by connecting the nodes associated with the variables $V_1 \ldots V_n$ to all three types of the basic circuits: equality, inequality and cost. We will refer to such nodes as variable nodes. Each row of the circuit in Fig. 5 is one of the basic circuits presented in Sections III-A, III-B and III-C. We claim that, if $U_{\text{cost}}$ is “small enough”, then the values of the potentials $V_1 \ldots V_n$ in this circuit are a solution of (1). This claim is proven in the next section.

Remark 2: Some of the potentials $V_i$ may be forced externally to a desired value. By doing so, the circuit can solve different optimization problems for varying values of those potentials. This is equivalent to adding equality constraints $V_i = b_i$ to (1) and modifying the value of the equality constraint free parameter $b_i$.

Remark 3: The circuit as shown in Fig. 5 contains no dynamic elements such as capacitor or inductance. Therefore, the time required to reach steady-state is governed by the parasitic effects (e.g. wires inductance and capacitance) and by the properties of the elements used to realize negative resistance (usually opamp) and diode. Hence, a good electronic design can achieve solution times in the order of these parasitic effects. This could lead to time constants as low as a few nanoseconds.

IV. ANALYSIS OF THE ELECTRIC CIRCUIT PROPERTIES

In this section we show that the circuit in Fig. 5 with $R_{ij}$ as defined by (16), is a solution of the optimization problem (1) for a range of $U_{\text{cost}}$ values. First we derive the steady state equation of the electric circuit and then we show the equivalence.
A. Steady state solution

Consider the circuit in Fig. 5. Let \( U = [U_1, \ldots, U_m]^T \) be the voltages of the constraint nodes as shown on Fig. 5. By applying the KCL (Kirchhoff’s current law) to every variable node with potential \( V_1, \ldots, V_n \), we obtain

\[
G_{0,j}(U_{\text{cost}} - V_j) + \sum_{i=1}^{m} G_{i,j}(U_i - V_j) = 0, \quad j = 1, \ldots, n
\]

which can be rewritten in the matrix form

\[
\begin{bmatrix}
  c_1 & \cdots & c_n \\
  A_{11} & \cdots & A_{1N} \\
  \vdots & \ddots & \vdots \\
  A_{m1} & \cdots & A_{mN}
\end{bmatrix}
\begin{bmatrix}
  U_{\text{cost}} \\
  U_1 \\
  \vdots \\
  U_m
\end{bmatrix}
= \begin{bmatrix}
  (\sum_{i=0}^{m} G_{i,1})V_1 \\
  \vdots \\
  (\sum_{i=0}^{m} G_{i,n})V_n
\end{bmatrix}
\]

Equation (18) can be compactly rewritten as

\[
cU_{\text{cost}} + A^T U = \text{diag}(c^T + 1^T A)V
\]

where \( 1 \) is vector of ones and \( \text{diag}(x) \) is a diagonal matrix with \( x \) on its diagonal.

Next, we apply KCL on all nodes with potentials \( [U_{\text{cost}}, U_1, \ldots, U_m] \) to obtain

\[
\sum_{j=1}^{n} c_j (U_{\text{cost}} - V_j) = I_{\text{cost}}
\]

\[
\sum_{j=1}^{n} G_{i,j}(U_i - V_j) = I_i, \quad i = 1, \ldots, m
\]

which can be written in matrix form

\[
\begin{bmatrix}
  c_1 & \cdots & c_n \\
  A_{11} & \cdots & A_{1N} \\
  \vdots & \ddots & \vdots \\
  A_{m1} & \cdots & A_{mN}
\end{bmatrix}
\begin{bmatrix}
  V_1 \\
  \vdots \\
  V_n
\end{bmatrix}
= \begin{bmatrix}
  U_{\text{cost}} U_1^{\sum_{j=1}^{n} c_j} \\
  \vdots \\
  U_{m} U_m^{\sum_{j=1}^{n} A_{m,j}}
\end{bmatrix}
+ \begin{bmatrix}
  I_{\text{cost}} \\
  \vdots \\
  I_i
\end{bmatrix}
\]

Equation (22) can be compactly rewritten as

\[
e^T V = 1^T cU_{\text{cost}} + I_{\text{cost}}
\]

\[
A V = \text{diag}(1^T A^T) U + I
\]

The equality voltage regulator law (6) and the inequality law (9) can be compactly written as

\[
\text{diag}(1^T A_{\text{eq}}^T) U_{\text{eq}} = b_{\text{eq}} - I_{\text{eq}}
\]

\[
\text{diag}(1^T A_{\text{ineq}}^T) U_{\text{ineq}} \leq b_{\text{ineq}} - I_{\text{ineq}}.
\]

By substituting (25) into (24) we obtain

\[
A_{\text{eq}} V = b_{\text{eq}}
\]

\[
A_{\text{ineq}} V \leq b_{\text{ineq}}.
\]
Fig. 8: Subnetwork that connects nodes \( i \) and \( j \), after assuming that all other resistors are zero.

**Proposition 1 (Network non-negativity):** The resistance network in Fig. 7 is equivalent to a resistance network with non-negative resistors.

**Proof:** [Proof of non-negativity proposition] Our goal is to obtain a lower bound of an equivalent resistance between any two ports. From Fig. 7 we see that a sub-network that connects two ports consists of two negative resistances — one for each port, and a mesh of positive resistors between them. We want to find an equivalent resistance, that exist for each port, and a mesh of positive resistors between any two ports. From Fig. 7 we see that a sub-network that connects nodes \( U \) has a lower bound of an equivalent resistance between the ports.

**Remark 5:** The resistance network is characterized by the Thevenin theorem [11]. Let Assumption 1 hold. Assume that \( A \) is non-negative, \( 1^T A > 0 \) and \( 1^T A^T > 0 \). Then, the equations \( (29a)-(29f) \) have a solution when \( c = 0 \).

**Proof:** First we rearrange \( (29a)-(29f) \). Equation \( (29a) \) can be split into an equality and inequality parts

\[
A_{eq} = \text{diag}(1^T A_{eq}^T) U_{eq} + I_{eq}
\]

\[
A_{ineq} = \text{diag}(1^T A_{ineq}^T) U_{ineq} + I_{ineq}
\]

Equation \( (29b) \) can be rewritten as

\[
A_{eq}^T U_{eq} + A_{ineq}^T U_{ineq} = \text{diag}(1^T A) V.
\]

Therefore, \( (29a)-(29f) \) can be written as

\[
A_{eq} V = \text{diag}(1^T A_{eq}^T) U_{eq} + I_{eq}
\]

\[
A_{ineq} V = \text{diag}(1^T A_{ineq}^T) U_{ineq} + I_{ineq}
\]

\[
A_{eq}^T U_{eq} + A_{ineq}^T U_{ineq} = \text{diag}(1^T A) V
\]

\[
A_{eq} V = b_{eq}
\]

\[
A_{ineq} V \leq b_{ineq}
\]

\[
I_{ineq} \geq 0
\]

\[
(A_{ineq} V - b_{ineq})_i I_{ineq} \geq 0, \quad \forall i \in \mathcal{I}.
\]

Next, consider the following quadratic program (QP)

\[
\begin{aligned}
\min_{V} & \quad V^T Q V \\
\text{s.t.} & \quad A_{eq} V = b_{eq} \\
& \quad A_{ineq} V \leq b_{ineq},
\end{aligned}
\]

This problem has a finite solution for any \( Q \) because the feasibility domain is bounded and not empty. The value of \( Q \) will be selected later. We use this problem to find a solution to \( (29a)-(29f) \). KKT is a necessary optimality condition for problems with linear constraints (Theorem 5.1.3 in [12]), therefore, there exist \( V^*, \mu^*, \lambda^* \) that satisfy the KKT conditions

\[
A_{eq}^T \mu^* + A_{ineq}^T \lambda^* + QV^* = 0
\]

\[
A_{eq} V^* = b_{eq}
\]

\[
A_{ineq} V^* \leq b_{ineq}
\]

\[
\lambda^* \geq 0
\]

\[
(A_{ineq} V^* - b_{ineq})_i \lambda^*_i = 0, \quad i \in \mathcal{I},
\]

where \( \mu^* \) and \( \lambda^* \) are the dual variables.
We choose $Q$ and use $\mu^*$, $\lambda^*$ and $V^*$ to compute $U^*_e$, $U^*_i$ and $I^*_i$.

$$Q = \text{diag} \left( I^T A - A^T \text{diag} \left( I^T A^T \right)^{-1} A \right)$$

$$I^*_e = \text{diag} \left( I^T A^T \right) \mu^*$$

$$U^*_e = \text{diag} \left( I^T A^T \right)^{-1} A \text{diag} \left( I^T A^T \right) \lambda^*$$

$$U^*_i = \text{diag} \left( I^T A^T \right)^{-1} A \text{diag} \left( I^T A^T \right) \mu^*$$

Note that $\text{diag} \left( I^T A^T \right)$ and $\text{diag} \left( I^T A^T \right)^{-1}$ are invertible and positive from the assumptions of Lemma 1. Equations (36) are combined with (35) to get

$$A_{eq} V^* = \text{diag} \left( I^T A^T \right) U^*_e + I^*_i$$

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These equations have a solution and are identical to (33). Therefore, there exist $V^*$, $U^*$ and $I^*$ solving (39a)-(39f) when $c = 0$.

Our next goal is to show that there exists a $U^* = U^*_{\text{cost}}$ such that circuit solution is also an LP (1) solution. To show this we concatenate the primal problem (1) with a corresponding dual problem [13]

$$\max _{\lambda} b^T \lambda$$

s.t. $A_{eq} V = b_{eq}$, $A_{eq} V \leq b_{ineq}$

$$\left[ A^T_{eq} - A^T_{ineq} \right] \lambda = c$$

$$[0 I_{|Z|}] \lambda \geq 0$$

$$c^T V + b^T_{\lambda} \lambda + b^T_{-} \lambda_- = 0, \lambda + \lambda_- = 0$$

where $b_+$ and $b_-$ are the absolute values of the positive and negative components of $b$ and $\lambda_-$ equals to $-\lambda$. Note that (39d) is equivalent to $c^T V = b^T \lambda$.

Remark 6: From the Assumption 3 and from the structure of (39d), it follows that the matrix of equality and inequality constraints has non-negative coefficients and non-zero rows and columns.

All feasible points of problem (39) are primal [13] and dual [38] optimal solutions [13].

Problem (39) is solved by the circuit shown in Fig. 9. This circuit contains two parts: the primal and the dual circuits, each has the general form as in Fig. 5 and consists of equality and inequality sub circuits corresponding to constraints of the primal and dual problems. Note that no cost circuit is present in the primal and in the dual circuit. Instead, those circuits are connected by equality sub circuit that corresponds to the zero duality gap constraint (39d).

**Proposition 2:** Let Assumptions [13] hold. The circuit in Fig. 9 admits a solution. Moreover, for any circuit solution, the voltages $V$ of the variable nodes are a solution to the original LP (1).

**Proof:** The circuit in Fig. 9 consists only of equality and inequality sub circuits. As shown in sections II-A and II-B the variable nodes voltages must satisfy the associated equality or inequality constraints and thus equations (39). The feasible set of problem (39) is the set of all primal optimal and dual optimal variables of problem (1). This feasible set is bounded by assumption. This fact and the results from Remark 6 imply that all the assumptions of Lemma 1 are satisfied. We conclude that the circuit admits a solution. Moreover, every solution must be a solution of the original LP (1), because it satisfies simultaneously dual and primal problems with zero duality gap [13].

In the circuit shown in Fig. 9 the dual and the primal circuits are connected with a single wire that has some voltage when the circuit settles. We call this voltage $U^*_{\text{cost}}$.

**Lemma 2 (Exists $U^*_{\text{cost}}$):** Let Assumptions [13] hold. Consider the circuit in Fig. 5 and its corresponding equations (29). A solution $V^*$ to (29) with $U^*_{\text{cost}} = U^*_{\text{cost}}$ is an optimizer of the LP (1).

**Proof:** If a voltage equals to $U^*_{\text{cost}}$ is applied externally to the wire that connects the primal and the dual parts (at point $\alpha$ in Fig. 9), we can remove the dual circuit without affecting the primal one. Therefore, the circuit in Fig. 5 admits the same solution as the primal circuit in Fig. 9.

To complete the proof of Theorem 1 we need to show that for any voltage $U^*_{\text{cost}} \leq U^*_{\text{cost}}$ the circuit will continue to yield the optimal solution. Assume that $U^*_{\text{cost}}$ is perturbed by
\( \Delta U_{\text{cost}} \) from the value \( U_{\text{cost}}^{\text{crit}} \). We denote perturbed values in variable voltages \( V \) and the cost current \( I_{\text{cost}} \) as \( \Delta V \) and \( \Delta I_{\text{cost}} \). Next, we examine the Thevenin equivalent resistance [11] as seen from the cost node. From Proposition 1 we already know that this resistance is non-negative, but more can be said for the cost node. Refer to Fig. 8 showing a subnetwork connecting two arbitrary nodes. When one of the nodes is the cost node, it does not have one of the negative resistances, therefore, the the total resistance, \( R_{\text{total}} \), which can be seen from this node is at least all the cost resistances in parallel

\[
R_{\text{total}} \geq \frac{1}{\sum_{i=1}^{n} c_i}. \tag{40}
\]

From (29g) follows that

\[
c^T \Delta V = \left( \sum_{i=1}^{n} c_i \right) \Delta U_{\text{cost}} + \Delta I_{\text{cost}}. \tag{41}
\]

Using the total equivalent resistance we know that

\[
\Delta I_{\text{cost}} = -\frac{\Delta U_{\text{cost}}}{R_{\text{total}}}. \tag{42}
\]

Combination of (41), (42) and (40) yields

\[
c^T \Delta V = \sum_{i=1}^{n} c_i - \frac{1}{R_{\text{total}}} \geq 0. \tag{43}
\]

The equation (43) states that the change in cost value must have the same sign as the change in \( \Delta U_{\text{cost}} \). Therefore, when \( U_{\text{cost}} \) is decreased the cost must decrease or stay the same. However, the cost cannot decrease, since it is already optimal. Therefore the cost must remain constant, and the circuit holds solution to the problem (1) for any \( U_{\text{cost}} \leq U_{\text{cost}}^{\text{crit}} \). This result completes the proof of Theorem 1.

V. Example Applications and Experimental Results

This section presents three examples where the approach proposed in this paper has been successfully applied. In the first example an LP is solved by the proposed electrical circuit simulated by using the SPICE [14] simulator. In the second example an analog LP is used to control a linear system by using Model Predictive Control. In the third example an experiment is conducted by realizing the circuit for a small LP with standard electronic components.

A. Linear Programming

We demonstrate capability of the method by solving an LP problem. The problem is a randomly generated and it has 120 variables, 70 equality constraints and 190 inequality constraints. In order to simulate parasitic effects of real circuit inductance values of 100nH are assumed for the wires, that roughly corresponds to inductance of 10 cm long wire.

The convergence of the electric circuit is shown in Fig. 10. The time scale in this example is determined by the selected value of parasitic inductance. The circuit transient can be partitioned to two phases. During the first 200\( \mu \text{s} \) rapid convergence to a solution close to the optimal one can be observed. Afterwards, at about 500\( \mu \text{s} \) the circuit converges to the true optimum value. Typical accuracy achieved in analog electronics is in the order of 0.5% of the dynamic range. The longer convergence time is not of practical interest, because the difference between the immediate cost value and the true optimal one is less than the accuracy that is expected from analog devices.

B. MPC example

This example demonstrates the implementation of a model predictive controller with an LP analog circuit. For this example we work with the dynamical system \( \frac{dx}{dt} = -x + u \), where \( x \) is the system state and \( u \) is the input. We want \( x \) to follow a given reference trajectory, while satisfying input constraints. The finite time optimal control problem at time \( t \) is formulated as

\[
\min_{u_0 \ldots u_N} \sum_{i=1}^{N} |x(i) - x_{\text{ref}}(i)| \tag{44a}
\]

\[
x_{i+1} = x_i + (u_i - x_i)\delta, \quad i = 0, \ldots, N \tag{44b}
\]

\[
-1.5 \leq u_i \leq 1.5, \quad i = 0, \ldots, N \tag{44c}
\]

\[
x_0 = x(t) \tag{44d}
\]

where \( N \) is the prediction horizon, \( x_{\text{ref}}(i) \) is the reference trajectory at step \( i \), \( \delta \) is sampling time and \( x(t) \) is the initial state at time \( t \). Only the first input, \( u_0 \), is applied at each time step \( t \).

With \( N = 16 \), the LP in (44) has 96 variables, 63 equality constraints and 49 inequality constraints. An electric circuit that implements system dynamics together with the circuit that implements the MPC controller were constructed and simulated using SPICE. The voltage value representing the system state was measured and enforced on the \( x_0 \) node of the LP. The optimal input value \( u_0 \) was injected as input to the simulated system dynamics. Fig. 11 shows the closed loop simulations results. Notice the predictive behavior of the closed loop control input and the satisfaction of the system constraints.

In order to demonstrate system performance for imperfect analog devices, another simulation result with 1% random Gaussian error in values of resistors is presented on the same Fig. 11. There is no significant change in system behavior.
The circuit analysis is at steady state. The theory of Linear Complimentary system [15] can be used to study the dynamic circuit behavior. This is a subject of ongoing research. Future research directions include solution of larger problems, possible expansion the method to solution of quadratic programming (QP) and solutions to the optimal circuit design.

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REFERENCES

[1] J. B. Dennis, Mathematical programming and electrical networks. Technology Press of the Massachusetts Institute of Technology [Cambridge], 1959.
[2] D. Tank and J. Hopfield, “Simple 'neural' optimization networks: An a/d converter, signal decision circuit, and a linear programming circuit," Circuits and Systems, IEEE Transactions on, vol. 33, pp. 533 – 541, may 1986.
[3] M. Kennedy and L. Chua, “Neural networks for nonlinear programming,” Circuits and Systems, IEEE Transactions on, vol. 35, pp. 554 –562, may 1988.
[4] C. E. Garcia, D. M. Prett, and M. Morari, “Model predictive control: theory and practice - a survey,” Automatica, vol. 25, no. 3, pp. 335–348, 1989.
[5] D. Q. Mayne, J. B. Rawlings, C. V. Rao, and P. O. Scokaert, “Constrained model predictive control: Stability and optimality,” Automatica, vol. 36, no. 6, pp. 789–814, 2000.
[6] L. O. Chua, G. N. Lin, and J. J. Lum, “The (p+q)-port transformer,” International Journal of Circuit Theory and Applications, vol. 10, no. 4, pp. 335–359, 1982.
[7] L. Chua and G.-N. Lin, “Nonlinear programming without computation,” Circuits and Systems, IEEE Transactions on, vol. 31, pp. 182 – 188, feb 1984.
[8] A. S. Jackson, Analog computation. McGraw-Hill, 1960.
[9] O. A. Palusinski, S. Vratdhu, L. Znamirowski, and D. Humbert, “Process control for microreactors,” in Chemical Engineering Progress, vol. 97, Bell & Howell Information and Learning Company, 2001.
[10] “Anadigm, the dpasp company," http://www.anadigm.com/fpaa.asp.
[11] W. Chen, The Electrical Engineering Handbook. AP Series in Engineering Series, Elsevier Science, 2004.
[12] M. S. Bazarraa, H. D. Sherali, and C. M. Shetty, Nonlinear programming: theory and algorithms. Wiley-interscience, 2006.
[13] D. Bertsimas and J. N. Tsitsiklis, Introduction to linear optimization. Athena Scientific Belmont, MA, 1997.
[14] L. Nagel and D. Pederson, “SPICE (Simulation Program with Integrated Circuit Emphasis),” Memorandum No. ERL-M382.University of California, Berkeley, 1973.
[15] W. Heemels, J. Schumacher, and S. Weiland, “Dissipative systems and complementarity conditions,” in Decision and Control, 1998, Proceedings of the 37th IEEE Conference on, vol. 4, pp. 4127 –4132 vol.4, dec 1998.