Abstract — The Crossroads supercomputer was designed to simulate some of the most complex physical devices in the world. These simulations routinely require 1/2 petabyte or more of system memory running on thousands of compute nodes for months at a time on the most powerful supercomputers. Improvements in time to solutions for these workloads can have major impact on our mission capabilities. In this paper we present early results of representative application workloads on 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM. These results demonstrate an extremely promising 8.57x improvement (node to node) over our prior generation Intel Broadwell (BDW) based HPC systems. No code modifications were required to achieve this speedup, providing a compelling path forward toward major reductions in time to solution and the complexity of physical systems that can be simulated in the future.

Index Terms — hardware architecture, memory technology, performance analysis.

I. INTRODUCTION

Los Alamos National Laboratory (LANL) has a long history in advancing the state-of-the-art in High Performance Computing for complex multi-physics simulations. The Crossroads supercomputer scheduled for deployment in 2023 will be the latest in a series of HPC systems developed in collaboration with Intel and HPE/Cray. Crossroads will include 4th Gen Intel Xeon Scalable processors, formerly codenamed Sapphire Rapids, based on the Intel 7 process node and the novel Embedded Multi-Die Interconnect Bridge (EMIB) chiplet integration technology. This CPU promises to deliver significant improvements in simulation performance with little if any code modifications. As many of our codes are significantly memory bound, LANL worked with Intel to develop a Intel Xeon Scalable Processor with High Bandwidth Memory (HBM) 2e integrated with EMIB technology.

Initial experience on pre-production 4th Gen Intel Xeon with Double Data Rate (DDR) memory shows up to a 5.83x performance improvement in our multi-physics simulations compared to our current Broadwell based production systems. Pre-production Intel Xeon Processors codenamed Sapphire Rapids with HBM shows up to a 8.57x performance improvement. These improvements were achieved with no code changes, simply a recompile of the code to target the new microarchitecture.

II. 4TH GEN INTEL XEON AND INTEL XEON PROCEESSORS CODENAMED SAPPHIRE RAPIDS WITH HBM ARCHITECTURES

4th Gen Intel Xeon is the latest generation Xeon server processor based on Golden Cove microarchitecture (using Intel 7 process technology). A number of significant innovations from Intel are present in the processor including EMIB, acceleration engines, CXL, and bandwidth improvements in Ultra Path Interconnect. Microarchitecture and instructions per cycle (IPC) improvements include a 2x increase in decode length, 50% increase in decode width, a 2.4x increase in branch target size, 1.8x increase in the \( \mu \)op cache, a larger number of execution ports and a 1.5x increased reorder buffer. These microarchitecture changes improve the IPC rate and enable increased parallelism within the CPU.

4th Gen Intel Xeon is also the first CPU to incorporate Intel’s EMIB technology providing a more scalable path to further performance improvements and efficiency relative to traditional monolithic designs that are limited to a single reticle. This ability to provide tight integration beyond the single reticle limit is an important advancement, and it has other benefits including the potential for higher yield and the ability to integrate disparate processor and memory technologies in a single package.

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of four $400\text{mm}^2$ tiles each with golden cove cores with 48KB instruction and 32KB data caches. L2 is private and is 2048KB. Our system configurations are either dual socket 4th Gen Intel Xeon or dual socket Intel Xeon Processors codenamed Sapphire Rapids with HBM each with 66 physical cores for a total of 112 physical cores per node. 4th Gen Intel Xeon configuration has 8 channels of 16 GB DDR-5 operating at 4800 MT/s per socket for a total of 256GB of memory per 2 CPU node. Intel Xeon Processors codenamed Sapphire Rapids with HBM configuration has 4 banks of 8 high 16 Gbit HBM2e operating at 3200 MT/s per socket for a total of 128 GB of memory per 2 CPU node.

## III. Multi-Physics Simulation Codes

LANL develops and maintains a suite of multi-physics simulation codes used to support our national security and science mission. These codes are used daily by hundreds of scientists and engineers to answer questions of national importance. Significant effort in validation and verification of these codes underwrite their capabilities and provide confidence in their use to simulate complex physical devices. As a result of this work, scientists are able to to explore complex issues in Inertial Confinement Fusion [1], a regime of physics that is only achievable at a single experimental device in the world, the National Ignition Facility (NIF). The ability to simulate multi-material reactive burn in high pressure regimes has enabled the simulation [2] of the overdriven detonation states in the triple point overdrive experiment conducted by LANL.

### A. xRAGE

xRAGE [3] is an Eulerian radiation/hydrodynamics code under active development at LANL. xRAGE (Radiation Adaptive Grid Eulerian) supports simulations in 1D, 2D, and 3D, multiple materials, and coupling of radiation diffusion and hydrodynamics. Adaptive Mesh Refinement (AMR) of unit aspect ratio cell volumes supports large dynamic ranges of state space (centimeters to kilometers, microns to meters) with refinement and derefinement of adjacent $2^d$ cells (2 in 1D, 4 in 2D, and 8 in 3D) each timestep.

Most simulations using xRAGE are DRAM bandwidth bound with relatively low arithmetic intensity. This may surprise some readers as conventional wisdom is that HPC applications are largely FLOP bound, but prior analysis has shown most subroutines in xRAGE simulations are completely or significantly memory bound with an arithmetic intensity of 0.001 to 0.2 FLOP/byte using Intel roofline [4] analysis. Analysis using BYFL [5] “software based performance counters” illustrated in Table I details the types of instructions and the percentage issued from a representative xRAGE simulation. Sparse memory operations result in load/store operations coupled with integer and array indexing operations and represent 56% of all instructions issued in this simulation as detailed in Table I in blue font. Fine- and coarse-grained branching can be seen in the relatively high (25%) percent of conditional/branching instructions issued in this simulation, as detailed in Table I in red font. Floating point operation represent only 6% of instructions issued. This and deeper analysis [6] motivated a focused effort on addressing the memory wall in the Crossroads architecture.

### B. FLAG

FLAG is a Lagrange-based radiation/hydrodynamics code that supports multiple mesh optimization strategies in 1, 2, and 3D with support for fully unstructured (polyhedral) grids. FLAG supports arbitrary Lagrangian-Eulerian (ALE) and adaptive mesh refinement methods to handle mesh distortions / tearing and multiple levels of resolution.

Similar to xRAGE simulations, most simulations using FLAG are also DRAM bandwidth bound with relatively low arithmetic intensity. Memory access patterns in FLAG are often sparse, which the Pennant [7] proxy application attempts to capture. Analysis of Pennant, done as part of the Spatter [8] work, shows a significant number of scatter/gather patterns with non-unit strides. Some evidence gathered with gem5 simulations [6] further suggests that loaded latency [8] can also impact the performance of these simulations significantly.

The performance characteristics of these two codes, xRAGE and FLAG, are representative of a large number of LANL codes that make use of similar data structures. Improving the performance of these codes through architecture innovation has a broad impact to wide range of codes and their applications at LANL and therefore motivates our focus here. While both codes are capable of simulating hydrodynamics coupled with radiation transport this early study focuses exclusively on multi-material hydrodynamics test problems.

### IV. Experiments and Results

All experiments were conducted on Linux based dual-socket nodes. 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM nodes were configured as detailed above in section II. Intel Broadwell nodes were configured with E5-2695 V4 with 4 channels per socket of DDR4 operating at 2400 MT/s. Linux processes were bound to individual cores and memory was affinitized to the core to

| Instruction                  | Count      | Percentage |
|-----------------------------|------------|------------|
| Load                        | 6,773,030,349 | 18%        |
| Branching                   | 6,063,697,070 | 16%        |
| Integer Add                 | 5,334,155,682 | 15%        |
| Array Indexing              | 4,855,537,532 | 13%        |
| Conditional                 | 2,599,248,274 | 9%         |
| Store                       | 2,599,966,427 | 7%         |
| Type cast                   | 1,995,938,043 | 5%         |
| Stack frame allocation      | 1,541,094,404 | 4%         |
| FP multiplication           | 1,221,684,111 | 3%         |
| FP comparison               | 1,141,415,386 | 3%         |
| INT multiplication          | 991,524,374  | 3%         |

TABLE I: Instruction breakout by type in a representative simulation [5]. Red denotes operations attributable to branching (25%). Blue denotes operations attributable to sparse data structures (56%).
eliminate QPI traffic. All benchmarks were conducted without hyperthreading and without over-subscription of cores. For node-to-node comparisons, benchmark problems were limited to the 128 GB available on our Intel Broadwell and Intel Xeon Processors codenamed Sapphire Rapids with HBM.

The xRAGE code was used to benchmark an Asteroid impact problem using a configuration similar to those described in the literature [9]. Three problem sizes are given, one using 3 million mesh cells and a resident set size of up to 46GB of system memory (Asteroid_3M), another using 6 million mesh cells and a resident set size of up to 53GB of system memory (Asteroid_6M), and a third using 16 million mesh cells and a resident set size of up to 104GB (Asteroid_16M). Table II details the time to solution improvements of Asteroid simulations using xRAGE on 4th Gen Intel Xeon relative to BDW DDR and Intel Xeon Processors codenamed Sapphire Rapids with HBM relative to 4th Gen Intel Xeon. Overall performance of both 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM is significantly higher than that achieved by BDW DDR. The smaller benchmark problem Asteroid_3M is 5.83x faster on 4th Gen Intel Xeon relative to BDW DDR and 7.58x faster on Intel Xeon Processors codenamed Sapphire Rapids with HBM relative to BDW DDR. Larger problems such as Asteroid_6M and Asteroid_16M result in speedups of 5.14x and 3.39x on 4th Gen Intel Xeon and 8.57x and 7.25x on Intel Xeon Processors codenamed Sapphire Rapids with HBM demonstrating the significant performance improvements resulting in the HBM memory bandwidth. Strong scaling plots from 1/4, 1/2 and a full dual socket Broadwell, 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM. Smaller problem sizes of 80 and 64 using ALE show a bit larger performance improvements on 4th Gen Intel Xeon (3.58x and 3.6x) and a bit lower on Intel Xeon Processors codenamed Sapphire Rapids with HBM (5.76x and 5.28x). ALE requires significantly more instructions relative to LH for each hydrodynamics cycle which likely accounts for some of these differences. Further analysis using roofline modeling and frontend / backend analysis to determine potential contributors to this result is warranted. Strong scaling plots from 1/4, 1/2 and a full dual socket Broadwell, 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM for the FLAG Lagrange Hydro SOD test problem are illustrated in Figure 2. Strong scaling results for the FLAG ALE SOD Hydro test problem are illustrated in Figure 3.

Table II: Results of three simulations run using xRAGE utilizing 36 cores on Intel Broadwell (BDW) and 112 cores on 4th Gen Intel Xeon (SPR+DDR) and Intel Xeon Processors codenamed Sapphire Rapids with HBM (SPR+HBM) nodes. The FLAG code was used to benchmark a Sod shock tube test problem described in [10]. Two mesh management strategies are used, one using Lagrange hydrodynamics where the mesh “moves” during the simulation, labelled “LH”. The second uses ALE in which a Lagrange step is calculated and the material is advected (Eulerian step) to the fixed mesh labelled “ALE” for ALE with 2 materials. Table III details the time to solution improvements of Sod shock tube simulations using FLAG on 4th Gen Intel Xeon relative to BDW DDR and Intel Xeon Processors codenamed Sapphire Rapids with HBM relative to 4th Gen Intel Xeon. Performance of Lagrange Hydro with a problem size of 130^3 (3D mesh) is 3.68x higher on 4th Gen Intel Xeon relative to BDW DDR and is 7.94x higher on Intel Xeon Processors codenamed Sapphire Rapids with HBM. Smaller problem sizes of 10^3 and 80^3 using LH show somewhat smaller but still quite respectable performance improvements on 4th Gen Intel Xeon and Intel Xeon Processors codenamed Sapphire Rapids with HBM. The smaller problem sizes likely have a negligible cache effect here as they are still relatively large. Performance of ALE Hydro with a problem size of 10^4 (3D mesh) is 3.49x higher on 4th Gen Intel Xeon relative to BDW DDR and is 6.07x higher on Intel Xeon Processors codenamed Sapphire Rapids with HBM. Smaller problem sizes of 80^3 and 64^3 using ALE show a bit larger performance improvements on 4th Gen Intel Xeon (3.58x and 3.6x) and a bit lower on Intel Xeon Processors codenamed Sapphire Rapids with HBM (5.76x and 5.28x).

V. CONCLUSIONS

Multi-physics codes designed to simulate large state and phase spaces with many materials are often memory bandwidth rather than FLOP bound. Addressing this bottleneck has proven quite challenging as many architectures have continued to grow in raw FLOP performance while memory bandwidth increases have been more modest. To address this, LANL has worked closely with Intel to integrate high-bandwidth memory in the Intel Xeon Processors codenamed Sapphire Rapids with HBM as part of the Crossroads Supercomputer design. Early experience with pre-production silicon shows extremely promising results with performance improvements up to 8.57x over current HPC systems at LANL. While other technologies have at times required significant refactoring or complete rewrites of major portions of a code, a simple recompile was all that was necessary when porting to Intel Xeon Processors.
Fig. 1: Strong scaling of xRAGE Asteroid test problem at 1/4, 1/2, and a full dual socket Broadwell (BDW), 4th Gen Intel Xeon (SPR+DDR), and Intel Xeon Processors codenamed Sapphire Rapids with HBM (SPR+HBM) nodes.

codenamed Sapphire Rapids with HBM. These results demonstrate a fruitful path towards efficient computing technologies in the future for LANL’s most challenging applications.

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Fig. 2: Strong scaling of the FLAG Lagrange Hydro SOD test problem at 1/4, 1/2, and a full dual socket Broadwell (BDW), 4th Gen Intel Xeon (SPR+DDR), and Intel Xeon Processors codenamed Sapphire Rapids with HBM (SPR+HBM) nodes.

Fig. 3: Strong scaling of the FLAG ALE Hydro SOD test problem at 1/4, 1/2, and a full dual socket Broadwell (BDW), 4th Gen Intel Xeon (SPR+DDR), and Intel Xeon Processors codenamed Sapphire Rapids with HBM (SPR+HBM) nodes.