Floating zone silicon wafer bonded to Czochralski silicon substrate by surface-activated bonding at room temperature for infrared complementary metal-oxide-semiconductor image sensors

Yoshihiro Koga* and Kazunari Kurita

SUMCO Corporation, Imari, Saga 849-4256, Japan
*E-mail: ykoga4@sumcosi.com

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We propose to use a bonding wafer as an alternative epitaxial wafer with an extra thick epitaxial layer of more than 100 μm thickness to fabricate vertical time-of-flight (TOF) complementary metal-oxide-semiconductor (CMOS) imaging sensors that can detect infrared (IR) radiation of wavelength greater than 1120 nm. This bonding wafer comprises a floating zone (FZ)-grown silicon wafer bonded to a Czochralski (CZ)-grown silicon substrate by room-temperature surface-activated bonding. Because the device-fabricating region is formed by bonding the FZ-grown wafer to the CZ-grown silicon substrate at room temperature, the oxygen concentration in this region is decreased to less than that in an epitaxial wafer. In addition, our bonded wafer can have a strong gettering capability for oxygen and transition metals (nickel, copper, and iron) in the bonding interface. Furthermore, the bonded wafer can inhibit out-diffusion of oxygen or transition metal to the device-fabricating region from the CZ-grown silicon substrate, and the device-fabricating region can have fewer impurities after fabricating the devices in the bonded wafer. Therefore, we consider that this bonded wafer can be fabricated by the simple processes of bonding and grinding (polishing) at room temperature without thermal stress, and this method is effective for decreasing the dark currents and white-spot defects generated owing to the presence of oxygen or transition metal, which are undesirable in advanced TOF-CMOS imaging sensors of a vertical structure. © 2020 The Japan Society of Applied Physics

1. Introduction

The realizations of global peace and safety are of particular importance for humans, as are the realizations of convenience and comfort. Much security is required to realize the former. For example, public facilities such as airports, station platforms, sports stadiums, shopping malls, and police boxes must be installed with many security cameras to prevent crime. Living spaces such as apartments and houses must also be equipped with security cameras. These security cameras must sensitively detect people and objects such as automobiles or buildings at distances of, for example, 30–40 m.

Many sensors are required to realize automation that will provide us with convenience and comfort. For example, automatic driving, industrial robots, and drones require sensors to move autonomously without human control.

These sensors must correctly detect people and objects such as automobiles or buildings. The cameras and sensors must include time-of-flight (TOF) complementary metal-oxide-semiconductor (CMOS) imaging devices that can correctly measure the distance from a person or object.1,2 Since infrared (IR) radiation is less diffused in air than other types of light, IR radiation has the characteristic of better straightness than other types of light. Thus, an IR beam is best for reaching and being reflected from an object at a distance of 30–40 m. Therefore, the TOF-CMOS imaging sensor must be able to detect IR radiation to correctly detect a person or object at a long distance.

Figure 1 shows a cross-sectional image of the chip fabricated with these devices in a silicon wafer. When CMOS-FETs and a detected sensor are fabricated in a silicon wafer, their size can be reduced and formed in a system on a chip (SoC).3 In addition, device yields are more stable than those of other semiconductor devices. However, since IR radiation is easily transmitted through a silicon crystal,4 the silicon crystal in a sensor for detecting IR radiation must be very thick. When IR radiation with a wavelength of over 1120 nm is detected in a silicon wafer, the thickness of the detected region must be greater than 100 μm. Epitaxial silicon layer growth takes a long time, such as more than 30 h at high temperatures beyond 1000 °C,5 when forming a detecting sensor in an epitaxial layer on a silicon crystal substrate. Consequently, the silicon substrate will be bent, have some slips, or be contaminated with metallic impurities from the equipment during the process of growing the epitaxial layer. In addition, oxygen dissolved in the silicon substrate diffuses out to the epitaxial layer during the process of its growth at high temperatures beyond 1000 °C.6,7 However, because the epitaxial growth process is very long, the production cost of this wafer is too high.

If the silicon substrate is bent, alignment cannot be achieved in the photolithography process for patterning devices in an integrated circuit. If slips are generated in the silicon substrate, it will be broken by thermal stress during heat treatment at high temperatures beyond 1000 °C in the device-fabrication process. Figure 2 shows the detailed cross-sectional structure of the detecting sensor region shown in Fig. 1, for a TOF-CMOS imaging sensor fabricated in an epitaxial wafer. Because the image sensor must super sensitively detect IR radiation, which is easily transmitted through the silicon wafer, the sensor is made of an avalanche photodiode (APD) that can be formed vertically and deeply.8 If metallic impurities contaminate the region of the APD in the epitaxial layer, they form deep energy levels in the contaminated region.9,10 These deep energy levels act as generation or recombination centers that mostly affect the electrical characteristics of the imaging sensor, such as dark current and white-spot defect density.11,12 Thus, they degrade the yield and reliability of the detecting sensors. If
Oxygen diffuses out from the silicon substrate to the region of the APD after fabricating the devices, and this oxygen also forms deep-level defects in the APD region. These oxygen-related defects cause incomplete transfer of the electrical charges accumulated in the APD when detecting IR radiation, and consequently, fixed-pattern noise occurs in the detected signal. That is, these metallic impurities and oxygen-related defects strongly affect the performance of the TOF-CMOS imaging sensor. Therefore, the epitaxial layer on the silicon substrate should be grown at a lower temperature to inhibit out-diffusion from the Czochralski (CZ)-grown silicon substrate to the epitaxial layer during its growth on the silicon substrate. Since epitaxial layers do not grow on the crystal silicon substrate below 900 °C, the layer grown at less than 900 °C is not epitaxial but polycrystalline or amorphous. There is a limit on the minimum temperature at which an epitaxial layer can be grown on a CZ-grown silicon wafer substrate as shown in Fig. 2.

In order that an epitaxial layer is formed on a silicon substrate without out-diffusing oxygen at low temperature, we previously studied the bonding wafer comprising an epitaxial wafer bonded to a silicon substrate at room temperature for CMOS imaging sensor devices, so that the concentration of oxygen in the device-fabricating region will be less than that of the epitaxial wafer. Figure 3 shows the custom epitaxial wafer and this previous bonding wafer for CMOS imaging sensor devices. In the case of the epitaxial wafer shown in Fig. 3(a), because oxygen is diffused from the silicon substrate to an epitaxial layer [shown as the buffer layer in Fig. 3(a)] during the growth of the epitaxial layer, an additional epitaxial layer must be grown. In the case of the bonding wafer shown in Fig. 3(b), because the epitaxial wafer is bonded to the silicon substrate, this epitaxial wafer must also have an additional epitaxial layer, and the silicon substrate and buffer layer of the bonded epitaxial wafer must be removed. When the thickness of the CMOS imaging sensor device is less than 10 μm, an additional epitaxial layer of about 4 μm can be grown as a buffer layer. However, for TOF-CMOS imaging devices thicker than 100 μm, because the epitaxial growth time is very long, the buffer layer is also thicker and will be about 40 μm. Thus, in the epitaxial wafer of TOF-CMOS imaging devices more than 100 μm thick, it is assumed to be impossible to keep the concentration of oxygen low.

On the other hand, for the concentration of oxygen to be low in an imaging device more than 100 μm thick, it is proposed that a floating zone (FZ)-grown silicon wafer be bonded to a CZ-grown silicon substrate at a high temperature of over 1000 °C for 3 or 4 h without growing an epitaxial layer on the silicon substrate. This bonded wafer is contaminated with metallic impurities from the heat-treatment equipment such as the stage or the tube during the heat treatment to bond the two silicon wafers. To be exact, because two silicon substrates are joined by Si–O bonds and a voidless thermal bond cannot form without SiO2 at the bonding interface, this thermal bonding wafer has a thin SiO2 layer in the bonding interface. Because the diffusion of metallic impurities such as nickel and iron through the SiO2 layer is negligible when these metals contaminate the bonded silicon layer during device-fabrication processes such as plasma etching, annealing, and implantation, the contaminant metals remain at the bonding interface of the bonded silicon layer after device fabrication. The device yield is consequently decreased because of the contamination by metals. In addition, because the wafer fabrication processes are long, the production cost of this bonding wafer is higher, like the SOI wafer, than that of an epitaxial wafer.

To solve the above issues, we propose a bonded wafer comprising an FZ-grown silicon wafer bonded to a CZ-grown silicon substrate at room temperature by surface-activated bonding (SAB) without a SiO2 layer. The bonded FZ-grown silicon wafer is ground and polished to the desired thickness of the device-fabricating region similar to an epitaxial layer. This bonded wafer can have a flexible FZ-grown silicon layer for a device-fabricating region thicker
than 100 μm that can be formed at room temperature without contamination by metallic impurities or oxygen. In addition, because this bonded wafer has a bonding interface under the FZ-grown silicon layer, this bonding interface acts as a gettering sink that will capture metallic impurities and oxygen. Thus, the FZ-grown silicon layer will not be contaminated by the impurities. Consequently, this FZ-grown silicon layer is as clean as an FZ-grown silicon wafer after fabricating the bonded wafer and the devices into the bonded wafer. Therefore, the performance of devices fabricated in the layer of the bonded wafer will be very good.

2. Experimental methods

Figure 4 shows our method of fabricating the bonded silicon wafer made of an active FZ wafer and a base CZ wafer. We fabricated two silicon wafers: an FZ wafer as the active wafer and a CZ wafer as the base wafer. The active FZ wafer was then bonded to the base CZ wafer as the silicon layer in which to fabricate devices, by SAB at room temperature in ultrahigh vacuum. After bonding the two wafers, the active FZ wafer was ground and polished from the back, which is the side opposite the bonding interface, to the desired thickness.

2.1. Sample preparation

Table I lists the characteristics of the 200 mm diameter wafer that was polished to a silicon layer of 725 μm thickness. The active wafer was (100) phosphorus-doped FZ-grown single-crystal silicon, and the base wafer was (100) phosphorus-doped CZ-grown single-crystal silicon. Their resistivities were 60 Ω cm for the FZ wafer and 10 Ω cm for the CZ wafer. Their oxygen concentrations were less than 0.1 × 10^{17} atoms cm⁻³ for the FZ wafer and 8.0 × 10^{17} atoms cm⁻³ for the CZ wafer.

As shown in Fig. 4, the FZ active wafer was bonded to the base CZ wafer as the device-fabricating region, by SAB in an ultrahigh vacuum of less than 1 × 10⁻⁵ Pa at room temperature (Mitsubishi Heavy Industries Machine Tool Co., Ltd., MWB-08-AX). The top surfaces of these wafers were irradiated with argon ions at energies of 1–2 keV for 3 min. After bonding the two wafers with a force of 100 kN, the back of the active FZ wafer was ground and polished to a thickness of 5 μm.

We also prepared a reference sample with an epitaxial layer grown on a CZ wafer. This CZ wafer was (100) phosphorus-doped CZ-grown single-crystal silicon. Its resistivity was 10 Ω cm, and its oxygen concentration was 3.0 × 10^{17} atoms cm⁻³. The CZ wafer was grown on a 5 μm thick n-type epitaxial layer using Si₃HCl and PH₃ gas sources at 1100 °C.

2.2. Experimental procedure

As shown in Fig. 4, voids and defects were searched for after bonding an active FZ wafer to a base CZ wafer [steps (a) and (b)] and after the heat treatment in the device fabrication [step (c)]. We then evaluated the concentration of oxygen in the bonded FZ wafer after grinding and polishing it to the thickness of the device-fabricating region and the heat treatment in the device fabrication [steps (d) and (e)]. In addition, we evaluated the capability of gettering for transition metals [steps (f) and (g)]. Finally, we evaluated the characteristics of real devices and studied the bonded wafer after fabricating actual devices [steps (h)–(k)].

2.2.1. Evaluation of voids remaining after bonding active FZ wafer to base CZ wafer.

The remaining voids were evaluated by IR transmission observation after bonding the active FZ wafer to the base CZ wafer by SAB at room temperature in an ultrahigh vacuum. An IRise (Moritex) system was used for the IR observation. In this system, because the wavelength of the IR radiation is higher than 1000 nm, the IR radiation is transmitted through the silicon wafer and reflected by the remaining voids. Thus, the remaining voids in the wafer can be detected using this IR radiation.

2.2.2. Observation of cross section and surface of studied bonded wafer.

An H9000UHR-I microscope (Hitachi) was used for transmission electron microscopy (TEM) to observe wafer-bonding-induced defects. Cross-sectional TEM and high-resolution TEM (HR-TEM) images were used to characterize structural defects, such as wafer-bonding-induced defects, created during the fabrication of the bonded wafer.

![Fig. 3.](https://example.com/fig3.png)

**Fig. 3.** (Color online) Cross-sectional images of the chip formed in epitaxial and bonded epitaxial wafers: (a) epitaxial wafer and (b) bonded epitaxial wafer.
bonded wafer, the heat treatment in the device-fabrication process, and the fabrication of actual devices. Small pieces were cut as chip samples from the studied wafers after each of the three processes.

Figure 5 illustrates the process of the heat treatment in the fabrication of the TOF-CMOS imaging sensor. The heat treatment was carried out above 900 °C in nitrogen atmosphere, and the sample stage was loaded and unloaded at 900 °C in an ambient gas of nitrogen in a furnace.

An OPTIPHOT-88 microscope (Nikon) was used for optical microscopy (OM) to observe the pits made by nickel silicide to evaluate nickel gettering after contaminating the sample with nickel and Wright etching. This etching treatment involves dipping the sample contaminated with nickel into the Wright etching solution with stirring for 3 min, followed by cleaning of the dipped sample in pure water for 10 min.

2.2.3. Evaluation of profile of concentrations of oxygen and transition metals. The concentrations of oxygen and transition metals (nickel, copper, and iron) were measured through secondary ion mass spectroscopy (SIMS) measurement using CAMECA IMS7f equipment. After the fabrication of the wafer, the heat treatment during the device fabrication, and the fabrication of actual devices, small pieces were cut from each sample for SIMS analysis after bonding the interface after fabricating actual devices.

Table I. Samples used in this study.

| Substrate wafer       | Activate layer                  | SIMS analysis                  |
|-----------------------|---------------------------------|--------------------------------|
| Studied sample (Bonded wafer) | CZ-silicon wafer n-type (phosphorus-doped) 10 Ω cm Op: 8.0 × 10^{17} atoms cm^{-3}          | Bonded FZ wafer n-type (phosphorus-doped) 60 Ω cm Op ≤ 0.1 × 10^{17} atoms cm^{-3}          |
| Reference sample (Epitaxial wafer) | CZ-silicon wafer n-type (phosphorus-doped) 10 Ω cm Op: 3.0 × 10^{17} atoms cm^{-3} | Epitaxial layer n-type (phosphorus-doped) 60 Ω cm 5 μm |

Fig. 4. Experiment flow. Step (a): IR observation after bonding two wafers. Steps (b), (c), and (j): Cross-sectional TEM image observation at bonding interface. Steps (d), (e), (g), and (i): SIMS analysis of silicon layer. Step (f): Surface observation after contaminating with metal. Step (h): Device measurement. Step (k): EDX analysis at bonding interface after fabricating actual devices.

Fig. 5. (Color online) Time sequence of heat treatment in device fabrication.
measurement. The concentration distributions of oxygen and transition metals from the surface of samples to a depth of 10 μm were estimated from the intensities of the impurity-related SIMS peaks in the SIMS spectra.

2.2.4. Evaluation of capability of gettering transition metals. Small pieces were cut as chip samples from the studied bonded wafer. Firstly, these chip samples were cleaned with hydrofluoric acid, SC1, and SC2 solutions. Secondly, the front of the samples was contaminated with nickel, copper, or iron metallic impurities to a concentration of 2 × 10¹³ atoms cm⁻² by spin-coating an acid solution containing one of these metals. Thirdly, these samples were heat-treated under the conditions where the spin-coated transition metals diffuse from the surface of the studied sample to the silicon substrate. The heat treatment was carried out at 1100 °C for 2 h in nitrogen, and the sample stage was loaded and unloaded at 900 °C in nitrogen atmosphere in a furnace. Finally, the pits made by nickel silicide were observed after Wright etching for 3 min to etch not the nickel silicide but only the silicon layer of a thickness of about 3 μm at the surface, and the depth profiles of the concentrations of nickel, copper, and iron were evaluated by SIMS analysis.

2.2.5. Evaluation of pn-junction diode. Figure 6 illustrates the process of fabricating the pn-junction diode as the basic device of the TOF-CMOS imaging sensor in order to understand the efficiency of the studied bonded wafer compared with that of the epitaxial wafer. This fabrication was carried out between 400 °C and 1050 °C in nitrogen atmosphere, and the sample stage was loaded and unloaded at 400 °C when the heat treatment temperature was 400 °C or at 900 °C when the heat treatment temperature was above 900 °C in an ambient gas of nitrogen in a furnace. The characteristics of the pn-junction diodes fabricated on two wafers (the studied bonded wafer and the reference epitaxial wafer) were measured by a voltage step-stress method. While zero voltage was supplied to metal β and the back of the sample, an input voltage from −3 to 3 V in steps of 0.1 V was supplied to metal α. A Keithley 237 High-Voltage Source-Measurement Unit (Keithley) was used as the measurement system and an STN-W010-D0.5-L32 system (Tiatech) was used as the probing equipment. The probe was made of tungsten and had a diameter of 10 μm.

2.2.6. Analysis of elements contained in bonding interface defects. The elements contained in the bonding interface defects were analyzed through energy-dispersive X-ray spectroscopy (EDX) analysis using JED-2300 and ARM200F Dual-X (JEOL). After fabricating actual devices on the studied wafer, small pieces were cut from the wafer for EDX analysis. After X-ray irradiation of the defects of the bonding interface in a cross section of the sample, the reflection X-rays were detected using a semiconductor detector. The element contained in the defect was elucidated from the detected energy of the electron–hole pair, and the concentration of the element contained in the defect was determined from the intensity of the detected energy.

3. Results and discussion

3.1. Evaluation and observation of voids formed during SAB of FZ wafer to CZ wafer

We evaluated the remaining voids by IR transmission imaging after SAB of the FZ wafer to the CZ wafer at room temperature under a pressure of 1 × 10⁻⁵ Pa. Figure 7 shows an IR transmission image of the studied sample. A lattice pattern shows a shot of the IR transmission image and does not show some defects in the bonding wafer. The studied sample does not have any voids in the 200 mm diameter wafer. Because this evaluation method can detect gaps larger than 200 nm, this studied sample does not have any voids larger than 200 nm.

In detail, we also observed the bonded interface on a cross-sectional TEM image of the chip obtained after dicing the
bonded wafer at its center. Figure 8(a) shows a cross-sectional HR-TEM image of the fabricated wafer. The bonding interface was flat and there were no voids with gaps larger than 0.2 nm at the bonding interface between the active FZ wafer and the base CZ wafer. Amorphous layers of 6 nm thickness were observed at the bonding interface of the active FZ wafer and the base CZ wafer.

In addition, we observed the bonded interface on a cross-sectional TEM image to evaluate thermal stability after the heat treatment in the device fabrication, as shown in Fig. 5. Figure 8(b) shows a cross-sectional HR-TEM image. The bonding interface was also flat and there were no voids with gaps larger than 0.2 nm at the bonding interface. The amorphous layer of 6 nm thickness was not observed in the bonding interface. Because the amorphous layer is recrystallized to a silicon crystal during the heat treatment. In addition, the white line marked by the red arrows in Fig. 8(b) and the strain regions enclosed by the blue dotted lines in Fig. 8(b) were observed in the bonding interface. Because the amorphous layer is recrystallized to the bonding interface from a single-crystal region of the base CZ wafer and the bonding FZ wafer, we assumed that lattice mismatch would arise and cause strain at the bonding interface.

3.2. Depth profile of oxygen concentration

For the studied bonded wafer and the reference epitaxial wafer after wafer fabrication, the heat treatment in device-fabrication processes, and device fabrication, we evaluated the depth profiles of the oxygen concentration by SIMS. Figures 9(a)–9(c) respectively show the depth profiles of the concentrations of oxygen after wafer fabrication, heat treatment, and device fabrication. The horizontal axis is the depth from the surface of samples, and the vertical axis is the concentration of oxygen obtained by SIMS analysis. The detection limit of oxygen in SIMS is about $3 \times 10^{16}$ atoms cm$^{-3}$.

Figure 9(a-i) shows the results for a reference epitaxial wafer after wafer fabrication. The oxygen concentration increased from the depth of 2 to 5 μm in the epitaxial layer. This result is the same as that in the previous study. The diffusion coefficient of oxygen into silicon crystal at 1100 °C indicates that oxygen can out-diffuse from at least 2 μm below the silicon substrate to the epitaxial layer during the growth of the epitaxial layer at 1100 °C. Therefore, the profile of the reference sample was that oxygen out-diffused from the silicon substrate to the epitaxial layer during the growth of the epitaxial layer. On the other hand, Fig. 9(a-ii) shows the results for the studied bonded wafer after wafer fabrication. The concentration of oxygen in the bonded FZ Si layer from the surface to the bonding interface is constant at $3 \times 10^{16}$ atoms cm$^{-3}$, which is the detection limit. The concentration of oxygen at the region of the bonding interface near 5 μm is high, beyond $1 \times 10^{20}$ atoms cm$^{-3}$. In the previous study, oxygen knocked into the surface of the silicon substrate by SAB, and oxygen exits at a high concentration at the bonding interface. Thus, the result shown in Fig. 9(a-ii) is reasonable. The concentration of oxygen in the bonded FZ Si layer can be less than that in the epitaxial layer of the device-fabricating region, in spite of the silicon substrate containing a higher concentration of oxygen, $8 \times 10^{17}$ atoms cm$^{-3}$, than that in the silicon substrate of the epitaxial wafer, $3 \times 10^{17}$ atoms cm$^{-3}$. The bonded wafer might also have a decreased concentration of oxygen in the silicon layer after fabricating devices.
Figure 9(b) shows the depth profile of the oxygen concentration after the heat treatment in the device fabrication shown as Fig. 5. Figure 9(b-i) shows the results for a reference epitaxial wafer. Compared with that before heat treatment, as shown in Fig. 9(a-i), the concentration of oxygen increased to beyond $1 \times 10^{17}$ atoms cm$^{-3}$ at depths from 1 to 5 $\mu$m in the epitaxial layer after heat treatment. According to the diffusion coefficient of oxygen into a silicon crystal at 1050 °C,28) oxygen can out-diffuse from at least 4 $\mu$m below the silicon substrate to the epitaxial layer during heat treatment at temperatures under 1050 °C. Thus, this result is reasonable. On the other hand, Fig. 9(b-ii) shows the results for the studied bonded wafer. The concentration of oxygen in the bonded FZ Si layer from the surface to the bonding interface is also constant at $3 \times 10^{16}$ atoms cm$^{-3}$, which is the detection limit after heat treatment. The oxygen concentration in the region of the bonding interface increased from $1.4 \times 10^{20}$ to $2.5 \times 10^{20}$ atoms cm$^{-3}$. The same phenomenon was observed in the previous study.7) Because the remaining strain at the bonding interface acts as a gettering sink, oxygen was captured at this interface and could not out-diffuse from the silicon substrate to the bonded FZ Si layer. Thus, the concentration of oxygen in the bonded FZ Si layer can be kept below $3 \times 10^{16}$ atoms cm$^{-3}$ after heat treatment. Upon comparison of the results for the reference epitaxial wafer shown in Fig. 9(b-i) and that of the studied bonded wafer shown in Fig. 9(b-ii), the concentration of oxygen in the bonded FZ Si layer of the bonded wafer is found to be one order smaller than that in the epitaxial layer of the epitaxial wafer after heat treatment.

For verification, the depth profiles of the concentration per volume of oxygen was analyzed in the studied sample and the reference sample by SIMS, after removing the metal and interlayer insulator of the samples with a pn-junction device fabricated as an actual device. Figure 9(c) shows the profiles of oxygen concentration. The oxygen concentration in the reference sample was more than $7 \times 10^{16}$ atoms cm$^{-3}$, and diffusion was from the inside of the silicon substrate to the device-fabrication region in the epitaxial layer, as shown in Fig. 9(c-i). This result is the same as that in Fig. 9(b-i) after the heat treatment in the device fabrication. On the other hand, the oxygen concentration in the studied sample was kept below $5 \times 10^{16}$ atoms cm$^{-3}$, and diffusion to the device-fabrication region was minimal, as shown in Fig. 9(c-ii). This result is the same as that in Fig. 9(b-ii) after the heat treatment in the fabrication of actual devices. Thus, the concentration of interstitial oxygen in the bonded FZ Si layer of the studied sample was lower than that in the epitaxial layer of the reference sample after fabricating the pn-junction diode.

From the above results, we conclude that the studied bonded wafer can inhibit the out-diffusion of interstitial oxygen from the silicon substrate (the base CZ wafer) to
The capability for nickel of at least 2 × 10^{13} atoms cm^{-2} and reference sample had a large amount of nickel silicide. On the other hand, the studied sample did not contain any nickel silicide. Wright etching etches not the nickel silicide (bonded wafer). No pits were observed in the surface of the chip. Because Wright etching etches not the nickel silicide but only the silicon layer, the silicon layer of the studied sample did not contain any nickel silicide. On the other hand, the reference sample had a large amount of nickel silicide. Therefore, this studied bonded wafer has the gettering capability for nickel of at least 2 × 10^{13} atoms cm^{-2} whereas the reference sample does not.

3.3. Gettering behaviors of transition metal

Figure 10 shows the OM images of the pits made by nickel silicide on the surfaces of two samples (studied bonded wafer and reference epitaxial wafer) after nickel contamination at 2 × 10^{13} atoms cm^{-2} and Wright etching. Figure 10(a) shows the result for the reference sample (epitaxial wafer). Many pits were observed in the surface of the chip. The reverse current of the studied sample (bonded wafer) was below 1 × 10^{-9} A cm^{-2}, as shown by solid line ii in Fig. 12. On the other hand, that of the reference sample was higher than 1 × 10^{-9} A cm^{-2}, as shown by solid line i in Fig. 12. The leakage current of the studied sample decreased to one-thousandth that of the reference sample.

In general, the leakage current of the pn-junction diode is increased by contamination with oxygen or a transition metal. In Sect. 3.2, the oxygen in the reference sample was shown to diffuse from the inside to the surface during the device fabrication, as shown in Fig. 9(c-i). On the other hand, the oxygen in the studied sample did not diffuse at all, as shown in Fig. 9(c-ii). In addition, as described in Sect. 3.3, the studied bonded wafer exhibited the gettering capability for transition metal (nickel, copper, and iron), as shown in Fig. 11, whereas the reference epitaxial wafer did not, as shown in Fig. 10. Therefore, we assumed that the leakage current of the studied sample was due to decreased oxygen.

3.4. Characteristic of actual devices

We measured the pn-junction diode fabricated as an actual device in two samples (studied bonded wafer and reference epitaxial wafer) by the process and with the structure shown in Fig. 6. Figure 12 shows the results of measurement of the pn-junction diode. Solid line i and dotted line ii in Fig. 12 respectively show the results for the reference epitaxial wafer and the studied bonded wafer. They had a reverse current of −3 to 0 V and a forward current of 0–3 V. Therefore, both of them showed characteristics of a pn-junction diode, indicating the successful fabrication of a pn-junction in the samples. The reverse electrical current of the studied sample was below 1 × 10^{-9} A cm^{-2}, as shown by solid line ii in Fig. 12. The reverse current of the studied sample decreased to one-thousandth that of the reference sample.

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![Fig. 11](image-url) (Color online) Depth profiles of metallic-impurity concentration for studied samples measured through SIMS analysis (i) after contamination of 2 × 10^{13} atoms cm^{-2} and (ii) after fabricating pn-junction diodes: (a) nickel, (b) copper, and (c) iron.
and transition-metal concentrations in the device-fabricating region.

For verification, we observed the bonded interface of the studied sample on a cross-sectional TEM image after fabricating the pn-junction diode. Figure 13 shows the cross-sectional HR-TEM image. The bonding interface was flat and there were no voids larger than 0.2 nm. Also, no amorphous layer of 3 nm thickness was observed in the bonding interface. This result is the same as that in Fig. 9 for after the heat treatment in the fabrication of actual devices, and we understood that the pn-junction diodes were fabricated in studied samples with no trouble. In addition, defect A was observed in the strain regions shown in Fig. 8, as indicated by the blue dotted line in Fig. 13. Thus, as discussed in Sect. 3.1, this defect A was formed as a result of lattice mismatch and strain of the silicon crystal after recrystallizing the amorphous layer generated by argon-ion irradiation in the SAB process during device fabrication. Because oxygen and transition metals were detected in the bonding interface at high concentrations, as shown in Figs. 9 and 11, we assumed that this defect A captured oxygen and transition metals and contained them.

When the concentration of an element in a silicon crystal is more than $1 \times 10^{20}$ atoms cm$^{-3}$, EDX analysis can yield a concentration map of that element.32,33) Because the concentration of oxygen detected at the bonding interface by SIMS analysis exceeded $1 \times 10^{20}$ atoms cm$^{-3}$ (Fig. 9), we analyzed the concentration map of elemental oxygen around the bonding interface by EDX analysis. Figure 14(a) shows the analyzed area, and Fig. 14(b) shows the concentration map of elemental oxygen in the studied sample. A high concentration of oxygen was detected at defect A. In addition, the depth profile of oxygen is shown in Fig. 14(c). Oxygen was detected at concentrations beyond the detection limit at defect A and was maximum at the bonding interface. In accordance with the Cottrell effect, impurities segregate to relieve strain in the silicon crystal,34,35) and the strain region acts as a gettering sink. Thus, we concluded that defect A with strain and the bonding interface with lattice mismatch acted as gettering sinks for oxygen.

On the other hand, because the concentrations of nickel, copper, and iron were lower than the detection limit ($1 \times 10^{20}$ atoms cm$^{-3}$) of EDX analysis, they could not be detected. However, nickel, copper, and iron were detected at the bonding interface by SIMS analysis, as shown in Fig. 11. Yu et al.26) showed that copper segregated at the bonding interface. Maurice and Colliex36) showed that copper and iron segregated into grain boundaries. Because our studied bonding wafer has defect A with strain and a bonding interface with lattice mismatch at the bonding interface, as shown in Fig. 13, we considered that their defects also act as a gettering sink for the metals. Therefore, we concluded that the studied bonding wafer could decrease the concentration of oxygen and metallic impurities in the device-fabricating region by gettering oxygen and metallic impurities at the bonding interface and also decrease the leakage current of the pn-junction diode formed in the bonded FZ Si layer.

4. Conclusions

We provided the first demonstration of the bonding characteristics and oxygen- and transition-metal-impurity gettering performances of a wafer comprising an FZ wafer and a CZ substrate bonded by SAB at room temperature. This bonded wafer has an amorphous layer of 6 nm thickness in the bonding interface. Because the remaining strain in the region where this amorphous layer was recrystallized acts as a gettering sink for oxygen and metallic impurities, and the reverse electrical current of the pn-junction diode formed in the studied bonded wafer decreased to one-thousandth that of a pn-junction diode fabricated in the reference epitaxial wafer, we believe that this bonded wafer will contribute to achieving a high sensitivity of the TOF-CMOS image sensor and be beneficial for advanced and next-generation TOF-CMOS image sensors.

Fig. 13. (Color online) Cross-sectional TEM image of the studied bonded wafer after fabricating pn-junction diodes.

Fig. 12. Characteristics of the pn-junction diode fabricated on (i) the reference epitaxial wafer and (ii) the studied bonded wafer.

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**Fig. 13.** (Color online) Cross-sectional TEM image of the studied bonded wafer after fabricating pn-junction diodes.
Fig. 14. (Color online) Map and depth profile of elemental oxygen for the studied bonded wafer, obtained by EDX analysis after fabricating pn-junction diodes: (a) cross-sectional TEM image of the analyzed region, (b) map of elemental oxygen concentration, and (c) depth profile of elemental oxygen.

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