Scaling behavior of InAlN/GaN HEMTs on silicon for RF applications

Peng Cui1,2* & Yuping Zeng2,2*

Due to the low cost and the scaling capability of Si substrate, InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions. In this paper, a high-performance 50-nm-gate-length InAlN/GaN HEMT on Si with a high on/off current \((I_{on}/I_{off})\) ratio of \(7.28 \times 10^6\), an average subthreshold swing (SS) of 72 mV/dec, a low drain-induced barrier lowering (DIBL) of 88 mV, an off-state three-terminal breakdown voltage \((BV_{ds})\) of 36 V, a current/power gain cutoff frequency \((f_{T}/f_{max})\) of 140/215 GHz, and a Johnson’s figure-of-merit (JFOM) of 5.04 THz V is simultaneously demonstrated. The device extrinsic and intrinsic parameters are extracted using equivalent circuit model, which is verified by the good agreement between simulated and measured S-parameter values. Then the scaling behavior of InAlN/GaN HEMTs on Si is predicted using the extracted extrinsic and intrinsic parameters of devices with different gate lengths \((L_g)\). It presents that a \(f_{T}/f_{max}\) of 230/327 GHz can be achieved when \(L_g\) scales down to 20 nm with the technology developed in the study, and an improved \(f_{T}/f_{max}\) of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrown ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

**Abbreviations**
- HEMT: High-electron-mobility transistor
- \(I_{on}\)/\(I_{off}\): On/off current ratio
- SS: Subthreshold swing
- DIBL: Drain-induced barrier lowering
- \(BV_{ds}\): Off-state three-terminal breakdown voltage
- \(f_{T}/f_{max}\): Current/power gain cutoff frequency
- JFOM: Johnson’s figure-of-merit
- \(g_m\): Extrinsic transconductance
- MOCVD: Metalorganic chemical vapor deposition
- SEM: Scanning electron microscopy
- \(I_d\): Drain current
- \(I_g\): Gate current
- \(L_g\): Gate length
- \(L_{sd}\): Source-drain spacing
- \(V_{gs}\): Gate-source voltage
- \(V_{ds}\): Drain-source voltage
- \(R_{on}\): On-resistance
- SCEs: Short-channel effects
- \(|h_{21}|\): Current gain
- U: Unilateral gain
- MSG: Maximum stable gain

InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions due to the low cost and the scaling capability of Si substrate\(^1\). Li et al. demonstrated an InAlN/GaN HEMT on Si with a gate length \((L_g)\) of 55 nm and a source-drain spacing \((L_{sd})\) of 175 nm\(^1\) using \(n^+\)-GaN regrowth source/drain contacts. The device presents a maximum drain current \((I_{d,max})\) of 2.8 A/mm, a peak extrinsic

\(^1\)Institute of Novel Semiconductors, Shandong University, Jinan 250100, Shandong, China. \(^2\)Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716, USA. \(^*\)email: pcui@sdu.edu.cn; yzeng@udel.edu
transconductance \((g_m)\) of 0.66 S/mm, and a current/power gain cutoff frequency \((f_T/f_{\text{max}})\) of 250/204 GHz. Xie et al. reported that a record \(f_T\) of 310 GHz was achieved on an InAlN/GaN HEMT on Si with a 40-nm gate length\(^6\). Cui et al. demonstrated an 80-nm-gate-length InAlN/GaN HEMT on Si with a record high on/off current \((I_{\text{on}}/I_{\text{off}})\) ratio of 1.58 \times 10^6, a steep subthreshold swing (SS) of 65 mV/dec, and a \(f_T\) of 200 GHz, resulting in a record high \(f_T \times L_g = 16 \text{ GHz \mu m}\)\(^7\). Chowdhury et al. demonstrated a complementary logic circuit (an inverter) on a GaN-on-Si platform with a record maximum voltage gain of 27 V/V at an input voltage of 0.59 V with \(V_{\text{DD}} = 5\) V\(^8\). Xie et al. reported an InAlN/GaN HEMT on Si with a \(f_T\) of 210 GHz and a three-terminal off-state breakdown voltage \((V_{\text{BD}})\) of 46 V, leading to a record high Johnson's figure-of-merit \((\text{JFOM} = f_T \times V_{\text{BD}})\) of 8.8 THz V\(^9\). Then et al. reported the high \(f_T/f_{\text{max}}\) of 190/300 GHz was achieved on the e-mode high-k InAlN/GaN transistor on 300 mm Si substrate\(^10\).

However, to the best of our knowledge, the highest \(f_T/f_{\text{max}}\) of 454/444 GHz and 348/340 GHz were achieved on 20-nm-gate-length AlN/GaN HEMTs and 27-nm-gate-length InAlN/GaN HEMTs on SiC\(^12\), respectively. Although excellent performances have been demonstrated, InAlN/GaN HEMTs on Si still presents much room to be improved compared with GaN HEMTs on SiC substrate. The InAlN barrier can be grown lattice-matched to GaN when the In component is 17%, which makes it easier grow than AlN on GaN\(^13\). The InAlN/GaN heterostructure also exhibits higher quantum well polarization-induced charge than AlGaN/GaN heterostructure, resulting in higher channel electron density and drain current\(^14,15\). In addition, compared with AlGaN/GaN, a thinner InAlN barrier in InAlN/GaN HEMTs not only can offer higher frequency performance with an improved device transconductance, but also can suppress the short-channel effect with the reduced gate-to-channel distance\(^16,17\). Hence, exploring the possible limiting factors of InAlN/GaN HEMTs on Si is significant to further improve the device performance. In this paper, high-performance InAlN/GaN HEMTs on Si are demonstrated. The extrinsic and intrinsic parameters of devices with different gate lengths are extracted and the scale behavior of InAlN/GaN HEMTs on Si is predicted. It presents that a \(f_T/f_{\text{max}}\) of 230/327 GHz can be achieved when \(L_g\) scales down to 20 nm with the technology developed in the study, and an improved \(f_T/f_{\text{max}}\) of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMTs with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

**Experiment**

Figure 1a shows the lattice-matched In\(_{0.17}\)Al\(_{0.83}\)N/GaN heterostructure, which is grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial layer structure consists of a 2-nm GaN cap layer, an 8-nm In\(_{0.17}\)Al\(_{0.83}\)N barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm In\(_{0.12}\)Ga\(_{0.88}\)N back-barrier layer, and a 2-μm undoped GaN buffer layer\(^18\). The electron sheet concentration and electron mobility measured by Hall measurements were 2.28 \times 10^{13} \text{ cm}^{-2} and 1205 \text{ cm}^{2}/\text{V s}, respectively.

Figure 1b shows the detailed device fabrication steps. The device fabrication started with mesa isolation using Cl\(_2\)/CH\(_4\)/He/Ar inductively coupled plasma etching. Then Ti/Al/Ni/Au stack was deposited and annealed at 850 °C for 40 s in N\(_2\) to form the alloyed ohmic contacts. The ohmic contact resistance is 0.3 Ω mm. An oxygen plasma treatment was then applied to form the oxide layer on top of the InAlN layer, which can effectively reduce the gate leakage current and improve RF performance\(^19,20\). Finally, a Ni/Au T-shaped gate with a gate width \((W_g)\) of 2 \times 20 μm was fabricated by electron beam lithography. Figure 1c shows a plan-view scanning electron microscopy image of the InAlN/GaN HEMT with a gate head length \((L_{\text{head}})\) of 400 nm and a source-drain spacing \((L_{\text{sd}})\) of 600 nm; (d) A SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

![Figure 1](https://www.nature.com/scientificreports/)
Results and discussion

**DC performance.** The DC current–voltage (I–V) measurements are carried out by using an Agilent B1500A semiconductor parameter analyzer. Figure 2a shows the output characteristic of the InAlN/GaN HEMT with a 50-nm gate length. The device on-resistance ($R_{on}$) extracted at gate-source ($V_{gs}$) of 0 V and drain-source voltage ($V_{ds}$) between 0 and 0.5 V is 1.33 Ω·mm. The gate-to-channel distance ($t_{bar}$) including a 2-nm GaN, an 8-nm InAlN, and a 1-nm AlN is 11 nm. Since $L_g$ is 50 nm, the device presents an aspect ratio ($L_g/t_{bar}$) of 4.5. Due to the low $L_g/t_{bar}$, the short-channel effects (SCEs) start to appear when $V_{ds}$ is larger than 5 V and $V_{gs}$ is between −4 to −1 V. At $V_{gs} = 1$ V, drain current ($I_d$) in saturation region presents a decrease with increased $V_{ds}$, an indication of the thermal effect.

Figure 2b shows the transfer characteristic with the extracted extrinsic transconductance ($g_m$) of the InAlN/GaN HEMT with a 50-nm gate length at $V_{ds} = 10$ V. The maximum saturation drain current ($I_{d, max}$) is 2.01 A/mm at $V_{gs} = 1$ V and $V_{ds} = 10$ V. The $g_m$ perk ($g_{m, peak}$) is 493 mS/mm. To the best of our knowledge, the record high $I_{d, max}$ of 2.8 A/mm and $g_{m, peak}$ of 660 mS/mm were achieved on a 55-nm-gate-length InAlN/GaN HEMT on Si with regrowth technology and $L_{sd}$ of 175 nm.5 The lower $I_d$ and $g_{m, peak}$ in this study result from the regrowth-free technology and the larger source-drain spacing ($L_{sd} = 600$ nm).

Figure 3a shows the transfer and gate current ($I_g$) characteristics in semi-log scale of the InAlN/GaN HEMT with a 50-nm gate length at $V_{ds} = 5$ V and 10 V, respectively. At $V_{ds} = 10$ V, the device off-current ($I_{off}$) is $2.76 \times 10^{-7}$ A/mm and the $I_{off}/I_{on}$ ratio is $7.28 \times 10^6$, which are higher than the record reported values ($I_{off}$ of $7.12 \times 10^{-7}$ A/mm and $I_{off}/I_{on}$ ratio of $1.58 \times 10^6$) achieved from the InAlN/GaN HEMTs on Si.6 An average subthreshold swing (SS) of 72 mV/dec over more than two orders of $I_d$ is extracted from the transfer curve. The drain-induced barrier lowering (DIBL) of 88 mV/V is extracted at $I_d = 10$ mA/mm between $V_{ds} = 10$ V and $V_{ds} = 5$ V, which is the lowest value among the reported GaN HEMTs on Si. The lowest DIBL value suggests a suppressed SCEs for the sub-100 nm gate-length device. Figure 3b shows the off-state three-terminal breakdown characteristic of the 50-nm InAlN/GaN HEMT measured at $V_{gs} = -8$ V. The device features a $BV_{dss}$ of 36 V at a drain leakage current of 1 mA/mm.

**RF performance.** The device RF performance is measured with a frequency range from 1 to 65 GHz. The network analyzer is calibrated using a two-port short/open/load/through method. On-wafer open and short structures is used to eliminate the effects of parasitic elements. Figure 4a shows the current gain ($h_{21}$), unilateral gain (U), and the maximum stable gain (MSG) as a function of frequency at $V_{ds} = 10$ V and $V_{gs} = -3$ V after de-embedding. $f_{r}/f_{max}$ of 140/215 GHz for the InAlN/GaN HEMT with a 50-nm gate length is obtained by
Figure 3. (a) The transfer and gate current characteristics in semi-log scale at $V_{ds} = 10$ V and 5 V, (b) the $I_d$ and $I_g$ as a function of $V_{ds}$ at $V_{gs} = -8$ V of the InAlN/GaN HEMT with a 50-nm gate length. A $BV_{ds}$ of 36 V was determined.

Figure 4. (a) RF performance of the InAlN/GaN HEMT with a 50-nm gate length at $V_{gs} = -3$ V and $V_{ds} = 10$ V with $f_T/f_{max} = 140/215$ GHz. (b) The $f_T$ and $f_{max}$ as a function of $V_{gs}$. 
extrapolation of \(|h_{21}|^2\) with a \(-20\) dB/dec slope. An \((f_T \times f_{\text{max}})^{1/2}\) of 173 GHz is obtained, which is the highest record value among the reported InAlN/GaN HEMTs on Si with regrowth-free ohmic contact technology. To the best of our knowledge, a high \((f_T \times f_{\text{max}})^{1/2}\) of 226 GHz \((f_T / f_{\text{max}} = 250/204\) GHz) was achieved on a 55-nm InAlN/GaN HEMT on Si\(^5\), and a high \((f_T \times f_{\text{max}})^{1/2}\) of 239 GHz \((f_T / f_{\text{max}} = 190/300\) GHz) was demonstrated on the e-mode high-k InAlN/GaN MISHEMTs with \(L_g\) of 50 nm\(^9\). The ohmic contact regrowth technology was used in both reported devices. Here for our device, the alloyed ohmic resistance \((R_C: 0.3 \Omega \cdot \text{mm})\) is higher than the reported regrowth ohmic contact resistance \((R_C: 0.05 \Omega \cdot \text{mm})\)\(^5\). This presents a high potential for the RF performance improvement by further decreasing the ohmic contact resistance. Due to \(f_T / f_{\text{max}}\) of 140/215 GHz, products of \(f_T \times L_g\) and \(f_{\text{max}} \times L_g\) of 7.0 and 10.75 GHz\(\cdot\)\(\mu\)m are achieved, respectively. Although neither passivation nor field plate technology is used, the 140-GHz InAlN/GaN HEMT with an \(BV_{ds}\) of 36 V presents a Johnson's figure-of-merit (JFOM = \(f_T \times BV_{ds}\)) of 5.04 THz\(\cdot\)V. Figure 4b shows the measured \(f_T\) and \(f_{\text{max}}\) of the 50-nm InAlN/GaN HEMT as a function of \(V_{gs}\). Both \(f_T\) and \(f_{\text{max}}\) show a gradual decrease compared with their peak values, presenting a good device linearity.

**Equivalent circuit model.** The classical 16-element equivalent-circuit model is used for the InAlN/GaN HEMT, as shown in Fig. 5a\(^5\). Based on this model, the device extrinsic and intrinsic parameters are extracted in Table 1\(^2\)\(^3\)\(^4\)\(^5\). The slight discrepancy between the simulated and measured S-parameter values is observed in Fig. 5b, verifying the accuracy of the extracted extrinsic and intrinsic parameters. The \(f_T\) and \(f_{\text{max}}\) can be calculated using\(^1\)\(^2\)\(^6\):

\[
\begin{align*}
    f_T &= \frac{G_m/G_0}{2\pi ((C_{gs} + C_{gd})(1/G_0 + (R_s + R_d)) + (C_{gd} \cdot G_m/g_0)(R_s + R_d))^2}, \\
    f_{\text{max}} &= \frac{f_T}{2 \sqrt{(R_s + R_d + R_l) \cdot G_0 + 2\pi f_T R_s C_{gd}}},
\end{align*}
\]

where \(G_m\) and \(G_0\) are the intrinsic transconductance and drain-source conductance, respectively; \(C_{gs}\) and \(C_{gd}\) are the gate-source and gate-drain parasitic capacitance, respectively; \(R_s\), \(R_d\), \(R_l\), and \(R_t\) are the parasitic source access resistance, drain access resistance, gate electrode resistance, and input resistance, respectively.
The calculated $f_T/f_{\text{max}} = 145/218$ GHz is very close to the value ($f_T/f_{\text{max}} = 140/215$ GHz) extracted by the extrapolation of $|h_{21}|^2$ with a $-20$ dB/dec slope, which confirms the excellent RF performance. The high intrinsic transconductance/drain-source conductance ($G_m/G_0$) ratio of 10.6 contributes to the high $f_{\text{max}}$.

### Scaling behavior

The InAlN/GaN HEMTs with $L_g$ between 50 and 350 nm are fabricated. Figure 6a shows the measured $f_T$ and $f_{\text{max}}$ as a function of $L_g$ at $V_{gs} = -3$ V and $V_{ds} = 10$ V. The devices with $L_g$ of 50, 70, 100, 150, 250, and 350 nm present $f_T/f_{\text{max}}$ of 140/215, 135/205, 120/170, 90/160, 60/136, and 36/128 GHz, respectively. $f_T \times L_g$ and $f_{\text{max}} \times L_g$ are obtained in Fig. 6b. A $f_T \times L_g$ peak of 15 GHz $\mu$m is achieved on the 250-nm-gate-length InAlN/GaN HEMT with a $f_T$ of 135 GHz. $f_{\text{max}} \times L_g$ presents a decrease from 44.8 GHz $\mu$m ($L_g = 350$ nm) to 10.75 GHz $\mu$m ($L_g = 50$ nm). The decrease of both $f_T \times L_g$ and $f_{\text{max}} \times L_g$ as $L_g$ scales down means that the effect of parasitic parameters is more pronounced, thus hindering the improvement of $f_T$ and $f_{\text{max}}$. Due to the large head length of T-shaped gate ($L_{\text{head}} = 400$ nm), the transistors features higher $f_{\text{max}}$ and $f_{\text{max}} \times L_g$.

To shed more light on the scaling behavior, the extrinsic and intrinsic parameters of these devices are further extracted using the equivalent circuit model discussed above. $C_{\text{gs}}$ can be separated to two parts: gate-source intrinsic capacitance ($C_{\text{gs, int}}$) and gate-source extrinsic capacitance ($C_{\text{gs, ext}}$). It means $C_{\text{gs}} = C_{\text{gs, int}} + C_{\text{gs, ext}}$. $C_{\text{gd}}$ can also be written as $C_{\text{gd}} = C_{\text{gd, int}} + C_{\text{gd, ext}}$. Figure 7 shows the extracted $C_{\text{gs}}$ and $C_{\text{gd}}$ as a function of $L_g$. Both $C_{\text{gs}}$ and

| Extrinsic parameters | Intrinsic parameters |
|----------------------|----------------------|
| $C_{\text{pgd}} = 1.16$ fF | $C_{\text{gs}} = 444$ fF/mm |
| $C_{\text{pgs}} = 26.35$ fF | $C_{\text{gd}} = 104$ fF/mm |
| $C_{\text{pds}} = 26.21$ fF | $C_{\text{ds}} = 318$ fF/mm |
| $L_s = 3.17$ pH | $R_i = 0.90$ $\Omega$ mm |
| $L_d = 44.03$ pH | $G_{\text{m}} = 573$ mS/mm |
| $R_s = 0.43$ $\Omega$ mm | $R_s = 0.26$ $\Omega$ mm |
| $R_d = 0.45$ $\Omega$ mm | $\tau = 1.09$ ps |

Table 1. The extracted extrinsic and intrinsic parameters for the 50-nm InAlN/GaN HEMTs.
Cgs present a linear dependence upon \( L_g \). By linear fitting, the Cgs,ext and Cgd,ext are obtained from Cgs and Cgd at \( L_g = 0 \) nm\(^2\), as shown in Fig. 7. Here Cgs,ext of 93.05 fF/mm and Cgd,ext of 97.65 fF/mm are determined, respectively. The total delay (\( \tau \)) of transistors can be written as\(^{27,28} \)

\[
\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{\text{ext}} + \tau_{\text{par}}
\]

Here \( \tau \) is partitioned into three components: transit time (\( \tau_t \)), parasitic charging delay (\( \tau_{\text{ext}} \)), and parasitic resistance delay (\( \tau_{\text{par}} \)).

\( \tau_t \) is the transit time under the gate region. It is related to the gate length as well as the electron velocity (\( v_e \)) under the gate region, and can be calculated by\(^{27,28} \)

\[
\tau_t = \frac{C_{gs} + C_{gd}}{G_m} = \frac{L_g}{v_e}
\]

\( \tau_{\text{ext}} \) is parasitic charging delay through \( C_{gs,\text{ext}} \) as well as \( C_{gd,\text{ext}} \), and can be written as\(^{27,28} \)

\[
\tau_{\text{ext}} = \frac{C_{gs,\text{ext}} + C_{gd,\text{ext}}}{G_m}
\]

\( \tau_{\text{par}} \) is parasitic resistance delay mainly associated with \( R_s \) as well as \( R_d \), and can be written as\(^{27,28} \)

\[
\tau_{\text{par}} = \frac{C_{gd}(R_s + R_d)}{G_0}\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{G_0}{G_m}\right].
\]

Figure 8 plots \( \tau_t \) and \( v_e \) as a function of \( L_g \) calculated from (3). As \( L_g \) decreases, \( \tau \) shows a monotonous drop, which corresponds to the increased \( f_T \). With decreased \( L_g \) \( v_e \) increases to a maximum value of \( 1.08 \times 10^7 \) cm/s (at \( L_g = 150 \) nm) and then drop to \( 0.80 \times 10^7 \) cm/s (at \( L_g = 50 \) nm). Figure 9 shows the extracted \( G_m \) and \( G_0 \) from the equivalent-circuit model as a function of \( L_g \). \( G_0 \) shows an increase with decreased \( L_g \). The dependence of \( G_m \) and \( v_e \) on \( L_g \) present the same trend. Based on (3), because \( C_{gs} \) and \( C_{gd} \) linearly depends on \( L_g \), we conclude that the change of \( G_m \) is attributed to \( v_e \) difference. The same trend of \( G_m \) and \( v_e \) on \( L_g \) is also observed in InAs HEMTs and result from the short channel effect\(^{29-31} \).

Figure 10 exhibits the calculated \( \tau_t \), \( \tau_{\text{ext}} \), and \( \tau_{\text{par}} \) using (3)–(5). \( \tau_{\text{ext}} \) and \( \tau_{\text{par}} \) is almost unchanged. Conversely, \( \tau_t \) decreases with decreased \( L_g \) and dominates the total delay in all devices. This makes it possible to decrease delay and improve \( f_T \) through downsizing of device gate length. However, for the device with \( L_g \) below 100 nm,
the effect of $\tau_{\text{ext}}$ and $\tau_{\text{par}}$ become non-negligible. The ratios of $(\tau_{\text{ext}} + \tau_{\text{par}})/\tau_t$ are 39% and 40% for the InAlN/GaN HEMTs with $L_g$ of 70 and 50 nm, respectively. This means the parasitic capacitance and resistance significantly hampers further $L_g$ scaling benefits in RF performance of sub-100 nm InAlN/GaN HEMTs.

Therefore, downscaling and decreasing parasitic resistances as well as capacitances are very important for further improving device performance of InAlN/GaN HEMTs on Si. Figure 11 plots the calculated $f_T$ and $f_{\text{max}}$.
based on the model and the extracted parameters (Blue-line in Fig. 11), which shows a good agreement with the measured results. In terms of the electron velocity saturation, the electron velocity of the InAlN/GaN HEMTs with \( L_g < 50 \text{ nm} \) is assumed to be the same as that with \( L_g = 50 \text{ nm} \). With the obtained \( v_e \), \( \tau_t \) can be obtained using (3), \( \tau_{ext} \) is parasitic charging delay through \( C_{gs,ext} \) and \( C_{gd,ext} \), and both are the constant as shown in Fig. 7. \( \tau_{par} \) is mainly associated with \( R_s \) and \( R_d \), which are independent on \( L_g \). As shown in Fig. 10, \( \tau_{ext} \) and \( \tau_{par} \) present slight change with \( L_g \). So here \( \tau_{par} \) of the device with \( L_g = 50 \text{ nm} \) is used during the model calculation. Then \( f_T \) can be calculated with the obtained \( \tau_t \), \( \tau_{ext} \) and \( \tau_{par} \) by using (2). When \( L_g \) decreases from the 50–20 nm, the T-shaped gate head length of 400 nm is unchanged, so the effect of the small gate length variation on \( R_g \) and \( R_i \) is minimal. Hence \( R_g \) and \( R_i \) of device with \( L_g = 50 \text{ nm} \) are used. \( C_{gd} \) is extracted from the linear fitting in Fig. 7b and then \( f_{max} \) is obtained using (1). The model results present that \( f_T/f_{max} \) of 230/327 GHz can be achieved when \( L_g \) scales down to 20 nm with the technology developed in the study. To decrease the parasitic resistance, the regrowth ohmic contact can be used. Here \( R_i \) (0.30 \( \Omega \) mm), \( R_j \) (0.32 \( \Omega \) mm), and \( G_m \) (573 mS/mm) are changed to 0.10 \( \Omega \) mm, 0.08 \( \Omega \) mm, and 620 mS/mm\(^2\). Then new model results with regrowth technology are plotted (Green-line in Fig. 11) and a \( f_T/f_{max} \) of 265/397 GHz is achieved on the device with a 20-nm gate length. Optimizing the detailed structure of T-shaped gate can decrease \( C_{gs} \) and \( C_{gd} \). Hence when 30% decreasing of \( C_{gs} \) and \( C_{gd} \) is added into the model, new results (Red-line in Fig. 11) are plotted and an improved \( f_T/f_{max} \) of 320/395 GHz on 20-nm-gate-length InAlN/GaN HEMT is demonstrated. These values are comparable to the 27-nm InAlN/GaN HEMTs on SiC with \( f_T/f_{max} \) of 348/340 GHz, suggesting the possibility of further improvement of InAlN/GaN HEMTs on Si.

**Conclusions**

In summary, high-performance 50-nm InAlN/GaN HEMT on Si with an \( I_{on}/I_{off} \) ratio of 7.28 \( \times \) 10\(^6\), a SS of 72 mV/dec, a DIBL of 88 mV/V, a \( BV_{ds} \) of 36, a \( f_T/f_{max} \) of 140/215 GHz, and a JFOM of 5.04 THz V are demonstrated. The extrinsic and intrinsic parameters of transistors with different \( L_g \) are extracted and the scaling behavior of InAlN/GaN HEMTs on Si is demonstrated. Based on extracted model, a \( f_T/f_{max} \) of 320/353 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

**Data availability**

The datasets supporting the conclusions of this article are included in the article.
References

1. Chen, K. J. et al. GaN-on-Si power technology: Devices and applications. *IEEE Trans. Electron Devices* **64**, 779–795 (2017).

2. Ishida, M., Ueda, T., Tanaka, T. & Ueda, D. GaN on Si technologies for power switching devices. *IEEE Trans. Electron Devices* **60**, 3053–3059 (2013).

3. Lee, H.-S., Ryu, K., Sun, M. & Palacios, T. Wafer-level heterogeneous integration of GaN HEMTs and Si (100) MOSFETs. *IEEE Electron Device Lett.* **33**, 200–202 (2012).

4. Minko, A. et al. AlGaN-GaN HEMTs on Si with power density performance of 1.9 W/mm at 10 GHz. *IEEE Electron Device Lett.* **35**, 453–455 (2004).

5. Li, L. et al. GaN HEMTs on Si with regrown contacts and cutoff/maximum oscillation frequencies of 250/204 GHz. *IEEE Electron Device Lett.* **41**, 689–692 (2020).

6. Xie, H. et al. Deeply-scaled GaN-on-Si high electron mobility transistors with record cut-off frequency $f_c$ of 310 GHz. *Appl. Phys. Express* **12**, 126506 (2019).

7. Cui, P. et al. High-performance InAlN/GaN HEMTs on silicon substrate with high $f_T$. *Appl. Phys. Express* **12**, 104001 (2019).

8. Chowdhury, N. et al. Regrowth-free GaN-based complementary logic on a Si substrate. *IEEE Electron Device Lett.* **41**, 820–823 (2020).

9. Xie, H. et al. CMOS-compatible GaN-on-Si HEMTs with cut-off frequency of 210 GHz and high Johnson’s figure-of-merit of 8.8 $\text{THzV}$. *Appl. Phys. Express* **13**, 026503 (2020).

10. Then, H. W. et al. Gallium nitride and silicon transistors on 300 mm silicon wafers enabled by 3-D monolithic heterogeneous integration. *IEEE Trans. Electron Devices* **67**, 5306–5314 (2020).

11. Tang, Y. et al. Ultrahigh-speed GaN high-electron-mobility transistors with $f_c/f_{max}$ of 454/444 GHz. *IEEE Electron Device Lett.* **36**, 549–551 (2015).

12. Schuette, M. L. et al. Gate-recessed integrated E/D GaN HEMT technology with $f_c/f_{max}$=300GHz. *IEEE Electron Device Lett.* **34**, 741–743 (2013).

13. Dadgar, A. et al. High-sheet-charge–carrier-density AlN/InN/GaN field-effect transistors on Si (111). *Appl. Phys. Lett.* **85**, 5400–5402 (2004).

14. Kuzmik, J. Power electronics on InAlN/(In) GaN: Prospect for a record performance. *IEEE Electron Device Lett.* **22**, 510–512 (2001).

15. Gomschorrek, M., Carlin, J.-F., Felten, E., Py, M. & Grandjean, N. High electron mobility lattice-matched AlN/InN/GaN field-effect transistor heterostructures. *Appl. Phys. Lett.* **89**, 062106 (2006).

16. Yue, Y. et al. INAIN/InGaN HEMTs with regrown ohmic contacts and $f_c$ of 370 GHz. *IEEE Electron Device Lett.* **33**, 988–990 (2012).

17. Jessen, G. H. et al. Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices. *IEEE Trans. Electron Devices* **54**, 2589–2597 (2007).

18. Cui, P. et al. Effects of N2O surface treatment on the electrical properties of the InAlN/GaN high electron mobility transistors. *J. Phys. D Appl. Phys.* **53**, 065103 (2020).

19. Chung, J. W., Roberts, J. C., Piner, R. E. & Palacios, T. Effect of gate leakage in the subthreshold characteristics of AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* **29**, 1196–1198 (2008).

20. Chung, J. W., Kim, T.-W. & Palacios, T. Advanced gate technologies for state-of-the-art $f_c$ in AlGaN/GaN HEMTs. In *2010 International Electron Devices Meeting*, 30.2.1–30.2.4 (2010).

21. Lee, D. S. et al. 245-GHz InAlN/GaN HEMTs with oxygen plasma treatment. *IEEE Electron Device Lett.* **32**, 755–757 (2010).

22. Wang, R. H. et al. 210-GHz InAlN/GaN HEMTs with dielectric-free passivation. *IEEE Electron Device Lett.* **32**, 892–894 (2011).

23. Bouzid-Driad, S. et al. AlGaN/GaN HEMT on silicon substrate with 206-GHz $f_{max}$. *IEEE Electron Device Lett.* **34**, 36–38 (2013).

24. Crupi, G. et al. Accurate multibias equivalent-circuit extraction for GaN HEMTs. *IEEE Trans. Microw. Theory Tech.* **54**, 3616–3622 (2006).

25. Campbell, C. F. & Brown, S. A. An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions. *IEEE Trans. Microw. Theory Tech.* **49**, 1241–1247 (2001).

26. Chung, J. W., Hoke, W. E., Chumbes, E. M. & Palacios, T. AlGaN/GaN HEMT With 300-GHz $f_{max}$. *IEEE Electron Device Lett.* **31**, 195–197 (2010).

27. Kim, D.-H., Bae, B. & Del Alamo, J. A. $f_T$ = 688 GHz and $f_{max}$ = 800 GHz in L= 40 nm In 0.7 Ga 0.3 As MHEMTs with g_m,max>2.7 mS/mm. In *2011 International Electron Devices Meeting*, 13.6.1–13.6.4 (2011).

28. Lee, D. S. et al. 300-GHz InAlN/GaN HEMTs with InGaN back barrier. *IEEE Electron Device Lett.* **32**, 1525–1527 (2011).

29. Endoh, A., Watanabe, I., Kasamatsu, A. & Mimura, T. Monte Carlo simulation of InAs HEMTs considering strain and quantum confinement effects. *J. Phys. Conf. Ser.* **354**, 012036 (2013).

30. Kim, D.-H. & Del Alamo, J. A. Logic performance of 40 nm InAs HEMTs. In *2007 IEEE International Electron Devices Meeting*, 629–632 (2007).

31. Kim, T.-W., Kim, D.-H. & del Alamo, J. A. 30 nm In0.7Ga0.3 As Inverted-Type HEMTs with reduced gate leakage current for logic applications. In *2009 IEEE International Electron Devices Meeting (IEDM)*, 1–4 (2007).

Author contributions

P.C. and Y.Z. contributed to the research design, experiment measurements, data analysis, and manuscript preparation. All authors reviewed this manuscript.

Funding

This work was supported in part by the NASA International Space Station under Grant 80NSSC20M0142, and in part by Air Force Office of Scientific Research under Grant FA9550-19-1-0297, Grant FA9550-21-1-0076 and Grant FA9550-22-0126.

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to P.C. or Y.Z.

Reprints and permissions information is available at www.nature.com/reprints.
Publisher's note  Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access  This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2022