Analysis of boundary point (break point) in Linear Delay Model for nanoscale VLSI standard cell library characterization at PVT corners

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Abstract—In VLSI chip design flow, Static Timing Analysis (STA) is used for fast and accurate analysis of data-path delay. This process is fast because delay is picked from Look Up Tables (LUT) rather than conventional SPICE simulations. But accuracy of this method depends upon the underlying delay model with which LUT was characterized. Non Linear Delay Model (NLDM) based LUTs are quite common in industries. These LUT requires huge amount to time during characterization because of huge number of SPICE simulations done at arbitrary points. To improve this people proposed various other delay models like alpha-power and piecewise linear delay models. Bulusu et. al. proposed Linear Delay Model (LDM) which reduces LUT generation time to 50 percent. LDM divides delay curve w.r.t input rise time\(^{(t_{rin})}\) into two different region one is linear and other is non-linear. This boundary point between linear and non-linear region was called break point \((t_{rb})\). Linear region will be done if we simulate at only two points. This advantage will be possible by having knowledge of this break point at various PVT corners. In this paper, We will analyze this break point and will give a formula to find out this at various PVT corners. Knowledge about \((t_{rb})\) will restrict LUT simulations only in non-linear region and will help us in saving huge amount of time during LUT characterization.

Keywords
Static Timing Analysis, Look Up Table characterization, data path delay estimation, linear delay model

I. INTRODUCTION

In Static Timing Analysis, hold and setup time violations have to be validated. For a combinational circuit, setup time of the flip-flop puts the constraint on upper limit of the delay while hold time puts a constraint on lower limit. This makes accurate estimation of data-path delay necessary.

There are various ways to estimate this data-path delay but LUT based delay estimation is fastest one. An LUT holds delay values of a circuit at various corners of input rise time\((T_{R})\) and output load \((C_{L})\). For different type of standard gate like NAND, NOR, NOT a different LUTs are characterized and this process is replicated at various Process, Supply Voltage and Temperature (PVT) corners.

These \(T_{R}\) and \(C_{L}\) points are chosen arbitrarily or at uniform intervals. Each point requires an SPICE simulation. If multiplied for all values of \(T_{R}\) and \(C_{L}\), it takes a huge amount of time. Bulusu et. al. used the fact that delay varies linearly up to some extent with \(T_{R}\) and \(C_{L}\) and could reduce the number of required simulations greatly. They exploited this linear variation by choosing simulation points of \(T_{R}\) and \(C_{L}\) only in non-linear region. Thereby getting away with only two simulations point in linear region.

In this paper, We will summarize the linear delay model in Section II. In Section III, We will calculate \(t_{rb}\) for various \(C_{L}\), Supply Voltage \((V_{DD})\), Temperature and in Section IV will verify these calculations using HSPICE simulation. Finally in section V, We will give a model for \(t_{rb}\) that will enable us to extract out linear region at various Voltage and Temperature corners. This in turn will reduce number of required simulations at any PVT corner.

II. SUMMARY OF LINEAR DELAY MODEL

For the NOT gate shown in the figure, delay (between 50% input to 50% output) can be written as

\[
\text{Delay} = \frac{T_{R}}{2} + \Delta t_{1} + \Delta t_{2} \tag{1}
\]

Here we assume that when input reaches \(V_{DD}\), \(V_{out}\) drops a little and keeps NMOS in saturation. NMOS is also in saturation for time \(T_{R}\) to \(T_{R} + \Delta t_{1}\). NMOS falls into linear region from \(T_{R} + \Delta t_{1}\) to \(T_{R} + \Delta t_{1} + \Delta t_{2}\). \(V_{out}(T_{R})\) can be calculated by charge discharged during time 0 to \(T_{R}\).

\[
\Delta Q(T_{R}) = \int_{0}^{T_{R}} I_{d} \, dt \tag{2}
\]
\[ I = 0.5\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \]  
where

\[ V_{GS} = \frac{V_{DD}}{T_R} t \]

\[ \Delta Q(T_R) = \frac{1}{6} \mu_n C_{ox} \frac{W}{L} T_R \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] \]

\[ \Delta Q(T_R) = S_T T_R \]

where

\[ S_T = \frac{1}{6} \mu_n C_{ox} \frac{W}{L} \frac{T_R}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] \]

\[ V_{out}(T_R) = V_{DD} - \frac{1}{6} \mu_n C_{ox} \frac{W}{L} \frac{T_R}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] \]

\[ \Delta t_1 \text{ can be calculated by same method, but in this current will remain constant as } V_{GS} \text{ is constant and is equal to } V_{DD}. \]

\[ [V_{out}(T_R) - (V_{DD} - V_{th})](C_L + C_P) = \int_{T_R}^{T_R+\Delta t_1} I_{const. dt} \]

where

\[ I = 0.5\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{th})^2 \]

Since I is constant, integration simplifies as

\[ [V_{out}(T_R) - (V_{DD} - V_{th})](C_L + C_P) = 0.5\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})^2 \Delta t_1 \]

\[ \Delta t_1 = \frac{(V_{th})(C_L + C_P) - S_T T_R}{0.5\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})^2} \]

Similarly we can calculate \( \Delta t_2 \), when NMOS is in linear region

\[ \Delta t_2 = \frac{\alpha(C_L + C_P)}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \]

Using Equation 11, 13, 14 we can write Delay as

\[ Delay = K_1 T_R + K_2 C_L + K_3 \]

where

\[ K_1 = [0.5 - \frac{1}{6} \mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] ] \]

\[ K_2 = \frac{V_{th}}{0.5\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})^2} + \frac{\alpha}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \]

\[ K_3 = \frac{V_{th} C_P}{0.5\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})^2} + \frac{\alpha C_P}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \]

Our initial assumption was of NMOS being in saturation till time \( T_R \). For this assumption to be valid, \( V_{out}(T_R) \) should be greater than \( V_{DD} - V_{th} \) i.e.

\[ V_{out}(T_R) \geq V_{DD} - V_{th} \]

\[ V_{DD} - \frac{S_T T_R}{C_L + C_P} \geq V_{DD} - V_{th} \]

\[ T_R \leq \frac{(C_L + C_P)V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] } \]

\[ t_{rb} = \frac{(C_L + C_P)V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] } \]

### III. \( t_{rb} \) Calculations for Various Voltages and Technology Corners

#### A. Variation with \( C_L \)

In this section we will mathematically analyze the behavior of \( t_{rb} \) with \( C_L \).

\[ t_{rb} = \frac{(C_L + C_P)V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] } \]

\( t_{rb} \) is directly proportional to \( C_L \), so we can write \( t_{rb} \) as

\[ t_{rb} = M_1 C_L + M_2 \]

where

\[ M_1 = \frac{V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] } \]

and

\[ M_2 = \frac{C_P V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} \left[ (V_{DD} - V_{th})^3 + (V_{th})^3 \right] } \]

Now to model the exact behavior of \( t_{rb} \), we need to know the behavior of constants \( M_1 \) and \( M_2 \) with supply voltage \( V_{DD} \) and with chip temperature.

#### B. Variation with Supply Voltage

On Simplifying Equation 25 and 26 we get

\[ M_1 = \frac{V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} V_{DD}^3 (1 - 3 \frac{V_{th}}{V_{DD}})^3 + (\frac{V_{th}}{V_{DD}})^3} \]

That can be further approximated. Since \( (\frac{V_{th}}{V_{DD}})^3 \ll 1 \), \( M_1 \) can be written as

\[ M_1 \approx \frac{V_{th}}{6\mu_n C_{ox} \frac{W}{L} \frac{1}{V_{DD}} V_{DD}^3 (1 - 3 \frac{V_{th}}{V_{DD}})} \]
On further simplification
\[ M_1 \approx \frac{V_{th}}{\frac{1}{6} \mu_n C_{ox} W L V_{DD}^2} \] (29)
So \( M_1 \) is inversely proportional to \( V_{DD}^2 \).
Similarly \( M_2 \) can be characterized, as
\[ M_2 \approx \frac{C_P V_{th}}{\frac{1}{6} \mu_n C_{ox} W L V_{DD}^2} \] (30)

C. Variation of \( M_1 \) and \( M_2 \) with chip temperature
In the formula of \( M_1 \) in equation (29) parameters which are varying with temperature are mobility (\( \mu_n \)) and threshold voltage (\( V_{th} \)).
For Silicon, mobility of electrons \( \mu_n \) varies with temperature as follows [5].
\[ \mu_n \propto T^{-2.4} \] (31)
Similarly \( V_{th} \) varies as -3mv/°C [6]
\[ V_{th}(T_1) = V_{th}(T_2) - 0.003 \Delta T \] (32)
Where
\[ \Delta T = T_1 - T_2 \] (33)
Combining equation (29) [31, 32], we see intuitively that while mobility increases \( M_1 \) and \( M_2 \) by a factor of \( T^{2.4} \), \( V_{th} \) reduces it to some extent. So we can roughly write it as
\[ M_1 \propto T^2 \] (34)
\[ M_2 \propto T^2 \] (35)

IV. OBSERVATIONS THROUGH HPSICE SIMULATIONS
We simulated CMOS NOT gate of figure 1 using HSPICE at 45nm technology node. We collected values of delay (from 50% input to 50% output) by varying input rise time (\( T_R \)) from 1ps to 500ps at various load capacitances. Figure 2 shows delay of NOT gate with respect to \( T_R \) for various values of \( C_L \).

Figure 2 verifies that delay varies linearly up to certain extent. We captured this extent (\( t_{rb} \)) and plot it with various values of \( C_L \).

Fig. 2: Delay vs \( T_R \) at various \( C_L \) and their linear regions

Fig. 3: \( t_{rb} \) vs \( C_L \) and a Linear Fit on it

Figure 3 verify our claims of equation 24 where we predicted \( t_{rb} \) to vary linearly with \( C_L \). We also plotted variations of \( t_{rb} \) with supply voltage (\( V_{DD} \)).

Fig. 4: \( t_{rb} \) vs \( V_{DD} \) and a power function Fit on it

Since \( M_1 \) [Eq. 29] and \( M_2 \) [Eq. 30] both were inversely proportional to \( V_{DD}^2 \), \( t_{rb} \) is also inversely proportional to \( V_{DD}^2 \). When we plotted simulation results of \( t_{rb} \) vs \( V_{DD} \) shown in figure 4, we observed that it is varying in the predicted way. By fitting power function we observed that it varies as \( V_{DD}^{-2.2} \), which is approximately equal to -2.

In Equation 34 we proved that both \( M_1 \) and \( M_2 \) are proportional to \( T^2 \). Which implies same with \( t_{rb} \). By Plotting \( t_{rb} \) with temperature (\( T \)) shown in figure 5, we observed that \( t_{rb} \) varies almost similar to the mathematical prove with \( T^{1.87} \).
V. Modelling $t_{rb}$

For NOT gate we have seen the behavior of $t_{rb}$ with Widths, Temperature, Supply Voltage and Load Capacitance.

A. Adjusting $\frac{W}{T}$ variations

From equation 25-26 it is clear that slope of $t_{rb}$ curve varies inversely with temperature while its intercept is constant. To model this, we will calculate two reference values of $t_{rb}$ at CL1 and CL2 and then we will model these for different widths.

$$Slope_{ref} = \frac{t_{rb\_ref2} - t_{rb\_ref1}}{C_{L2} - C_{L1}}$$  \hspace{1cm} (36)

$$Slope_{new} = Slope_{ref} \cdot \left(\frac{W}{T}\right)_{new}$$  \hspace{1cm} (37)

$$Intercept_{ref} = \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}}$$  \hspace{1cm} (38)

$$Intercept_{new} = Slope_{ref} \cdot \left(\frac{W}{T}\right)_{new} \cdot \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}}$$  \hspace{1cm} (39)

So $t_{rb}$ at any width can be written as

$$t_{rb} = Slope_{ref} \cdot \left(\frac{W}{T}\right)_{ref} \cdot C_L + \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}} \cdot \left(\frac{W}{T}\right)_{new} + \frac{T_{new}}{T_{ref}} \cdot \frac{V_{DD_{new}}}{V_{DD_{ref}}}$$  \hspace{1cm} (40)

B. Adjusting $T$ variations

From equation 34 it is clear that both slope and intercept varies in accordance with square of temperature. So $t_{rb}$ can be generalize as follow.

$$t_{rb} = Slope_{ref} \cdot \left(\frac{W}{T}\right)_{ref} \cdot C_L + \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}} \cdot \left(\frac{T_{new}}{T_{ref}}\right)$$  \hspace{1cm} (41)

C. Adjusting $V_{DD}$ variations

From equation 29 it is clear that both slope and intercept varies in accordance with inverse square of supply voltage. So $t_{rb}$ can be generalize as follow.

$$t_{rb} = \frac{Slope_{ref} \cdot \left(\frac{W}{T}\right)_{ref} \cdot C_L + \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}} \cdot \left(\frac{T_{new}}{T_{ref}}\right)}{\left(\frac{V_{DD_{new}}}{V_{DD_{ref}}}\right)^2}$$  \hspace{1cm} (42)

D. Adjusting Technology node variations

From equation 29 it is clear that both slope and intercept varies linearly with technology node. So $t_{rb}$ can be generalize as follow.

$$t_{rb} = \frac{Slope_{ref} \cdot \left(\frac{W}{T}\right)_{ref} \cdot C_L + \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}} \cdot \left(\frac{T_{new}}{T_{ref}}\right)}{\left(\frac{V_{DD_{new}}}{V_{DD_{ref}}}\right)^2 + \frac{L_{new}}{L_{ref}}}$$  \hspace{1cm} (43)

VI. LUT CHARACTERIZATION USING BREAK POINT FORMULA

In previous sections we captured how $t_{rb}$ behaves with output load, supply voltage $V_{DD}$ and on chip temperature variations. This formula tells that if we have $t_{rb}$ value at one corner, we can calculate it’s value at other node very easily. This approach will help us in determining linear region of delay curve at any $C_L$, $V_{DD}$ and temperature value. For LUT characterization, we will store the value of $t_{rb}$ for two different corners and will calculate subsequent $t_{rb}$ using $t_{rb}$ model developed in previous sections. To get a feel of this, we can consider characterization of a look up table for NOT gate between $T_R$ range 1ps to 100ps and $C_L$ range 1ff to 10ff.

If we use traditional LUT characterization methods, we will divide this range into equal intervals. We will divide $T_R$ range into 20 points each of 5ps interval and $C_L$ range into 10 point each of 1ff interval, it will require 20x10 i.e. 200 SPICE simulations. With this new approach, we will calculate $t_{rb}$ values from our model at various $C_L$, which turns out as in figure 6.

$$t_{rb} = \frac{Slope_{ref} \cdot \left(\frac{W}{T}\right)_{ref} \cdot C_L + \frac{C_{L1} \cdot t_{rb\_ref2} - C_{L2} \cdot t_{rb\_ref1}}{C_{L1} - C_{L2}} \cdot \left(\frac{T_{new}}{T_{ref}}\right)}{\left(\frac{V_{DD_{new}}}{V_{DD_{ref}}}\right)^2 + \frac{L_{new}}{L_{ref}}}$$  \hspace{1cm} (43)

Fig. 6: $t_{rb}$ at various values of $C_L$

Figure 6 tells that we need only 2 simulations for $C_L$ having values 2ff to 10ff as whole region is linear, where as we will need 2+8 =10 simulations for $C_L$ of value 1ff as 60% of region would
is linear. This in turn requires a total of only 28 (10+2x9=28) simulations. Thus we could save around 86% of simulations.

VII. CONCLUSION

SPICE simulation at any particular corner has many advantage. Apart from giving delay it also gives power. In linear region we can do our LUT characterization without the need of simulations. But we will not have any idea about power consumption. So if power consumed is not our concern, demarcation of delay curve into two different region viz linear and non-linear helps us in fastening the process of LUT characterization. In future we can investigate similar kind of linear behavior in power consumption also which will obviate the need of SPICE simulation in linear region completely.

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