High Voltage Intelligent Power Module Layout Design for Parasitic Inductance Reduction

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Abstract. When designing the high voltage intelligent power module, layout design is as important as circuit design. Appropriate layout design can avoid many problems associated with these types of power modules. This paper relates generally to the layout design of the power stage components within a 600V/30A high voltage SiC intelligent power module for low inductance. Several crucial aspects when designing the power stage layout have been pointed out. It also presents how to optimize the layout design to minimize the parasitic inductance.

1. Introduction

In variable speed motor drive applications, the use of intelligent power modules is widespread due to its advantages in terms of compactness, ruggedness, built-in control and lower overall-cost. However, layout design of intelligent power module is not trivial and requires special considerations and techniques to achieve the best performance. Low parasitic inductance is a primary factor that must consider when laying out an intelligent power module [1-3]. Otherwise, the parasitic inductances associated with the commutating layout traces and the bond wires between the power devices and the copper traces can be too high, which is undesirable and can cause voltage spikes, ringing, switching loss and EMI issues [4]. As wide bandgap semiconductors become available, the operation frequency and power level continue to increase making parasitic inductance effects even more important [5-8].

To improve the efficiency and the reliability of intelligent power modules, the physical layout must introduce minimal parasitic inductance, which may cause adverse effects on the system performance either electrically, magnetically or thermally. To reduce the parasitic inductance, several optimized module structures have been developed [9-11].

The purpose of this paper is to highlight the primary factors of an intelligent power module when using SiC devices and provide a better practice guideline for a high performance solution that reduces parasitic inductance. The structure is organized as follows: Section 2 presents a 600V/30A SiC intelligent power module, and describes the basic principle of association circuit. Section 3 establishes several crucial layout design methods based on theory and performs instance study. Finally, Section 4 concludes the paper.
2. High voltage SiC intelligent power module
In this paper, the 600V/30A three-phase SiC MOS intelligent power module is used as an analysis object. Figure 1 shows an external view of the 600V/30A rated three-bridge SiC MOS intelligent power module, which is constructed in a 71 mm x 32 mm x 6 mm package. This intelligent power module is dedicated to high speed switching drive. Characteristics of the high voltage SiC intelligent power module are given in Table 1.

![High voltage SiC intelligent power module outlines.](image)

Table 1. Characteristics of the SiC intelligent power module.

| Item                  | Ratings | Unit |
|-----------------------|---------|------|
| Voltage               | 600     | V    |
| Current               | 30      | A    |
| PWM input frequency   | 20      | KHz  |
| Isolation voltage     | 2500    | Vrms |
| Max junction temperature | 175   | °C   |

3. Analysis of parasitic inductance and layout design
In this paper, for the 600V/30A high voltage SiC intelligent power module discussed further below, the power stage is the part of primary concern. The power stage in this high voltage SiC intelligent power module is defined to include the high-side SiC MOSFETs and SBDs, and the low-side SiC MOSFETs and SBDs. Since this design is based on a space-constrained single-layer board, in this scenario, the physical layout becomes even more significant. The following sections describe some common layout topologies and present basic layout examples.

3.1. Optimized placement and routing algorithm for power stage
For SiC intelligent power module, carefully placement of the power devices and routing of the trace layout is critical for correct functionality and optimal performance, especially with integrated SiC devices. Appropriate layout design can effectively reduce the parasitic inductance.

An instance layout to achieve an effective low inductance is shown in Figures 2 and 3. In the exemplary instance, two layout patterns have been modeled. The changes made in these two layouts are minor, placement and routing direction is the only parameter varying between these layouts, in order to indicating how a small effort can have a large impact.

A typical placement and routing of the power stage components is shown in Figure 2. Typically, the power devices are arranged in the same direction. Figure 3 shows an optimized placement and routing of the power stage components is shown. In Figure 3, the commutating traces of heat sink plates U and V have been rotated 180° and placed to the left of the commutating traces of heat sink plates W. Therefore, the direction of current, which flows under the heat sink plate W is designed to be opposite to the direction of current flow in heat sink plates U and V.
Such a placement and routing algorithm lowers the parasitic inductance of the layout due to counteracting magnetic fields generated by the commutating traces during operation of the intelligent power module. Consequently, the placement and routing effect on the parasitic inductance has become practically reduced.

Table 2 summarized the parasitic parameters of the physical layout example depicted in Figures 2 and 3. It can be noticed that, by simply optimizing the placement and routing direction of the power SiC MOSFETs and SBDs, the AC parasitic inductance value can be reduced by about 27.8%. This shows the great influence of a proper placement and routing direction on parasitic inductance.

3.2. High di/dt current loop paths
In the SiC intelligent power module, high di/dt exists in the circuit due to the large current switching action with high frequency, which may cause voltage spike according to the following formula:

$$V_{\text{spike}} = L \cdot \frac{di}{dt}$$  \hfill (1)

where \(L\) is the parasitic inductance of the current loop path, \(\frac{di}{dt}\) is the value of current transition rate, and \(V_{\text{spike}}\) is the voltage spike amplitude at the moment of the switching event, respectively.

Figure 4 shows a high \(\frac{di}{dt}\) current loop path example relating to a high side SiC MOSFET and two low side SiC MOSFETs. Initially, the high side SiC MOSFETs \(M_1, M_3\) and the low side SiC MOSFET \(M_5\) are in on-state. As shown in the Figure 4, the dashed line indicates the current flow direction. When \(M_3\) switching to off-state, the current flow direction is changed which is indicated by the solid line. Thus, the high \(\frac{di}{dt}\) current loop path in this topology is formed by the positive power supply.
terminal P, the high side SiC MOSFET M3, low side SBD D6 and the negative power supply terminal N. Because the high frequency and high current properties of the signal on this loop path, it is the source of the voltage noise and EMI \[^{12}\]. Therefore, it is crucial to minimize the overall loop inductance and enclosed area of the high \(\frac{di}{dt}\) current loop path.

Figure 4. High \(\frac{di}{dt}\) current loop path example of the SiC intelligent power module.

Figure 5 shows a power stage layout example of the SiC intelligent power module. The power devices are placed on the same side of the intelligent power module and placed as close as possible to each other. The copper traces connecting to the power devices contain large currents and have been designed short and wide. This makes the parasitic inductances very low and results in minimum area of the high \(\frac{di}{dt}\) current loops.

3.3. High Frequency Switching Note

The switching node is the connection between the source of the high-side SiC MOSFET and the drain of the low-side SiC MOSFET as shown in Figure 6. This node is ultimately connected to the AC motor load and is the most critical net to be routed in the intelligent power module. Because it switches the DC bus voltage at a high frequency, minimizing this inductance can minimizes the voltage spike and ring. In addition, for intelligent power module, interconnect from power devices to copper traces are typically implemented by wire bonding. This leads the modelling of bond wires influence to be of great interest.
The influence of bond wires on the parasitic inductance is shown in Table 3, where number and wire diameter are the only parameter varying between these bond wires. Two bond wire schemes have been modeled. It can be noticed that the DCL with one 565.6 μm bond wire is 4.38 nH, and the DCL with two 400 μm bond wires is 3.82 nH, which is reduced by 12.8%. The ACL with one 565.6 μm bond wire is 3.99 nH, and the ACL with two 400 μm bond wires is 3.56 nH, which is reduced by 10.8%.

| Bond wire number | Wire diameter (μm) | DCL (nH) | ACL (nH) |
|------------------|--------------------|----------|----------|
| one              | 565.6              | 4.38     | 3.99     |
| two              | 400                | 3.82     | 3.56     |

In order to research the impact of heat sink plate on the parasitic inductance, parametric sweep has been carried out by changing the thickness of heat sink plate. Figure 7 illustrates the parasitic inductance varying with the thickness of the heat sink plate. It can be seen that the DCL and ACL are increased from 2.523 pH to 81.921 pH and 2.9744 pH to 77.934 pH respectively as the heat sink plate thickness changed from 0.25 mm to 1.5mm. It is obviously that the thicker the heat sink plate, the larger the DCL and ACL. The DCL increased approximately 32 times and the ACL increased approximately 26 times when the heat sink plate increased 6 times.
4. Conclusions
The placement and routing of the power stage components in a SiC intelligent power module requires special attention in order to optimize the overall performance of the system. In particular, AC parasitic inductance which commonly found to be evident can be reduced up to 27.8% by simply optimizing the placement and routing of the power devices. In addition, strive to minimize the high d/dt current loop areas during layout design of the high voltage SiC intelligent power module is necessary to alleviate parasitic inductance, electromagnetic coupling and interference.

Acknowledgments
This work was supported by the National Natural Science Foundation of China under Grant No. 51741706.

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