1-D Simulation of the Electron Density Distribution in a Novel Nonvolatile Resistive Random Access Memory Device

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The operation of a novel nonvolatile memory device based on a conductive ferroelectric/non-ferroelectric thin film multilayer stack is simulated numerically. The simulation involves the self-consistent steady state solution of Poisson’s equation and the transport equation for electrons assuming a Drift-Diffusion transport mechanism. Special emphasis is put on the screening of the spontaneous polarization by conduction electrons as a function of the applied voltage. Depending on the orientation of the polarization in the ferroelectric layer, a high and a low resistive state are found giving rise to a hysteretic $I$-$V$ characteristic. The $R_{\text{high}}$ to $R_{\text{low}}$ ratio ranging from $> 50\%$ to several orders of magnitude is calculated as a function of the dopant content.

Keywords: Ferroelectric, screening, conductivity, simulation, nonvolatile memory, FRAM, resistive RAM (RRAM).

I. Introduction

Nonvolatile memories based on ferroelectric capacitor structures (FRAM) are considered as a potential candidate to replace the current Flash memory generation\cite{1,2,3}. However, the ongoing trend to miniaturization may level the technological efforts in bringing FRAM into production, since charge based devices require a minimum area for a save information readout. Various concepts of resistive memories (RRAM) e.g. based on magnetic tunnel junctions (MRAM)\cite{4}, phase change materials (PCM, Ovonics)\cite{5,6}, ferroelectric tunnel junctions\cite{7}, ferroelectric diodes\cite{8,9,10}, or charge trapping/detrapping effects\cite{11}, which do not show this disadvantage, are currently under development. The key issue of all approaches is to overcome the limitations of today’s Flash memories concerning writing speed, cycling endurance and large programming voltages.

This contribution reports on numerical simulation studies of a memory device consisting of a planar conductive ferroelectric/ non-ferroelectric multilayer stack, which combines the ferroelectric information storage principle with a low resistive information readout. In the following, it will be referred to as Ferro Resistive Random Access Memory, FRRAM. The storage mechanism is based on the establishment of potential well or a potential barrier for electrons, which can be controlled by polarization reversal in the ferroelectric layer. This causes an enrichment or depletion of the majority charge carrier electrons at the ferroelectric/non-ferroelectric interface, whereby the structure is electrically characterized by a high and a low resistive state. In contrast to a ferroelectric diode concept, the proposed device consists of two highly conductive thin film layers sandwiched between two low ohmic contacts.

II. Model

Fig. 1(a) shows the capacitor-like memory device structure consisting of a ferroelectric and a non-ferroelectric layer in contact with metal electrodes. To elucidate the operation principle of the device, we first regard the ferroelectric and the non-ferroelectric layer to be ideal insulators. In a refined model approach, a high concentration of conduction electrons will be assumed to be present in both layers.

FIG. 1: Simplified operation principle of the proposed memory device consisting of (a) an ideal ferroelectric/insulator stack, (b) space charge distribution $\rho$ in the multilayer, (c) the resulting inner electric field $E$ and (d) inner potential $\varphi$ for different orientations of the spontaneous polarization. Depending on the orientation of $P_S$ in the ferroelectric layer, a potential barrier or a potential well for electrons is formed.
A. Ideal Ferroelectric/ Insulator Multilayer

In the absence of mobile charge carrier in the multilayer, the space charge distribution \( \rho(x) \) for short circuit conditions is given by

\[
\rho(x) = \begin{cases} 
\rho_{\text{free}} & x = 0 \\
\rho_S & x = l_1 \\
\rho_{\text{free}} - \rho_S & x = l_1 + l_2 \\
0 & \text{else}
\end{cases},
\]

whereby \( \rho_{\text{free}} \) denotes the influenced charge on the metal electrode and \( \rho_S \) is the spontaneous polarization charge of the ferroelectric as shown in Fig. 1(b). The relationship between space charge and the inner electric field \( E \) or the electric potential \( \varphi \) are given by Maxwell's first equation and the material equation

\[
\frac{dE}{dx} = \frac{\rho}{\varepsilon},
\]

and by Poisson’s equation

\[
\frac{d^2\varphi}{dx^2} = -\frac{\rho}{\varepsilon},
\]

where \( \varepsilon \) is the permittivity of the respective material. From the space charge distribution, the inner electric field and the inner potential are estimated (see Fig. 1(c)-(d)). It is found that the shape of the inner potential is strongly affected by the orientation of the polarization. For \( \vec{P}_S \uparrow \uparrow \vec{e}_x \) we predict the formation of a potential barrier, whereas a potential well is formed for \( \vec{P}_S \uparrow \downarrow \vec{e}_x \). Here, \( \vec{e}_x \) denotes the normal vector in \( x \)-direction. Both states can be addressed by application of an external voltage of respective polarity, so that the voltage drop across the ferroelectric layer exceeds the coercive voltage of the ferroelectric material. The present state of the potential barrier can easily be sensed by measuring the current, which is driven by an external voltage.

B. Conducting Ferroelectric/ Semiconductor Multilayer

If conduction electrons are present in the structure due to shallow donor impurities, Eq. (1) has to be replaced

\[
\rho(x) = \begin{cases} 
\rho_{\text{free}} & x = 0 \\
\rho_S & x = l_1 \\
\rho_{\text{free}} - \rho_S & x = l_1 + l_2 \\
\epsilon_0(n - N_D^+) & \text{else}
\end{cases},
\]

with

\[
\rho(x) = \begin{cases} 
\rho_{\text{free}} & x = 0 \\
\rho_S & x = l_1 \\
\rho_{\text{free}} - \rho_S & x = l_1 + l_2 \\
\epsilon_0(n - N_D^+) & \text{else}
\end{cases},
\]

where \( \epsilon_0 \) is the elementary charge, \( n \) denotes the concentration of conduction electrons and \( N_D^+ \) is the concentration of ionized donor atoms. Following a Drift-Diffusion approach, the redistribution of electrons under the inner electrical field and a concentration gradient is given by

\[
n = -D_n \frac{dn}{dx} - \mu_n n E,
\]

where \( D_n \) is the diffusion coefficient of the electrons, \( \mu_n \) the electron mobility and \( j_n \) the current density. Under steady state conditions, the transport equation simplifies to

\[
\frac{dn}{dt} + \frac{dj_n}{dx} = 0.
\]
Low ohmic contact properties of the electrode interfaces were approximated by neutral contacts. Then, the boundary conditions for electrons are given by

\[ n(x = 0) = n(x = l_1 + l_2) \equiv N_D^+ . \]  

(7)

The potential difference between the system boundaries is determined by the applied external voltage. For the sake of simplicity, a homojunction between the ferroelectric and the semiconducting layer and identical electrodes on both sides are assumed

\[ \varphi(x = l_1 + l_2) - \varphi(x = 0) = V_{\text{extern}}. \]  

(8)

Under conservation of charge in the system, the redistribution of electrons can be calculated as a function of the external voltage and the orientation of the spontaneous polarization.

### III. Results

Numerical simulation techniques are applied to determine the self-consistent solution of Eqs. (2)-(8). The electron profile for \(-1V < V_{\text{extern}} < 1V\) for charge carrier enrichment is shown in Fig. 2. The case of depletion of electrons as a function of the applied voltage is illustrated in Fig. 3. Both ferroelectric and semiconducting layer have a donor concentration of \(N_D = 10^{19}\text{cm}^{-3}\) and the spontaneous polarization is set to \(|P_S| = 10\mu\text{C/cm}^2\). Note: A switching of the ferroelectric polarization has not yet been considered. For \(P_S > 0\), a strong enrichment of electrons leads to a highly conductive state. In case of \(P_S < 0\), the depletion of electrons at the ferroelectric/semiconductor interface correlates with a poorly conductive state. As shown in the simulation, even if a large number of electrons is present in the ferroelectric layer, the polarization charge is not perfectly screened, but still significantly affects the concentration of electrons in the system. Although the inner potential reveals a certain distortion of the triangular shape as shown in Fig. 1d, which is caused by a band bending, the formation of a potential barrier or a potential well can still be observed.

An estimation of the \(I-V\) curve from the electron distribution under consideration of a switching of the ferroelectric polarization at an external voltage exceeding 0.5V and an electron mobility of \(\mu_n = 1\text{cm}^2/\text{Vs}\) is illustrated in Fig. 4. A hysteretic resistance curve is observed, whereby the high or the low resistive state can be read out by a voltage below the threshold voltage. The inset illustrates the scalability of the resistivity under variation of the donor content. Further adjustment can be achieved e.g. by variation of the layer thicknesses, the value of the spontaneous polarization (different material systems) or the contact properties of the electrode interfaces. Even materials with a small spontaneous polarization, which can not be used in FRAM applications, may be suitable for the proposed memory concept. We regard complex oxides (Perovskites), II-VI mixed crystals (ZnCdS), polymers (PVDF-TFE), but also liquid crystals as possible candidates for the realization of the FFRAM device.

### IV. Conclusion

We have demonstrated by numerical simulation studies the resistive storage properties of a novel memory device built from a conducting ferroelectric semiconductor bilayer structure. A high and a low resistive state of the memory can be addressed by switching the polarization in the ferroelectric layer. Special emphasis was put on the interaction between conduction electrons and the ferroelectric leading to a redistribution of the majority charge carrier and a partial screening of spontaneous polarization. An estimation of the \(I-V\) characteristic as well as the influence of the dopant concentration shows a wide scalability of the resistance. This illustrates the potential of the proposed device as an alternative concept for future high integrated non-volatile random access memories ranging from Si-based technology to polymer applications.

### Acknowledgment

The authors would like to thank N. A. Pertsev, R. Waser, K. Szot and R. Oligschlaeger (the flying dutchman) for fruitful discussions. Special thanks to A. Rüdiger for carefully reading the manuscript.
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