A grid-tied photovoltaic transformer-less inverter with reduced leakage current

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Abstract. The importance of transformer-less inverters has been increased since these are highly efficient, less costly, reduced in weight compared to conventional inverters for PV systems connected to grid. This fact led researchers to propose various topologies of transformer-less inverters, which have been validated for only injection of real power towards grid. However, recently new regulation has been imposed by all international power regulatory agency is that these PV inverters integrated with grid should have the capability of handling flow of a certain quantity of reactive power. By considering this point, a noble topology of transformer-less inverter has been developed for grid integrated PV system. Unlike previous topologies during reactive power injection, the new topology does not face reverse recovery issues, which helps to enhance the efficiency of the proposed inverter by exploiting MOSFET switches. Moreover, leakage current becomes low by keeping the common mode (CM) voltage at input DC voltage’s midpoint.

1. Introduction

Usually, PV inverters can be classified into two groups on the basis of the galvanic isolation. First one is isolated inverter and the other is non-isolated inverter. A transformer which is operated in high or low frequency can be used in isolated inverter [1-8]. The efficiency of PV inverter is reduced due to the use of transformers. As the size of the low frequency transformer is big, it also increases the total system area [9-16]. Non-isolated (transformerless) inverter has higher efficiency and it is small in size than isolated inverter [17-19]. Yet, because of no transformer, there is leakage current in non-isolated inverter (galvanic isolation) [20-23]. However, parasitic capacitance can be a problem between the PV array and grounded mechanical structure. The connection between PV array and grid is direct if non-isolated inverter is used and it is made without galvanic isolation. During the operation of the switching components (at starting), with the help of common node capacitive current is injected in the inverter [24-27]. This induced leakage current affects the normal characteristics of the inverter and eventually the PV array is disconnected from the grid when residual current is tripped. This induced leakage current can be the reason of tripping residual current and then the whole system has to be reactivated manually [28-31]. So, the leakage current should be eliminated or it must be kept in a low value.

In [32], full-bridge inverter based topologies have been presented to provide solutions to low efficiency and leakage current problem associated with the previous inverters. Further, to reduce the
leakage current and increase the efficiency a DC bypass topology has been introduced in [33], by adding two diodes and two switches with full-bridge inverter.

For decoupling the converter during freewheeling mode, the full H-bridge topology has been modified by adding an extra MOSFET switch which is referred as H5 topology [34]. By connecting AC bypass with Full-Bridge inverter another topology named highly efficient and reliable inverter concept (HERIC) has been designed in [35]. In [36], another two topologies of HERIC known as extended HERIC have been presented. H6-type MOSFET inverter topology is described in [37] which has been designed by adding two diodes and two switches in the DC side. By introducing two MOSFET switches and two capacitors in the conventional full-bridge inverter another topology named optimized H5 (oH5) has been designed in [38]. The advantages of these topologies belong to the improvement of efficiency and reduction in leakage current. However, no evidence have been found in the literature to analyze their performance in terms of reactive power controlling capability.

To address the aforementioned issues with the previous transformer-less inverters, a novel grid connected transformer-less PV inverter has been developed. The advantage of the prototype is unlike previous inverters during reactive power injection, the new PV inverter does not face reverse recovery issues, which helps to enhance the efficiency of the proposed inverter by exploiting MOSFET switches. Moreover, leakage current becomes low by keeping the common mode (CM) voltage at input DC voltage’s midpoint. For the proposed PV inverter a new control method has also developed to provide utility grid with sufficient reactive power support.

2. Proposed New H6-Type Topology
2.1. Circuit structure of the new inverter

The proposed transformerless inverter topology is depicted in Figure 1, which constitutes of six switches (G1-G6) and two diodes (D1-D2). Grid side lowpass LC-type filter has been made by L_A, L_B, and Co. V_PV and C_dc represent the input voltage and DC-link capacitor. The unipolar-SPWM is employed to the proposed topology with three-level output voltage. The super-junction MOSFETs is utilized as the main power switches to increase the efficiency because no reverse-recovery issues are required for the proposed configuration.

![Figure 1. Proposed improved H6 transformerless PV inverter](image)

2.2. Operating principle of the proposed topology

Figure 2 shows the switching pattern for the proposed topology with unity power factor. As can be seen, (G1, G4) and (G2, G5) commutate at the switching frequency with identical commutation order in the positive and negative half cycle of the grid current, respectively.
In Figure 3, the operating principles of the proposed topology are shown. Four operation modes are proposed to generate the output voltage state of $+V_{PV}$, 0, and $-V_{PV}$, which can be explained as follows:

1) Mode 1 is the active mode in the positive half cycle of the grid current. When G1 and G4 are turned-on, the voltage $V_{AN} = V_{PV}$ and $V_{BN} = 0$, thus $V_{AB} = V_{PV}$ and the CM voltage, $V_{CM} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

2) Mode 2 is the freewheeling mode in the positive half cycle of the grid current. The freewheeling current flows through G6 and D2. In this mode, $V_{AN} = V_{BN} = V_{PV}/2$, thus $V_{AB} = 0$ and the CM voltage, $V_{CM} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

3) Mode 3 is the active mode in the negative half cycle of grid current. Similar to mode 1, when G2, G3 and G5 are turned-on, the voltage $V_{AN} = 0$ and $V_{BN} = V_{PV}$, thus $V_{AB} = -V_{PV}$ and the CM voltage, $V_{CM} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

4) Mode 4 is the freewheeling mode in the negative half cycle of grid current. When G5 and G2 are turned-off, the freewheeling current flows through G3 and D1. In this mode, $V_{AN} = V_{BN} = V_{PV}/2$, thus $V_{AB} = 0$ and the CM voltage, $V_{CM} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

As described above, the CM voltage remains constant during the four commutation modes of the proposed inverter and equals $V_{PV}/2$. As a result, the inverter hardly generates any ground leakage current. However, the anti-parallel diodes of the MOSFETs will be activated if a phase shift is occurred between the inverter output voltage and current. Accordingly, the dependability of the system will be reduced because of the low reverse recovery issues of MOSFET anti-parallel diode.
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2.3. Operating principle of the proposed topology

The switching power losses for MOSFET switches and diode reverse-recovery can simply be defined as [28]:

\[
P_{SW\_MOSFET} = f_{sw}E_{oss}(V_{ds})
\]

\[
P_{Diode\_RR} = V_{d}f_{sw}\left[\left(\frac{I_{m}}{\pi} + \frac{I_{RR}}{4}\right) t_{a} + \frac{I_{RR}}{6} t_{b}\right]
\]

where, \(P_{SW\_MOSFET}\) and \(P_{Diode\_PR}\) are the power losses in MOSFET switches and diodes respectively.

2.4. Efficiency and current harmonic Calculation

The efficiency has been calculated using the following equations:

\[
\eta_R = \left(\frac{P_o}{P_i}\right) \times 100
\]

where \(\eta_R\) is the rated output efficiency (%); \(P_o\) is the rated output power (kW); \(P_i\) is the input power at rated output (kW). The total harmonic current distortion (THD) can be defined as:

\[
THD_i = \sqrt{\sum_{n=2}^{\infty} \frac{I_n^2}{I_1}}
\]

where \(I_1\) is RMS value of fundamental current, \(I_n\) is RMS value of \(n^{th}\) order harmonic.

3. Proposed New H6-Type Topology

The performance of the proposed improved H6 topology has been experimentally verified with a laboratory prototype rated 1kW/50Hz. The detail specification is presented in Table I. The PV module, and the stray capacitance between the PV module and the ground have been replaced with a 400V DC source and two capacitors of 75nF each, respectively. The switching frequency is 16 kHz.

3.1. Experimental Results

The gate signals of the proposed new topology are shown in Figure 4. It is clear that the gate signals are in agreement with the theoretical analysis made in section II (subsection B) and the gate drive voltages are kept constant at the desired level. Figure 5 shows the drain-source voltage waveforms of the switches G1, G2 and G5, indicating the switching voltages of the switches are half of the DC input voltage without any overstress. The current stress on the switches G1, G2 and G4 is shown in Figure 6. It can be seen that the current stress is smooth and no extra current is present.
Table 1. Specifications of the prototype

| Inverter Parameter         | Value         |
|----------------------------|---------------|
| Nominal Input Voltage      | 400VDC        |
| Grid Voltage / frequency   | 240V / 50Hz   |
| Rated Power                | 1000 W        |
| Nominal AC current         | 4.2A          |
| Switching Frequency        | 20kHz         |
| DC bus capacitor           | 470µF         |
| Filter capacitor           | 2.2µF         |
| Filter Inductor L<sub>A</sub>, L<sub>B</sub> | 3mH          |
| PV parasitic capacitor C<sub>pv1</sub>, C<sub>pv2</sub> | 75nF          |

**Figure 4.** Experimental gating signals of the switches

**Figure 5.** Drain-source voltage waveform of the switches G1, G2, and G5

**Figure 6.** Current stress on the switches G1, G2 and G4

The measured value of leakage current is effectively limited within the peak value of 50mA and RMS value of 15mA, which is shown in Figure 7. This peak and RMS values are lower in magnitude corresponding to the German standard VDE0126-1-1.

The experimental waveform of the load current and voltage are shown in Figure 8 in case of full-load condition. As seen in Figure 8, the inverter output voltage V<sub>AB</sub> has three levels, +V<sub>PV</sub>, 0, and -V<sub>PV</sub>. Therefore, it is experimentally verified that the proposed topology is modulated with unipolar-SPWM and the DM characteristics is good.
The current harmonic distribution is depicted in Figure 9, which shows that the THD is 2.9%. Therefore, it is clear that the proposed inverter presents low harmonic distortion and a high power factor that can meet the requirement of IEEE Std 1547.1™-2005.

The efficiency of the proposed topology with 20 kHz and 40 kHz operating frequencies are measured and compared, as illustrated in Figure 10. The YOKOGAWA WT1800 precision power analyzer is used to measure the efficiency of the proposed inverter. Note that the presented efficiency diagram covers the total power device losses and the filter inductor losses but it does not contain the losses for the control circuit. It is obvious that the efficiency of the proposed topology for 40 kHz operating frequency is very close to the efficiency with 20 kHz, which allows the proposed inverter to operate at high switching frequency. The maximum efficiency of the proposed inverter for 20 kHz and 40 kHz frequency operations are measured and found to be 98.6% and 98.36%, respectively. The European efficiency is calculated by combining several weighted factors at various output power, as expressed in equation (3). The calculated European efficiency for 20 kHz and 40 kHz operating frequencies is 98.44% and 98.18%, respectively. It can be seen that the European efficiency at 20 kHz is about 0.26% higher than at 40 kHz operating frequency. Therefore, the proposed topology can operate with high frequency by retaining high efficiency. Furthermore, the maximum conversion efficiency is slightly higher than European efficiency, indicating an optimal inverter topology.
Finally, the performance comparison among the bipolar FB topology, H5 topology, improved topology and proposed new topology is summarized in Table II. It can be seen that the bipolar FB topology has the lowest efficiency due to the high losses as a result of two-level output voltage. The H5 topology improves the efficiency (97.29%), but draws higher leakage current (45.6mA) due to the fluctuating CM voltage. On the other hand, the improved topology keeps the efficiency as high as H5 topology with low leakage current (13.3mA). However, the proposed new topology achieves highest efficiency (98.44%) with low leakage current. Therefore, it can be concluded that the proposed new topology is very suitable for grid-tied PV application.

### Table II. Performance comparison among the bipolar FB topology, H5 topology, H6 topology, and proposed improved H6 topology

| Parameters          | Bipolar FB Topology | H5 Topology | Improved Topology | Proposed Topology |
|---------------------|---------------------|-------------|-------------------|-------------------|
| PWM pattern         | Bipolar             | Unipolar    | Unipolar          | Unipolar          |
| DM characteristics  | Poor                | Good        | Good              | Good              |
| CM voltage          | Constant            | Floating    | Constant          | Constant          |
| Leakage current (mA)| 16.8                | 45.6        | 13.3              | 15.0              |
| European efficiency (%)| 95.06             | 97.29       | 97.45             | 98.44             |

### 4. Conclusions

A new single-phase transformerless topology for grid-tied PV system has been developed using MOSFETs and SiC diodes as no reverse recovery issues are required for the main power switches. Two additional switches and two diodes with the conventional FB topology ensure the disconnection of the PV module from the grid at the freewheeling mode. As a result, the CM voltage kept constant and the leakage current is reduced to safe level. The developed inverter can also operate with high frequency by retaining high efficiency to reduce the size of the output filter. The experimental results show 98.6% maximum efficiency and 98.44% European efficiency on the 1kw prototype circuit with 20 kHz switching frequency.
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