Modeling of Dual-Gate GaAs-Nanowire FET for Room Temperature Charge-Qubit Operation: An NEGF Approach

Basudev Nag Chowdhury¹ and Sanatan Chattopadhyay¹,²*

¹Department of Electronic Science, University of Calcutta, Kolkata, India
²Centre for Research in Nanoscience and Nanotechnology (CRNN), University of Calcutta, Kolkata, India

*E-mail address: scelc@caluniv.ac.in

Abstract

The current work investigates the performance of dual-gate GaAs-nanowire FET as a charge-qubit device operating at room temperature. In compatibility with the state-of-the-art classical bit technology, it is shown that the single gate of a nanowire FET can be replaced by two localized gates to achieve such charge-qubit operation. On application of relevant biases to the localized gates, two voltage tunable quantum dots are created within the nanowire channel with electrostatically controlled single-state-occupancy and inter-dot coupling leading to charge-qubit operation at room temperature. The associated electron transport is theoretically modeled on the basis of non-equilibrium Green’s function (NEGF) formalism. The ‘initialization’ and ‘manipulation’ for qubit operation are performed by applying suitable gate voltages, whereas the ‘measurement’ is executed by applying a small drain bias to obtain a pulse current of ~pA order. A ~25 MHz frequency of coherent oscillation is observed for the qubit and a characteristic decay time of ~ 70 ns is achieved. The results suggest that such dual gate nanowire FET is a promising architecture for charge-qubit operation at room temperature.

Keywords

Charge-Qubit; Quantum Dot; Coherent oscillation; Nanowire FET; NEGF
I. Introduction

The advent of quantum computation and quantum information processing in practice is fundamentally based upon the development of qubits, where quantum superposition principle leads to coherent oscillation between two qubit-states within their characteristic coherence time \([1, 2]\). Amidst various approaches to develop spin and charge based qubits, the exploitation of SQUID including Josephson junction \([3-6]\) and semiconducting quantum dots (QDs) \([7-14]\) have drawn key attention for achieving desired control over the coherent manipulation of their quantum states. Especially, the double quantum dot (DQD) device with a single excess charge have emerged as one of the most promising qubit architectures due to its electrostatically controlled operation by implementing a number of voltage gates \([7, 9-13]\). However, a principal challenge for implementing all such device schemes for practical applications is that such qubits can operate only at very low temperature (~ mK). Further, such device schemes for qubits are fundamentally different from the state-of-the-art classical bits generation schemes, which use the matured metal-oxide-semiconductor field-effect-transistor (MOSFET) technology or their emerging evolutionary counterparts, such as, nanowire FETs. Evidently, the relevant mature technology for qubit generation is still a concern in terms of reliability, complexity and cost-effectiveness. Therefore, despite the successful and systematic progress in prototype experiments of the aforesaid approaches, the increasing social drive for quantum computation and quantum information processing demand for the innovative architectures, that needs to be compatible, scalable and integrable with state-of-the-art of matured semiconductor technology.

In this context, the current work proposes a scheme with dual-gate GaAs-nanowire FET architecture for charge-qubit operation at room temperature. The conventional approach of generating classical bits is to use a single gate over the entire channel of a FET. However, it is shown in the current work that charge-qubit operation can be achieved if two localized gates are used over the channel of a nanowire FET instead of a single gate. In such architecture, appropriate biases on the two localized gates can create two voltage tunable quantum dots (VTQDs) with single state each, when the inter-dot tunneling is insignificant. The occupancy of such state of QDs can be controlled by appropriate biases at the respective gates with respect to source/drain. However, the coupling between two QDs can be tuned from the ‘non-resonant’ to ‘resonant’ condition by manipulating gate voltages relative to each other, and thereby, either localizing an electron at one of the QDs, or to delocalize it over both the QDs, respectively.
Accordingly, the basic modes of qubit operation such as ‘initialization’ and ‘manipulation’ are obtained by varying relevant voltages at the two gates, and the ‘measurement’ is performed by applying a small bias at the drain terminal. The results of such operations are predicted in the current work by self-consistently solving the relevant quantum-electrostatic equations for such proposed dual-gate nanowire FETs, employing non-equilibrium Green’s function (NEGF) approach.

II. Scheme of device and qubit-operation

The schematic of dual-gate GaAs-nanowire FET device considered in the current work is depicted in Fig. 1(a), where an Ω-gate configuration is assumed, owing to their lesser complexity for fabrication process. The nanowire material is chosen to be GaAs due to its symmetric effective mass tensor of low values (m*=~0.06), which can lead to create discrete quantized states at room temperature [15]. SiO₂ of 2 nm thickness is selected as the gate insulator since it has been reported to exhibit minimum gate tunneling leakage current in nanoscale MOS architecture [16]. The source/drain are considered to be GaAs with a doping level of 5×10¹⁷/cm³ since such order of doping concentration is sufficient to make it degenerate [17]. In order to achieve strong quantum confinement for realizing a one-level device at room temperature, diameter of the nanowire is taken to be 5 nm, which is significantly smaller than the excitonic Bohr radius of GaAs (~12 nm) [15]. Its channel length is considered to be 20 nm that refers to the ballistic transport regime with minimized scattering [18, 19], which is necessary for reducing the associated decoherence effects. Further, the phase breaking effect in the device current due to phonon scattering, which might be the another source of decoherence, has already been shown to be negligibly small in a one-level system [20] and therefore it is not considered in the present work. It is also imperative to mention that the energy gap between ground state and first excited state in the present VTQDs with considered materials and dimensions is ~500 meV, and thus, thermal voltage at room temperature (~25 mV) is insufficient for corresponding excitation. Moreover, charge-qubit operation in the present device architecture is associated with the lowest unoccupied state (i.e. single ground state only) unlike the conventional DQD charge-qubits that exploit highest unoccupied state with already occupied lower sates. Therefore, conventional noise in charge-qubits is expected to be minimized in the present dual-gate nanowire FET device structure. Analyzing the penetrability of electron wave from source/drain into the two adjacent
VTQDs, the source-to-gate-1 and gate-2-to-drain distances are assumed to be 3 nm and 8 nm, respectively.

Consequently, the two gate voltages can be defined in such a manner that the electron from source can tunnel into VTQD-1 to occupy its single state, however, such single state of VTQD-2 remains unoccupied due to negligible electron tunneling probability through its larger distance.

Fig. 1. (a) The schematic of dual-gate GaAs-nanowire FET device on IOS platform; (b) schematic band alignment along the nanowire channel representing the modes of qubit operation by varying the voltages at two gates and drain.
from the drain. Both the gate lengths are considered to be 3 nm with their spacing of 3 nm also. In order to electrically isolate the active device from substrate, the entire device is assumed to be fabricated on an insulator-on-substrate (IOS) platform as schematically shown in Fig. 1(a).

Fig. 1(b) represents the scheme of qubit operation in such a dual-gate nanowire FET device. When appropriate voltages are applied to the gates (i.e., \( V_{G1} \) at gate-1 and \( V_{G2} \) at gate-2), two 3D-quantized potential wells with single state each are created locally within the channel underneath the gates, which are referred to \( |L\rangle \) and \( |R\rangle \), respectively. Due to positional asymmetry of the gates (i.e., difference in source-to-gate-1 and gate-2-to-drain distances), \( |L\rangle \)-state is initially occupied due to the inflow of an electron from source whereas \( |R\rangle \)-state remains unoccupied. The gate biases can then be tuned to manipulate the inter-dot tunnel coupling to get resonance by creating a superposed state, \( |\psi\rangle = \alpha(V_{G1}, V_{G2})|L\rangle + \beta(V_{G1}, V_{G2})|R\rangle \), where \( |\alpha|^2 \) and \( |\beta|^2 \) are probabilities of the electron to be within the corresponding QDs. If a small drain bias \( (V_{D}) \) is applied at such condition, the electron will solely be in either of the QDs suffering collapse to \( |L\rangle \)-state or \( |R\rangle \)-state, resulting to ‘no drain current’ or ‘a pulse current’ (∼pA order), respectively, leading to qubit oscillation. Such order of current at room temperature can be measured by a suitable semiconductor characterization setup [21]. It may be worthy to note that the collapse of such superposed state can also be executed by measuring one of the gate capacitances, which is of the order of ∼aF. Such a small capacitance can be measured by following the approach reported in [22]. Further, the degeneracy of the superposed state splitting into ‘bonding’ and ‘anti-boding’ states is discussed later in the present work.

III. Theoretical modeling

The general transport properties of nanowire FET devices have been extensively studied by developing the relevant NEGF formalism [23-27]. Following such approach, the qubit operation using the present dual gate nanowire FET is theoretically modeled by considering Hamiltonian of the nanowire channel coupled with source and drain as,

\[
H = \sum_i H_{iso} c_i^\dagger c_i + \sum_{i,r} \left( \tau^{S/D}_{i\alpha} c_i^\dagger c_r + \tau^{S/D}_{r\alpha} c_r^\dagger c_i \right)
\]

(1)
where, $H_{iso}$ is the Hamiltonian of isolated nanowire when it is not coupled to the source/drain, whereas the couplings between $i^{th}$ state of nanowire channel and $\nu^{th}$ state of source/drain are given by $\tau_{\nu}^{S/D}$. The second quantization field operators $c_i^+$ and $c_i$ (or $c_{r}^+$ and $c_{r}$) represent creation and annihilation of electrons within the nanowire channel (or in source/drain), which follow the Fermi-Dirac anti-commutation relations,

\[
\begin{align*}
\{c_i, c_j^+\} &= \delta_{ij} \\
\{c_i, c_j\} &= 0 \\
\{c_{i}^{+}, c_{j}^{+}\} &= 0
\end{align*}
\]

indicating single occupancy of each quantum state for electrons obeying the exclusion principle.

It is apparent that the source/drain consists of a large a number of electrons at several energy states, whereas the gate voltage-assisted quantum dots within the nanowire channel have single state each with single occupancy. Therefore, the low-energy field theory including fermionic second quantization is necessary to model such one-to-many state coupling along with single occupancy. The relevant equations of motion for electrons are derived from the Hamiltonian using Heisenberg equation and can be solved from the local non-equilibrium Green’s function as a function of electron energy ($E$) in the nanowire coupled to source/drain as given by [23-25],

\[
G(E) = [E - H_{iso} - \Sigma_S(E) - \Sigma_D(E)]^{-1}
\]

where, $\Sigma_S$ and $\Sigma_D$ are the self-energies of source and drain, respectively, which depend on the corresponding coupling strength, $\tau_{\nu}^{S/D}$ [25]. The local density of states (LDOS) occupied by electrons are therefore obtained to be,

\[
D(E) = \frac{i}{2\pi a} \left[ (G(E)[\Sigma_S(E) - \Sigma_S^+(E)]G^+(E)f_S(E) + (G(E)[\Sigma_D(E) - \Sigma_D^+(E)]G^+(E)f_D(E) \right]
\]

where $f_S$ and $f_D$ are Fermi-Dirac distribution functions corresponding to source and drain, and ‘$a$’ is the grid spacing considered for simulation. Integrating the occupied LDOS over energy, followed by its normalization in coordinate space (suppose $z$-axis along nanowire channel), gives rise to the positional probability ($|\psi(z)|^2$) of electron within the device. For numerical analysis, the carrier profile ($n(z)$), obtained by assuming an initial potential distribution in
isolated Hamiltonian \( (H_{iso}) \), is put into the Poisson’s equation to get resultant potential
distribution along the channel \((\varphi(z))\) including two VTQDs. Such potential distribution is then
incorporated again into the isolated Hamiltonian \((H_{iso})\), and the iteration process is continued
until self-consistency is achieved. It is worthy to mention at this point that the Poisson’s equation
for nanowire FET with an \( \Omega \)-gate structure leads to [27],

\[
\left[ \frac{d^2}{dz^2} - \frac{2}{R^2} \frac{\varepsilon_{ox}}{\varepsilon_{NW}} \ln(1 + t_{ox}/R) \right] (\varphi(z) - V_G(Z)) = \frac{e}{\varepsilon_{NW} (\pi - \theta) R^2} n(z) \tag{5}
\]

where, \( \varepsilon_{NW} \) and \( \varepsilon_{ox} \) are permittivity of the nanowire and gate oxide, respectively; \( t_{ox} \) is oxide
thickness and \( R \) is the nanowire radius; \( V_G(Z) = V_{G1} \) and \( V_G(Z) = V_{G2} \) throughout the gate-1 and
gate-2, respectively; and \( \theta = \cos^{-1}(R/(R + t_{ox})) \) for \( \Omega \)-gate without any insertion of nanowire
into the IOS [27]. Finally, on application of a small drain bias \((V_D)\), the amplitude of the pulse
current is obtained to be [25],

\[
I_0 = \frac{2e}{h} \int Trace\left(i[\Sigma_S(E) - \Sigma_S^+(E)]G(E)[\Sigma_D(E) - \Sigma_D^+(E)]G^+(E)\right) (f_s(E) - f_D(E - V_D)) dE \tag{6}
\]

whereas the oscillatory decay of such pulse in time, originated due to coherent oscillation of
qubit, can be obtained from the retarded Green’s function following [26] as,

\[
I = I_0 \left( F.T._{E \rightarrow t} [G_{iso}(E)\Sigma_D(E)G(E)] \right) \tag{7}
\]

where \((F.T._{E \rightarrow t})\) indicates Fourier transform from energy space to the time domain and \( G_{iso}(E) \)
represents the Green’s function for isolated channel when its coupling with source/drain is
negligibly small.

**IV. Results and discussion**

The performance of dual gate GaAs nanowire FET considered in the present work as a charge-
qubit is studied from the results obtained by numerically solving the above equations in Matlab
and Fig. 2 depicts its basic modes of operation including ‘initialization’, ‘manipulation’ and
‘measurement’. The variation of occupied LDOS in energy space along the nanowire channel
consisting of two VTQDs at such operational modes is plotted in Fig. 2. The dotted lines
represent the corresponding self-consistent conduction band alignments. The ‘initialization’ \((|\psi\rangle = |L\rangle)\) condition is obtained by applying a voltage of 1.15 V at gate-1 and 1.3 V at gate-2 without any bias at the drain. It is apparent from the plot of Fig. 2 that asymmetric position of the gates enables to create a significant difference between the geometry of voltage-assisted 3D-quantized potential wells of the two QDs and thereby makes it possible for electron to occupy the single state of QD-1 keeping the state of QD-2 empty which is essential for such ‘initialization’.

![Diagram showing the variation of occupied LDOS](image)

Fig. 2. Plots of the variation of occupied LDOS (contour) in energy space along the nanowire channel with conduction band alignment (dotted line) showing the two VTQDs at different modes of qubit operation.

If an incremental pulse voltage \((\Delta V_{G2} \sim \text{mV})\) is now applied on gate-2, the superposed state \(|\psi\rangle = \alpha |L\rangle + \beta |R\rangle\) is obtained, where the single electron is partially at QD-1 and partially at QD-2 at the same time due to inter-dot resonance tunneling. The corresponding probabilities, \(|\alpha|^{2}\) and \(|\beta|^{2}\), can be manipulated by varying the pulse voltage that modulates the broadening of resonance; and almost an equal probability in both QDs is obtained at \(\Delta V_{G2} = 42 \text{ mV}\) shown in Fig. 2. At such condition, a small bias of 42 mV is sufficient for the collapse of superposed state.
into either of $|R\rangle$ or $|L\rangle$ and accordingly it creates either a ‘pulse current’ or ‘no current’ through the device. It is imperative to note that the drain voltage must be small enough so that the electric field along the nanowire axis does not influence the result of measurement toward collapsing into the state $|R\rangle$ in comparison to $|L\rangle$.

The manipulation of superposition of the states $|L\rangle$ and $|R\rangle$ is demonstrated in Fig. 3(a), which represents the positional probability of electron, delocalized over the two VTQDs, for the pulse voltage at gate-2 varying in the range of 30-48 mV. It is apparent from such plots that probability of $|L\rangle$-state decreases with increasing $\Delta V_{G2}$ in the considered range, leading to a corresponding increase of the probability of $|R\rangle$-state. A close inspection of the results shown in Fig. 3(a) indicates the positional probability distribution in QD-1 to be asymmetric with the maxima being nearer to the source, which is attributed to the asymmetric well shape of QD-1 due to conduction band bending near the source (Fig. 2). Such position of the maxima may be beneficial for reducing the possible source induced decoherence by Coulomb blockade effect.

![Fig. 3. (a) The plots of positional probability of electron, delocalized over the two VTQDs, for the pulse voltage at gate-2 leading to manipulation of superposition of the states; (b) Bloch sphere representing the superposed states $|\psi\rangle = \alpha|L\rangle + \beta|R\rangle$ varying $V_{G1}$ (1.12-1.16 V) and $V_{G2}$](image-url)
(1.33-1.348 V) at \( V_D = 0 \) V; two different set of dotted colour points represent the opposite phases.

The manipulation of qubit in terms of relative amplitude along with phase of the two states is represented by plotting the corresponding Bloch sphere, as shown in Fig. 3(b), where the opposite phases are shown by two different set of dotted colour points. Since \(|\alpha|\) and \(|\beta|\) can be manipulated by changing the bias at gate-2 for a given voltage at gate-1 under the normalization constraint as shown in Fig. 3(a), the polar angles are obtained by varying the \( \Delta V_{G2} \) in the range of 30-48 mV around the operating point (\( i.e., V_{G1} = 1.15 \) V, \( V_{G2} = 1.342 \) V). On the other hand, the different azimuthal angles represent relative phases between the states \( |L\rangle \) and \( |R\rangle \) which are resulted from small variation of \( V_{G1} \) in the range of 1.12-1.16 V. Such azimuthal angles are calculated from the phase difference of local values of Green’s function at the two QDs.

![Fig. 4](image)

Fig. 4. The variation of output signal (drain current) with time at different operating points defined by the corresponding \( V_{G1}-V_{G2} \) combinations with \( V_D = 42 \) mV, indicating coherent oscillation enveloped by qubit dephasing.

The manipulation of such superposed state, in time domain, can be conducted by applying \( \Delta V_{G2} \) as the pulses with its duration less than the overall pulse repetition time [11]. Such repetition time in the present dual gate nanowire FET device is considered to be the average lifetime of the electron pulse, entering QD-1, which is calculated by following [26] and obtained to be ~336.5
ns. Therefore, the pulse duration of $\Delta V_{G2}$ is varied up to ~250 ns and the corresponding response of pulse current is studied with a combination of voltages at gate-1 and gate-2 around the operating point, and plotted in Fig. 4. The qubit oscillation frequency is found to be ~25 MHz, exhibiting a negligible variation for the considered values of $V_{G1}$ and $V_{G2}$. Such coherent oscillation frequency of the qubit generated by present dual gate nanowire FET is of the order of previously reported results [11]. The characteristic decay time for qubit dephasing is obtained to be ~73 ns, which is almost 1/3rd of the reported value for Si-DQD at a temperature of ~20 mK, however, significantly higher than the results (~1 ns and less) obtained for GaAs/AlGaAs based DQD structure at ~100 mK [9, 10].

Fig. 5. Mapping of output signal amplitude (maximum drain current) on the $V_{G1}$-$V_{G2}$-plane at $V_D$=42 mV. The dotted hyperbolic curves represent the ‘bonding’ and ‘anti-bonding’ states during resonance and dotted lines indicate such states of isolated QDs.

It is imperative to mention that the operating point for maximum amplitude of the output signal ($I_0$) is observed to shift marginally in both the gate voltage axes due to the applied drain bias for ‘measurement’, and it splits into two states, i.e. $(V_{G1}, V_{G2}) = (1.14 \text{ V}, 1.342 \text{ V})$ and $(1.144 \text{ V}, 1.346 \text{ V})$. This is attributed to the fact that during inter-dot resonance tunneling while
manipulating the qubit superposition, the single electronic state splits into two states, namely, ‘bonding’ and ‘anti-bonding’, distributed over both the QDs [7]. The energy variation of such ‘bonding’ and ‘anti-bonding’ states is a function of energy difference between the isolated states of the two QDs and their anticrossing energy for coupling [7]. Such effect is manifested in the mapping of output signal amplitude on the plane of two gate voltage axes as shown in Fig. 5. It is apparent from Fig. 5 that the ‘bonding’ and ‘anti-bonding’ states of the coupled-QDs (|b⟩ and |ab⟩) and isolated-QDs (|QD1⟩ and |QD2⟩) as a function their gap of eigenstates and the anticrossing energy are expressed as the output current variation with the two gate voltages. This is schematically traced in Fig. 5 by the dotted hyperbolic curves and lines, respectively. The energy gap of coupled-QDs and isolated-QDs are functions of both $V_{G1}$ and $V_{G2}$, and therefore, the output signal mapping on ‘$V_{G1}$-$V_{G2}$’-plane is a coordinate transformation of the hyperbolic variation of such energy gaps between the ‘bonding’ and ‘anti-bonding’ states. Mappings of similar nature are reported in the experimental results obtained by studying GaAs/AlGaAs based DQD structure [10]. However, Fig. 5 also shows the appearance of ‘excited’ ‘bonding’ and ‘anti-bonding’ states (above |b⟩ and below |ab⟩) in the present device, which are attributed to the asymmetry in quantum well-shape of the two VTQDs.

V. Conclusion

To summarize, the present work shows that a replacement of the single gate of a nanowire FET by two localized gates can create charge qubit that is compatible with the state-of-the-art classical bit generation technology. The selection of GaAs as nanowire material and its appropriate dimensions can enable such charge-qubit operation involving single electron state at room temperature. The qubit operation is theoretically modeled by developing a quantum-electrostatic simultaneous solver based on non-equilibrium Green’s function (NEGF) formalism. The operational scheme and the obtained values of coherent oscillation frequency and characteristic decay time of the proposed qubit suggest that such dual gate nanowire FET architecture is promising for room temperature charge-qubit operation.

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Data availability statement
The datasets generated and analysed during the current study are available from the corresponding author on reasonable request.

Conflict of interest
The authors have no conflicts to disclose.

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