Enabling Design Methodologies and Future Trends for Edge AI: Specialization and Co-design

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Abstract—Artificial intelligence (AI) technologies have dramatically advanced in recent years, resulting in revolutionary changes in people’s lives. Empowered by edge computing, AI workloads are migrating from centralized cloud architectures to distributed edge systems, introducing a new paradigm called edge AI. While edge AI has the promise of bringing significant increases in autonomy and intelligence into everyday lives through common edge devices, it also raises new challenges, especially for the development of its algorithms and the deployment of its services, which call for novel design methodologies catered to these unique challenges. In this paper, we provide a comprehensive survey of the latest enabling design methodologies that span the entire edge AI development stack. We suggest that the key methodologies for effective edge AI development are single-layer specialization and cross-layer co-design. We discuss representative methodologies in each category in detail, including on-device training methods, specialized software design, dedicated hardware design, benchmarking and design automation, software/hardware co-design, software/compiler co-design, and compiler/hardware co-design. Moreover, we attempt to reveal hidden cross-layer design opportunities that can further boost the solution quality of future edge AI and provide insights into future directions and emerging areas that require increased research focus.

Keywords—Edge AI, edge device, machine learning, IoT, design methodology, co-design

1 INTRODUCTION

We are witnessing an unprecedented boom in artificial intelligence (AI), in particular deep learning (DL), which has made remarkable progress in various areas such as computer vision, natural language processing, health care, autonomous driving, and surveillance. To accomplish this, AI technologies have broadened from a centralized fashion to mobile or distributed fashion, opening a new era called edge AI, with dramatic advancements that are substantially changing everyday technology, social behavior, and lifestyles.

Edge AI couples intelligence and analysis to a broad collection of connected devices and systems for data collection, caching, and processing \cite{1}. It enables a wide variety of new promising applications where data collection and analysis are combined together. For example, billions of mobile users are exploiting various smartphone applications such as translation services, digital assistants, and health monitoring services. Meanwhile, the ever-increasing demands of edge AI create tremendous technical challenges, especially for application development and deployment. Edge devices usually have strict device constraints, such as limited computing capability, memory capacity, and power budget, often with order-of-magnitude differences from those in server environments. In addition, as the adoption of edge AI technologies increases, the scale of their applications expands. The design and deployment for heterogeneous, large-scale edge AI systems and applications require tremendous engineering efforts and introduce complex research challenges.

Novel design methodologies and design automation tools are necessary to face the increasing sets of edge AI applications and challenges. A number of recent works tackle the challenges by spanning the entire development stack, from high-level software/algorithmdesign to low-level hardware design. Their enabling design methodologies can be grouped into the two categories, specialization and co-design. Design specialization carefully adapts common technologies for edge AI application scenarios, such as aggressive model compression or dedicated hardware accelerators. Co-design takes one step further to combine two or more specialized technologies to reveal more optimization opportunities.

In this paper, we aim to provide a comprehensive survey of the design methodologies for the new era of edge AI. There are recent efforts \cite{2,3} that survey the fundamental concepts and recent advancements of edge AI, but they approach from different angles, such as major domains, applications, and general technologies. Complementary to these surveys, we discuss Edge AI from a point of view of design methodology. To the best of our knowledge, we are the first to systematically summarize the representative works from different layers (software, compiler, hardware) of the entire develop-deploy stack, and provide a quantitative analysis across layers. By summarizing related works from different layers and scopes, we hope to motivate cross-layer co-design opportunities that can further contribute to high-quality and flexible edge AI solutions. Fig. 1 provides an overview organization of this work.
**2 EDGE AI FUNDAMENTALS**

In this section, we briefly introduce the four major domains of edge AI, followed by the prevailing edge AI devices, development tools, and frameworks.

### 2.1 Major Domains

Edge AI contains four primary domains: edge caching, edge training, edge inference, and edge offloading. First, **edge caching** refers to data collection, generation, and storage from edge devices and surrounding environments to support edge applications. For example, mobile users’ information generated by themselves is stored in their smartphones, while environmental monitoring devices and sensors store data at nearby edge servers. Second, **edge training** exploits the local data and computing power at the edge, without the high bandwidth requirements of transferring the data first to the cloud. Edge training often requires reduced bit-widths to stay within the device constraints. As an additional benefit, edge training preserves user data privacy by avoiding transferring data first offsite.

Third, **edge inference** is the execution of AI algorithms at the edge. Considering the network, memory, and computational needs of training, edge inference is often the most common form of edge AI and has received the majority of the recent research attention. Finally, **edge offloading** is a distributed computing scheme where devices offload their application tasks to the cloud. Offloading is a promising approach to increase the computation capability of edge devices with limited resources and power budget.

### 2.2 Edge Devices

The devices that span these major domains are a heterogeneous mix of devices including sensors, monitoring devices, CPU/GPU-based, and ASIC-based. Fig. 1 provides a brief summary of different edge devices, noting their advantages, limitations, and prominent examples.

**CPU-based.** CPUs have the longest history and are the most common in many processing and control systems. CPU-based edge devices have the advantages of versatility, low power, low cost, multitasking, and ease of programming. Since they are primarily designed for general instruction sequences, they usually have limited parallelism. Multi-core architectures improve parallelism, yet CPU-based devices are still not ideal for massively parallel computation. The prevailing CPU-base edge devices include Arm Cortex-M series [5], Raspberry Pi series [6], Nano Pi series [7], Sipeed MAIX series [8], and others.

**GPU-based.** GPUs were originally designed for image processing and computation with a highly parallel structure, yet now are increasingly used to accelerate AI tasks that require massively parallel computing. Favoring the high performance through parallelism and programmability, embedded GPUs are specifically designed to be low-power and low-cost, and now are prevalent in many edge devices that accelerate deep learning tasks. Popular GPU-based edge devices include Nvidia Jetson family [9], AMD Ryzen family [10], and Arm Mali GPUs [11].

**FPGA-based.** FPGAs (field-programmable gate array) are integrated circuits designed to be configured through an array of programmable logic blocks. They have high application flexibility, for example, supporting arbitrary bit-width and custom numerical formats [12], and achieve higher efficiency and power efficiency.
performance than CPUs and GPUs in many tasks [13–15]. FPGAs usually outperform GPUs on low-latency designs for time-sensitive tasks [16] and consume lower power compared to CPUs and GPUs while delivering the same throughput. FPGAs, however, suffer from limited on-chip memory and low programmability.

The leading FPGA vendors, such as Xilinx, Intel, and Lattice, provide a large range of FPGA boards and System-on-Chips (SoCs) targeting various workloads, from power-efficient edge applications to compute-intensive cloud applications [17][18][18–20].

ASIC-based. ASICs (application-specific integrated circuits) can significantly outperform other processors, with a much higher computational throughput and lower power consumption. Often being massively produced, ASICs take advantage of economies of scale to lower their production price, yet much of these savings are offset by high design and verification costs. Some popular ASICs targeted at edge AI applications include the Google Edge TPU [21] and Ascend 310 AI processor [22]. There are also merging ASIC technologies such as in-memory computing chips [23] and neuromorphic chips [25].

Development Tools & Frameworks. Many design automation tools and frameworks have been developed for edge AI development, such as: the TensorFlow Lite [26] and the Arm NN SDK [27] for CPUs, Nvidia TensorRT [28] for GPUs, Intel OpenVINO [29] for heterogeneous edge devices, the Xilinx Edge AI Platform [30] for embedded-CPU-based FPGAs, and the Apache TVM [31] for CPUs, GPUs, and specialized ASICs.

## 3 ENABLING METHODOLOGY OVERVIEW

The widespread adoption of edge AI across different domains is currently limited by its challenging development process, which requires novel design methodologies. In this section, we discuss the general problem setup of edge AI by introducing prevailing applications and models, development challenges of edge AI technologies, and then provide an overview of enabling methodologies.

### 3.1 Applications and Challenges

**Applications.** Fig. 2 provides a brief summary of prevailing edge AI applications with their most common inputs, models, and optimization objectives. In particular, one commonly accelerated class of models, GNNs, have gained more attention in recent years. There is also a growing need for trustworthy, private, and secured edge application developments.

The diagram in Fig. 3 illustrates a typical AI system, spanning from the cloud server, edge server, to the end-to-end edge devices, with a typical latency requirement of 1ms, 10ms, 100ms, respectively [32]. Three use cases at the edge are presented. The left set of edge devices are environmental and health sensors that collect at the edge and process data at nearby edge servers to reduce the memory footprint and computation. This is an example of edge offloading, and the most important design metrics are often low-power and...
robustness. The middle set of devices are cameras for crime prevention and traffic monitoring, which may require edge training and edge inference to adaptively adjust the current detection targets. Edge offloading may also be necessary to obtain higher quality results. The key design metrics with connected cameras are often privacy and trustworthiness. Finally, the rightmost devices are autonomous vehicles that involve edge training, inference, and offloading. In this case, accuracy and computation latency are more important for making safe decisions on the road.

Challenges. To successfully design and deploy solutions for those applications, many challenges must be overcome. The largest challenge is achieving high performance under strict device constraints, which include limited computing capability, memory capacity, and power budget. For instance, the battery life for a personal drone is only 20 to 30 minutes, where only a small portion of power (less than 5%) can be allocated for computing and processing system. Another challenge is the complexity of the application at scale. Large-scale AI applications contain numerous edge nodes, e.g., a smart city may contain millions of surveillance cameras and sensor nodes. In addition, with complexity comes heterogeneity. An IoT application may contain largely different devices with varying resources, computing capability, memory capacity, and power budgets.

3.2 Design Methodology Overview

Driven by the broad applications and challenges, edge AI technologies are largely empowered by rapidly improving design methodologies. The development and deployment stack for edge AI contains multiple layers: high-level software development, model training, compiler, and low-level hardware deployment. Their design methodologies can be summarized into two categories, single-layer specialization and cross-layer co-design:

Specialization Methodologies:

1) Training: low-precision and on-device training methods, to develop lightweight AI models and enable on-device training.
2) Software: edge-oriented inference algorithm design methods, to assure high-quality algorithms.
3) Hardware: accelerator design methods, to achieve low latency and low power.
4) Benchmarking, automation, and design space exploration (DSE): to effectively evaluate and improve design quality as well as productivity.

Co-design Methodologies:

1) Software/hardware co-design: mutually specialized software model and hardware accelerator, to simultaneously deliver accurate models and accelerators.
2) Software/compiler co-design: software model design with compiler customization, to enable efficient on-device execution.
3) Compiler/hardware co-design: specialized hardware architecture and the supporting compiler and programming library, to deliver efficient accelerators with efficient executions.

In the following sections, we provide a comprehensive review of related works based on their dominant design methodology: specialization (Sec. 4) or co-design (Sec. 5). Moreover, in Fig. 5 we analyze the effectiveness of these methodologies and demonstrate their benefits, discuss our observations, and provide insight where possible. By summarizing related works from various layers and scopes all together, we indicate potential optimization opportunities that can further contribute to high-quality and flexible edge AI solutions.

4 SPECIALIZATION METHODOLOGIES

Highly specialized designs and technologies are the foundations of successful edge AI development and deployment. Fig. 5 provides several representative examples for edge training, software development, and hardware deployment. For on-device training, one important idea is to intelligently “skip” uncritical operations to pursue energy, latency, and memory reduction (Fig. 5(a)). For software development, in addition to model compression and pruning, adaptive inference is a promising technique where different models are dynamically chosen based on varied task requirements (Fig. 5(b)). For hardware deployment, especially FPGAs and ASICs, there are multiple levels of specialization, from the architectural level to the gate level (Fig. 5(c)).

4.1 Low-precision and On-device Training

Low-precision and on-device edge training can be optimized by varying different components, such as training algorithm, data type, optimizer. For instance, E2-Train and FracTrain aim to reduce on-device training energy from the algorithmic level. E2-Train proposes stochastic mini-batch dropping, selective layer update, and sign prediction; FracTrain proposes to gradually increase the precision of activations, weights, and gradients. Other works propose different data type formats during training, HFP8 proposes a hybrid FP8 format that uses different floating point formats during forward and backward propagation,
achieving negligible accuracy degradation. Ultra-4bit [37] further reduces the bit-width down to 4-bit by proposing adaptive gradient scaling to deal with the insufficient data range and resolution in quantized gradients. HALO [38] proposes a practical meta-optimizer dedicated to resource-efficient on-device adaptation by introducing a new regularizer that reduces data size or training iterations to reach a specified accuracy. To reduce the memory footprint on edge devices during fine-tuning, TinyTL [39] proposes freezing the weights and only learns the bias modules.

Recently, Federated Learning (FL) [40][41] has emerged as a promising distributed training paradigm at the edge. Yang et al. [42] provide a comprehensive survey on FL, so we omit the detailed discussions in this paper.

**Observations and Insights.** Various works of on-device training can be potentially combined to achieve better performance. For example, TinyTL may be seamlessly integrated into other training algorithms for fine-tuning, while FracTrain and Ultra-4bit may be complementary to each other as they both exploit progressive scaling for gradients.

Notably, most novel training techniques require specific hardware support. For example, both HPF8 and Ultra-4bit require specially designed floating point units (FPUs); FracTrain assumes BitFusion [43] architectures to support dynamic precision, but there is still no dedicated training hardware. While Wang et al. [24] propose an MRAM-based process in-memory accelerator for floating point DNN training, more training hardware design is expected.

### 4.2 Software Design

Powerful AI applications require increasingly more computing resources, which complicates their deployment on edge devices. Specialized software models, including compact and hardware-aware model design, compression, and adaptive inference, are essential to building edge systems that perform under strict constraints.

#### 4.2.1 Compact Model Design

Many works focus on directly designing lightweight AI models, each of which applies different methods for sparsifying the model. These include the SqueezeNet [44], MobileNet family [45][47], the ShuffleNet family [48][49], and ChannelNets [50]. SqueezeNet aggressively reduces the number of channels through $1 \times 1$ convolutions, while MobileNet decomposes the standard convolution into a depthwise separable convolution followed by a $1 \times 1$ point-wise convolution. ShuffleNet reduces the convolution complexity through channel grouping, while ChannelNets further proposes channel-wise, group channel-wise, and depth-wise separable channel-wise convolutions.

More recently, other works also suggest model structures specifically optimized for efficient inference. EEG-TCNet [51] proposes a temporal convolutional network (TCN) that achieves impressive accuracy while requiring few trainable parameters. HadNet [52] proposes a Hadamard variant of the ShuffleNet [48], which more efficiently mixes channel information. Further, BFT [53] extends this line of research and uses the butterfly transform to perform channel fusion, finding increased performance especially in very small networks.

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**Fig. 5:** Examples of specialization methodologies: on-device training, software development, and hardware deployment.
4.2.2 Hardware-aware Model Design

In contrast to handcrafted models by machine learning experts, a more recent approach is neural architecture search (NAS) to automatically design the model architecture to achieve outstanding performance. Extended from compact model designs, the work SqueezeNext \([54]\) proposes a new family of SqueezeNet-like architectures, whose designs were guided by simulation results on a neural network accelerator. MNasNet \([55]\) targets on-device latency within its NAS objective, leading to execution speedup on edge devices such as mobile phones. Similarly, MobileNetV3 \([67]\) proposes hardware-aware NAS accompanied by the NetAdapt \([55]\) algorithm.

Most recently, SkyNet \([57]\) uses a different bi-directional DNN design approach with a comprehensive understanding of the hardware constraints, demonstrating its effectiveness by winning the System Design Contest for low power object detection in the 56th IEEE/ACM Design Automation Conference (DAC-SDC). Besides computer vision, hardware-aware NAS also demonstrates success in natural language processing (NLP) tasks. For example, a recent work HAT \([58]\) proposes hardware-aware transformers that exploit NAS to discover efficient models on various devices.

Observations and Insights. The great success of NAS and hardware-aware NAS suggests that it could be a promising tool to assist future AI edge designs. For example, NAS has been applied to defend against adversarial attacks \([59]\) and ensure secure inference \([60]\). While these works are in their early stage, they reveal a potential solution to edge AI robustness, security, privacy, and trustworthiness.

One disadvantage is that NAS uses a lot of computational resources and power. On the one hand, NAS can be a powerful tool to search for light-weight and compact AI models; on the other hand, the search process itself may have a large carbon footprint \([61]\). Designing environment-friendly NAS algorithms is as important as designing hardware- and environment-friendly models.

4.2.3 Model Compression

Model compression includes a series of techniques to reduce the model size, allowing for lower latency, power, and potential area reduction. Within model compression, quantization has become standard practice in deploying models at the edge. For instance, VecQ \([52]\) introduces a DNN quantization solution, which utilizes a vector loss rather than traditional L2 loss as the quantization objective function to achieve higher model accuracy. Likewise, outlier channel splitting (OCS) \([63]\) devises an extension to existing quantization methods to handle weight outliers to reduce quantization accuracy loss without DNN retraining.

In addition to general model compression methods, several techniques target specific edge devices such as low-power microcontroller units (MCUs). For example, Rusci et al. \([54]\) propose a mixed-precision quantization on microcontrollers, while Capotondi et al. \([55]\) propose an open-source mixed low-precision inference library called CMIXNN for quantized networks on edge MCUs.

4.2.4 Adaptive Inference

Adaptive inference is another promising technology that can effectively reduce the model execution latency and energy consumption. The core idea is to adapt models during inference based on the complexity of the current task. So far, the model adaption happens at least along four common dimensions: number of layers or cascaded models \([66,68]\), number of channels \([69,72]\), input image resolution \([73]\), and computation precision \([74,75]\).

Along the layer dimension, Panda et al. \([66]\) propose a conditional deep learning (CDL) network, which can identify the variability in the difficulty of input instances and conditionally activate the deeper layers of the network. Extended from CDL \([66]\), Jayakodi et al. \([67]\) propose on-the-fly classifier selection: simple classifiers for easy inputs and complex classifiers for hard inputs. Stamoulis et al. \([68]\) propose a systematic approach for hyper-parameter optimization of adaptive CNNs, using Bayesian optimization to determine the number of channels, kernel sizes, and the number of units in the fully connected layers.

Along the channel dimension, SlimNets \([69]\) is an early work that allows the DNN to adjust the number of channels according to on-device benchmarks and resource constraints with switchable batch normalization. LEANets \([71]\) further allows finer energy-accuracy tradeoffs by introducing confidence threshold vectors. The work PareCO \([70]\) proposes varied width multipliers for different layers and pursues Pareto solutions between theoretical speedup and accuracy. The channel gating (CG) \([72]\) uses a base set of channels and a conditional set and determines whether to compute the additional channels based on learnable thresholds.

Instead of changing the model structure, some works focus on the resolution and precision of the model. Adascale \([73]\) proposes to dynamically change the input image resolution to improve both accuracy and speed for video object detection tasks. Precision gating (PG) \([74]\) uses a dual-precision mode for edge inference that dynamically selects which features to run in half and full precision.

Observations and Insights. Adaptive inference is a relatively independent approach, thus could be integrated with other techniques to pursue larger benefits. First, different dimensions of adaptive inference can be jointly considered, such as channel dimension, precision dimension, and layer dimension. Second, NAS techniques may help discover better adaption strategies and network architectures. Third, similar to on-device training, the pre-determined or learned adaption strategy may drift when input data change; therefore, adaptive inference may also require on-line training and adjustment. Adaptive inference can be expected to be combined with software/hardware co-design to improve performance. Hua et al. \([75]\) advances this line of work by proposing an RTL accelerator for channel gating.

4.3 Hardware Deployment

The hardware must also be specialized for edge AI applications. Currently, these applications often use devices from one of the following categories: CPU, GPU, FPGA, and ASIC. Among them, CPU and GPU do not allow users to alter the hardware design, while FPGA and ASIC provide more flexibility so designers can customize the designs to meet particular requirements. FPGA and ASIC designs can both optimize at architectural level, processing element
level, and register level, while ASIC designs can further customize at the gate level.

### 4.3.1 CPU-/GPU-based

Since CPUs and GPUs provide very limited flexibility for designers to alter hardware architecture, most of the deployments focus on software optimizations. Nevertheless, there are opportunities for efficient memory management and power control. The work Q-EEGNet [77] proposes algorithmic and implementation optimizations for EEGNET [78], a compact convolutional neural network (CNN) on an ultrasound power RISC-V based System-on-Chip, to achieve significant speedup and reduction of memory footprint. Di et al. [79] discuss the development of a power management infrastructure based on the Dynamic Voltage and Frequency Scaling (DVFS), significantly saving power without penalty to the execution performance.

### 4.3.2 FPGA-based

With high flexibility of bit-width manipulation and data flow customization, FPGA accelerators are extremely suitable for quantized, sparse, hybrid, or customized neural networks [80-82] with the high-level synthesis (HLS) and automated compilation tools [83-85]. For edge applications, Zhao et al. [85] are the first to study FPGA acceleration for binarized neural networks (BNNs), T-DLA [87] is the first instruction-based accelerator for ternary neural networks (TNNs), and Wang et al. [88] support hybrid low bit-width quantized DNNs. For sparse and hybrid DNNs, Huang et al. [89] propose a configurable inference engine capable of processing different sizes of sparse DNNs, while HybridDNN [90] has a hybrid architecture composed of spatial/Winograd convolution processing elements. Additionally, Carreras et al. [91] present an enriched architectural template supporting efficient TCNs, together with an algorithm for optimal execution/scheduling of data-transfers to boost the implementation performance.

### 4.3.3 ASIC-based

Compared with the other solutions, ASICs usually achieve higher performance, smaller area, and orders of magnitude of better energy efficiency. The DianNao family [92] is an early series of machine learning acceleration chips in academia. Eyeriss [93] is a representative work for reconfigurable CNN acceleration, composed of an array of processing elements (PEs) with a reconfigurable on-chip network. ChewBaccaNN [94] is a recent binary CNN acceleration chip, which especially optimizes at gate-level.

Not limited to DNN designs, accelerators for common operations, such as tensor-based and matrix-based multiplications, are also of great importance. One recent work, Tensaurus [95], is a hardware accelerator capable of both sparse and dense tensor computation and other common mixed sparse-dense matrix operations.

**Observations and Insights.** Efficient hardware designs are the foundation of high-quality edge AI solutions. Almost every design approach requires dedicated hardware consideration, such as low-precision training, quantization, structured or non-structured pruning, hardware-aware model design, and adaptive inference. Ignoring hardware considerations may result in large gaps between theoretical and actual benefits. For example, a study by Ma et al. [96] points out that non-structured pruning without dedicated hardware is even considered harmful. Therefore, hardware design should always be considered when developing the application, and in Section 5 we discuss hardware-related co-design methodologies in detail.

### 4.4 Benchmarking, Design Automation and DSE

Edge AI development requires intensive domain knowledge and engineering efforts. It comes with many optimization parameters that result in an extremely large design space. Second, future edge AI systems bring in scalability problems and make it time-consuming to search for high-quality solutions. Thus, informative benchmarking, design automation, and DSE tools are indispensable for rapid and high-quality edge AI development.

#### 4.4.1 Scalable Benchmarking of Models, SW, and HW

Scalable benchmarking offers many combinations of different design metrics, such as accuracy, performance, power/energy, and cost, that enable quick iteration and evaluation of designs. A recent work, titled MModelScope [97, 98], proposes a scalable benchmark platform mainly for deep learning based workloads. MModelScope supports different combinations of DL models, frameworks, and hardware devices, allows scalable evaluation, and reports informative benchmarking results. On GPU devices, MModelScope further provides an automated analysis tool, called XSP [99], to build an integrated view of various performance-related metrics of workloads across the entire stack. Another recent benchmarking platform is called ML-Commons [100], which provides benchmarking, datasets, and practical innovative ML models.

**Observations and Insights.** An interesting yet challenging future direction is to extend benchmarking platforms to better support edge devices with higher flexibility, such as ASICs and FPGA devices. One major challenge is to incorporate hardware design flexibility while still providing the same level of abstraction for software tools, i.e., when users actively change the target hardware architecture, the benchmarking tools must capture the new features and provide accurate performance reports. Also, the software tools for edge devices are much more diverse than those for servers and clouds, and the commonly accepted software interfaces (such as Tensorflow, PyTorch, and MxNet) and capabilities (such as CUDA, cuBlas, and cuDNN [101]) are still lacking. There are no well-developed profiling and tracing tools for edge devices either, such as VTune [102] for CPUs, and Nsight [103] and CUPTI [104] for GPUs.

#### 4.4.2 Design Automation and Design Space Exploration

Design automation and DSEs can be applied on different devices and platforms including CPUs, FPGAs, ASICs, and System-on-Chips (SoCs). Targeting embedded CPUs, De et al. [105] apply reinforcement learning for DSE at different levels of the software stack to search for optimized solutions. Targeting FPGA platforms, DNNBuilder [15] is a representative automation and DSE tool including RTL
DNN templates, a layer-based pipeline architecture, and an automatic DNN accelerator generator. Meanwhile, the tool LAMDA\textsuperscript{105} speeds up the configuration tuning during FPGA design flow by automatically selecting the configuration options. Targeting both FPGAs and ASICs, AutoDNNChip\textsuperscript{102} first predicts DNN accelerator performance such as area and throughput, applies DSE search for optimal configurations, and then automatically generates synthesizable RTL code. Targeting SoC platforms, Zuo et al.\textsuperscript{108} first present an automated SystemC generation and DSE flow, which converts a subset of C/C++ into a full SystemC description through polyhedral models and generates Pareto-optimal solutions. A follow-up work, named RIP\textsuperscript{109}, is proposed to enable hardware acceleration by utilizing hardware/software partitioning to minimize the overall program latency.

**Observations and Insights.** Design automation and DSE enable highly productive edge AI development by breaking the boundaries between different layers of the development stack, opening more opportunities for co-design without requiring domain-specific knowledge. For example, an automated FPGA\textsuperscript{15} or ASIC development tool\textsuperscript{107} can be directly used by software designers to evaluate their models. Vice versa, a well-established low-precision training and quantization framework can be very helpful for hardware developers. Ultimately, design automation and DSE tools can significantly improve design productivity, contribute to the ecosystem of edge AI, and enable open-source software and hardware development.

5 CO-DESIGN METHODOLOGIES

While specialization for individual design layers has led to accurate and effective Edge AI, optimizing multiple layers concurrently, i.e. cross-layer co-design unleashes more opportunities. In this paper, we summarize three major co-design methodologies, as shown in Fig.\textsuperscript{5} software/hardware, software/compiler, and compiler/hardware. Software/hardware co-design aims at simultaneously designing DL models and accelerators that best accommodate each other (Fig.\textsuperscript{5}(a)). Software/compiler co-design develops specialized models based on compiler features, and meanwhile customizes compiler instructions for efficient execution (Fig.\textsuperscript{5}(b)). Compiler/hardware co-design involves specialized hardware architecture, instruction set extensions, and specialized programming libraries (Fig.\textsuperscript{5}(c)).

5.1 Software/Hardware Co-design

While hardware-aware NAS approaches (in Sec.\textsuperscript{4.2.2}) show promising results, its sequential design methodology limits its effectiveness. During hardware-aware NAS, the hardware accelerator is fixed during NAS but independently optimized afterward. This may result in time-consuming iterations between model and accelerator development, or sub-optimal solutions since the model design does not have sufficient performance feedback from hardware and the hardware deployment does not have a direct impact on model design. Thus, software models and hardware accelerators show additional benefits from being simultaneously designed.

![Fig. 6: Examples of co-design methodologies: software/hardware co-design, software/compiler co-design, and compiler/hardware co-design.](image-url)
Hao et al. [121] highlight the opportunities of simultaneous software model and hardware accelerator co-design with a prototype solution. Following this work, Hao et al. [122] propose the first simultaneous FPGA/DNN co-design framework, including a hardware-oriented bottom-up DNN model design, and a DNN-driven top-down FPGA accelerator design. A similar work called FNAS, proposed by Jiang et al. [123], is a hardware-aware NAS framework that can find an optimal neural network under required FPGA implementation latency through reinforcement learning.

NAIS [124] and EDD [125] further push co-design to a generalized and unified approach, i.e., fully simultaneous neural architecture and implementation co-search, targeting arbitrary hardware platforms. NAIS first proposes a stylized design methodology targeting both FPGAs and GPUs, then it takes autonomous driving as a key use case to demonstrate how such a co-design methodology can impact the autonomous driving industry significantly. Based on NAIS, EDD [125] proposes a fully simultaneous, efficient differentiable DNN architecture and implementation co-search methodology. Targeting ASICs, Yang et al. [126] propose a framework named NASAIC that can simultaneously identify multiple DNN architectures and the associated heterogeneous ASIC accelerators to meet both software accuracy and hardware performance requirements.

Observations and Insights With the great success of software/hardware co-design, we further provide a quantitative comparison to showcase its effectiveness in solving a real edge AI task: a light-weight object detection task on drones. The task comes from the Design Automation Conference System Design Contest (DAC-SDC) [110]. Contestants propose their own object detection models, implement them on either embedded FPGA or GPU, and evaluate them with respect to a common set of metrics, i.e., accuracy, speed, and energy.

Fig. 7 summarizes all the solutions including the years of 2018, 2019, and 2020. The designs located in the bottom-left, such as A, B, and C, are designed by model compression and/or compact model design. The designs locate in the top-right corner, such as J, K, F, H, employ software/hardware co-design and/or aggressive model compression. The figure shows that co-designed models perform better in general. Software/hardware co-design can significantly boost the edge AI solution quality, while applying model compression can further improve the speed and energy efficiency. Further, this figure shows that on average, a well-designed FPGA accelerator (e.g., design H) can outperform GPU (e.g., design J) with respect to energy efficiency while often maintaining the same efficiency.

5.2 Software/Compiler Co-design

While software/hardware co-design has been attracting growing research interest, software/compiler co-design remains largely underexplored. This may be partially because designers are more inclined to treat compilers as well-developed tools that should not be touched. Some recent works [127, 128] address this issue and successfully demonstrate the practicality of software/compiler co-design.

Software/compiler co-design includes PCONV [127], PatDNN [128], and CoCoPIE [129], which tackle model comp-
presssion and compilation simultaneously. During model compression, they focus on structured pruning, guided by pre-determined compiler-friendly patterns (as the example in Fig. 6 (b)). During compilation, they propose efficient compiler code generation, enabling the compilers to maximize or maintain both instruction-level and thread-level parallelism. MCUNet \[130\] is another framework that integrates model design and compiler optimization. It is composed of two components, TinyNAS and TinyEngine; TinyNAS searches for specialized DNNs, while TinyEngine generates specialized code to eliminate instruction and memory redundancy.

5.3 Compiler/Hardware Co-design
Within compiler and hardware co-design, a series of works named PULP \[131\] are among the most important works. PULP stands for open Parallel Ultra-Low-Power processing platform, and it achieves leading energy-efficiency and widely-tunable performance especially suitable for IoT devices. As illustrated in Fig. 6 (c), the PULP family demonstrates three types of specializations in promoting co-design quality: specialized instruction set architecture (ISA) designs, ISA extensions, and specialized programming libraries.

For specialized processor architecture, there are many chip designs in the PULP family, such as PULP v1 to v3 \[132,134\], Mr. Wolf \[135\], and GAP-8 \[136\]. For specialized ISA extensions, the work XpulpNN \[137\] proposes a set of extensions on top of the RISC-V compatible processor architectures for low bit-width quantized DNN executions. For specialized programming library, PULP-NN \[138\] targets a cluster of PULP processors, providing an open-source optimized library to support quantized neural networks. Similarly, the work FANN-on-MCU \[139\] provides an open-source toolkit targeting ARM Cortex-M series and PULP platforms.

Observations and Insights. Given the great success of compiler/hardware co-design, one can expect that this methodology can be extended to other ASIC architectures and FPGAs. For example, High-Level Synthesis (HLS) \[140\] is a behavior-level compiler and programming tool for FPGA and ASIC, which compiles C/C++ directly to hardware description languages such as Verilog. Currently, both parties, the software developers and the FPGA and ASIC designers, see HLS as a black-box tool. Thus, the final hardware quality largely relies on the quality of HLS tools, and the improvements gained from software and hardware may be canceled due to inefficient code transformation and scheduling inside the HLS compiler. Therefore, it is expected that such compilers should also be co-optimized with specialized hardware architecture in the future.

6 CONCLUSIONS AND FUTURE DIRECTIONS
In this paper, we discussed the enabling design methodologies for edge AI spanning the entire development stack, categorized into specialization methodologies and co-design methodologies. The representative single-layer specialization methodologies we discussed include on-device training algorithms, compact and hardware-aware model design, model compression, adaptive inference, and specialized hardware accelerator designs. We elaborated three cross-layer co-design methodologies, software/hardware co-design, software/compiler co-design, and compiler/hardware co-design. Throughout the work, we discussed a few cross-layer co-design opportunities that can boost edge AI solution quality, hoping to inspire future researches in these directions. Meanwhile, we highlight potential future directions for edge AI, hoping to pave the path of edge AI development and attract more research interest.

Robust, Secure, and Private AI. As discussed in Sec. 5.1 the most common design objectives for edge AI are accuracy, latency, energy, and memory, while robustness, security, and privacy issues are still largely underexplored. AI model training often includes data that requires strict privacy, such as faces, fingerprints, biometrics, financials, and medical information. This introduces risks of attackers injecting malicious data to disrupt edge AI functionality, such as attacks in federated learning \[42\]. Likewise, to preserve privacy, the communication between edge and cloud devices needs to be secure. These qualities are necessary for creating practical AI systems that are widely adopted across applications.

Green, Ethical, and Trusted AI.

The increasing computational power of AI systems enables higher accuracies yet introduces potential environmental impacts. Strubel et al. \[61\] showed that modern training of AI models results in a significant amount of carbon emissions (e.g., a large NLP model can emit as much carbon as five cars in their lifetimes.). In addition, existing AI algorithms are vulnerable to biases and errors introduced by human developers or by biased datasets during training. Datasets sometimes include racial, gender, political, or ideological biases, which may result in wrong, unfair, or discriminatory decisions \[141\]. Furthermore, despite the high quality of the existing AI algorithms, the fundamental principles and rationale of the AI outputs are largely unclear to us. This is problematic in the real world where AI algorithms are making critically important decisions. Developing AI technologies that are environmentally-friendly, fair, trustworthy is essential to the widespread adoption of successful AI systems.

Quantum AI with Q-bits. An incredible observation has been made by OpenAI that the amount of compute used in the largest AI training runs has been increasing at an unsustainable rate, doubling every 3.4-months (whereas Moore’s Law had a 2-year doubling period) \[142\]. As a consequence, IBM recently made a statement that future AI systems will require digital bits and Q-bits working in collaboration \[143,144\]. It has been demonstrated that a superconducting quantum processor is able to perform a traditional machine learning classification task \[144\], showing significant potential in using quantum computing for machine learning by exploiting the exponentially large quantum state space. A neural network and quantum circuit co-design framework, QuantumFlow \[145\], has pioneered the study of designing neural network models that are suitable for quantum circuits. Towards this interesting yet challenging new trend of quantum AI, revolutionary design methodologies for software and hardware are required.
Fig. 8: An holistic analysis of representative works from different stages in the development-deploy stack. The performance data are shown in ranges as reported in the proposed solutions. For example, Accuracy: 3.67% ↓~0.95% ↑ represents the range of accuracy changes due to the proposed solution. Due to the different scales and design metrics, the lengths of the bars are normalized categorically (energy efficiency, accuracy, etc.) based on their mean values within the range.
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