Impact of technology scaling on analog and RF performance of SOI–TFET

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Abstract

This paper presents both the analytical and simulation study of analog and RF performance for single gate semiconductor on insulator tunnel field effect transistor in an extensive manner. Here 2D drain current model has been developed using initial and final tunneling length of band-to-band process. The investigation is further extended to the quantitative and comprehensive analysis of analog parameters such as surface potential, electric field, tunneling path, and transfer characteristics of the device. The impact of scaling of gate oxide thickness and silicon body thickness on the electrostatic and RF performance of the device is discussed. The analytical model results are validated with TCAD sentaurus device simulation results.

Keywords: SOI–TFET, tunneling path, drain current, intrinsic gate capacitance, cut-off frequency
Classification numbers: 2.01, 3.00, 3.02, 4.12

1. Introduction

Continuous scaling of metal oxide semiconductor field effect transistor (MOSFET) leads to various short channel effects (SCEs) like drain induced barrier lowering (DIBL), punch-through, threshold voltage roll-off etc. The SCEs result in degradation of the device performance with increase in leakage current \( I_{leak} \) and power dissipation [1, 2]. Many authors developed a number of multi-gate semiconductor on insulator (SOI) MOSFETs (MuG-MOS) having double-gate, tri-gate, pi-gate, gate-all-around structures which address the issues effectively [3–5]. The MuG-MOS device improves the drain current and reduces SCEs significantly. However, subthreshold swing (SS) still remains a concern and it has been reported as a minimum 60 mV/decade in the ideal condition. This is due to the drift–diffusion carrier transport mechanism. Also SS increases due to the downscaling of device dimensions. Increase in SS results high OFF-state current in the sub-threshold region which limits the device performance [6].

Tunnel field effect transistor (TFET) has been proposed by several authors as a potential alternative to MOSFET for low power applications as it exhibits low SS [7–14]. TFET is a gated P–I–N structure that primarily operates in the reverse bias condition and is less dependent on temperature variation [15, 16]. Band-to-band tunneling (BTBT) phenomenon is the major carrier injection mechanism in TFET which limits the SS below 60 mV/decade [8, 9, 11–13]. Also the leakage current is very small in TFET, in the range of femto-amperes due to the reduced lateral electric field at the interface in the off state. Therefore a number of ambipolar TFET models have been reported in recent times to counter the limitation of ON-current and enhance scaling capability [17–22].

In this paper a single gate SOI–TFET analytical model is developed to calculate the tunneling current using nonlocal BTBT phenomena. Here the tunneling process of charge carriers has been realized analytically using initial and final tunneling point. Both the tunneling points play important roles for the estimation of the dc parameters such as SS, ON-current and transconductance. The surface potential profile and electric field characteristics are also derived for the developed model. The effect of scaling gate oxide thickness and Si body thickness on electrostatic and RF performance is extensively studied for 40 nm channel SOI–TFET. Moreover,
2. Analytical modeling

The cross sectional view of n-channel single-gate SOI–TFET model is shown in figure 1 and the supported sentaurus structure with corresponding doping profile is displayed in figure 2. The structure is designed on a thin buried oxide (BOX) layer which reduces the short-channel effect and improves current drive capability. The source and drain regions are highly doped with p-type and n-type impurity of concentration 10^{20} \text{ cm}^{-3} respectively. However the channel region is made up of intrinsic material which is lightly doped of the order of 10^{16} \text{ cm}^{-3}. The potential across the box region is assumed to be zero due to small thickness of the layer. For the above model, the thickness of the box layer (t_{box}), oxide layer (t_{ox}) and rectangular silicon body (t_{si}) are 2 nm, 2 nm and 10 nm, respectively, and the length of source/drain regions are taken as 30 nm each. Aluminum with work-function 4.2 eV has been used as the gate contact.

2.1. Electrostatic analysis

The potential profile \( \varphi(x, y) \) in the channel region of the single gate SOI–TFET is governed by two-dimensional Laplace’s equation [11]

\[
\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} = 0.
\]  

(1)

Here the effect of electron space charge has been neglected due to the light doping nature of intrinsic channel. The potential distribution in the channel can be further realized by the 2nd order polynomial distribution [11]

\[
\varphi(x, y) = A_0(x) + A_1(x)y + A_2(x)y^2,
\]  

(2)

where \( A_0, A_1 \) and \( A_2 \) are the x-dependent coefficients of the potential distribution along the channel. The surface potential \( V_s(x) \) is the potential profile along the x-axis at the gate–channel interface which plays a crucial role in the analysis of tunneling path and drain current

\[
\varphi(x, y)|_{y=0} = V_s(x).
\]  

(3)

The required boundary conditions in the channel region for the realization of surface potential are defined as follows: potential at the source–channel interface

\[
\varphi(0, y) = V_{b1},
\]  

(4)

potential at the channel–drain interface

\[
\varphi(L, y) = V_{ds} - V_{b1},
\]  

(5)

electric flux along the x-axis at the gate–channel interface

\[
\left. \frac{\partial \varphi(x, y)}{\partial y} \right|_{y=0} = \frac{V_s(x) - V_{gs} + V_{FB}}{t'_{ox}},
\]  

(6)

electric flux along the x-axis at the channel–BOX interface

\[
\left. \frac{\partial \varphi(x, y)}{\partial y} \right|_{y=t_{si}} = 0,
\]  

(7)

where \( V_{b1} \) is the built-in-potential at the source/drain interface, \( V_{gs} \) is the gate-to-source voltage, \( V_{ds} \) is the drain-to-source voltage, \( V_{FB} \) is the flat-band voltage and \( t'_{ox} \) is the equivalent oxide thickness. However \( t'_{ox} \) can be expressed as follows

\[
t'_{ox} = \frac{t_{ox} \varepsilon_{si}}{\varepsilon_{ox}}.
\]  

(8)

Here \( \varepsilon_{si} \) is the relative permittivity of silicon and \( \varepsilon_{ox} \) is the relative permittivity of silicon dioxide.

Applying the above boundary conditions, we obtained the coefficients \( A_i(x) \):

\[
A_0(x) = V_s(x),
\]  

(9)

\[
A_1(x) = \frac{V_s(x) - V_{gs} + V_{FB}}{t_{ox}},
\]  

(10)

\[
A_2(x) = -\frac{1}{2t_{si}} \frac{V_s(x) - V_{gs} + V_{FB}}{t'_{ox}}.
\]  

(11)

Substituting these coefficients, we found following 1D differential equation

\[
\frac{d^2 V_s(x)}{dx^2} - \varphi V_s(x) = V_{FB} - V_{gs},
\]  

(12)
where
\[
\alpha^2 = \frac{1}{t_0 t_{ox}}. \tag{13}
\]

The solution of equation (12) can be expressed as
\[
V_x(x) = C_0 e^{\alpha x} + C_1 e^{-\alpha x} - (V_{FB} - V_{gs}), \tag{14}
\]
where
\[
C_0 = \frac{1}{2 \sinh(\alpha l)} \left[ -V_{bi} \left( 1 + e^{-\alpha l} \right) + (V_{FB} - V_{gs}) \left( 1 - e^{-\alpha l} \right) + V_{ds} \right], \tag{15}
\]
\[
C_1 = \frac{1}{2 \sinh(\alpha l)} \left[ -V_{bi} \left( 1 + e^{\alpha l} \right) + (V_{FB} - V_{gs}) \left( 1 - e^{\alpha l} \right) + V_{ds} \right]. \tag{16}
\]

The tunneling of charge carriers occur at the region of high electric field near the source–channel interface created by applying positive gate voltage [23, 24]. So the electric field along x-axis is crucial for the calculation of the tunneling volume and can be determined by differentiating the surface potential. The lateral electric field along the x-axis is found to be
\[
E_x = -\frac{\partial \phi(x, y)}{\partial x} = -C_0 \alpha e^{\alpha x} + C_1 \alpha e^{-\alpha x}. \tag{17}
\]
Similarly, the electric field along y-axis is
\[
E_y = -\frac{\partial \phi(x, y)}{\partial y} = -A_1(x) + 2y A_2(x). \tag{18}
\]

2.2. Drain current analysis

The energy band diagram of n-channel SOI–TFET in both OFF-state and ON-state are shown in figures 3 and 4. When the applied gate voltage is zero, no BTBT of charge carriers occur due to the wide potential barrier between the source and channel region. Therefore the device is said to be in OFF-state due to the absence of carriers as shown in figure 3. As positive gate voltage is applied, the potential barrier between source and channel region gets narrower gradually. When the gate voltage exceeds the threshold voltage, the barrier becomes narrow enough to allow tunneling of charge carriers as shown in figure 4. In the ON-state, the conduction band of channel aligns with the valence band of source which enables the charge carriers to tunnel from source to drain [25].

However the charge carriers move to the drain end by the process of drift–diffusion mechanism [11, 12].

Tunneling path is the distance between [l₁, l₂] along the x-axis of the channel and is responsible for BTBT of carriers [24]. When \( x = l₁ \), the conduction band of source and valence band of channel are in-line to each other
\[
V_s(x)|_{x=l_1} = V_s(x)|_{x=0} + \frac{E_g}{q} = V_{bi} + \frac{E_g}{q}, \tag{19}
\]
where \( l_1 \) is defined as the initial tunneling length from the source which indicates the start of BTBT tunneling process and can be evaluated as
\[
l_1 = \frac{1}{\alpha} \ln \left( \frac{Z + \sqrt{Z^2 - 4C_0 C_1}}{2C_0} \right), \tag{20}
\]
where
\[
Z = V_{bi} + \frac{E_g}{q} + (V_{FB} - V_{gs}), \tag{21}
\]
and \( E_g = 1.12 \text{ eV} \) and \( q = 1.6 \times 10^{-19} \text{ C} \).

Similarly the final tunneling length \( l_2 \) indicates the end of the tunneling process and can be calculated as the value of ‘x’ in the channel region at which surface potential is maximum
\[
l_2 = \frac{1}{\alpha} \ln \left( \frac{C_1}{\sqrt{C_0}} \right). \tag{22}
\]

The drain current in the BTBT process can be evaluated by the help of band to band generation rate. The band-to-band generation rate \( G_{\text{BB}}(x, y) \) for single gate TFET is defined as...
\[ G_R(x, y) = A_k E_{avg} F^{-1} E_v e^{-B_k/E_{ox}}, \] (23)

where \( A_k \) and \( B_k \) are the Kane’s tunneling-dependent parameters having magnitude of \( 9.66 \times 10^{18} \text{ cm}^{-1} \text{V}^{-2} \text{s}^{-1} \) and \( 3.0 \times 10^7 \text{ V cm}^{-1} \), respectively [11]. Similarly the type of BTBT tunneling phenomena is defined by a constant \( D \). In Kane’s model, \( D = 2 \) represents direct tunneling process and \( D = 2.5 \) for indirect tunneling. However in this model, we have taken the value of \( D \) as 2 for the direct BTBT tunneling phenomena. The average electric field is expressed as \( E_{avg} = \frac{E_x}{l_{path}} \), where \( l_{path} \) is the length of tunneling path varying from \( l_1 \) to \( l_2 \) as shown in figure 4.

The tunneling current can be determined by integrating the band to band generation rate over the tunneling volume [24]

\[ I_D = q \int G_R(x, y) \, dx \, dy \] (24)

or

\[ I_D = q \int^{l_2}_{l_1} \int^{E_v}_{E_g} A_k E_{avg} E_v e^{-B_k/E_{ox}} \, dx \, dy. \] (25)

It is assumed that tunneling process mainly takes place along the channel in the \( x \)-axis [24]. Therefore the lateral electric field has been considered in the drain current analysis. We have

\[ I_D = q \int^{E_v}_{E_g} \int^{l_2}_{l_1} \frac{E_x}{l_s} A_k E_{avg} \, dx \, dy. \] (26)

In the interval from \( l_1 \) to \( l_2 \) along the channel, the exponential term is dominant in comparison with the polynomial term \( 1/x \). Integrating the exponential term in the equation (26), we get

\[ I_D = q A_k l_s \frac{E_x}{q} \left( -C_0 \alpha \frac{T_1(x_2) - T_1(x_1)}{\alpha - \frac{B_k q}{E_g}} + C_1 \frac{T_2(x_2) - T_2(x_1)}{\alpha + \frac{B_k q}{E_g}} \right), \] (27)

where

\[ T_1(x) = e^{\frac{-B_k q}{E_g} x}, \] (28)

\[ T_2(x) = e^{\frac{B_k q}{E_g} x}. \] (29)

2.3. Subthreshold swing

The SS is the reciprocal of subthreshold slope which displays the log-linear behavior of MOSFET in the subthreshold region. It also illustrates the drain current dependence on gate voltage in the subthreshold region [10] and can be defined as

\[ \text{SS} = \frac{dV_{gs}}{d \log I_D} = \left( \frac{d \log I_D}{dV_{gs}} \right)^{-1} \]

\[ = \left( -C_0 \alpha \frac{T_1(x_2) - T_1(x_1)}{\alpha - \frac{B_k q}{E_g}} + C_1 \frac{T_2(x_2) - T_2(x_1)}{\alpha + \frac{B_k q}{E_g}} \right)^{-1}, \] (30)

where

\[ \beta = \left( -C_0 \alpha \frac{T_1(x_2) - T_1(x_1)}{\alpha - \frac{B_k q}{E_g}} + C_1 \frac{T_2(x_2) - T_2(x_1)}{\alpha + \frac{B_k q}{E_g}} \right)^{-1} \] (31)

2.4. Transconductance and drain conductance

Transconductance \((g_m)\) is the transfer characteristics of a device which displays the ability to amplify the signal. However TFETs exhibit higher transconductance per bias current compared to the conventional MOSFETs due to its low SS. It is defined as

\[ g_m = \frac{dI_D}{dV_{gs}} \bigg|_{V_{ds}=cont} = E_v A_k l_s \frac{\alpha \beta}{2 \sinh (\alpha l)} \] (32)

and therefore

\[ g_m = \frac{E_v A_k l_s \alpha}{2 \sinh (\alpha l)} \left( \frac{T_1(x_2) - T_1(x_1)}{\alpha - \frac{B_k q}{E_g}} \left( 1 - e^{-\alpha l} \right) \right. \] (33)

\[ + \frac{T_2(x_2) - T_2(x_1)}{\alpha + \frac{B_k q}{E_g}} \left( 1 - e^{\alpha l} \right). \]

Here the effect of gate bias on shortest tunneling distance is neglected. Similarly drain conductance \((g_d)\) is one of the important parameter which measures the current driving
capability of the device and is expressed as

\[
g_d = \left. \frac{d|D|}{dV_{ds}} \right|_{V_{gs}=\text{const}} = -\frac{E_g A_1 t_0 \alpha}{2 \sinh (\alpha l)} \left( \frac{T_1(x_2) - T_1(x_1)}{\alpha - \frac{B_k q}{E_g}} \right) + \frac{T_2(x_2) - T_2(x_1)}{\alpha + \frac{B_k q}{E_g}}. \tag{34}
\]

3. Results and discussion

The device simulation has been performed using sentaurus, a 2D numerical simulator from Synopsis [27] and the results are compared with the analytical results to check their accuracy and validity. Here the non-local path BTBT model is considered as the primary carrier transport mechanism. Shockley–Read–Hall recombination model, quantum potential model, and bandgap narrowing concentration models are also considered for the simulation. The analog/RF performance of the simulated device has been extensively investigated through the variation of Si body thickness and gate oxide thickness.

3.1. Analog performance

Figure 5 illustrates the surface potential distribution of the n-channel SOI–TFET along the channel for constant drain voltage. As the gate voltage increases, the potential at the middle of the channel increases due to the enhanced gate-control over the channel. But the potential remains unchanged at the source and drain end due to the boundary condition at the interface as shown in figure 5. For constant \(V_{ds}\) and \(V_{gs}\), it has been observed that the electrostatic potential varies linearly near to the source and drain interface and remain almost constant in the middle of the channel/silicon body.

The variation of surface potential along the channel for different drain voltages is shown in figure 6. The potential increases across the drain region with the increase in drain voltage which is due to the higher influence of drain bias in the drain–channel interface. This indicates a small amount of DIBL effect due to large change in \(V_{ds}\). However the variation of drain voltage does not affect the slope of the surface potential at the source end and hence the tunneling current is independent of drain bias.

Figure 7 shows the electric field variation along the channel for different gate voltages. It has been observed that the magnitude of electric field along the x-axis is maximum at the source–channel junction. This high electric field allows the charge carriers to tunnel from the source to the drain end. However the magnitude becomes zero at the middle of the channel due to the zero-slope of surface potential.
The initial tunneling length as a function of gate voltage for different silicon body thickness and gate oxide thickness are displayed in figures 8 and 9. As the gate bias increases beyond the threshold, the tunneling of charge carriers starts along the x-axis, because of the increase of gate control on the channel. As the silicon body thickness scaled down from 10 nm to 6 nm, the impact of gate voltage on the source-channel interface increases. This results in a reduction in initial tunneling length of BTBT process. Similarly with the increase in gate oxide thickness from 2 nm to 4 nm, the impact of gate bias on the channel region reduces. This is due to the reduction in the capacitive coupling effect between gate and channel. So the initial tunneling length reduces with reduction in the oxide thickness for constant drain voltage.

Figures 8 and 9 illustrate the variation of tunneling path \((l_2-l_1)\) versus gate voltage for different silicon body thickness and oxide thickness respectively. It has been observed that the tunneling path reduces significantly with the increase in gate voltage. This is due to reduction in both the initial tunneling length \((l_1)\) and final tunneling length \((l_2)\). As the thickness of silicon body and oxide layer decreases, the tunneling path also reduces as depicted in figures 10 and 11.

Figures 10 and 11 display the variation of initial tunneling length versus gate voltages for different silicon body thickness.

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Figures 12 and 13 display the drain current characteristics for different gate metal work-functions. As gate voltage increases beyond threshold, the current increases exponentially at constant drain bias. This is due to higher gate influence on the tunneling volume. Similarly the drain current changes linearly for small value of drain bias because of the improvement in tunneling of charge carriers and remains saturated for higher value of drain voltage.

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The effect of variation of metal work-function on the drain current has also been illustrated in figures 12 and 13. As the work-function of gate metal decreases, the initial tunneling length reduces significantly due to the lowering in flat-band voltage. This improves the amount of band bending at the source interface and thus surges the tunneling volume. Thus the drain current along x-axis improves for metal contact having lower work-function. The same improvement can be seen in p-type TFET for higher work-function. Similarly the transconductance of the device improves for lower work-function at higher gate voltage due to the reduction in gate over-drive voltage \((V_{gs}-V_{th})\) as displayed in figure 14.

Figures 15 and 16 show the effect of scaling of silicon body thickness and gate oxide thickness on drain current for constant drain voltage. With reduction in \(t_{si}\), the influence of gate on the channel region improves. This leads to increase in the tunneling probability of charge carriers across the source interface and provides higher drain current. Also the threshold condition has been achieved for low gate bias due to reduced channel barrier height. Similarly the higher drain current is obtained with low gate oxide thickness as the capacitive coupling between gate and channel increases.
Figures 17 and 18 show the transconductance as a function of gate voltage for different silicon body thickness and gate oxide thickness. As $t_{si}$ is scaled from 10 nm to 6 nm, the transconductance of the device improves due to increase in tunneling volume in the channel. This illustrates the higher current drive capability of gate at low $t_{si}$. Similarly figure 18 displays improved transfer characteristics of the model for low $t_{ox}$ because of large capacitive effect.

Figure 19 shows the variation of the output characteristics of the proposed model for different gate voltages at constant $t_{si}$ and $t_{ox}$. However the drain conductance increases linearly versus gate voltage for low $V_{ds}$ and gets saturated to minimum value for higher drain voltage. This indicates the negligible effect of drain voltage on the BTBT tunneling process.

The effect of scaling of silicon body thickness and gate oxide thickness on the electrical parameters such as threshold
voltage. ON-current and OFF-current has been illustrated in table 1. The comparison of the above electrostatic parameters has been performed with work-function of 4.2 eV and drain voltage of 1 V. It is concluded from the above statistics that the scaling of gate oxide thickness and silicon body thickness result reduction in ambipolar leakage current and threshold voltage. Similarly the drain current and transconductance also improves with the down-scaling of $t_{si}$ and $t_{ox}$. But the improvement may not extend for very small value of $t_{si}$ and $t_{ox}$ due to the introduction of hot carrier effect and punch-through effect.

3.2. RF analysis

The radio-frequency performance of the proposed model is analyzed in this section. The section includes analysis of gate capacitance ($C_{gg}$) and cut-off frequency ($f_t$) for different drain voltages. The above parameters play significant role in the analysis of RF performance of the device. However the investigation has also been extended for different values of $t_{si}$ and $t_{ox}$. The performance degradation in RF analysis is primarily due to the influence of bias dependent parasitic capacitance $C_{gg}$ which is the approximate combination of drain capacitance ($C_{gd}$) and source capacitance ($C_{gs}$).

The effect of the variation of drain voltage on intrinsic gate capacitance of the model for constant silicon body and gate oxide thickness has been displayed in figure 20. It has been observed that the intrinsic capacitance $C_{gg}$ increases continually as the gate voltage goes beyond threshold ($V_{gs} > V_{th}$). The increased capacitive effect is due to the combined enhancement of both drain capacitance ($C_{gd}$) and source capacitance ($C_{gs}$). However low drain voltage indicates high value of $C_{gg}$ due to low threshold voltage. This is
because of improved coupling between gate and source and increase of the potential barrier at the drain side.

However higher $C_{gg}$ limits the cut-off frequency of the device. Cut-off frequency is one of the important figures of merit to represent the device performance and defined as the frequency at which we get unity current gain. The magnitude of cut-off frequency is expressed as [28]

$$f_t = \frac{g_m}{2\pi C_{gg}} \quad (35)$$

Figure 21 illustrates the variation of cut-off frequency of the device as a function of gate voltage for different drain voltages. With the increase in drain voltage, the higher mobility has been achieved for the device and thus transconductance improves. Also the intrinsic gate capacitance ($C_{gg}$) reduces with the increase in $V_{ds}$. Low capacitive effect and high $g_m$ lead to higher cut-off frequency of the device.

The effect of scaling of silicon body thickness and gate oxide thickness on unity gain cut-off frequency of the device at constant drain voltage is depicted in figures 22 and 23, respectively. As the silicon body thickness scaled down from 10 nm to 6 nm, the gate controllability on the channel improves. However this increases the mobility of charge carriers across the source interface and provides higher transconductance. The cut-off frequency for $t_{si} = 6$ nm improves by leaps and bounds due to the reduced gate capacitance and high transconductance. Similarly the cut-off frequency improves significantly with the reduction of gate oxide from 4 nm to 2 nm. The scaling of $t_{ox}$ develops high

| $t_{si}$ (nm) | $t_{ox}$ (nm) | $V_{th}$ (V) | $I_{on}$ ($\mu A\, \mu m^{-1}$) | $I_{off}$ ($\mu A\, \mu m^{-1}$) | $g_m$ ($S\, \mu m^{-1}$) |
|---------------|---------------|--------------|-------------------------------|-------------------------------|--------------------------|
| 10            | 4             | 1.39         | $7.142 \times 10^{-11}$       | $7.639 \times 10^{-19}$       | $1.19 \times 10^{-10}$   |
| 10            | 3             | 1.32         | $5.879 \times 10^{-10}$       | $1.298 \times 10^{-20}$       | $2.01 \times 10^{-9}$    |
| 10            | 2             | 1.27         | $7.065 \times 10^{-9}$        | $9.463 \times 10^{-21}$       | $1.57 \times 10^{-8}$    |
| 8             | 2             | 1.26         | $1.830 \times 10^{-8}$        | $1.994 \times 10^{-20}$       | $2.01 \times 10^{-8}$    |
| 6             | 2             | 1.25         | $5.312 \times 10^{-8}$        | $4.006 \times 10^{-20}$       | $2.61 \times 10^{-7}$    |

$t_{si}$: silicon body thickness, $t_{ox}$: gate oxide thickness, $V_{th}$: threshold voltage, $I_{on}$ and $I_{off}$: ON-and OFF-current, $g_m$: transconductance.
different values of gate oxide thickness. In this paper, a 2D drain current model for n-channel SOI TFET has been proposed. The DC performance of the model such as surface potential, electric field, drain current and transconductance are found to be in agreement with the sentaurus simulated results. DC and RF analysis of the present model has been carried out by scaling down the device dimensions like gate oxide thickness and Si body thickness. There is a significant improvement of drain current, and unity gain cut-off frequency has been observed for the scaling of $t_{si}$ from 10 nm to 6 nm and $t_{ox}$ from 4 nm to 2 nm.

4. Conclusion

In this paper, a 2D drain current model for n-channel SOI–TFET has been proposed. The DC performance of the model such as surface potential, electric field, drain current and transconductance are found to be in agreement with the sentaurus simulated results. DC and RF analysis of the present model has been carried out by scaling down the device dimensions like gate oxide thickness and Si body thickness. There is a significant improvement of drain current, and unity gain cut-off frequency has been observed for the scaling of $t_{si}$ from 10 nm to 6 nm and $t_{ox}$ from 4 nm to 2 nm.

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Figure 23. Variation of cut-off frequency versus gate voltage for different values of gate oxide thickness.