An efficient coding algorithm for general Framed Pulse Width Modulations

Soon-Won Kwon, Hyun-Min Bae

Abstract—This paper introduces a new coding algorithm for Framed Pulse Width Modulation (FPWM). The proposed algorithm requires 93% fewer look-up tables (LUTs) than the previous FPWM coding algorithm and increases a bitrate by 25%. The proposed algorithm is compatible with general FPWM with various frame lengths and pulse width resolutions. Theoretical bitrates and the sizes of LUT required for coding various FPWMs are also provided. The MATLAB simulation demonstrates the proposed FPWM signal which contains 14-bit information in 8 UI frame length, showing 75% higher bitrate than the NRZ signal with the same baud rate. The decoding algorithm restores the original bit without any bit error and validates the proposed FPWM and its coding scheme.

I. INTRODUCTION

Despite the ever-increasing data rate demands, the channel capacity of copper cables suffers fundamental bandwidth limitation. Such limited bandwidth is leading the industry to adopt PAM4 modulation for data rates above 56Gbps.[1-8] However, tight linearity requirements for multi-level signaling techniques make it difficult to meet low BER conditions and consequently impede rapid application of PAM4 in various industries.[3,4,6-8] To alleviate this linearity issue, a Framed Pulse Width Modulation (FPWM) technique was introduced[9]. The FPWM transmits bit data by modulating the edge phase of a binary signal. However, the previous FPWM coding scheme, which relies solely on a look-up table (LUT), is not suitable for more complex FPWMs with higher bitrates, since the size and complexity of LUT increase exponentially as the frame length increases. Therefore, this paper introduces a new FPWM scheme and its coding algorithm that reduces the size of the LUT by 93% and increases the bitrate by 25% compared to the previous FPWM. The proposed algorithm can be applied to general FPWMs with various frame lengths and pulse width resolutions.

The remainder of this paper is organized as follows: Section II.A explains the concept of general FPWM and its theoretical bitrate. Section II.B discusses the encoding and decoding algorithms for the proposed FPWM scheme. In Section III, MATLAB simulation results are presented to verify the feasibility of proposed algorithms. Section IV is the conclusion.

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II. GENERAL FRAMED PULSE-WIDTH MODULATIONS (FPWM)

A. Theoretical bitrate calculation

FPWM encodes binary data into the edge phases of transmitted signals. As shown in Fig.1, symbols with edges at K different phases within 1 UI period are denoted as ‘S1’, ‘S2’, ‘S3’, ..., ‘SK’, respectively. If there is no signal transition, the symbol is denoted as ‘S0’. The rising or falling state of the symbol depends only on the state of the previous symbol and is independent of the encoded data. The symbols in Fig.1 are combined into one frame of m UI length. If the number of possible combinations of symbol arrays in a frame is N, then the maximum number of binary data that can be carried by one frame is

\[
\left\lfloor \log_2 N \right\rfloor
\]

Since only an integer number of bits can be encoded, the floor function \( \lfloor \cdot \rfloor \) is applied.

The pulse width of the FPWM signal must be at least 1 UI to maintain the same bandwidth as NRZ. This constraint on the minimum pulse width requires some rules between adjacent symbols as shown in Fig.2. If a single pulse created by combining two consecutive symbols has a width equal to or larger than 1 UI, the next symbol after ‘SK’ must be ‘S0’~ ‘SK’. However, all symbol can be placed after ‘S0’ since the pulse width is already greater than 1 UI. Therefore, only ‘Sx’ and ‘S0’ symbols allow all kinds of symbols to be connected behind. On the other hand, FPWM signals are encoded on a frame-by-frame basis, meaning that complete independence between frames must be guaranteed. This independence can be achieved by setting the last symbol of the frame to ‘Sx’ or ‘S0’ only.

Fig. 1. K+1 FPWM symbols with pulse width resolution K
Current Symbol | Next Symbol | Current Symbol | Next Symbol | Current Symbol | Next Symbol | Current Symbol | Next Symbol | Current Symbol | Next Symbol
---|---|---|---|---|---|---|---|---|---
$S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$ | $S_K$
$S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$ | $S_{K-1}$
... | ... | ... | ... | ... | ... | ... | ... | ... | ... 
$S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$ | $S_4$
$S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$ | $S_3$
$S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$ | $S_2$
$S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$ | $S_1$
$S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$ | $S_0$

Forbidden transition 

Forbidden transition Examples (K=4)

<1 UI | <1 UI | <1 UI | <1 UI | <1 UI
---|---|---|---|---
S3 | S3 | S2 | S2 | S2
1 2 3 4

Fig. 2. The coding rules for proposed FPWM

Fig. 3. The bitrate calculation for proposed FPWM

The number of possible symbol arrays in a frame satisfying these rules is derived as shown in Fig. 3. The component value $V_{m,q}$ of vector $V_m$ denotes the number of possible combinations of $m$ symbol arrays starting with symbol $'S_q'$. For example, if the frame length is 1 UI, only 'S0' or 'SK' symbol is possible. Therefore,

$$V_1' = \begin{bmatrix} 1 & 0 & 0 & \ldots & 0 & 1 \end{bmatrix}. \quad (1)$$

According to the rules in Fig. 2, the number of symbol arrays of length $m$ starting with 'S0' is the sum of the number of symbol arrays of length $m-1$ starting with 'S0' ~ 'SK'. Then, the relationship between $v_{m,q}$ and $v_{m-1,q}$ can be expressed as follows.

$$v_{m,q} = \begin{cases} \sum_{h=0}^{K} v_{m-1,h} & \text{if } q > 0 \\ \sum_{h=0}^{K} v_{m-1,h} & \text{if } q = 0 \end{cases} \quad (2)$$

Eq. (2) can be expressed in a matrix form, and it is possible to derive $V_m$ from $V_1$ as follows.

$$V_m = M v_{m-1,K}$$

The total number of symbol arrays that can be represented as one frame of FPWM with $m$ UI length is

$$N = \sum_{h=0}^{K} v_{m,h}$$

so that $\lfloor \log_2 N \rfloor$ bits can be encoded into the frame. The normalized bitrate of the
proposed FPWM scheme with the frame length of \( m \) UI and pulse width resolution of \( K \) is calculated as follows.

\[
\text{bitrate (bit / UI)} = \frac{\log_{2} \left( \sum_{h=0}^{K-1} v_{m,h} \right)}{m}
\]  

(4)

The normalized bitrate means the number of bits encoded per 1 UI. The normalized bitrates of the NRZ, PAM4, and the previously published FPWM scheme are 1, 2, and 1.33 bit/UI, respectively.\(^9\) Fig.4 plots the normalized bitrates of the proposed FPWMs at various frame lengths and pulse width resolutions. It shows that the bitrate of the proposed FPWM at \( m = 6 \) and \( K = 4 \) is about 25% higher than the previous FPWM with the same frame length and pulse width resolution.

Fig. 4. The calculated bitrates of the proposed FPWMs with various Frame lengths and pulse width resolutions

B. Coding algorithm

The encoder converts the input binary data into its corresponding FPWM symbol array. The array composed of \( K+1 \) different symbols (‘S0’ ~ ‘S4’) can be regarded as a numeral system of radix \( K +1 \) with Least Significant Digit (LSD) on the right and Most Significant Digit (MSD) on the left. Table 1 shows an example of FPWM code with \( K = 4 \) corresponding to the input binary data. If the coding rule in Fig.2 is not applied, the encoder structure can be represented simply as a binary to base-5 converter as shown in Fig.5. Conversion starts sequentially from the MSD. At each step, the input value is quantized to five levels. The result of the quantization in blue is then removed from the input, and the residual value passes to the next step for further quantization. Each step performs quantization independently of each other, enabling pipeline operation.

| Decimal | binary | FPWM (w/o coding rule) | FPWM (with coding rule) |
|---------|--------|------------------------|------------------------|
| MSD→LSB | MSD→LSD | MSD→LSD | MSD→LSD |
| 0       | 00…0000 | S0…S0S0S0S0 | S0…S0S0S0S0 |
| 1       | 00…0001 | S0…S0S0S0S1 | S0…S0S0S0S4 |
| 2       | 00…0010 | S0…S0S0S0S2 | S0…S0S0S0S6 |
| 3       | 00…0011 | S0…S0S0S0S3 | S0…S0S0S0S8 |
| 4       | 00…0100 | S0…S0S0S0S4 | S0…S0S0S0S9 |
| 5       | 00…0101 | S0…S0S0S0S5 | S0…S0S0S0S5 |
| 6       | 00…0110 | S0…S0S0S0S6 | S0…S0S0S0S6 |
| 7       | 00…0111 | S0…S0S0S0S7 | S0…S0S0S0S7 |

Table I

Fig. 5. Block diagram of binary to base-5 converting algorithm

However, if the coding rule in Fig.2 is applied, the forbidden transition should be excluded. Fig.6 shows the modified encoder structure. According to the coding rule, the number of possible symbols in the next digit depends on the quantization result of the current digit. However, by subtracting the quantization result from the input value by the quantity indicated by blue in Fig.6, it is possible to perform independent pipeline encoding operation for each digit. This independent pipeline operation dramatically reduces the size of the LUT for encoding and enables unified FPWM coding theory for various frame lengths and pulse width resolutions.

Fig. 6. Block diagram of encoding algorithm for FPWM with \( K = 4 \)
The quantized results at each stage of the encoder are converted into FPWM symbols stored in the LUT. Each symbol requires $K$ bits to represent $K$ different edge phases. The symbols stored in the LUT have only rising edges. However, the rising and falling edges must alternate. Therefore, in order to transfer continuous FPWM symbols, the current symbol must be inverted to have the edge direction opposite to that of the previous symbol. The information of the edge direction of the current symbol is transmitted to the subsequent symbol while continuously toggling. This information transfer is performed between frames as well as symbols within a frame. However, if the current symbol is ‘$S_0$’, it means that there is no edge, so the information of the edge direction is transmitted to the next symbol without toggling. Then, the TX driver sends the connected FPWM symbols to the RX side.

The proposed FPWM with the same frame length ($m=6$ UI) and pulse width resolution ($K=4$) can encode 10 bits in one frame. Therefore, as shown in Fig.6, the input bit-depth of the LUT for one digit is $5(=K+1)$, and the LUT output is $14$ bit ($=n+K$). A total of six LUTs are required, from MSD to LSD. If the size of LUT is estimated as a product of input bit-depth and the number of output bits, the LUT size for the previous encoding scheme is $6144(=2^9 \times 24)$. However, the size of the LUT required for the proposed coding algorithm is $420(=5 \times 14 \times 6)$, which is about 93% smaller than the conventional FPWM. Since the LUT is the biggest bottleneck of the previous coding method, the significantly reduced LUT in size enables more complex FPWM coding with higher bitrates.

The decoding algorithm converts the input FPWM symbol array into the original binary data, and it can be implemented by inverting the encoding algorithm as shown in Fig.8. Therefore, the decoder only requires much smaller LUT than conventional methods. This decoding procedure can be understood as an operation of adding all the vector components $v_{ni}$ below the row corresponding to the received symbol in each $V_m$ vector, as shown in the lower part of Fig.8.

The simulated results at each stage of the encoder are converted into FPWM symbols stored in the LUT. Each symbol requires $K$ bits to represent $K$ different edge phases. The symbols stored in the LUT have only rising edges. However, the rising and falling edges must alternate. Therefore, in order to transfer continuous FPWM symbols, the current symbol must be inverted to have the edge direction opposite to that of the previous symbol. The information of the edge direction of the current symbol is transmitted to the subsequent symbol while continuously toggling. This information transfer is performed between frames as well as symbols within a frame. However, if the current symbol is ‘$S_0$’, it means that there is no edge, so the information of the edge direction is transmitted to the next symbol without toggling. Then, the TX driver sends the connected FPWM symbols to the RX side.

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This spectrum imbalance of FPWM is due to different probabilities between symbols. Table II shows the probabilistic ratio between the symbol ‘S0’ and other symbols for various FPWMs. As the pulse width resolution increases, the total number of available symbols also increases, relatively lowering the probability of ‘S0’. Since all symbols except ‘S0’ have edges, an increase in the probability of these symbols boosts the mid-frequency components of the FPWM signal.

### TABLE II

| K  | m | # of symbols in all possible arrays \((m \times N)\) | \# of S0(no edge) | \# of S1,S2,S3,S4,S5,S6,S7,S8\(\times K\) |
|----|----|-----------------------------------------------|-----------------|---------------------------------------------|
| 1  | 8  | 2048                                          | 1024 (50%)      | 1024 (50%)                                  |
| 2  | 8  | 12776                                         | 5911(46.3%)     | 6865(53.7%)                                 |
| 3  | 8  | 47168                                         | 20636(43.8%)    | 26532(56.2%)                                |
| 4  | 8  | 131944                                        | 55296(41.9%)    | 76648(58.1%)                                |

* FPWM with \(K=1\) is equivalent to NRZ.

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**Fig. 10.** Simulated eye-diagram and power spectral density

**IV. CONCLUSION**

This paper proposes a general FPWM scheme and its coding algorithm. The proposed FPWM scheme shows 25% higher bitrate than the previous FPWM at the same frame length and the pulse width resolution. Meanwhile, its encoding and decoding algorithms require 93% less LUT size than the prior art. The simple coding algorithm derived from the unified FPWM theory enables designing and implementing other complex FPWMs having different frame lengths and pulse width resolutions. The FPWM encoder and decoder with longer frame length than previous FPWM were simulated as an example in MATLAB. In the simulation, 14bit was coded in 8UI to have bitrate close to PAM4. The received FPWM signals were successfully decoded without bit error, and their logical feasibility was verified.