Modeling of interelectrode parasitic elements of V-groove SiC MOSFET

Rui Zhou¹a), Michihiro Shintani², Masayuki Hiromoto¹, and Takashi Sato¹

¹ Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University
Yoshida-hon-machi, Sakyo, Kyoto 606-8501, Japan

² Graduate School of Information Science, Nara Institute of Science and Technology
8916-5 Takayama-cho, Ikoma, Nara 630-0192, Japan

a) paper@easter.kuee.kyoto-u.ac.jp

Received November 20, 2017; Revised February 28, 2018; Published July 1, 2018

Abstract: We propose a physics-based model of interelectrode parasitic elements of a V-groove SiC power MOSFET with buried p-layers. The proposed model considers the voltage dependence of parasitic resistances and capacitances on the basis of the observations through technology computer aided design (TCAD) simulations. The gate-voltage dependence of the body diode is also modeled in accordance with device physics. Through comparison with measurement results, it is demonstrated that the proposed model successfully reproduces both I-V and C-V characteristics. The transient behavior using a buck converter is also well reproduced.

Key Words: SiC power MOSFET, V-groove structure, device modeling, SPICE simulation

1. Introduction

Silicon carbide (SiC) is one of the most promising materials to realize high frequency switching converters. SiC devices can tolerate high-voltage and high-temperature operations with low power loss compared to silicon (Si) devices that have been a mainstream material in power electronics area for a long time [1, 2].

The vertical double-diffused MOSFET (VDMOSFET) structure is widely utilized in high power applications of SiC power MOSFETs. Other structures are also studied to sufficiently elicit the superior property of SiC materials [3, 4]. An example is a V-groove trench structure with buried p-layers [4]. This structure is expected to improve the efficiency of power conversion while maintaining high breakdown voltage. The cross section of the V-groove SiC power MOSFET is shown in Fig. 1. The V-groove structure utilizes high mobility facet and eliminates JFET region at which the on-resistance of regular DMOSFETs becomes high, thereby improving on-resistance of the SiC MOSFETs. In order to prevent from the oxide breakdown to occur, due to the concentration of electric field at the bottom of the trench structure, p-layers are buried in the n⁻ epitaxial layer [4].

In order to effectively design high power converters using the V-groove SiC power MOSFETs, design
optimization using a circuit simulator is an important step [5]. Obviously, an accurate device model of the power MOSFET is crucially important because simulation accuracy is strongly dependent on the accuracy of the simulation model. Parasitic components, such as resistance, capacitance, and body diode of the MOSFET, are particularly important since they significantly affect the switching behavior of the circuit as well as the power loss in the device.

In this paper, we propose accurate models of the parasitic resistance, capacitance, and body diode of the V-groove SiC MOSFET with buried p-layers. While the buried p-layer is useful to prevent from the oxide breakdown, voltage dependence of the parasitic components becomes complicated with it. Through technology computer aided design (TCAD) simulations [6], we show that the voltage dependence of the parasitic resistances and capacitances in V-groove MOSFETs are important to construct accurate models. In addition, the body diode is also modeled on the basis of the device physics [7]. The proposed models are integrated into the charge-based transistor model [8]. In our experiments using a V-groove SiC power MOSFET, we observed good agreements between measurement results and simulations in I-V and C-V characteristics. Good match in transient behaviors using a buck converter is also confirmed.

The remainder of this paper is organized as follows. Section 2 provides the analysis of the V-groove SiC power MOSFET through TCAD simulation. Section 3 proposes the parasitic resistance and capacitance model based on the observation of the TCAD simulation and device physics. In Section 4, we present experimental results that validate the accuracy of the proposed model against measurement data. Finally, we conclude this paper in Section 5.

2. TCAD simulation

A V-groove SiC power MOSFET uses \{033\} facets for its channel. This orientation is known to yield high carrier mobility [9]. The absence of the depletion region in the drift layer also eliminates the parasitic resistance associated with the JFET region, which contributes to realize much lower on-resistance than the VDMOSFET structure. The V-groove power MOSFET in [4] utilizes embedded p-layers to mitigate high electric field, which is mostly concentrated at the bottom of the gate terminal. In this section, through TCAD simulations, bias dependence of the parasitic components in the V-groove power MOSFET is analyzed.

2.1 TCAD model

Figure 2 shows a 2-D TCAD simulation model for V-groove MOSFET. The dimensions and material properties are obtained according to the published article [4]. The dimension and doping concentration of the embedded p-layer, which are not described in [4], are determined referring to [10–13]. Current flows upwards, from the bottom (drain) to top (source), in the figure. In the drift region, a buried p-layer can be found.

2.2 Current characteristics

Figure 3 shows simulated $I_{DS}$-$V_{DS}$ characteristics of the V-groove power MOSFET. The gate-source voltage, $V_{GS}$, is altered from 6 V to 10 V by a 0.5 V step, and $V_{DS}$ is altered from 0 V to 20 V. This
model reproduces MOSFET operation with a threshold voltage of about 7 V. The drain current in Fig. 3 is five orders magnitude smaller than that of the actual devices because the normalized channel width of 1 μm is used in the simulation.

Figure 4 shows the current path of the power MOSFET at the bias voltage of \( V_{GS} = 10 \) V. The four profiles from left to right shows current density of the MOSFET at \( V_{DS} = 5, 10, 15, \) and \( 20 \) V. In Fig. 4, the current flow starts from the drain terminal, then goes through the n-drift2 region, right hand side of the buried p-layer, the device-channel, and finally reaches the source terminal. Current is concentrated toward the channel due to the depletion layer developed around the buried p-layer. The current path becomes narrower as \( V_{DS} \) becomes higher and depletion region expands toward the region below the channel. This narrowing of the current path strongly affects current characteristic of the device, and hence it needs to be considered to improve the model accuracy.
2.3 Capacitance characteristic

Parasitic capacitance models are also very important since they determine transient response of the device. Parasitic capacitance of a MOSFET consists of gate-source capacitance $C_{GS}$, drain-source capacitance $C_{DS}$, and gate-drain capacitance $C_{GD}$.

Figure 5 shows source-drain voltage dependence of the parasitic capacitances of a V-groove SiC power MOSFET, at $V_{GS} = 0$ V and $V_{DS} = 0–50$ V. Again, the capacitance shown in this figure is smaller than the measurement results by about five orders magnitude. This difference owes to the lack of thickness direction in the TCAD model.

In the figure, $C_{GS}$ is mostly flat except for the small increase at about $V_{DS} = 0$ V. $C_{DS}$ and $C_{GD}$ both have a kink at the bias voltage of $V_{DS} = 18$ V. These kinks are considered specific to the V-groove structure device, as they are never observed in the capacitances of planar SiC power MOSFETs. In order to model switching behavior of the power MOSFET, we model the kink in the parasitic capacitances.

TCAD simulations are conducted to investigate how the kinks are formed. Figure 6 shows carrier density profiles of a V-groove MOSFET at $V_{GS} = 0$ V and $V_{DS} = 5, 10, 15, and 20$ V. As the drain voltage $V_{DS}$ increases, depletion region grows downwards from the p-n junction formed between the p-base region and the n-drift region. The depletion region of the p-n junction and that around the buried p-region touch with each other at about $V_{DS} = 15$ V, forming a large depletion region beyond that bias voltage. This is the mechanism that the kink in the parasitic capacitances appears only for the V-groove MOSFET with buried p-layer.

3. Modeling of parasitic elements

According to the observations obtained using the TCAD simulations, we propose new models for the interelectrode parasitic resistance and capacitance of the V-groove SiC power MOSFET. In addition, we also propose a parasitic body diode model based on the device physics.
3.1 Resistance model

Figure 7 shows the cross section of the V-groove MOSFET with buried p-layers. The on-resistance $R_{ON}$ of the V-groove MOSFET structure is defined by considering the current flow in Fig. 4. Resultant resistance components are summarized in Table I. $R_{source}$ and $R_{drift2}$ are the constant resistances determined by the geometry and physical properties of the V-groove MOSFET. $R_{ch}$ represents the resistance in the MOSFET channel, which is represented by the model equations for the MOSFET current. The resistance components, $R_{acc}$, $R_{buried1}$, $R_{buried1}$, and $R_{drift1}$ are formulated as voltage dependent equations, while the other resistances are defined as constants that are independent of the bias voltages.

According to [1], due to the charge density of accumulation layer, the value of $R_{acc}$ changes as $V_{GS}$ changes:

$$R_{acc} = \frac{1}{W L \mu C_{ox}} (V_{GS} - V_{T0}),$$ (1)

where $W$ and $L$ are the channel length and width, respectively. $C_{ox}$ is the oxide capacitance and $V_{T0}$ is the threshold voltage at the zero bias. Although Eq. (1) is an empirical model, it is useful to predict $R_{acc}$.

$R_{buried1}$ also varies by the horizontal extension of the depletion region of the buried p-layer, which is modeled as

$$R_{buried1} = \frac{\rho H_1}{W(D - \sqrt{\frac{2\varepsilon_{SiC} N_a}{q N_d (N_a + N_d)} (V_{bi} + V_{bx})})},$$ (2)

where $D$, $H_1$, and $\rho$ are the cell width of the MOSFET, the depth of $R_{buried1}$, and the electrical resistivity, respectively. $\varepsilon_{SiC}$ is the permittivity of SiC. $N_a$ and $N_d$ are the acceptor and donor concentrations. $V_{bi}$ is the built-in voltage, and $V_{bx}$ is the voltage at the buried layer in the horizontal direction. $q$ is the elementary charge.

$R_{buried2}$ is also expressed as
Parasitic capacitances of the V-groove SiC power MOSFET with the p-buried layers.  

Extension of the depletion layer.

Table II. Components of the parasitic capacitance.

| Capacitance | Description                                      |
|-------------|--------------------------------------------------|
| (a) $C_{\text{conc}}$ | Inter electrode capacitance                      |
| (b) $C_{\text{ox}}$ | Gate oxide capacitance                           |
| (c) $C_{\text{pbd}}$ | Depletion capacitance of the p-body layer        |
| (d) $C_{\text{buried}}$ | Depletion capacitance of the buried p-layer       |
| (e) $C_{\text{gs mos}}$ | MOS capacitance at the p-body                    |
| (f) $C_{\text{gd mos}}$ | MOS capacitance at the drift layer               |

\[
R_{\text{buried}2} = \int_0^{H_2} \frac{\rho h}{A + h \frac{B - A}{H_2}} dh,  
\]

where $A$ is the distance between two depletion regions in between p-buried layers, in which current flows as shown in Fig. 8. $H_2$ is the depth of $R_{\text{buried}2}$ and it is modeled as a function of the voltage of the buried p-layer in the vertical direction $V_{\text{by}}$:

\[
H_2 = \sqrt{\frac{2 \varepsilon_{\text{sic}} N_a}{q N_d (N_a + N_d)}} (V_{\text{bi}} + V_{\text{by}}).  
\]

Using Eq. (4), Eq. (3) is rewritten as

\[
R_{\text{buried}2} = \int_0^{H_2} \frac{\rho h}{A + h \frac{B - A}{H_2}} dh = \frac{2 \varepsilon_{\text{sic}} N_a}{q N_d (N_a + N_d)} (V_{\text{bi}} + V_{\text{by}}) \frac{\rho}{D - A} (\log D - \log A) - D \log D + D + A \log A - A.  
\]

As a result, $R_{\text{buried}2}$ changes linearly depending on $V_{\text{by}}$.

The on-resistance $R_{\text{ON}}$ of the V-groove MOSFET is considered as the series connection of all the above parasitic resistances. Thus, by rearranging the sum of the parasitic resistances by using the parameters $N_1$–$N_5$, $R_{\text{ON}}$ is expressed as

\[
R_{\text{ON}} = \frac{N_1}{(V_{\text{GS}} - V_{\text{T0}})} + \frac{N_2}{N_3 - \sqrt{(V_{\text{DS}} + V_{\text{bi}})}} + N_4 V_{\text{DS}} + N_5.  
\]

3.2 Capacitance model

According to Section 2, a kink appears in the $V_{\text{DS}}$ dependence of $C_{\text{DS}}$ and $C_{\text{GD}}$ as shown in Fig. 5 due to the extension of the depletion regions of the buried p-layer $C_{\text{buried}}$ and the n-epitaxial layer $C_{\text{pbd}}$. The proposed model considers these kinks. Figures 9 and 10 illustrate the extension of the depletion layers. The components of the parasitic capacitances shown in Fig. 9 are summarized in Table II.
3.2.1 Gate-source capacitance $C_{GS}$
The gate-source capacitance $C_{GS}$ is related to $C_{con}$, $C_{ox}$, and $C_{gs,mos}$, and it is given as

$$C_{GS} = C_{con} + \frac{C_{ox}}{C_{gs,mos}} = C_{GS}(0). \quad (7)$$

$C_{gs,mos}$ is the nonlinear MOS capacitance formed at the channel surface. However, the change of $C_{gs,mos}$ is much smaller than $C_{DS}$ and $C_{GD}$ [14]. Hence, $C_{GS}$ is modeled as a constant $C_{GS}(0)$ in the proposed model.

3.2.2 Drain-source capacitance $C_{DS}$
$C_{DS}$ is composed of $C_{pbd}$ and $C_{buried}$. The $V_{DS}$ dependency of its depletion region $C_{pbd}$ is expressed as

$$C_{pbd} = \frac{\varepsilon \varepsilon_0 N_{ap} N_d}{2(N_{ap} + N_d)(V_{DS} + V_{bi})}, \quad (8)$$

where $N_{ap}$ is the acceptor concentration in the p-body layer. The depletion capacitance of the buried p-layer $C_{pbd}$ extends concentrically. This equation is simplified as

$$C_{pbd} = C_{pbd}(0) \sqrt{1 \over (V_{DS} + V_{bi})}, \quad (9)$$

where the terms that are independent of $V_{DS}$ are replaced with $C_{pbd}(0)$.

Let the radii of the extension by depletion of the PN junction to the directions of the p-layer and drift layer be $r_1$ and $r_2$, respectively. Then, $C_{buried}$ can be written as

$$C_{buried} = 2\pi W \varepsilon \varepsilon_0 \log {r_2 \over r_1}. \quad (10)$$

We denote $2l_p$ as the depth of the buried p-layer. The radii $r_1$ and $r_2$ become

$$r_1 = l_{buried} - \sqrt{\frac{2 \varepsilon \varepsilon_0 (V_{DS} + V_{bi}) N_d}{q(N_{ab} + N_d) N_{ab}}}, \quad (11)$$

$$r_2 = l_{buried} + \sqrt{\frac{2 \varepsilon \varepsilon_0 (V_{DS} + V_{bi}) N_{ab}}{q(N_{ab} + N_d) N_d}}. \quad (12)$$

Here, $N_{ab}$ is the acceptor concentration in the buried p-layer. Similarly to Eq. (9), Eq. (10) is represented using the constant parameter $C_{buried}(0)$ as

$$C_{buried} = C_{buried}(0) \log \left(\frac{r_2}{r_1}\right). \quad (13)$$

The proposed model approximates $C_{DS}$ by connecting the two capacitance equations depending on the bias voltages:

$$C_{DS} = \begin{cases} 
C_{pbd} & (V_{DS} < V_{conn,ds}) \\
C_{pbd} + C_{buried} & (V_{DS} \geq V_{conn,ds}), 
\end{cases} \quad (14)$$

where $V_{conn,ds}$ is the voltage at which the depletion regions are connected.

3.2.3 Gate-drain capacitance $C_{GD}$
$C_{GD}$ is the series capacitance of the oxide capacitance under the gate terminal $C_{ox}$ and MOS capacitance $C_{gd,mos}$ at the surface [5]. In the proposed model, $C_{gd,mos}$ is approximated as a PN junction [14]. Hence, $C_{gd,mos}$ is computed in a similar way to the $C_{DS}$ calculation using Eq. (9) by replacing $(C_{ds}(0), N_{bi}, V_{DS})$ with $(C_{gd}(0), N_{ed}, V_{GD})$, respectively. Then, $C_{GD}$ is derived as
When $V_{GD} = V_{conn, gd}$, the MOS capacitance $C_{gd, mos}$ connects with the capacitance of the buried p-layer. The body diode is structurally formed between the source and drain terminals. In [7], it is reported that the built-in voltage $V_{bi}$ of the PN junction of the body diode fluctuates depending on the gate-source voltage $V_{GS}$. When $V_{GS}$ is positive, electrons in the p-region are induced to the gate oxide. Consequently, potentials of the p-region and the p+ region increase as shown in Fig. 11. Due to this fact, the carrier density of the p-region and p+ region changes as

$$n_{p,p} = n_{n,n} = n_{i}^{2} \exp \left( \frac{qV_{pn}}{kT} \right),$$

(16)

where $k$ is the Boltzmann’s constant, $T$ is the absolute temperature, and $n_{i}$ is the intrinsic carrier density. $p_{p}$, $n_{p}$, $n_{n}$, and $p_{p}$ denote the hole density of the p region (majority carrier), the electron density of the p region (minority carrier), the electron density of the n region (majority carrier), and the hole density of the n region (minority carrier), respectively. $V_{pn}$ is the voltage at the PN junction. $V_{bi}$ is calculated by the carrier density of the PN junction as

$$V_{bi} = \frac{kT}{q} \log \left( \frac{p_{p}}{p_{n}} \right).$$

(17)

Let us consider the case where $V_{bi}$ is reduced by increasing the minority carrier of the p+ region depending on $V_{GS}$. From the above equations, $V_{bi}$ can be written as

$$V_{bi} \propto \frac{n_{i}^{2}}{n_{p,p}} V_{pn}.$$ 

(18)

In addition, since a part of the gate voltage $V_{GS}$ also contributes to the PN junction voltage $V_{pn}$, $V_{pn}$ is expressed as $V_{pn} = cV_{GS}$, where $c$ is a linear coefficient. From the above derivation, $c$ can be written as

$$c \propto \frac{n_{i}^{2}}{n_{p,p}}.$$ 

(19)

The body diode current $I_{diode}$ considering $V_{GS}$ dependency becomes

$$I_{diode} = I_{0} \left( \exp \left( \frac{qV_{SD} - V_{R} + c_{0}V_{GS}}{nkT} \right) - 1 \right).$$

(20)

where $V_{SD}$ is the source-drain voltage, which is the negated drain-source voltage $V_{DS}$, $I_{0}$ is the saturation current, and $n$ is the correction value of the recombination current. $V_{R}$ is the voltage drop due to the parasitic resistance $R_{d}$ in the drift layer. In the proposed diode model, $R_{d}$ is modeled as a constant resistance.
4. Experiments
In order to verify the proposed model, the simulation results are compared with the measurement results obtained by using a V-groove SiC MOSFET.

4.1 Setups
4.1.1 Model implementation
The proposed model is implemented as a transistor model using Verilog-A hardware description language. In the transistor model, channel current $I_{\text{ch}}$ is modeled based on the charge-based model [15]. Parasitic components are integrated as shown in Fig. 12. A commercial circuit simulator [16] is used to calculate the I-V, C-V, and transient characteristics.

Model parameters of the V-groove SiC power MOSFET including the body diode are determined by a simulated annealing (SA) method [17]. We use the evaluation function for the SA as

$$f = \sqrt{\frac{1}{N} \sum (I_{\text{meas}} - I_{\text{sim}})^2},$$

where $N$ is the total number of measurement data, $I_{\text{meas}}$ and $I_{\text{sim}}$ are the measurement and the simulation results at voltages $(V_{\text{GS}}, V_{\text{DS}})$, respectively.

4.1.2 Measurement of static characteristics
The I-V, C-V, body diode characteristics of the V-groove SiC power MOSFET are measured by using a power MOSFET curve tracer B1505A [18]. For the I-V characteristics, drain-source current $I_{\text{DS}}$ is measured by sweeping $V_{\text{DS}}$ from 0 V to 20 V with a 0.2 V step and $V_{\text{GS}}$ from 6 V to 10 V with 0.5 V steps. For the C-V characteristics, capacitances between three terminals ($C_{\text{GS}}$, $C_{\text{GD}}$, and $C_{\text{DS}}$) are measured for $V_{\text{DS}}$ from 0 V to 500 V with 1 V steps and $V_{\text{GS}} = 0$ V. Finally, for the diode characteristics, current flown through the diode is measured for $V_{\text{DS}}$ from 0 V to −20 V and $V_{\text{GS}}$ from 0 V to 20 V with a 1 V step.

4.1.3 Measurement of transient characteristics using a buck converter
The transient characteristics are evaluated using a synchronous rectification buck converter. The synchronous rectification buck converter has advantages of higher efficiency operation, faster response, and lower noise in comparison to the asynchronous ones [19, 20]. The circuit diagram of the synchronous rectification buck converter is shown in Fig. 13. M1 and M2 transistors are SiC power MOSFETs. The MOSFET M1 works as a switching element and M2 works as a diode. $V_{\text{GS1}}$ and $V_{\text{GS2}}$ are the gate voltages of M1 and M2, respectively, each of which controls the corresponding MOSFET. M1 controls the amount of energy supplied from the input to the inductor $L$, and M2 performs a rectification operation to boost the output voltage, which is different from the input voltage.

A square wave with a frequency of 100 kHz, an amplitude of 0–18 V for peak-to-peak, and duty ratio of 50% is applied for $V_{\text{GS1}}$, and the inverted waveform is applied for $V_{\text{GS2}}$. However, there is a possibility that $V_{\text{GS1}}$ and $V_{\text{GS2}}$ become simultaneously high due to the transition time of the rising

![Fig. 12. Overview of the transistor model with the proposed parasitic components model.](image-url)
and falling edges of $V_{\text{GS1}}$ and $V_{\text{GS2}}$. When the two power MOSFETs M1 and M2 are simultaneously turned on, the power source is short-circuited to the ground through M1 and M2. In order to avoid this, dead time of 500 ns is given to $V_{\text{GS2}}$, yielding 40% duty ratio with 55% delay offset from $V_{\text{GS1}}$.

The gate resistance of the SiC power MOSFET, $R_g$, is set to 33, 47, and 68 \(\Omega\). We use $C = 330 \mu\text{F}$ for the smoothing capacitor, and $R_L = 10 \Omega$ for the load resistance. The parasitic resistance and capacitance of the inductor $L$ is shown in a right-top box in Fig. 13. In addition, we add 20 nH parasitic inductor at each terminal of the MOSFETs to consider the parasitics of TO-247 package and its socket.

The function of the buck converter designed for 80 V input and 40 V output is confirmed through circuit simulation and measurement. From the simulation, it takes about 30 ms to obtain a stable output of the buck converter. Therefore, we set the simulation time to 50 ms with 1 ps time steps in the following experiments.

### 4.2 Experimental results

#### 4.2.1 I-V characteristic

Figure 14 shows the measurement and simulation results of the I-V characteristics. The simulation results of the proposed model well agrees with the measurement results both in the linear and saturation regions. Particularly better agreements are found around $V_{\text{GS}} = 7$ V, which is close to the threshold voltage of the device. The mean squared error between the measurement and simulation results is 0.21 A. These results show that the proposed model well reproduces the current characteristic of the device.

#### 4.2.2 C-V characteristics

Figure 15 shows the measurement and simulation results of the parasitic capacitances, $C_{\text{GS}}$, $C_{\text{DS}}$, and $C_{\text{GD}}$. The simulation results of all the three capacitances well agree with the corresponding measurement results. The mean squared error of $C_{\text{GS}}$ is 4.5 pF. This result supports our assumption that the capacitance model of $C_{\text{GS}}$ can be modeled by a constant value. The mean squared errors of
4.2.3 Body diode model

Figure 16 shows the measurement and simulation results of the body diode current characteristics. The simulation results well agree with the measurement results, and the mean squared error is 0.45 A. It is shown that the turn-on voltage of the body diode decreases as the gate voltage $V_{GS}$ increases. Particularly, the resistance of the body diode significantly increases around $V_{DS} = -3$ V. In the region of $V_{DS} < -3$ V, the simulation result slightly differs from the measurement. The difference is considered to be caused by the difference of the parasitic resistance parameters in the body diode.

4.2.4 Transient characteristic

The measurement and simulation results of the transient analysis using the buck converter are shown in Figs. 17 and 18. Each graph shows three waveforms with different gate resistances of $R_G = 33$, 47, and 68 Ω. The transient waveforms of $V_{GS}$, $V_{DS}$, and $I_{DS}$ obtained by the proposed model again agree well with the measurements, except that only the measurement waveforms contain large ringing noise that is not reproduced in the simulation. In power converters, high frequency ringing noise is caused by the resonance of the parasitic elements in the current loop. In our circuit simulation, the part of the parasitic component models, such as those with the device package and with inductor are included. However, those associated with printed circuit board (PCB) wires or with decoupling
capacitors are not modeled accurately. Noise waveforms of this type of converters are known sensitive to small parasitic elements, and the accurate modeling of parasitic elements as in [21, 22] is one of our future works.

5. Conclusion
In this paper, a novel transistor model that accurately considers parasitic components for V-groove SiC power MOSFETs. Through TCAD simulations, the sources of drain parasitic resistance and that of the kinks in parasitic capacitances are analyzed and accurate models are developed. In addition, a body diode model that considers gate-voltage dependence of the V-groove SiC power MOSFET with buried p-layers is proposed. Through the experiments, we found that the current, capacitance, and body-diode characteristics matched well with the measurement results. The transient simulation
using a synchronous buck converter also well reproduced measurement waveform.

Acknowledgments
This work was partially supported by JST Super Cluster Program and NEDO Cross-ministerial Strategic Innovation Promotion Program. The authors also gratefully acknowledge the support of Sumitomo Electric Industries, Ltd.

References

[1] B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer Science & Business Media, 2008.

[2] T. Kimoto and J.A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*, Wiley-IEEE Press, 2014.

[3] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, and Y. Yokotsuji, “High performance SiC trench devices with ultra-low ron,” in *IEEE International Electron Devices Meeting Technical Digest*, pp. 26.5.1–26.5.3, 2011.

[4] T. Hiyoshi, K. Uchida, M. Sakai, M. Furumai, T. Tsuno, and Y. Mikamura, “Gate oxide reliability of 4H-SiC V-groove trench MOSFET under various stress conditions,” in *Proceedings of International Symposium Power Semiconductor Devices and ICs*, pp. 39–42, 2016.

[5] Y. Nakamura, M. Shintani, K. Oishi, T. Sato, and T. Hikihara, “A simulation model for SiC power MOSFET based on surface potential,” in *Proceedings of International Conference on Simulation of Semiconductor Processes and Devices*, pp. 121–124, September 2016.

[6] R.W. Dutton and A.J. Strojwas, “Perspectives on technology and technology-driven CAD,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 12, pp. 1544–1560, 2000.

[7] A. Elhami Khorasani, M. Griswold, and T. Alford, “Gate-controlled reverse recovery for characterization of LDMOS body diode,” *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1079–1081, 2014.

[8] C.C. Enz and E.A. Vittoz, *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design*, John Wiley & Sons, 2006.

[9] Y. Saitoh, T. Hiyoshi, K. Wada, T. Masuda, T. Tsuno, and Y. Mikamura, “4H-SiC V-groove trench MOSFETs with the buried p+ regions,” *SEI Technical Review*, no. 80, pp. 75–80, 2015, [Online available] http://global-sei.com/technology/tr/bn80/pdf/80-16.pdf.

[10] M. Furno, F. Bonani, and G. Ghione, “Calibration of 4H-SiC TCAD models and material parameters,” *IEEE Trans. Electron Devices*, vol. 55, pp. 3347–3353, 2008.

[11] R. Kraus and A. Castellazzi, “A physics-based compact model of SiC power MOSFETs,” *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5863–5870, August 2016.

[12] G.D. Licciardo, L.D. Benedetto, and S. Bellone, “Modeling of the SiO2/SiC interface-trapped charge as a function of the surface potential in 4H-SiC vertical-DMOSFET,” *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1783–1787, April 2016.

[13] J.A. Schrockand, B.N. Pushpakaran, A.V. Bilbao, W.B. Ray, E.A. Hirsch, M.D. Kelley, S.L. Holt, and S.B. Bayne, “Failure analysis of 1200V/150A SiC MOSFET under repetitive pulsed overcurrent conditions,” *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1816–1821, March 2016.

[14] N. Phankong, T. Yanagi, and T. Hikihara, “Evaluation of inherent elements in a SiC power MOSFET by its equivalent circuit,” in *Proc. European Conf. Power Electronics and Applications*, pp. 1–8, 2011.

[15] R. Zhou, M. Shintani, M. Hiromoto, and T. Sato, “A Charge-Based SiC Power MOSFET Model Considering On-State Resistance,” *NOLTA*, pp. 177–180, November 2016.

[16] SIMetrix Technologies Ltd., *SIMetrix SPICE and Mixed Mode Simulation*, 2012.

[17] S. Kirkpatrick, C.D. Gelatt, and M.P. Vecchi, “Optimization by simulated annealing,” *Science*, vol. 220, no. 4598, pp. 671–680, 1983.
[18] Keysight Technologies, Inc., *B1505A Power Device Analyzer/Curve Tracer*, 2015.

[19] X. Zhou, M. Donati, L. Amoroso, and F.C. Lee, “Improved light-load efficiency for synchronous rectifier voltage regulator module,” *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826–834, 2000.

[20] S. Deuty, “Optimizing transistor performance in synchronous rectifier buck converters,” in *Proceedings of IEEE Applied Power Electronics Conference and Exposition*, pp. 675–678, 2000.

[21] Z. Chen and D. Boroyevich, “Modeling and simulation of SiC MOSFET fast switching behavior under circuit parasitics,” in *Proceedings of International Conference on Grand Challenges in Modeling & Simulation*, pp. 352–359, 2010.

[22] J. Noppakunkajorn, D. Han, and B. Sarlioglu, “Analysis of high-speed PCB with SiC devices by investigating turn-off overvoltage and interconnection inductance influence,” *IEEE Transactions on Transportation Electrification*, vol. 1, no. 2, pp. 118–125, 2015.