Cascode Cross-Coupled Stage High-Speed Dynamic Comparator in 65 nm CMOS

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Abstract—Dynamic comparators are the core of high-speed, high-resolution analog-to-digital converters (ADCs) used for communication applications. Most of the dynamic comparators attain high-speed operation only for sufficiently high input difference voltages. The comparators’ performance degrades at small input difference voltages due to a limited preamplifier gain, which is undesirable for high-speed, high-resolution ADCs. To overcome this drawback, a cascode cross-coupled dynamic comparator is proposed. The comparator improves the differential gain of the preamplifier and reduces the common-mode voltage seen by the latch, which leads to a much faster regeneration at small input difference voltages. The proposed comparator is designed, simulated, and compared with the state-of-the-art techniques in a 65 nm CMOS technology. The results show that the proposed comparator achieves a delay of 46.5 ps at 1 mV input difference, and a supply of 1.1 V.

Index Terms—Cascode cross-coupled pair, dynamic comparator, high-speed analog-to-digital converters (ADCs).

I. INTRODUCTION

Analog-to-digital converters (ADCs) are widely used in various applications due to the increased demand for mixed-signal systems [1]. The comparator, an essential block in ADCs, plays a vital role in determining the speed and accuracy of the ADCs. The performance of an ADC relies on the robustness of the comparator [2], especially for low noise, low-power, and high-speed operations. Dynamic comparators are preferred in low-power and high-speed designs due to their zero static power. They are classified as single-tail (ST) and double-tail (DT) topologies. Various ST circuits are reported to suffer from tradeoffs between energy consumption (EC), offset, and speed [3]. ST topology also suffers from large kickback (KB) noise and requires a large voltage headroom since the input transistors are directly stacked with the latch stage. Due to these drawbacks, the DT configuration is preferred for the design of high-speed comparators [4].

Designing a high-speed comparator that can resolve small input difference voltages while holding on to the high-speed capability over a wide range of common-mode voltage is challenging [5]. The conventional DT comparator reported in [6] has mitigated the drawbacks of the ST comparator. However, it fails to give valid outputs for small input difference voltages. This has a direct impact on the resolution of ADCs. Moreover, at higher common-mode levels, the performance of the conventional DT comparator degrades because the input pair enters the triode region without providing sufficient gain. A dynamic comparator resistant to common-mode variations with the delayed operation of the latch is presented in [7]. However, it requires a large area and suffers from increased KB noise. Furthermore, the insufficient preamplifier gain makes it impractical to use in high-precision ADCs. In the dynamic bias DT comparator presented in [8] the preamplifier partially discharges the drains of the input transistor pair to reduce EC. However, the speed is compromised to attain energy efficiency. To improve the latch regeneration time, a transconductance-enhanced latch stage is presented in [9]. It has the same drawback as the conventional DT comparator in its common-mode performance. Additionally, due to stacking in the latch stage, the delay increases swiftly for lower supply voltages.

Our work targets to reduce the comparator delay by enhancing the preamplifier gain compared to other high-speed DT architectures reported. The performance improvement is achieved by including a cascode cross-coupled pair in the preamplifier stage. The circuit is designed and implemented in a 65 nm CMOS technology with a 1.1 V supply. The proposed technique offers better delay performance throughout the input voltage range, especially at smaller input differences. Also, the cascode cross-coupled pair alleviates the delay degradation at higher common-mode voltages. These advantages make the proposed comparator suitable for high-speed, high-resolution ADCs.

This brief is organized as follows. Section II presents the conventional DT comparator and its operation. The proposed comparator and its delay analysis are provided in Section III. Simulation results and discussions are presented in Section IV, and the conclusion is given in Section V.

II. CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

The conventional DT dynamic comparator has an input stage and a latch stage that have separate tail transistors. Two independent tail currents enable us to optimize the tradeoff between speed, offset, and EC. This topology has fewer transistors stacked [10], making it suitable for low-voltage applications. It also reduces the KB noise due to the isolation between the input transistors and the output nodes.

In the conventional DT, at smaller input difference voltages ($\Delta V_{IN}$), the latch is unable to sense the differential voltage due to the limited differential gain of the preamplifier. The proposed comparator mitigates this drawback by lowering the common-mode voltage and improving the differential voltage at the preamplifier output. This helps the latch to regenerate faster even at smaller $\Delta V_{IN}$.

III. PROPOSED CASCODE CROSS-COUPLED DYNAMIC COMPARATOR

A PMOS cross-coupled pair is employed to increase the differential gain of the preamplifier in [11]. To enhance the performance further, the proposed topology, shown in Fig. 1, introduces a cascode cross-coupled pair made up of $M_1$, $M_4$, $M_{c1}$, and $M_{c2}$. As a result, a higher difference voltage, $\Delta V_{IN}$, is observed by the latch. This helps to reduce latch regeneration time and to resolve for smaller $\Delta V_{IN}$.

Operation: During the reset phase ($\text{CLK} = 0$), the tail transistors $M_{T1}$ and $M_{T2}$ are off along with the cascode transistors $M_{c1}$ and $M_{c2}$. The switching transistors $M_{s1}$ and $M_{s4}$ charge the $f_n$ and $f_p$ nodes to $V_{DD}$. Similarly, $M_{s2}$ and $M_{s3}$ charge the drain nodes of $M_3$ and $M_4$ to $V_{DD}$. Therefore, $M_3$ and $M_4$ are off. The transistors $M_{R1}$ and $M_{R2}$ ensure a proper start condition for the comparator. During the comparison phase ($\text{CLK} = V_{DD}$), $M_{T1}$ and $M_{T2}$ are on, and $M_{s1}$–$s4$ are off. At the beginning of this phase, the pMOS cascode cross-coupled pair is still inactive, and the transistors $M_{sw1}$...
The proposed comparator achieves both with the help of the cascode ing a higher common-mode voltage seen by the latch, and performance.

Subsequently, the initial voltage difference sensed by the latch before the pMOS cascode cross-coupled structure increases the differential voltage $\Delta V_{fn,fp}$. Consequently, the initial voltage difference sensed by the latch before regeneration, $\Delta V_O$, is improved as demonstrated below. nMOS transistor switches $M_{sw1}$ and $M_{sw2}$ take care of the static power dissipation in the preamplifier. They also contribute to the increased $\Delta V_{fn,fp}$ by manifesting another nMOS cascode cross-coupled pair with the input transistors $M_1$ and $M_2$. As a result, the latch regeneration time is decreased.

To demonstrate the enhanced $\Delta V_{fn,fp}$, the procedure used in [5] is adopted. The delay analysis of the conventional DT comparator holds for the proposed comparator as well except for calculating the gain from input to the $fn$ and $fp$ nodes.

**Delay Analysis**: The delay of the proposed comparator is the sum of amplification time, $t_{amp}$, and the latch delay time, $t_{latch}$. The latch delay is given by [5]

$$t_{latch} = t_{inv} \times \ln \frac{V_{DD}/2}{\Delta V_O} + \frac{C_L}{K_{5,7}(V_{DD}-V_{CM})^2 - V_{Thp}} \times V_{Thn}$$

(1)

where $t_{inv} = C_L/(G_m5.6 + G_m7.8 + G_mR12)$. $V_{CM}$ is the common-mode voltage seen by the latch, and $K_{5,7} = 0.5 \times \mu_pC_ox(W/L)_{5,7}$. This equation indicates that a higher $\Delta V_O$, implying a higher $\Delta V_{fn,fp}$, and a lower $V_{CM}$ provide a smaller delay. The proposed comparator achieves both with the help of the cascode cross-coupled pair.

To demonstrate the efficacy of the proposed comparator, the half-circuit analysis can be used. Here, transistors $M_3$ and $M_4$ are modeled as current sources as they operate in the saturation region in the initial stages of the comparison phase. Transistors $M_{c1}$ and $M_{c2}$ are in the saturation region as their gate terminals are at ground potential.

Applying Kirchhoff’s current law (KCL) at nodes $fn$ and $fp$ gives the following expressions:

$$V_{fn} = (A_I g_{m3} V_{fp} - I_1) t_{amp}/C_P$$

$$V_{fp} = (A_I g_{m4} V_{fn} - I_2) t_{amp}/C_P$$

(2)

where $C_P$ is the parasitic capacitance at nodes $fn$ and $fp$. $g_{m3} = g_{m4} = g_m$. $I_1$ and $I_2$ are the drain currents of $M_1$ and $M_2$, respectively. $A_I$ is the current gain provided by the common gate stage formed by the cascode transistors $M_{c1}$ and $M_{c2}$, which is less than unity. Using the small signal analysis $A_I$ can be expressed as

$$A_I = -\frac{1/[r_{c1,2} + (g_{mcl1,2} + g_{mbc1,2})r_s]}{1 + I/r_{c1,2} + (g_{mcl1,2} + g_{mbc1,2})r_s}$$

(3)

where $r_{c1,2}$ and $g_{mcl1,2}$ are the channel resistance and transconductance of cascode transistors, respectively, and $r_s$ is the source resistance.

By solving the linear equations (2), we get

$$V_{fn} = \frac{t_{amp}/C_P[g_m I_2(t_{amp}/C_P) + I_1]}{1 - A_I g_m(t_{amp}/C_P)^2}$$

$$V_{fp} = \frac{t_{amp}/C_P[g_m I_1(t_{amp}/C_P) + I_2]}{1 - A_I g_m(t_{amp}/C_P)^2}.$$  

(4)

The common-mode voltage at the preamplifier output is given by

$$V_{CM,fn,fp} = (V_{fn} + V_{fp})/2.$$  

By substituting (4) in $V_{CM,fn,fp}$, we get

$$V_{CM,fn,fp} = \frac{I(t/C_P)}{1 - A_I g_m(t/C_P)}$$

(5)

where $I = I_1 + I_2$.

The differential voltage at the preamplifier output nodes is expressed as

$$\Delta V_{fn,fp} = V_{fn} - V_{fp}$$

and is given by

$$\Delta V_{fn,fp} = \frac{\Delta I(t/C_P)}{1 - A_I g_m(t/C_P)}$$

(6)

where $\Delta I = I_1 - I_2$.

From (5) and (6), the factor $A_I(< 1)$ obtained due to the cascode cross-coupled pair reduces the common-mode voltage and improves the differential voltage at $fn$ and $fp$ nodes. This helps the latch to regenerate faster than the other comparator architectures. Reducing the $g_m$ of $M_3$ and $M_4$ will also achieve the same result but at the cost of an increased offset voltage.

**IV. RESULTS AND DISCUSSION**

The performance metrics of analog circuits, in general, are technology-dependent. Dynamic comparators are no exception and are prone to both analog and digital nonidealities. Therefore, to make a fair comparison between the proposed and the reported dynamic comparator topologies, all the comparators are simulated in 65 nm technology with a minimum channel length of 60 nm, load capacitance of 2 fF, CLK of 5 GHz, $V_{DD}$ of 1.1 V, and $V_{CM}$ of 0.77 V. It is also ensured that all the comparators are designed and optimized to obtain a similar offset standard deviation, $\sigma_{os}$.

Schematic level transient analysis results of the comparator are shown in Fig. 2. The reference input, $V_p$, is fixed at 0.77 V to attain the optimum performance [11]. The voltages at the output nodes, Outp and Outn, and the intermediate nodes are shown at a $\Delta V_{IN}$ of 10 mV. The delay is evaluated when the output node voltages attain a difference of $V_{DD}/2$. The delay of the proposed comparator is found to be 33.3 ps whereas, it is 39.3 ps for the conventional one.

Fig. 1. Schematic of the proposed double tail comparator with cascode cross-coupled pair to enhance preamplifier gain. The cascode cross-coupled pair made up of $M_3$, $M_4$, $M_{c1}$, and $M_{c2}$ improves the preamplifier performance.
Fig. 2. Transient analysis results of the proposed comparator in comparison with the conventional one when $\Delta V_{IN} = 10$ mV, $V_{CM} = 0.77$ V: (a) output nodes and (b) intermediate nodes.

Fig. 3. Delay variation with $\Delta V_{IN}$ of the proposed comparator. Inset shows the improved delay for small values of $\Delta V_{IN}$.

Fig. 4(a) depicts the simulated delay variation with $V_{CM}$. For a sufficiently large $V_{CM}$, the proposed comparator is faster than the state-of-the-art comparators. Conventional DT architectures enter the triode region and thus limit preamplifier gain. The proposed topology overcomes this problem to some extent by achieving higher $V_O$ with the help of the cascode cross-coupled pair. Fig. 4(b) shows the simulation results of the delay versus the supply voltage. As expected, the delay performance worsens at lower $V_{DD}$. However, the plot shows that at lower $V_{DD}$, the speed of the proposed circuit is 30% faster than the conventional one.

To confirm the high-speed characteristic of the proposed comparator, a layout is drawn as shown in Fig. 5 with proper care to attain symmetry with equal capacitance at the differential nodes to steer off the aspects that increase the delay of the comparator. Monte-Carlo simulations of 200 runs were performed to observe the standard deviation of the offset voltage, $\sigma_{os}$. The results are shown in Fig. 6(a). $\sigma_{os}$ of 11.38 mV is observed from the prelayout simulations and 11.52 mV is obtained from the postlayout simulations. The offset deviation is slightly more than [11] due to the mismatch contribution of $M_{c1}$ and $M_{c2}$. The postlayout simulation results of

| Table I: Comparison Between the Proposed and Other Comparators Based on Authors’ Simulations |
|---------------------------------|-----------------|----------------|-----------------|-----------------|-----------------|
| $L = 60$ nm                     | Offset KB       | $E_C$          | RMS KB          | Delay (ps)      | PDP             |
| $C_L = 2$ fF                   | $\sigma_{os}$   | $\mu$/bit     | $\Delta V_{IN}$ | $\Delta V_{IN}$ |
| $V_{DD} = 1.1$ V               | (mV)            | (mV)          | (mV)            | (mV)            |
| $V_{CM} = 0.77$ V              |                 |               |                 |                 |
| JSSC ’04 [14]                  | 9.9             | 2.8           | 27.4            | 1.3             | 46.8            | –               |
| ISSCC ’07 [6]                  | 10.2            | 3.3           | 48.1            | 1.5             | 39.3            | –               |
| ISSCC ’10 [15]                 | 9.5             | 7.9           | 82.9            | 0.16            | 52.6            | 67.9            | 6.9 |
| TVLSI ’13 [11]                 | 10.9            | 3.0           | 59.3            | 0.6             | 38.3            | 59.3            | 4.2 |
| EL’15 [7]                      | 13.6            | 3.3           | 44.9            | 2.6             | 36.7            | –               |
| TVLSI ’18 [5]                  | 15.1            | 51.8          | 41.7            | 3.5             | 56.7            | –               |
| JSSC ’18 [8]*                  | 8.9             | 2.4           | 32.9            | 0.5             | 119.8           | –               |
| Access ’19 [9]                 | 11.5            | 3.7           | 83.3            | 0.5             | 38.1            | 53.9            | 4.98 |
| TCASII ’20 [16]                | 8.4             | 15.4          | 135.9           | 0.7             | 46.8            | 70.4            | 10.3 |
| This Work                      | 11.38           | 5.99          | 80.8            | 0.75            | 33.3            | 46.5            | 3.8  |

* $CLK = 2.5$ GHz. † Comparator is not able to resolve the input.
Fig. 6. (a) Monte Carlo simulation results of the proposed comparator’s prelayout and postlayout offset voltages and (b) postlayout delay versus $V_{\text{IN}}$ (top) and delay versus $V_{\text{CM}}$ (bottom) of the proposed comparator.

noise, and preamplifier gain. Additionally, input-referred rms noise is calculated from the transient noise simulations as explained in [13]. Input is applied and incremented in steps of 10 $\mu$V to obtain the probability of error as 16% to get the total input-referred rms noise and is tabulated.

V. CONCLUSION

In this brief, we presented a novel DT comparator topology suitable for high-speed applications. It consists of a cascode cross-coupled pair, which increases the preamplifier gain in the comparison phase. Furthermore, the common-mode voltage at the preamplifier output is lowered by the cascode cross-couple pair. As a result, the latch regenerates quickly. Postlayout simulations in a 65 nm CMOS technology with a supply of 1.1 V confirmed that the delay is reduced considerably without much increase in the EC compared to the state-of-the-art architectures.

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