Design and Implementation of 13 Levels Multilevel Inverter for Photovoltaic System

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Abstract: This paper approaches the appearing and modernization of S-Type PV based 13-level multilevel inverter with less quantity of switch. The current S-Type Multi level inverter contains more number of switches and voltage sources. Multilevel level inverter is a be understandable among themost gainful power converters for high power application and present day applications with reduced switches. The fundamental good arrangement of the 13-level multilevel inverter is to get ventured voltage from a couple of levels of DC voltages. The controller gives actual way day andage to switches through driver circuit using PWM methodology. The execution assessment of proposed multilevel inverter is checked using MATLAB/Simulink. This is the outstanding among other techniques appeared differently in relation to all other existing system

1. Introduction

Multilevel inverter expected basic part in control structures, Electric Traction, PV framework. Examined in [1]. In this E-sort multilevel inverter pass on 13 Level yield for unequal Dc sources. The negative level in like way made without H-relate. So this framework requires less number of essentialness semiconductor contraptions and warm anxiety diminishes in [2]. The 13 level yield can be gotten by 12 switches, this framework utilizes lifeless stage move beat width regulation mentioned in [3]. The Eleven Level yield voltage can be gotten by 10 switches and three DC sources and equation is 2n-1. The present structure utilizes 14 switches. It is shown by PSCAD programming and basic exchanging can be utilized as a bit represented in [4]. The five level yield can be gotten by 6 Switches which utilizes a heading structure and controlled by PI Controller and the Maximum power can be master by 750 W solar board by joining Boost and H-Bridge inverter in [5]. The nine level inverter utilizes 12 switches utilized for 13 level
inverter, utilizes 18 switches utilized for 19 level the yield as Half cycle. the THD of the inverter around 19 % acknowledged in [6].

It utilizes three specific methodologies for relationship, in like manner structure 28 changes to deliver 15 level yield. in [7]. The specific consonant disposal utilized as a bit of this multilevel inverter which utilizes diverse exchanging plan. In which 43 social events of exchanging plot for the change list 0.12 for get 13 level. is discussed in [8] Switched capacitor help multilevel inverter utilizes 11 switches and 2 capacitor and diodes , the 2 capacitor utilized for exchanging for produce 13 level yield for fragmentary charging , this can be acknowledged in Electric vehicles .This topology gives blend of fell multilevel inverter and capacitor support exchanged capacitor converter and the get of the inverter is unprecedented is talked about in [9]. The DC Bus bar related among PV and CHB inverter, This inverter can be reenacted in MATLAB and research center show executed and give the brisk reaction without changing control startegies.For more than 10 MW application utilized as a part of [10]

2. Photo Voltaic system
This multilevel inverter uses DC supply from solar panel. for example 10 watts panel has voltage of 17.6 at current of 0.56 A Respectively. Basic unit of a solar PV component is a solar cell. Assemblies of solar cells are used to make solar module. Numerous of solar modules make solar panel and gathering of sun based board. Photovoltaic module equivalent circuit is shown in Fig.1

![Figure 1 Equivalent circuit of solar panel](image)

This sun oriented cell is not specifically associated with the inverter and the diode associated in parallel. This is said current source parallel with the diode and shunt resistance. The yield current of the sun oriented cell is communicated as

\[ I_d = I_s \exp\left(\frac{qV}{nkt}\right) - I_{ph} \tag{1} \]

Id – Diode current, Is-dispersion current, T-incomparable temperature-Boltzmann consistent (1.3805×10−23J/K), Charge q =1.6 ×10−19 C Considering the fabricate misfortunes, the identical circuit of the PV cell comprises of two resistances Rs and Rp associated in arrangement and parallel individually, where Rs speaks to the misfortunes because of the contacts and associations and R sh speaks to the spillage streams in the diode as specified and represented in [11].

3 Pulse Width Modulation

The Pulse creator is portrayed as the switch ON period to the entire day and age is called as obligation cycle as described in the figure 2. Here central pulse plan frameworks used to give the passage pulse to the Switches. The ON time is unswervingly in respect to the aggregate conveyed voltage

\[ \text{PWM} = \quad \text{---------- (2)} \]

The beats are encircled by the switch activity for create ventured waveform. Here 8 switches are initiate to produce 13 level yield waveform. The beat generator utilizing OR entryway utilized for creating positive voltage waveform and alongside invert gate used to deliver negative voltage ventured waveform .It is essential thing technique to give the entryway pulse to the control circuits.

4 Conventional systems

The conventional 13 level inverter as shown in the figure .3 shows The conventional topology comprises of one dc source connected across seven capacitors and six switches along with one H bridge which has 4 switches .Totally this circuit uses 10 switches to get Thirteen level output voltage waveform and which uses time frame switching scheme for generate output voltage With reference to the sine wave .The each step of the output voltage can be obtained by adding and reducing the capacitor in the thirteen level
inverter is discussed in the conventional system. This can be checked by tangle lab reenactment and tentatively confirmed. This framework utilizes Sinusoidal heartbeat width balance for setting off the switches. By contrasting reference and vocation flag the sinusoidal Pulse balance created and we have considered inverter topology just is discussed about in [21]. The one leg of the H-extension can be expelled from this framework and the proposed framework acquainted with be talked about in the following chapter.

5 Proposed System

The s-type PV based 13 level symmetric Multilevel inverter as shown in the figure 4. The proposed topology has 8 switch where as conventional topologies has 10 switches, and hence Thermal stress and operating time of this circuit better than the conventional systems. This system uses basic pulse width modulation as a switching the switches. The Total harmonic of the proposed inverter is better than the conventional systems. PIC microcontroller PIC16F877A is used to generate pulse for Switches.

Number of level obtained ------(3)

The equation (3), represents the Number of level of inverter by number of switches

The output voltage of the inverter ------(4)

multilevel inverter. If increment the quantity of switches is 9, at that point the 15 level voltage got in light of the equation. The Equation (4)

Figure 4. Proposed Multilevel inverter

speaks to the aggregate yield voltage of the inverter for various level, this can be gotten by the result of info voltage and the capacity of switches. In proto sort display,
6. Results and discussion

6.1 simulation of PWM 13 level inverter

Figure 5. 8 switches of the inverter circuit

The figure 5. Demonstrates the beat design for the 8 switches of the inverter circuit, and it is specify plainly for each heartbeat. What's more, beat 3 associated with from three heartbeat generator and additionally entryway and extension, likewise beat 4, 5, 6&7 associated 4 beat generator as well as doors separately. The PWM balance is fundamental and basic strategy for pulse generation.

Figure 6. Simulation of 13 level inverter
The DC input voltage wave form obtained from Solar panel is shown in the figure 7. The input voltage of the solar panel is 200V and it clearly mentioned with respect to time period. The constant voltage obtained from solar panel with respect to time.

The simulation of PV based S-type multilevel inverter produced 13 level stepped waveforms \((V_{dc}, V_{dc}/2, V_{dc}/3, V_{dc}/4, V_{dc}/5, V_{dc}/6, 0, -V_{dc}, -V_{dc}/2, -V_{dc}/3, -V_{dc}/4, -V_{dc}/5, -V_{dc}/6)\) are obtained in the proposed inverter as shown in the figure 8. This results indicates a reduced Total Harmonic Distortion.
THD of the Existing system is 10.80

Figure.9. THD Analysis of Proposed inverter

The Figure.8. shows the proposed thirteen level multi level inverter and Total Harmonic Distortion of the inverter 10.2 % and is Less distortion with respect to conventional Inverter,

6.2. Experimental Results

The Experimental diagram of multilevel inverter as shown in above figure 10. The solar panel is used give DC supply to the inverter. The 13 level output obtained from Digital CRO

Figure.10. Proto type model of PV based 13 level Multilevel inverter
Figure 11. Experimental prototype Model output wave form of S-type PV based multilevel inverter

The Experimental The 13 level output obtained from Digital CRO as shown in the figure 11., and which provide high accurate results while compare to Analog CRO so it is preferred

7. Conclusion

In this paper, 13-level multilevel inverter with less competence of switches is proposed using PWM Technique. The current Multilevel inverter has only 8 switches to produce 13 level output wave form with Single DC source, waveform and furthermore utilized as a part of sustainable power sources. The s-type Multilevel inverter simulated using Mat lab and demonstrated as a Porto-type model. Whereas conventional inverter uses 10 switches to produce 13 level output voltage.

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