Design a Continuous Switching Test Circuit for Power Devices to Evaluate Reliability

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This study presents a design method for the continuous switching test circuits of power devices. Depending on the relationship between the rated voltage of a DC voltage source and device under test (DUT), two types of test circuits are proposed. These test circuits comprise a cascaded buck-boost (or boost-buck) converter to achieve power regeneration. Based on analysis of the test circuits, a design method is proposed to ensure that any failure does not spread to the test circuit even when the DUT fails during the continuous switching tests. A test circuit is designed according to the proposed method, and its experimental results demonstrate the validity of the proposed design.

**Keywords:** continuous switching test, long-term reliability, SiC MOSFET

1. Introduction

Silicon carbide (SiC) exhibits a dielectric breakdown strength that is approximately 10 times greater than that of Si, which is conventionally used in power devices\(^{(11-12)}\). Owing to their features, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are required for practical use in various applications\(^{(13-15)}\). However, long-term reliability issues in SiC MOSFETs, such as bias temperature instability (BTI), have been reported\(^{(13-15)}\). Various test methods have been used in accelerated aging tests to evaluate their long-term reliability. A feature of conventional accelerated aging tests is that static stress is applied to accelerate the aging of devices. Although the static-stress condition is effective in clarifying a specific cause of degradation, it is not suitable for evaluating the dynamic stress that is applied under continuous switching conditions, which are the actual operating conditions of power devices. The long-term reliability of Si power devices caused by dynamic stress has been achieved through years of experience and development\(^{(16)}\).

With these considerations, the Joint Electron Device Engineering Council (JEDEC) developed a standard that provides continuous switching tests for the long-term reliability evaluation of gallium nitride (GaN)\(^{(16)}\) in 2020. However, in the standard, the test circuit for the continuous switching test was not discussed in detail. In addition, the standard requires that the test should be continued until the device under test (DUT) fails to wear out. Therefore, it is necessary to consider a continuous switching test circuit that does not spread the failure even if the DUT fails during the test.

Several research papers have discussed continuous switching test circuits\(^{(17-18)}\). In these studies, half-bridge or full-bridge inverter circuits were proposed as continuous switching test circuits. In addition, power regeneration was achieved by using an inductor as the load of the inverter circuit. However, in Ref.\(^{(17)}\), the DUT failure during the test was not considered. Although Ref.\(^{(18)}\) takes the DUT failure into account during the test, a protection circuit is implemented between the DC link capacitor and DUT. Such a circuit configuration is different from that of a typical power-conversion circuit. In addition, long-term reliability tests of power devices require test results from a large number of samples. Therefore, multiple test circuits are used, and it is important that each test circuit has a simple circuit configuration.

In this paper, a design method for continuous switching test circuits that considers DUT failure is proposed. A cascaded buck-boost (or boost-buck) converter circuit was applied as the test circuit to achieve power regeneration. The proposed design method can prevent DUT failure from spreading to the test circuit without using additional components by designing the circuit parameters. The design method is effective in simplifying the configuration of the test circuit. In Section 2, an overview of the circuit configuration of the proposed test circuits is described. In Sections 3 and 4, the circuit analysis considering the DUT failure is discussed, and the design methods of the test circuit are described. Section 5 presents the validity of the proposed design methods through simulations and experiments. In the experiments, a test circuit of 12.5 kW was designed using a SiC MOSFET of 1.2 kV as the DUT.

2. Overview of proposed test circuits

Fig. 1 shows the ideal voltage and current waveforms of the DUT under the continuous switching test. In Fig. 1, \(V_{DS}\) is the test voltage, \(I_D\) is the test current, \(D_0\) is the on-duty ratio of the DUT, \(f_{SW}\) is the switching frequency, \(T_S\) is the switching period, and \(\Delta I_D\) is the current ripple of the test current \(I_D\). To achieve continuous switching operation and power regeneration, a cascaded buck-boost (or boost-buck) converter is adopted as the test circuit. Furthermore, because the load current of the circuit is DC, the test current \(I_D\) is constant, and therefore, suitable for continuous switching tests.

In continuous switching tests, unlike switching tests, the energy consumed during the continuous test must be supplied...
from a power supply. A power supply with a large voltage rating and large capacity is required for testing power modules with large voltage and current ratings\(^{(19)}\)(\(^\text{20}\)). Hence, two types of test circuits are proposed for testing DUTs of various voltage and current ratings: the first type is the cascaded buck-boost converter that is referred to as the “buck-type test circuit” hereinafter. The buck-type test circuit can be used only when the test voltage \(V_{DS}\) is lower than the output voltage of the power supply. The second type is the cascaded boost-buck converter that is referred to as the “boost-type test circuit” hereinafter. The boost-type test circuit can boost the input voltage and be set to a test voltage \(V_{DS}\) that is higher than the output voltage of the power supply. In this paper, each design method is proposed. By considering the design method, it is shown that the buck-type test circuit is more suitable than the output voltage of the power supply. In this paper, the continuous switching test. A control method for the test voltage \(V_{DS}\) is equal to the input voltage \(E\), it can be set arbitrarily by the DC voltage source, as shown in the following equation:

\[ V_{DS} = E. \]  

The inductor current \(i_{L1}\) is feedback-controlled by a transistor \(Q_1\) of the buck converter to arbitrarily set the test current \(I_D\). However, the volume of the inductor should be large owing to the DC current \(I_D\) that flows through the inductor constantly. Therefore, a control method that can reduce the current ripple \(i_{r,L1}\) is applied to reduce the inductance \(L_{1}\).

The circuit operation can be divided into four modes according to the on/off state of the transistor \(Q_1\) and the DUT. Table 1 shows an inductor voltage \(\Delta V_{L1}\) in the four modes. Even in modes B and C, the inductor current \(i_{L1}\) decreases owing to the power loss in the circuit. Therefore, mode A occurs, and energy is supplied to the inductor. Fig. 3 shows the gate waveforms and inductor current waveform of the buck-type test circuit.

Table 1. Operating modes of buck-type test circuit

| Operating mode | \(Q_1\) | DUT | \(\Delta V_{L1}\) |
|----------------|--------|-----|-----------------|
| A              | ON     | ON  | \(E\)           |
| B              | ON     | OFF | 0               |
| C              | OFF    | ON  | 0               |
| D              | OFF    | OFF | \(-E\)          |

3. Design of buck-type test circuit

Fig. 2 shows the circuit diagram of the buck-type test circuit\(^{(21)}\). The buck and boost converters are connected in this order from a DC voltage source side, and the output of the boost converter is connected to the input of the buck converter to achieve power regeneration. The DUT is implemented as a transistor of the boost converter because it acts as a low-side transistor, which is suitable for measurement. A diode BD is inserted to prevent a voltage exceeding the input voltage from being applied to the DC voltage source. As shown in Fig. 2, the inductor of the buck converter and boost converter can be shared\(^{(22)}\).

In this paper, when the DUT fails, it is called “abnormal operation,” whereas it is called “normal operation” during the continuous switching test. A control method for the test voltage \(V_{DS}\) and test current \(I_D\) during normal operation is described below. In addition, because the circuit parameters are dominated by the influence of an overvoltage or overcurrent during abnormal operation, the circuit parameter design method that considers abnormal operation is described.

3.1 Control method for normal operation

As the test voltage \(V_{DS}\) is equal to the input voltage \(E\), it can be set arbitrarily by the DC voltage source, as shown in the following equation:

\[ V_{DS} = E. \]  

The inductor current \(i_{L1}\) is feedback-controlled by a transistor \(Q_1\) of the buck converter to arbitrarily set the test current \(I_D\). However, the volume of the inductor should be large owing to the DC current \(I_D\) that flows through the inductor constantly. Therefore, a control method that can reduce the current ripple \(i_{r,L1}\) is applied to reduce the inductance \(L_{1}\).

The circuit operation can be divided into four modes according to the on/off state of the transistor \(Q_1\) and the DUT. Table 1 shows an inductor voltage \(\Delta V_{L1}\) in the four modes. Even in modes B and C, the inductor current \(i_{L1}\) decreases owing to the power loss in the circuit. Therefore, mode A occurs, and energy is supplied to the inductor. Fig. 3 shows the gate waveforms and inductor current waveform of the buck-type test circuit.

\[ D_T^\ast = \frac{D_T}{E} \left( i_{L1}^\ast - i_{L1} \right), \]  

where \(K_P\) is the proportional gain, and \(i_{L1}^\ast\) is the inductor current command value, which is equal to the test current \(I_D\). Fig. 4 shows the control block diagram.

The ratio \(d_A\) in mode A is a single period, given by the following equation:
Taking this into consideration.

3.2.2 Design of capacitor

The design of the capacitor should consider the open failure of the DUT. Fig. 7 illustrates the equivalent circuit when open failure of the DUT occurs. When transistor Q1 is on, the inductor current \(i_{L1}\) is freewheeling in the circuit. When transistor Q1 is off, the inductor current \(i_{L1}\) decreases owing to the inductor voltage \(v_{L1} = -E\). Fig. 8 shows the inductor current \(i_{L1}\) when open failure of the DUT occurs. In the event of the DUT open failure, the inductor current \(i_{L1}\) decreases and gradually reaches 0 A. However, because the energy of the inductor is transferred to the capacitor, the capacitor voltage \(v_{C1}\) increases and exceeds the input voltage \(E\). The maximum value of the capacitor voltage \(V_{\text{Cmax}}\) is given by the following equation:

\[
V_{\text{Cmax}} = \sqrt{\frac{L_1}{C_1} I_D^2 + E^2}.
\]  

In Eq. 6, the resistance components in the test circuit were ignored when considering the worst case.

4. Design of Boost-type Test Circuit

Fig. 9 depicts the circuit diagram of the boost-type test circuit. The boost and buck converters are connected in this order from the DC voltage source side. The output of the buck converter is connected to the input of the boost converter to achieve power regeneration \(^{24}\). The DUT was implemented as a transistor for the buck converter. If the transistor of the boost converter is the DUT, and short-circuiting of the DUT occurs, a short circuit occurs in the DC voltage source via the inductor \(L_1\). This short circuit of the DC voltage source cannot be stopped by the transistor of the buck converter. Therefore, the DUT should be the transistor of the buck converter.

The control method of the test voltage \(V_{\text{DS}}\) and test current \(I_D\) during normal operation is described below. In addition, because the circuit parameters are dominated by the influence of an overvoltage or overcurrent during abnormal operation, the circuit parameter design method that considers abnormal operation is described.

4.1 Control method for normal operation

The test voltage \(V_{\text{DS}}\) is bucked to the input voltage \(E\) by a buck converter with a duty ratio of \(D_0\). Therefore, the test voltage \(V_{\text{DS}}\)
Fig. 9. Circuit diagram of the boost-type test circuit.

Table 2. Operating modes of the boost-type test circuit

| Operating mode | \( Q_1 \) | DUT | \( t_{c2} \) |
|----------------|---------|-----|-----------|
| A              | ON      | ON  | \(-t_{c2}\) |
| B              | ON      | OFF | 0         |
| C              | OFF     | ON  | 0         |
| D              | OFF     | OFF | \( t_{c2} \) |

Mode

An inductor current \( i_{L1} \) is feedback-controlled by a transistor \( Q_1 \) of the boost converter to set the test current \( I_D \) arbitrarily. As there are no limitations on the set value of the test voltage \( V_{DS} \), theoretically, the design limits of the test voltage \( V_{DS} \) are small. However, because it is necessary to select a capacitor with a high rated voltage, film capacitors should be applied. As the test current \( I_D \) flows through capacitor \( C_2 \), the voltage ripple tends to increase. Therefore, the control method described below was applied to reduce the capacitance \( C_2 \).

The circuit operation can be divided into four modes according to the on/off state of the transistor \( Q_1 \) and the DUT. Table 2 shows the capacitor current \( t_{c2} \) in the four modes. Even in mode C, the capacitor voltage \( t_{c2} \) increases because the energy that corresponds to the loss of the buck converter is supplied from the DC voltage source. Therefore, mode A occurs, and capacitor \( C_2 \) supplies energy to the buck converter. Fig. 10 shows the gate waveforms and the capacitor voltage waveform of the boost-type test circuit.

The off-duty ratio command value \( D_{Q1} \) of the transistor \( Q_1 \) is as follows:

\[
D_{Q1} = D_D - \frac{K_P}{E} (i_{L1} - i_{L1}). \tag{8}
\]

The control block diagram is the same as that of the buck-type test circuit shown in Fig. 4.

The ratio \( d_A \) in which mode A occurs is a single period, which is given by the following equation:

\[
V_{DS} = \frac{E}{D_D}. \tag{7}
\]

An inductor current \( i_{L1} \) is feedback-controlled by a transistor \( Q_1 \) of the boost converter to set the test current \( I_D \) arbitrarily. As there are no limitations on the set value of the test voltage \( V_{DS} \), theoretically, the design limits of the test voltage \( V_{DS} \) are small. However, because it is necessary to select a capacitor with a high rated voltage, film capacitors should be applied. As the test current \( I_D \) flows through capacitor \( C_2 \), the voltage ripple tends to increase. Therefore, the control method described below was applied to reduce the capacitance \( C_2 \).

The circuit operation can be divided into four modes according to the on/off state of the transistor \( Q_1 \) and the DUT. Table 2 shows the capacitor current \( t_{c2} \) in the four modes. Even in mode C, the capacitor voltage \( t_{c2} \) increases because the energy that corresponds to the loss of the buck converter is supplied from the DC voltage source. Therefore, mode A occurs, and capacitor \( C_2 \) supplies energy to the buck converter. Fig. 10 shows the gate waveforms and the capacitor voltage waveform of the boost-type test circuit. The off-duty ratio command value \( D_{Q1} \) of the transistor \( Q_1 \) is as follows:

\[
D_{Q1} = D_D - \frac{K_P}{E} (i_{L1} - i_{L1}). \tag{8}
\]

The control block diagram is the same as that of the buck-type test circuit shown in Fig. 4.

The ratio \( d_A \) in which mode A occurs is a single period,
4.2.1 Short circuit failure of DUT  
Fig. 11 shows the equivalent circuit when a short circuit of the DUT occurs. Fig. 12 shows the theoretical waveforms when the short circuit occurs. In Fig. 12, a short circuit occurs at time \( t = t_0 \). In the period \( t_0-t_1 \), the inductor current \( i_L \) increases owing to the capacitor voltage \( v_{C1} < v_{C2} \). The inductor current \( i_{L1} = I_D \), owing to the constant current control. Therefore, an overcurrent \( I_{OC} \) of the inductor current \( i_{L2} \) should be detected. At time \( t = t_1 \), the operation of the transistor \( Q_1 \) is stopped by the overcurrent \( I_{OC} \) of the inductor current \( i_{L2} \). After \( t = t_1 \), it can be divided into two patterns depending on the inductor current \( i_{L1} \). One pattern is the inductor current, \( i_{L1} \), in the continuous conduction mode. The other pattern is the inductor current \( i_{L1} \) in a discontinuous conduction mode for \( t = t_2 - t_1 \), as shown in Fig. 12.

When the inductor current \( i_{L1} \) is in the continuous conduction mode, that is, when the minimum value \( I_{min} \) of the inductor current \( i_{L1} \) satisfies the following equation:

\[
I_{min} \approx I_D + I_{OC} - \sqrt{\frac{C}{L} (1 - D_D)^2 V_{DS}^2 + (I_D - I_{OC})^2} > 0, \quad \cdots (16)
\]

the maximum current \( I_{max} \) is given by the following equation:

\[
I_{max} \approx \frac{1}{2} \left( I_D + I_{OC} \right) + \frac{1}{2} \sqrt{\frac{C}{L} (1 - D_D)^2 V_{DS}^2 + (I_D - I_{OC})^2}, \quad \cdots (17)
\]

The approximate expressions \( v_{C2} (t_2) = V_{DS} \) and \( v_{C1} (t_1) = E_1 \) are applied to Eq. 16 and Eq. 17.

When \( I_{min} \leq 0 \), the inductor current \( i_{L1} \) reaches 0 A at time \( t = t_2 \). In the period \( t_2-t_3 \), the inductor current \( i_{L1} \) = 0 A because the diode \( D_1 \) is off. At time \( t = t_3 \), the inductor current \( i_{L2} \) reaches the maximum current \( I_{max} \), which is given by the following equation:

\[
I_{max} \approx \frac{C}{2L} (1 - D_D)^2 V_{DS}^2 + (I_D + I_{OC})^2. \quad (18)
\]

The approximate expressions \( v_{C2} (t_2) = V_{DS} \) and \( v_{C1} (t_1) = E_1 \) are applied to Eq. 18.

4.2.2 Open failure of DUT  
Fig. 13 depicts the equivalent circuit when open failure of the DUT occurs. Similarly, Fig. 14 shows the theoretical gate, inductor current, and capacitor voltage waveforms when an open failure of the DUT occurs. The inductor currents \( i_{L1}, i_{L2} \), and capacitor voltage \( v_{C1} \) gradually decrease because their energy is transferred to the capacitor \( C_2 \). Therefore, the capacitor voltage \( v_{C2} \) increases, and its maximum voltage \( V_{Cmax} \) is given by the following equation:

\[
V_{Cmax} = \sqrt{\frac{2L}{C} V_{DS}^2 + V_{DS}^2 + E^2}. \quad (19)
\]

4.3 Design of inductor and capacitor  
From Equations 17–19, the maximum voltage \( V_{Cmax} \) and maximum current \( I_{max} \) depend on the ratio of inductance \( L \) and capacitance \( C \) (thus \( L/C \)). Fig. 15 illustrates the calculation and simulation results of \( V_{Cmax} \) and \( I_{max} \). The calculation and simulation conditions are listed in Table 3. In Fig. 15, \( \Delta V_{Cmax} \) and \( \Delta I_{max} \) are defined by the following equations:

\[
\Delta V_{Cmax} = V_{Cmax} - V_{DS}, \quad (20)
\]

\[
\Delta I_{max} = I_{max} - I_{OC}. \quad (21)
\]

The calculated results almost replicated the simulation results. As \( V_{Cmax} \) and \( I_{max} \) have a trade-off relationship, it is necessary to design \( L/C \) by considering both.

During normal operation, because the current ripple \( \Delta I_D \) is equal to the current ripple of the inductor current \( i_{L2} \), it is given by the following equation:

\[
\Delta I_D = \frac{[(R_{L2} + R_{DS}) I_D + E] (1 - D_D)}{L_2 f_{SW}}. \quad (22)
\]

From the above equations and the relationship of Fig. 15, the inductance \( L \) and capacitance \( C \) can be designed.

![Fig. 13. Equivalent circuit of the boost-type test circuit when open failure of the DUT occurs.](image)

![Fig. 14. Theoretical waveforms when open failure of the DUT occurs.](image)

![Fig. 15. Calculation and simulation results of \( \Delta V_{Cmax} \) and \( \Delta I_{max} \).](image)

### Table 3. Calculation and simulation conditions of the boost-type test circuit

| Parameters | Value |
|------------|-------|
| Test voltage \( V_{DS} \) | 800 V |
| Test current \( I_D \) | 20 A |
| Duty ratio of DUT | 0.5 |
| Over current detection value \( I_{OC} \) | 30 A |
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5. Experimental results

Experiments were performed to validate the design methods described in Sections 3 and 4. Fig. 16 shows the experimental setup of the test circuit. Table 4 shows the circuit parameters of both the buck- and boost-type test circuits. The test circuit becomes a buck- and boost-type test circuit by changing the wiring. The boost-type test circuit requires two capacitors and inductors. As these two capacitors were used in parallel and the inductors were used in series in the buck-type test circuit in this experiment, both the capacitance and inductance were twice as high as those in the boost-type test circuit in this experiment, both the capacitance and inductance were twice as high as those in the boost-type test circuit. Table 5 shows the specifications of the power devices used in the experiment. To verify the operation of the test circuit, the same devices were used for transistors Q1 and DUT. The proportional gain $K_P$ was set to 5.0\(^{10}\). Table 6 shows the specifications of the measuring instruments used in the experiment.

### 5.1 Buck-type test circuit

Table 7 shows the experimental conditions of the buck-type test circuit. The test voltage $V_{DS}$ was set to 500 V, which is the rated voltage of the DC voltage source. The test current $I_D$ was set to 50 A. Under these conditions, the conversion capacity was 12.5 kW because the duty ratio of the DUT was set to 0.5.

Fig. 17 depicts the experiment waveforms during the normal operation. As the test current $I_D$ was measured by a Rogowski coil, the DC component is offset in Fig. 17. There is almost no current ripple $\Delta I_D$ because the control method described in Section 3.1 was applied. The input power of the DC voltage supply was 610 W, which was 4.9% of the conversion capacity.

Fig. 18 shows the experimental waveforms when short circuiting of the DUT occurs. The overcurrent detection value of the inductor current $i_{L1}$ was set to 70 A. The transistor Q1 stopped operating owing to the detection of the overcurrent. In addition, the inductor current $i_{L1}$ gradually decreases and reaches 0 A. Therefore, the test can be stopped without spreading the DUT failure to the test circuit.

Fig. 19 shows the experiment waveforms when the open failure of DUT occurs. After open failure of the DUT occurs, when the transistor Q1 is on, the inductor current $i_{L1}$ is freewheeling in the circuit. Therefore, the reduction rate of the inductor current $i_{L1}$ is small. In contrast, when transistor Q1 is off, the inductor current $i_{L1}$ charges the capacitor $C_1$. Therefore, the reduction rate of the inductor current $i_{L1}$ is large. Whether the transistor Q1 is on or off, the inductor current $i_{L1}$ gradually reaches 0 A. As the drain-source voltage of the DUT is equal to the capacitor voltage $V_{C1}$, the maximum value of the capacitor voltage $V_{C1_{\text{max}}}$ is applied to the drain-source of the DUT. The maximum value of the drain-source voltage of the DUT was 522 V, which was 4.4% higher than the test voltage $V_{DS} = 500$ V. Furthermore, the maximum value was approximately equal to the value (523 V) calculated using Eq. 6. The test circuit can be stopped without spreading the failure to the test circuit.

### 5.2 Boost-type test circuit

Table 8 shows the experi-
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Fig. 18. Experimental gate waveform and inductor current waveform when short circuit of the DUT occurs.

Fig. 19. Experimental gate waveform and inductor current waveform when open failure of the DUT occurs.

mental conditions of the boost-type test circuit. The test voltage $V_{DS}$ was set to 800 V, which is larger than the rated voltage of the DC voltage source. The test current $I_D$ was set to 20 A. Under these conditions, the conversion capacity was 8 kW because the duty ratio of the DUT was set to 0.5.

Fig. 20 shows the experiment waveforms during the normal operation. As the test current $I_D$ was measured by the Rogowski coil, the DC component is offset in Fig. 20. The current ripple $\Delta I_D$ is about 5.6 A, which is in good agreement with the calculated value obtained by applying Eq. 22. The input power of the DC voltage supply was 480 W, which was 6.1% of the conversion capacity.

Table 8. Experimental conditions of the boost-type test circuit

| Contents                  | Value  |
|---------------------------|--------|
| Test voltage $V_{DS}$     | 800 V  |
| Test current $I_D$        | 20 A   |
| Switching frequency $f_{SW}$ | 100 kHz |
| Duty ratio of DUT $D_D$   | 0.5    |
| Over current detection value $I_{OC}$ | 30 A |

Fig. 21 shows the experimental waveforms when the short circuit of the DUT occurs. At this time, the overcurrent set value of the inductor current $i_L$ was set to 30 A. The transistor Q1 stopped operating owing to the detection of the overcurrent. The maximum current $I_{L_{max}}$ was approximately 97 A, which was approximately 8% smaller than the value calculated using Eq. 18. The reason for the error is that the approximate expressions are applied to Eq. 18, and the resistance components in the circuit are not considered for the worst case. The inductor currents $i_L$ and $i_2$ gradually decrease and reach 0 A. The maximum voltage $V_{C_{max}}$ does not exceed the test voltage $V_{DS}$, and the capacitor voltages $v_{C_1}$ and $v_{C_2}$ converge to an intermediate value between the input voltage $E$ and the test voltage $V_{DS}$. Therefore, the test can be stopped without spreading the DUT failure to the test circuit.

Fig. 22 shows the experiment waveforms when open failure of the DUT occurs. After the open failure of the DUT occurs, the inductor current $i_L$ decreases. At this time, a low current of inductor current $i_L$ was detected, and the operation of the transistor Q1 was stopped (the low current detection value was set to 5 A in this experiment). Subsequently, the inductor current $i_L$ decreases. The maximum voltage $V_{C_{max}}$ was smaller than the value calculated by Eq. 19 because the operation of the transistor Q1 could be stopped by detecting the low current of the inductor current $i_L$.

6. Conclusions

Continuous switching test circuits have been developed to evaluate the long-term reliability of power devices. In this study, circuit analysis was performed when the DUT failed.
As a result, a design method for circuit parameters has been proposed that does not spread the failure to the test circuit even if the DUT fails during the test.

Two types of test circuits and their design method were proposed. Compared with the boost-type test circuit, the buck-type test circuit has the following advantages: the DUT acts as a low-side transistor, which is suitable for measurement, the number of components is small, and the circuit design in consideration of the abnormal operation is easy. On the other hand, as a result of the experiment in this study, the DC voltage source supplied 4.9% of the conversion capacity of the DUT in the buck-type test circuit. Therefore, it can be said that the power supply with large output voltage and sufficient capacity is required for continuous switching tests of power modules with large voltage and current ratings. When the test voltage exceeding the output voltage of the existing power supply is required, the boost-type test circuit is suitable.

Furthermore, the proposed test circuits do not implement complicated protection circuits, thereby enabling a simplified test circuit configuration. This facilitates the preparation of multiple test circuits to simultaneously test many samples.

The proposed design method was verified using a circuit simulation, and the circuit operation was verified using an experimental circuit under the conditions of 500 V and 50 A, or 800 V and 20 A, and the effectiveness of the design method was demonstrated.

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Design a Continuous Switching Test Circuit for Power Devices to Evaluate Reliability (Shin-Ichiro Hayashi et al.)

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