A Fully Memristive Spiking Neural Network with Unsupervised Learning

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Abstract—We present a fully memristive spiking neural network (MSNN) consisting of physically-realizable memristive neurons and memristive synapses to implement an unsupervised Spike Timing Dependent Plasticity (STDP) learning rule. The system is fully memristive in that both neuronal and synaptic dynamics can be realized by using memristors. The neuron is implemented using the SPICE-level memristive integrate-and-fire (MIF) model, which consists of a minimal number of circuit elements necessary to achieve distinct depolarization, hyperpolarization, and repolarization voltage waveforms. The proposed MSNN uniquely implements STDP learning by using cumulative weight changes in memristive synapses from the voltage waveform changes across the synapses, which arise from the presynaptic and postsynaptic spiking voltage signals during the training process. Two types of MSNN architectures are investigated: 1) a biologically plausible memory retrieval system, and 2) a multi-class classification system. Our circuit simulation results verify the MSNN’s unsupervised learning efficacy by replicating biological memory retrieval mechanisms, and achieving 97.5% accuracy in a 4-pattern recognition problem in a large scale discriminative MSNN.

Index Terms—Neuromorphic computing, memristor, spiking neural network, unsupervised learning, STDP.

I. INTRODUCTION

NEUROMORPHIC computing is guided by the rich neural dynamics present in the brain, the highly parallelized nature of neural computation, and the sparse encoding of data as spikes, in pursuit of optimizing memory and computation for energy efficiency. The pervasive von Neumann architecture disaggregates memory and computation which leaves much room for improvement for threads with a deterministic set of instructions. This deficiency has spurred the development of a variety of neuromorphic computing systems [1]–[9], which integrate spiking neurons and simplified synaptic models onto a silicon substrate. In almost all instances, synaptic weights are stored in random access memory (RAM), thus moving memory closer to processor. But memory access and computation remain as two separate steps, which does not address the cost of data communication and memory access, which impose the most overhead in both neuromorphic and general purpose computing systems.

The memristor has been presented as an option to merging the computation and memory substrates [10]–[12]. What was once a theoretical postulate proposed by Chua in 1971 [10] has become a commercially available technology that can be integrated in the back-end-of-the-line (BEOL) of modern CMOS processes [13], [14]. Their non-volatile retention capacity is often likened to synapses [15]–[19], and their threshold-switching characteristics occasionally exploited as a spiking neuron model [20]–[23]. For example, the modulation of device resistance has been correlated to synaptic plasticity, where achieving short-term plasticity (STP) and long-term plasticity (LTP) using memristors is as simple as applying programming pulse trains [24]. The benefits of memristive neurons and synapses arise from CMOS-compatibility, high-density, nanoscale vertical integration, and their ability to directly implement biological features, as opposed to requiring several arithmetic steps as with transistor-only circuits [25].

The use of spiking neural networks (SNNs) as opposed to modern deep learning paradigms has shown significant energy and latency benefits as a result of activation sparsity, spike-based representations of data, and event-based data processing [26]–[30], and can be harnessed using the growing infrastructure to support SNN simulations [31]–[33].

Much of the prior work on memristive spiking neural networks (MSNNs) is constrained to using either memristive synapses or memristive neurons. The work in [36] demonstrated a fully integrated memristive system that emulated both synapses and spiking neuron models to achieve simple pattern recognition tasks. The result is demonstrated using an in-house fabricated diffusive memristor, which is not readily accessible to the broader research community. In this work, we introduce a fully memristive approach to designing a system that shows the capacity to learn pattern recognition tasks using memristive neurons and synapses. We achieve this using models of commercially available, low-cost memristors [37]. We use a memristive neuron circuit which consists of the minimum number of circuit elements necessary to achieve distinct depolarization, hyperpolarization, and repolarization voltage phases. This neuron is integrated in a multi-layer MSNN with memristive synaptic interconnections, modelled using an equivalent SPICE model of a memristive array to train the MSNN with the STDP learning rule [38]. We successfully demonstrate the potential of MSNN to perform associative memory retrieval, as well as pattern recognition achieving 97.5% accuracy on a multi-class classification task. Our results validate homogeneous memristive systems that are capable of neuromorphic learning without global error signals.

II. METHODS

A. MIF model

In this paper, we apply the MIF neuron model [39]. The MIF circuit is shown in Fig. [1]. The proposed MIF circuit is...
characterized by the differential equations below:

\[
\frac{dv}{dt} = \frac{I - G_1(v - E_{rest}) - G_2(v - E_{reset})}{C} \tag{1a}
\]

\[
\frac{dx_1}{dt} = \frac{1 - x_1}{\tau_1} \left( 1 + e^{-\frac{v_{on1} - (v - E_{rest})}{k_{th}}} \right) - \frac{x_1}{1 + e^{-\frac{(v - E_{rest}) - v_{off1}}{k_{th}}}} \tag{1b}
\]

\[
\frac{dx_2}{dt} = \frac{1 - x_2}{\tau_2} \left( 1 + e^{-\frac{v_{on2} - (v - E_{reset})}{k_{th}}} \right) - \frac{x_2}{1 + e^{-\frac{(v - E_{reset}) - v_{off2}}{k_{th}}}} \tag{1c}
\]

\[
G_1 = \frac{x_1}{R_{on1}} + \frac{1 - x_1}{R_{off1}} \tag{1d}
\]

\[
G_2 = \frac{x_2}{R_{on2}} + \frac{1 - x_2}{R_{off2}} \tag{1e}
\]

where \( G_1 \) and \( G_2 \) are the memductances, \( x_1 \) and \( x_2 \) are a pair of internal states, \( \tau_1 \) and \( \tau_2 \) are time constants governing the rate of change in internal states, \( k_{th} \) is the effective thermal voltage. They are the characteristic variables of \( M_1 \) and \( M_2 \), respectively. This system of equations mirrors several prominent SPICE memristor models, and has been used to emulate the commercially available Kown memristor [37].

To show the dynamics of the above system, we apply an alpha-shaped input current, with the resultant memristor internal states and voltage waveforms shown below in Fig. 2.

![Fig. 1. Pre-synaptic and post-synaptic memristive neurons with a trainable memristive synapse interposed between the two. The neuron model is a memristive integrate-and-fire (MIF) neuron circuit, consisting of two memristors \( M_1 \) and \( M_2 \), connected to DC voltage sources \( E_{rest} \) and \( E_{reset} \), in parallel with a capacitor \( C \). Voltage spikes generated by the MIF neuron propagates through the synapse, and trigger an input current to the post-synaptic MIF neuron, which in turn will generate spikes.](image)

![Fig. 2. Simulation result of MIF receiving an alpha shape input current. (a) Internal states \( z_1 \), \( z_2 \). (b) Voltage response \( v \).](image)

The alpha current is modeled by Eq. (2):

\[
\tau_{syn} \frac{dI}{dt} = a - I \tag{2a}
\]

\[
\tau_{syn} \frac{da}{dt} = -a + W_j \sum f \delta(t - t_{j}^f) \tag{2b}
\]

where \( W_j \) is a weighted synaptic current generated between presynaptic neuron \( j \) and associated postsynaptic neuron. \( \sum f \delta(t - t_{j}^f) \) indicates the total number of spikes emitted by presynaptic neuron \( j \), and \( I \) is the input current.

The parameters used in this network are listed in Table I.

| TABLE I | MIF CIRCUIT PARAMETERS |
|--------|------------------------|
| Parameter | Value | Parameter | Value |
| \( E_{rest} \) | 0 mV | \( E_{reset} \) | 50 mV |
| \( C \) | 100 pF | \( k_{th} \) | 10 mV |
| \( v_{on1}, v_{off1} \) | 0 mV | \( v_{on2}, v_{off2} \) | 100 mV |
| \( R_{on1}, R_{off1} \) | 0.1 M\( \Omega \) | \( R_{on2}, R_{off2} \) | 1 k\( \Omega \) |

B. Memristive Synapse with STDP

The Spike-timing-dependent plasticity (STDP) learning rule modulates synaptic weights based on the time difference of pre- and postsynaptic spike arrivals [33]. This type of learning rule can be be achieved by using memristors [18], [40], and can be verified using SPICE-level models [41]. As Fig. 1 shows, a synaptic memristor is interposed between two neurons, where the pre- and postsynaptic spikes will generate a voltage across the memristor that causes the memristance to be updated. Moreover, the time difference between pre- and postsynaptic spikes will modulate the changes in the memristance of the synapse.

In the memristive synapse with STDP learning mechanism, the weight change will increase rapidly and then decrease slowly when the time difference of a pre- and postsynaptic spike increases from zero. The weight change of a memristive synapse is determined by the voltage across the memristor. The largest voltage will result in the largest weight change, and occurs when one of the pre- or post- synaptic neuron reaches the threshold level, while the other is at the reset voltage level. Therefore, the learning window of memristive STDP will rise with a fast time constant, followed by a slow decay. Thus, it is reasonable to model the memristive synapse behavior with an alpha shape learning window as:

\[
W_{pre}(x) = U_{pre} \cdot \frac{|\Delta t|}{\tau_{pre}} \cdot e^{-\frac{|\Delta t|}{\tau_{pre}}} \tag{3a}
\]

\[
W_{post}(x) = U_{post} \cdot \frac{|\Delta t|}{\tau_{post}} \cdot e^{-\frac{|\Delta t|}{\tau_{post}}} \tag{3b}
\]

where \( U_{pre}, U_{post}, \tau_{pre}, \tau_{post} \) are fitted constants, and \( \Delta t = t_{post} - t_{pre} \). Generally, the curve in the learning window will take an alpha shape in both the positive and negative planes of the \( x \)-axis. This type of STDP can be modeled with a system of differential equations defined in Eq. (4):

\[
\tau_{pre} \frac{dA_{pre}}{dt} = T_{pre} - A_{pre} \tag{4a}
\]

\[
\tau_{pre} \frac{dT_{pre}}{dt} = T_{pre} + U_{pre} \cdot \sum f \delta(t - t_{j}^f) \tag{4b}
\]
\[ \tau_{\text{post}} \frac{dA_{\text{post}}}{dt} = T_{\text{post}} - A_{\text{post}} \quad (4c) \]
\[ \tau_{\text{post}} \frac{dT_{\text{post}}}{dt} = -T_{\text{post}} + U_{\text{post}} \cdot \sum_{n} \delta(t - t_{n}^{i}) \quad (4d) \]
\[ W_{j} \leftarrow W_{j} + A_{\text{post}} \quad \text{upon presynaptic spike} \quad (4e) \]
\[ W_{j} \leftarrow W_{j} + A_{\text{pre}} \quad \text{upon postsynaptic spike} \quad (4f) \]

where \( f \) indicates the total numbers of spikes emitted by the presynaptic neuron \( j \), and \( n \) defines the total number of spikes emitted by the postsynaptic neuron \( i \). \( U_{\text{pre}} \) is typically positive, while \( U_{\text{post}} \) is usually negative. \( W_{j} \) is the weighted synaptic current. Upon arrival of a presynaptic spike, \( W_{j} \) immediately increases by the amount of \( A_{\text{post}} \). \( T_{\text{pre}} \) induces a rise by the amount of \( U_{\text{pre}} \), which then evolves according to Eq. (4b). This in turn modulates \( A_{\text{pre}} \). Upon arrival of a postsynaptic spike, \( W_{j} \) immediately increases by the amount of \( A_{\text{pre}} \). \( T_{\text{post}} \) increases by the amount of \( U_{\text{post}} \), and then affects \( A_{\text{post}} \) in a similar manner to the impact from a presynaptic spike.

An example of the temporal evolution of the learning rule is shown in Fig. 3, where an update occurs if presynaptic spike arrival occurs before the postsynaptic spike. Fig. 3(a) shows \( T_{\text{pre}} \) and \( T_{\text{post}} \) instants, at which the curve takes an immediate increase followed by an exponential decay. Fig. 3(b) shows \( A_{\text{pre}} \) and \( A_{\text{post}} \) as functions of time, which have alpha-shaped curves, and Fig. 3(c) shows the fast weight increase when the presynaptic spike occurs before the postsynaptic spike. When the presynaptic spike arrives at \( t = 5\mu s \), \( W_{j} \) increases by the amount of \( A_{\text{post}} \) at this time, which is zero. At \( t = 10\mu s \), the postsynaptic spike arrives, \( W_{j} \) increases by the amount of \( A_{\text{pre}} \) at this time, which is around 0.3 \( \mu A \).

**Fig. 3.** An example of the proposed memristive STDP with \( \tau_{\text{pre}} = \tau_{\text{post}} = 3\mu s, U_{\text{pre}} = 1\mu A, U_{\text{post}} = -1\mu A \). (a) \( T_{\text{pre}} \) and \( T_{\text{post}} \) in Eq. (4) are determined by a pre- and a post- synaptic spike, respectively. (b) \( A_{\text{pre}} \) and \( A_{\text{post}} \) in Eq. (4) are determined by a pre- and a post- synaptic spike, respectively. (c) The weight is updated according to Eq. (4).

### C. Type-1 MSNN for Memory Retrieval

The neural network architecture we implement with the fully memristive neuron and synapse models consists of three layers [42]. The input layer applies a Poisson spike train which encodes the input patterns via rate encoding. The second layer is a MIF excitatory layer. The third layer is an inhibitory layer and includes feedback connections to the excitatory layer. The architecture is shown in Fig. 4. The input to the excitatory layer consists of excitatory synapses with fixed weights between the input layer and the MIF excitatory layer, with one-to-one connections. The output of the excitatory layer includes trainable (via STDP) excitatory recurrent synaptic connections, in addition to fixed-weight excitatory synapses between the MIF excitatory layer and the inhibitory layer, also with one-to-one connections. The inhibitory layer includes inhibitory feedback synapses with fixed weights between the inhibitory layer and the MIF excitatory layer with one-to-(all-1) connections (not including the single MIF neuron connected to the inhibitory neuron). In this neural network, the number of neurons in all three layers are identical, and STDP is enabled within the MIF excitatory layer. The input patterns consist of 32×32 pixels, such that the total number of neurons in each layer is 1024. Each pattern generates a Poisson spike train of 35 \( \mu s \) duration, followed by a 15 \( \mu s \) refractory period without any input such that each input pattern does not affect the network dynamics upon arrival of the next input pattern. Each input spike will generate an alpha current where \( \tau_{\text{sym}} = 10ns \). The threshold of each MIF neuron is set to 25 mV. As in the MIF neuron, there is no extra control circuit to force reset, and we set a refractory of 3 \( \mu s \) to prevent duplicating spikes during the simulation. We find the weight increase has a more significant effect when compared with the weight decrease, and it also enables the network to learn faster. Therefore, we set \( U_{\text{pre}} = 10\mu A \) and \( U_{\text{post}} = -0.1\mu A \). Note that \( U_{\text{pre,post}} \) refers to an internal state variable that is modulated by the current-based neuron model, and is in dimensions of amperes. The recurrent connections are initialized with randomly weighted synaptic currents between 0 to 0.2 \( \mu A \). The exact weight values between excitatory layer and inhibition layer do not have a large effect, which enables the inhibitory neurons to trigger a spike following an output from excitatory neurons. On the other hand, the weights between input-to-excitatory layers and the inhibitory feedback mechanism both need to be carefully tuned to be neither too weak, nor too strong, to prevent complete suppression of downstream spikes, or excessive reinforcement of firing. We chose the fixed input to the excitatory weight to be 50 \( \mu A \), and the fixed inhibitory layer feedback weight to be 20 \( \mu A \).

**Fig. 4.** The memristive spiking neural network architecture, which consists of the input layer, MIF excitatory layer, and the inhibitory layer. The blue arrow indicates excitatory synaptic recurrent connections, the orange arrow shows the inhibitory synaptic forward connection.

### D. Type-2 MSNN for Pattern Recognition

The sequence of the MSNN for pattern recognition is identical to the memory retrieval network, in that we use a Poisson input layer, an excitatory layer, and an inhibitory layer. To improve unsupervised learning we modify the nature of the synaptic connections. STDP-based learning is enabled between the input layer and the excitatory MIF layer with all-to-all connections. As before, each excitatory neuron connects to one inhibitory neuron and the inhibitory layer uses inhibitory synapses with fixed weights connected to the excitatory layer. In this network, no recurrent connections are present due to
the lack of temporal dependencies in the pattern recognition task. The number of neurons between the excitatory and inhibitory layers must be identical, though they no longer need to match the input layer. We use 1024 neurons in the input layer, and 320 neurons each in the excitatory and inhibitory layers, where STDP takes place between the input and the excitatory layers. We set $U_{\text{pre}} = 10nA$, $U_{\text{post}} = -0.1nA$, and the fixed inhibitory layer feedback weight to 200 $\mu A$. The weighted synaptic current between input and excitatory layers are randomly initialized between 0 and 12 $\mu A$ based on empirical evaluation. Additionally, a random 0-2 $\mu s$ delay between input layer and excitatory layer is assigned to avoid excessive simultaneous spiking, thus mitigating the exploding weights problem. All other neuron and input parameters are identical to the memory retrieval tasks.

III. RESULTS

A. Type-1 MSNN for Memory Retrieval Result

We provided four different patterns to the MSNN successively for each iteration, and simulated across multiple epochs. This is to coarsely emulate how biological systems experience real-world data in a batch size of ‘1’ in online learning systems. The Poisson input layer converts each pixel intensity of the input pattern into a spiking probability of each neuron. We used four different patterns, as shown in the top row of Fig. 5. The weight matrix is updated with the STDP rule. The training phase consists of 20 epochs for all patterns, corresponding to 80 iterations.

![Fig. 5. Top row: the four input spiking patterns (1:Square, 2: Cross, 3: Diamond, 4: Triangle) applied to the input of the MSNN. Bottom row: the number of spikes in the excitatory layer during the test stage, upon receiving these four input patterns.](image)

After training, the same four patterns are successively applied to the MIF. The MSNN is expected to ‘recall’ the patterns as the connections have ideally made associations in the form of synaptic memory. When one of the patterns is applied to the MSNN again, other patterns are also recalled with less intensity, which is related to ‘memory retrieval’, illustrated in the bottom row of Fig. 5. In order to evaluate memory retrieval performance, we calculate the percentage of overlapping spike count with incorrect patterns, with the results shown in Fig. 6. We find that when an input pattern is provided to the network, its resemblance to the spiking behavior with the target behavior is at a maximum. This is depicted in Fig. 6 where the values along the diagonal are the largest. As shown in the bottom row of Fig. 5 for each input pattern, the network continues to recall features of the other three patterns, which is a result of low-resistance pathways that cause overlap with other patterns, but with less resemblance to the target pattern.

B. Type-2 MSNN for Pattern Recognition Result

During training, we applied the four different patterns (Fig. 5) to the MSNN successively, then accumulated and recorded the number of spikes in each output MIF neuron for each pattern. During the training process, each MIF neuron is randomly assigned a pattern and updated after every 5 epochs. This allows each MIF neuron to be associated with a pattern such that it may be used to encode one of four patterns during the test stage. After assignments are updated, we use the current weights to test the accuracy of the network. During the test stage, the four patterns are passed to the network for 40 epochs and the total number of spikes are counted for each pattern for all output excitatory neurons. The neuron with the highest spike count is deemed as the winner neuron for this input pattern. The accuracy evolution during training is shown in Fig. 7, where a total accuracy of 97.5% is attained at the 70th iteration, shown by the dashed orange line. Early stopping is applied here, as further training causes excessive reinforcement of high-conductance pathways.

![Fig. 7. Accuracy across multiple iterations.](image)

IV. DISCUSSION AND CONCLUSION

In this paper, we proposed two different types of fully memristive neural networks for unsupervised learning, based on a memristive integrate-and-fire neuron model together with memristive synapses. The synapses and neuron models are designed using SPICE-level memristor models to relate circuit-level plausibility with the biological plausibility of spiking neurons. We demonstrated memory retrieval and pattern recognition across the four input patterns, and validated the potential of our fully-memristive approach across both tasks. Future work will address more challenging tasks, such as testing memory retrieval for incomplete patterns, and increasing dataset complexity for the multi-pattern classification problems. Explorations of new learning paradigms that rely on error-propagation may need to be integrated together with the STDP update rule to enable the success of more complex tasks. The proposed framework will render circuit-level implementations using a broad class of memristors to perform neuromorphic computing.
