Frequency Throttling Side-Channel Attack

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ABSTRACT
Modern processors dynamically control their operating frequency to optimize resource utilization, maximize energy savings, and conform to system-defined constraints. If, during the execution of a software workload, the running average of any electrical or thermal parameter exceeds its corresponding predefined threshold value, the power management architecture will reactively adjust CPU frequency to ensure safe operating conditions. In this paper, we demonstrate how such power management-based frequency throttling activity forms a source of timing side-channel information leakage, which can be exploited by an attacker to infer secret data even from a constant-cycle victim workload. The proposed frequency throttling side-channel attack can be launched by both kernel-space and user-space attackers, thus compromising security guarantees provided by isolation boundaries. We validate our attack methodology across different systems and threat models by performing experiments on a constant-cycle implementation of AES algorithm based on AES-NI instructions. The results of our experimental evaluations demonstrate that the attacker can successfully recover all bytes of an AES key by measuring encryption execution times. Finally, we discuss different options to mitigate the threat posed by frequency throttling side-channel attacks, as well as their advantages and disadvantages.

CCS CONCEPTS
• Security and privacy → Side-channel analysis and countermeasures.

KEYWORDS
Power Management, Frequency Throttling, Side-Channel Analysis

1 INTRODUCTION

Power management architectures of modern processor designs play a central role in optimizing for and balancing between high performance and low power consumption requirements, a product of decades of academic and industry innovation [11, 19, 21, 28, 44, 49]. For example, a widely-used power management architectural mechanism known as Dynamic Voltage and Frequency Scaling (DVFS) is available on Intel®, AMD and ARM CPUs [34, 36]. DVFS dynamically adjusts CPU frequency and voltage in order to reduce system power consumption, yielding higher performance per Watt, or to quickly alter CPU frequency during workload execution, in order to ensure that different electrical and thermal parameters of the system remain below predefined safe limits [5, 8, 28]. Similar such throttling has been recently identified as enabling covert channels [22], given its reliance on shared infrastructure across security domains. In this work, we investigate if such workload-dependent CPU frequency adjustments yield exploitable side-channels.

Modern systems also provide multiple software-accessible telemetry which allow users to characterize bottlenecks at scale [10], monitor resource utilization, power and performance [12, 15, 45], and gain insights into system reliability [23]. Recently, researchers have demonstrated how a processor’s energy telemetry reporting framework can be used maliciously to perform power side-channel analysis attacks [38, 39]. These attacks allow a user-space attacker (having Ring 3 privilege) to infer secret information from a targeted victim workload running inside a Trusted Execution Environment (TEE). In order to thwart such side-channel attacks, CPU vendors (both Intel and AMD) have provided security patches [4, 25] which remove Ring 3 software access to the energy telemetry data via the Linux kernel module. In addition, Intel has also provided a filtering-based mitigation patch [26] to safeguard the reported energy telemetry readings even from a kernel-space attacker (having Ring 0 privilege).

In this paper, we study the potential threat posed by a new type of side-channel information leakage source termed the frequency throttling side-channel. Such a side-channel arises due to the dynamic adjustment of CPU frequency when workload execution causes one or more electrical or thermal system parameters to exceed predefined limits. Typically, in such a scenario, the power management architecture throttles CPU frequency to a lower value to ensure safe operating conditions of the system. Then, depending on the
running average of the parameter(s) in question, CPU frequency is again boosted to a higher value until any limit threshold is violated. Therefore, increases and decreases in CPU frequency (hereinafter, referred to as average throttling frequency) during workload execution are dependent on the instantaneous electrical and thermal parameters being capped by system-defined limits. The average throttled frequency in turn affects the overall execution time of the workload, even if its implementation follows constant-cycle coding principles [24], or it is being executed inside a TEE. The objective of a side-channel attacker is to deduce the targeted secret from a victim workload by monitoring fluctuations in its execution time for processing different inputs. Unlike software-accessible telemetries, frequency throttling side-channel leakage cannot be thwarted by enforcing access restriction or filtering-based mitigation patches. This is because any presumed malicious Ring 3 software can precisely monitor the execution time of a targeted process by reading timestamp counter values (e.g., using the RDTS instruction).

In this work, we demonstrate the applicability of the throttling side-channel attack to retrieve secret information from cryptographic primitives by considering an AES-NI-based AES implementation as a case study, as considered previously in the Platypus attack [38]. While the Platypus attack relies on power consumption information directly exposed to privileged software through a telemetry interface, a frequency throttling side-channel converts the power differences to power limit-induced execution time differences, which are easily accessible by malicious software. It is to be further noted that the Platypus attack and the proposed frequency throttling side-channel attack are two different attacks that exploit the same information leakage source, namely data-correlated power consumption resulting from inherent CMOS circuit properties. Also, both attacks require neither physical access to the target platform nor any additional high-precision power measurement setup as required in traditional side-channel attacks. The results of our experimental evaluations reveal the effectiveness of such an attack in successfully recovering the secret AES key, by performing statistical analysis on the collected timing side-channel traces. In addition, we also discuss potential mitigation options to thwart throttling side-channel attacks, and their pros and cons. The main contributions of this paper can be summarized as follows:

- Presentation and comprehensive explanation of a new type of side-channel attack which exploits the workload-dependent CPU frequency adjustments performed by the power management architecture of modern processors
- Detailed experimental evaluation of the frequency throttling side-channel attack, showing extraction of cryptographic secrets (e.g., AES key) with different reactive limits, attack models, and systems
- Enumerating necessary conditions of a frequency throttling side-channel attack and providing discussion of mitigation options thwarting each of the necessary conditions

The rest of the paper is organized as follows: Section 2 presents background information of power management algorithms and related side-channel attacks. Section 3 presents detailed reasoning behind the frequency throttling side-channel leakage and provides an overview of threat model and attack methodology. Section 4 showcases an attack using the throttling side-channel against an AES-NI-based cryptographic implementation in various scenarios. Section 5 discusses different options to mitigate a frequency throttling side-channel. Section 6 discusses related work. Section 7 concludes the paper.

2 BACKGROUND

2.1 Side-Channel Analysis and Mitigations

2.1.1 Power Side-Channel. Power side-channel analysis attacks exploit the fact that the dynamic power consumption $P_{dyn}$ of a digital CMOS-based circuit is data-dependent in nature [35], as evident in the following equation:

$$P_{dyn} = \alpha \cdot C \cdot V_{DD}^2 \cdot f$$

where, $\alpha$, $C$, $V_{DD}$, and $f$ represent switching activity factor, load capacitance, supply voltage, and clock frequency, respectively. The main objective of a power side-channel analysis attack is to retrieve a targeted secret by analyzing the data-dependent power consumption of a cryptographic implementation during a selected time window. Traditional physical side-channel analysis techniques such as Correlation Power Analysis (CPA) perform statistical analysis on a large number of side-channel traces which are collected by varying the input data [40]. In a typical CPA attack, the attacker correlates the actual power consumption values $P_a$ from the collected power traces with the corresponding hypothetical power leakage values $P_h$ (as calculated using standard Hamming weight or Hamming distance power models). This is done for different key guesses using the following measure:

$$\rho^k = \frac{\text{cov}(P_a, P_h^k)}{\sigma_{P_a} \sigma_{P_h^k}}$$

where, $\rho^k$, $\sigma_{P_a}$, and $\sigma_{P_h^k}$ represent the Pearson’s correlation coefficient for key guess $k$, the standard deviation of the actual power values $P_a$, and the standard deviation of the hypothetical power values $P_h^k$ for key guess $k$, respectively.

2.1.2 Telemetry Side-Channel. Software-accessible telemetry side-channel attack is an emerging topic discussed in recent works [38, 39]. Unlike the traditional physical power side-channel attacks, telemetry side-channel attacks can be conducted remotely by malicious software, exploiting telemetry reading provided by the underlying hardware. For example, Platypus [38] utilizes RAPL energy counter as the side-channel to deduce secret information such as AES keys from Intel® Software Guard Extensions Enclave (Intel® SGX Enclave). The variation in power consumption values due to processing of different data as measured by existing CPU telemetry interfaces (low sampling rates) is much less pronounced when compared to the variations as captured by traditional physical side-channel setups (high sampling rates). In addition, measurement inaccuracy and noise in the telemetry readings further reduce the signal-to-noise ratio (SNR) of the collected side-channel traces. However, in spite of these challenges, it has been demonstrated in [38] that the CPA attack is powerful enough to distinguish minute secret-dependent biases in the telemetry readings and thus, can successfully recover the underlying secret data. In this work, we also use a variation of CPA attack (details in section 4.2.3) to perform statistical analysis on collected telemetry traces.
A number of possible countermeasures to thwart power telemetry attacks were listed in [38]. These mitigation strategies include restricting user-space access (Ring-3 privilege) to powercap driver in Linux and limiting the measurement resolution of telemetry interfaces. In response to the Platypus attack, the Linux powercap driver has been updated to restrict unprivileged access to RAPL interface [4, 25]. In addition, Intel issued a mitigation adding white noise to reported RAPL interface readings, which is enforced when Intel SGX is enabled and can be enabled by software via a software switch [26]. These approaches effectively thwart the CPA attack leveraging software-accessible power telemetry data.

2.1.3 Traditional Timing Side-Channel. In traditional timing side-channel analysis, an attacker exploits differences in execution cycles of victim code to deduce the targeted secret. Such timing differences can arise due to data-dependent execution cycles of the victim process or mutual access of shared system resources (e.g., cache lines, branch predictors, etc.) by the victim and attacker processes.

Several countermeasures have been proposed in related literature, which use constant-cycle coding principles to address the issue of traditional timing side-channel leakage [24]. A short summary of such coding principles is as follows:

- Ensure code processes secret data consistently (i.e., requires same number of clock cycles irrespective of secret data values).
- Ensure secret data values (or values derived from secret data) do not affect the sequence of instructions executed due to a conditional branch or an indirect branch target in the code.
- Ensure memory access patterns (or the data size of load/store operations) are invariant with respect to secret data.

Existing work largely assumes that traditional timing side-channel leakage can be mitigated by applying these principles to the secret data-dependent portions of the code.

2.2 CPU Power Management

We introduce how modern CPU power management algorithms control processors’ power efficiency.

2.2.1 Processor Performance States. Intel processors implement performance states (referred to as P-States, defined per ACPI [13]), by realizing a DVFS mechanism for optimizing power consumption. Such P-States correspond to different voltage-frequency pairs, which can be proactively controlled either by the operating system (using SpeedStep [30]) or by the hardware (using Speed Shift [31]). As per convention, the highest CPU P-State is referred to as P0, and it corresponds to the highest achievable operating frequency, as determined during manufacturing, enabling the processor to enter the so-called turbo mode. AMD processors also implement various schemes to optimize energy efficiency, including ACPI P-States [52]. The platform provides P-States limits, status and voltage, frequency definitions through MSRs [3].

During execution of a workload, if any system-specific limit (electrical or thermal) is violated, the processor P-State is reactively controlled by the power management algorithm. The remainder of the paper focuses on reactive limits, which induce the frequency throttling side-channel. Depending on the criticality of the limit being hit, reactive control of P-States may be performed with various response times (in the order of a few ms to tens of seconds) to promptly bring the system back to safe operating conditions.

2.2.2 P-State Control under Reactive Limits. The power management algorithm of a CPU periodically calculates different running averages of electrical parameters (e.g., power, current, etc.) of windows of pre-specified lengths. Power budget is then computed as the difference between the running averages and the respective reactive limit values. Based on the power budget, the power management algorithm PL_ALG(·) computes the new P-State limit \( f_{\text{max}} \) which is the highest possible CPU operating frequency that satisfies all the reactive limits of the system. An overview of the new \( f_{\text{max}} \) selection process by the controller is presented in Algorithm 1.

When none of the reactive limits are hit, all power budgets remain positive and CPU operating frequency is not capped by \( f_{\text{max}} \) (or, in other words, \( f_{\text{max}} \) is higher than the highest turbo frequency). If any of these calculated running averages exceed a specific reactive limit (e.g., power limit PL1), the power management algorithm will trigger CPU throttling activity and reduce \( f_{\text{max}} \). In such cases, in order to maximize performance while satisfying the reactive limits, the processor may run at the frequency limit \( f_{\text{max}} \) as governed by its feedback control mechanisms [9].

**Algorithm 1 Determination of new P-State limit \( f_{\text{max}} \)**

**Input:**
1. (i) System reactive limit \( PL_i \) with running average time window \( \tau_i \), \( i \in [1, N] \)
2. (ii) Polling interval \( T \)
3. (iii) Current P-State limit \( f_{\text{max}} \)
4. (iv) Power management control algorithm \( PL_{\text{ALG}}(\cdot) \)

**Output:** New P-State limit \( f_{\text{max}} \)

**Input:**
1. for every \( T \) time units do
2. for \( i \) from 1 to \( N \) do
3. \( \bar{P}_i \leftarrow \text{Calculate avg. power over } \tau_i \)
4. \( \Delta \leftarrow T_i - PL_i \) /*Available power budget*/
5. \( f_{\text{max},i} \leftarrow PL_{\text{ALG}}(\Delta) \)
6. if \( f_{\text{max}} > f_{\text{max},i} \) then
7. \( f_{\text{max}} = f_{\text{max},i} \) /*Throttling activity*/
8. end if
9. end for
10. end for

2.2.3 Reactive Limits on Intel processors. We describe two of the reactive limits present in several modern Intel processors [28].

- **Running Average Power Limit (RAPL):** RAPL is a feature supported by Intel power management architecture to cap the power consumption on the system. When the configured power limit is exceeded, the CPU will be forced to run at a lower frequency to maximize performance while meeting the power limit requirement. Intel currently provides multiple power limit capabilities. The most commonly used ones are the package-level power limit 1 (PL1) and package-level power limit 2 (PL2). PL1 is used to track the long-term power consumption, so typically its limit value is set to be lower and the time window \( \tau \) is longer (tens of seconds). On the other hand, PL2 is used to track the...
short-time power burst events, so typically the limit is set to be higher than PL1 and $\tau$ is much shorter (several milliseconds). Ring 0 software can configure the running average window $\tau$ and the power limit of each capability through interfaces such as MSRs (e.g., MSR_PKG_POWER_LIMIT for package-level power limits).

- **Voltage Regulator Thermal Design Current Limit (VR-TDC):** VR-TDC is a power management feature supported by Intel power management architecture. It is a current limit specified in Amperes, maintained in order to satisfy VR electrical constraints. Generally, the algorithm monitors the running average current in Amperes by reading the VR current sensor during the configured time window. If the limit is hit, the processor will engage its frequency throttling to reduce its frequency, in order to ensure current remains within the limit and budget.

2.2.4 *Reactive Limits on AMD processors.* Precision Boost Overdrive (PBO) is a feature available on AMD Ryzen to overclock processors to achieve more performance by controlling power/thermal limits [55]. Some of the reactive limits are described as follows:

- **Package Power Tracking (PPT):** analogous to PL1 on Intel processors, this limit caps the total power capacity of the processor socket in Watts [7].
- **Package Power Tracking Fast (PPT Fast):** analogous to PL2 on Intel processors, this limit is a PPT limit with faster response time (shorter $\tau$).
- **Thermal Design Current (TDC):** analogous to VR-TDC on Intel processors, this limit caps the total current capacity in Amperes at the thermal throttling limit of the processor [7].

The aforementioned reactive limits can be configured from system software via System Management Unit (SMU) mailbox interface with support from a kernel driver [1, 37]. The SMU is a subcomponent of the AMD processor that is responsible for a variety of system and power management tasks during boot and runtime [2]. The command to configure the reactive limits is described in [37]. It specifies the SMU mailbox ID and power/thermal limit value to set the reactive limit [37]. The SMU mailbox IDs for the reactive limits on different AMD platform are described in [32].

### 3 FREQUENCY THROTTLING SIDE-CHANNEL

In this work, we demonstrate how an attacker can leverage reactive limit triggered frequency throttling to create a novel source of timing side-channel leakage during workload execution. We show that mere application of constant-cycle coding principles is insufficient to thwart timing side-channel attacks, as system clock frequency may vary during the code execution phase and may be data-dependent to leak information.

#### 3.1 Attack Primitives

In modern processors, a major source of throttling side-channel information leakage is related to the workload-dependent reactive control of $P$-States (line 11 of Algorithm 1). Let us consider the example presented in Fig. 1 to understand the underlying implementation details leading to such throttling side-channel leakage. Suppose that the workload under execution is a constant-cycle implementation of a function, $\text{foo}(\text{arg data})$, with input argument $\text{data}$. As noted in section 2.1.3, such a constant-cycle implementation has no traditional timing side-channel leakage. On the other hand, the power consumption of the workload due to processing different data inputs ($\text{data}_1$ and $\text{data}_2$) might vary due to the differences in internal data-dependent computations of the $\text{foo}$ function. Without loss of generality, let us assume that the processing of $\text{data}_1$ consumes higher power ($P_1$) compared to that of $\text{data}_2$ ($P_2$) (i.e., $P_1 > P_2$). As illustrated in Fig. 1(a), if both $P_1$ and $P_2$ are below all system-defined reactive limits, there is no throttling activity and system frequency $f_{\text{default}}$ remains the same irrespective of data consumed by $\text{foo}$. Therefore, in this case, there is no data-dependent timing side-channel information leakage, as the execution time of the workload is independent of the inputs.

However, when power consumption reaches or crosses the system’s electrical reactive limits (e.g., the limit is configured to a lower value, or a power-hungry stressor code is executed in parallel with function $\text{foo}$) as illustrated using Fig. 1(b), reactive limit induced throttling activity will be triggered, resulting in a change to $P$-States, as shown in Fig. 1(c). Since $P_1 > P_2$, the average throttling frequency $f_1$ for data input $\text{data}_1$ will be lower than the average

![Figure 1: Conversion of power side-channel to timing side-channel leakage by reactive limit-induced throttling.](image_url)
throttling frequency $f_2$ for data input $data_2$ to satisfy the same reactive limit. Both of these throttling frequencies will be lower than the default system frequency prior to throttling (i.e., $f_1 < f_2 < f_{default}$). Crucially, as shown in Fig. 1(c), the execution time of $foo$ with frequency $f_1$ is higher compared to its execution time with frequency $f_2$. Therefore, even though $foo$ is a constant-cycle workload implementation, its execution time becomes data-dependent due to such frequency throttling activity. This forms a new type of side-channel information leakage source in modern processors, which we refer to as the frequency throttling side-channel.

To visually appreciate the primitive, we design and run a proof-of-concept (PoC) code on an Intel E3-1230V5 system, plotted in Figure 2. The function $foo$ we use is composed of 2.8 billion IMUL instructions, which is a cycle-constant instruction. Each IMUL instruction has one operand fixed and the other operand set to either $data_1 = 0x0$ or $data_2 = 0xAA.AA$. In the first run, we configure reactive limits to high values that will not be reached, to prevent throttling from happening, and then execute $foo$ with $data_1$ and $data_2$, measuring aggregated package energy consumption and time elapsed for $foo$. After repeating 100 times, we plot histograms of the average power consumption (calculated from energy dividing by time) and the time elapsed in Figure 2 (a), respectively. As can be observed, the $0xAA$ case consumes more power than the $0x00$ case and the time it takes to execute $foo$ for the two operands is identical. The second run duplicates the first run, except for reducing Power Limit 1 (PL1) to 8W and corresponding PL1 $\tau$ to 1s. With this setting, PL1 is hit, and frequency throttling is triggered. As can be seen from Figure 2 (b), power consumption distributions with different data become indistinguishable and both are capped at 8W, which is the power limit. Critically, $foo$ now takes a longer time to execute with $0xAA$ compared to $0x00$, while both are slower than the case without throttling. The results confirm that reactive limit induced throttling converts a power side-channel to a timing side-channel. Of note, Intel’s Platypus mitigation can hide the information leakage exhibited in the power domain, but is not designed to mitigate the frequency throttling side-channel. Therefore, the frequency throttling side-channel is observable even if such mitigation is enabled.

3.2 Overview of Frequency Throttling Side-Channel Attack

3.2.1 Threat Model. We assume the following attack scenarios for an adversary exploiting a frequency throttling side-channel against a victim workload across security boundaries.

- **Attack Scenario 1:** The attacker is a privileged software attacker, such as kernel-space software or a hypervisor. The victim workload is executed inside a Trusted Execution Environment (TEE), such as Intel SGX [14, 27] or AMD SEV [33, 43]. Such TEEs help protect secret information of the victim application from direct access by even privileged software. In order to enable higher throttling activity during the execution of code residing in a TEE, a privileged attacker may alter reactive limit configurations. Discussion of this scenario is provided in section 4.4.

- **Attack Scenario 2:** The attacker is a user-space attacker with Ring 3 privilege, and the victim is another application or the kernel. Unlike the previous scenario, the attacker does not have the privilege to alter the values or $\tau$ of the reactive limits. A Ring 3 attacker instead may execute a stressor code in parallel to the victim code to boost the system power consumption beyond the default limits, such that throttling activity is triggered. Note that the long $\tau$ and additional noise introduced by the stressor code will make the attack harder. Discussion of this scenario is provided in section 4.5.

In addition, we assume that the victim code under consideration is implemented following the constant-cycle coding principles highlighted in section 2.1.3. In order to attack such a workload, an attacker utilizes the reactive limit-induced throttling (see section 3.1) to make the execution time of the code vary for different known data inputs. The main objective of the attacker (for both of the above attack scenarios) is to deduce the targeted secret information of victim code by correlating the secret data-dependent computations with the collected execution time of the code for different data inputs.

3.2.2 Attack Methodology. Fig. 3 presents an overview of the throttling side-channel attack against a constant-cycle implementation of victim workload. Such an attack consists of the following three phases:

- **Configuration Phase:** The attacker profiles a victim-like workload with a known asset to either configure the related power
management settings (Ring 0 attacker) or identify a suitable stressor code (Ring 3 attacker) such that victim workload execution will result in triggering frequency throttling.

- **Online Phase:** The attacker provides different data inputs to the victim code, which in turn performs one or more secret asset-dependent computations. The attacker also runs a monitor program in parallel to measure the execution time of the victim code with various data inputs.

- **Analysis Phase:** The attacker applies analysis methods (such as CPA) on the collected execution time values, to deduce the targeted secret asset of the victim code.

4 CASE STUDY: ATTACK AGAINST AES ENCRYPTION

In this section, we consider a victim workload comprising an AES-NI-based implementation of AES-128 as a case study to illustrate the proposed throttling side-channel attack. In order to assess the side-channel leakage due to throttling activity, we use statistical analysis methods derived from Test Vector Leakage Assessment (TVLA) [18, 53] and correlation-based analysis.

4.1 Victim Workload

4.1.1 AES-128 Algorithm. AES is a block cipher established by NIST in 2001 [46]. The algorithm encrypts a fixed size plaintext block of 128-bit using key-size of 128, 192, or 256 bits and outputs a 128-bit ciphertext. In this work, we consider the AES-128 primitive to demonstrate frequency throttling side-channel attack.

4.1.2 AES-NI-Based AES Implementation. AES-NI is an instruction set which improves the AES implementation by accelerating its complex performance-intensive steps using dedicated hardware [20]. AES-NI instructions also provide improved security against side-channel attacks due to their constant-cycle implementations. AES-NI instructions are supported by x86 processors of major vendors, including Intel and AMD. To perform encryption, first individual round keys are derived using the KeyExpansion procedure [20]. This is followed by the Initial AddRoundKey operation, which computes the bitwise XOR between the plaintext and the initial round key. AESENC instruction is then used to perform a single round of encryption with round state and round key as the input operands. The AESENCLAST instruction performs the last round of encryption and returns the ciphertext.

4.2 Attack Methodology Details

As outlined in section 3.2.2, the frequency throttling side-channel attack against a victim workload comprises three distinct phases: the configuration, the online, and the analysis phases. Next, we present the details of each of these phases as adopted in our case study, using power limit as an example.

4.2.1 Configuration phase. During the configuration phase, the privileged software attacker first profiles the AES-NI-based victim workload to estimate $P$, which is the power consumption of the victim workload without frequency throttling. Then, in order to trigger throttling activity, a privileged software attacker may adjust the system’s power limit value $PL$ such that $P > PL$. As per Algorithm 1, such an adjustment will lead to a change in $P$-State that satisfies the available power budget. In order to ensure that there is data-dependent frequency throttling activity, the value of the reactive limit $PL$ should be carefully adjusted: setting the $PL$ value too high will not satisfy the requirement of $P > PL$ whereas setting the $PL$ value too low will cause the system to execute in a constant low frequency. For a user-space attacker who does not have the privilege to configure $PL$, an alternative approach is to run a stressor workload to boost power consumption. The details will be discussed in section 4.5.

4.2.2 Online phase. During the online phase, the attacker inputs plaintext to the victim workload and obtains the corresponding ciphertext as output. Note that due to PL-induced throttling activity, different plaintexts will result in different processing times which correspond to the side-channel traces. During the $i^{th}$ trace collection, the attacker first records the starting time stamp counter value ($T_0^i$) just before sending the $i^{th}$ plaintext to the victim workload and subsequently, also records the end time stamp counter value ($T_1^i$) just after receiving the $i^{th}$ ciphertext. Then, the attacker calculates the corresponding execution time $T_1^i = T_2^i - T_0^i$. On most of the modern CPUs, incrementing of the time stamp counter is frequency-invariant so the $T_0^i$ captures wall clock time of the victim’s execution time and will not be impacted by frequency throttling [6, 28].

Techniques to reduce Minimum Time to Disclosure: We define Minimum Time to Disclosure (MTD) as the minimum time spent to collecting enough side-channel traces to recover the secret information. Reduction in MTD can be achieved by (i) increasing the Signal-to-Noise (SNR) of the captured traces, or (ii) decreasing the collection time of each trace [40]. In our experiments, we adopted the following techniques to lower the MTD of frequency throttling side-channel attack:

- Multiple instances of the victim workload were executed simultaneously across different processor cores to amplify its average power consumption, which in turn results in higher SNR of the collected traces.

- Each instance of the victim workload was executed repeatedly $N$ times with the same input to collect one trace. This approach not only ensured that the on-chip sensors accurately sampled the average power consumption of the victim workload during a reactive limit’s $r$ window but also boosted the SNR of collected traces for a sufficiently large value of $N$ (which spans across multiple $r$ windows) due to the denoising effect of averaging [56].

- Selection of a system reactive limit having the lowest possible configurable value of $r$ to trigger throttling activity during victim workload execution. For a chosen value of $N$, the trace collection time corresponding to a reactive limit having lower $r$ will be shorter compared to that corresponding to a reactive limit with higher $r$. Of course, such selection or adjustment of a reactive limit is only applicable to a privileged attacker.

4.2.3 Analysis phase. We utilize two statistical techniques to analyze potential side-channel information leakage arising from throttling side-channel activity: (i) First, in order to ascertain if different data exhibit different PL-induced throttling behavior, we apply TVLA to the corresponding timing traces. (ii) Second, depending upon the positive outcome of the TVLA, we perform a CPA attack
in order to determine if the targeted AES encryption key can be recovered by analyzing the collected timing side-channel traces. Next, we present the details of these statistical techniques as adopted in our experiments.

**TVLA:** TVLA methodology utilizes t-scores generated from Welch’s t-test to assess potential side-channel leakage in cryptographic implementations [17]. Welch’s t-test defines a statistical measure, t-score, as shown in equation (3) to compare two datasets A and B

\[ t \text{-score} = \frac{\mu_1 - \mu_2}{\sqrt{s_1^2/N_1 + s_2^2/N_2}} \]  

where, \( \mu_1, \mu_2 \) are sample means, \( s_1^2, s_2^2 \) are sample variances, and \( N_1, N_2 \) are the number of samples in datasets A and B, respectively. A |\( t \text{-score} | > 4.5 \) rejects the null hypothesis with 99.999% confidence, indicating datasets A and B are statistically distinguishable [51].

In this case study, we assess the throttling side-channel leakage of an AES-NI based AES implementation victim workload using the above-mentioned TVLA methodology. We collect the timing traces corresponding to encryption of three different sets of plaintexts: All_one, All_zero and Random. We apply TVLA test on timing traces for all possible pairs of chosen plaintexts.

**CPA Attack:** We also apply CPA attack to recover the secret key from the AES-NI based victim workload by collecting timing traces \( T_b \) corresponding to different randomly generated plaintexts. Then, we utilized the following equation to calculate the Pearson’s correlation coefficient metric \( \gamma^k \) for different key guess \( k \).

\[ \gamma^k = \frac{\text{cov}(T_b^k, T_h^k)}{\sigma_{T_b^k} \sigma_{T_h^k}} \]  

where, \( \sigma_{T_b^k} \) and \( \sigma_{T_h^k} \) represent the standard deviations of the actual PL-induced execution time traces \( T_b \) and the hypothetical execution time estimations \( T_h^k \), respectively. Note that similar to power estimates, such execution time estimates can also be obtained using standard Hamming weight (HW) or Hamming distance (HD) models. This is because the PL-induced execution time variations of the victim workload are proportional to the corresponding power consumption variations.

The attacker may choose either the initial round (targeting initial AddRoundKey round key \( k_0 \)) or the last round (targeting last round key \( k_{10} \)) of AES implementation as point of attack. Intermediate AES rounds are typically not considered as attack points because in those cases the corresponding hypothetical execution time values become a function of multiple round keys, thus substantially increasing attack complexity. Selection of hypothetical execution time model \( T_h^k \) is based on the point of attack [42, 50]:

- **Round0-HW:** To recover the initial round key \( k_0 \), the hypothetical execution time values can be modeled using HW of the initial AddRoundKey output.

- **Round10-HW:** To recover the last round key \( k_{10} \), the hypothetical execution time values can be modeled using HW of last round input, derived using ciphertext and hypothesis of \( k_{10} \).

- **Round10-HD:** Also, the attacker can model the hypothetical execution time values using HD between last round input and ciphertext, derived using ciphertext and hypothesis of \( k_{10} \).

- **Round10-HW+HD:** We also considered a leakage model comprising the sum of Round10-HW and Round10-HD models, derived using ciphertext and hypothesis of \( k_{10} \).

We use Guessing Entropy (GE) to evaluate the success of a CPA attack, based on the metric from [48]. For byte \( i \) of the round key, all possible key guesses are sorted in descending order of their correlation coefficient, to obtain the rank of the correct key byte. For all bytes of the guessed key, the ranks are summed up (logarithmically) to get GE, as shown in Equation (5).

\[ \text{GE} = \sum_{i=1}^{16} \log_2 [\text{rank}(k_i^{\text{correct key}})] \]  

Lower GE indicates lower average ranks across all key bytes and, most of the time, means more key bytes are recovered successfully. A value of \( \text{GE}=0 \) implies all key bytes have been recovered. In practice, a successful CPA attack should result in a GE value lower than a pre-defined threshold which allows the recovery of the key bytes with reasonable computational complexity.

### 4.3 Evaluation

In this section, we implement a Proof-of-Concept (PoC) code to demonstrate secret key recovery from an AES-NI based victim workload as outlined in section 4.1. Our experiments mainly focus on Intel systems, where we consider both power limit induced and current limit induced frequency throttling activity during trace collection. We also demonstrate cross-platform applicability of the attack through experimental evaluation on an AMD processor.

#### 4.3.1 Experimental Setup

In our PoC, the AES encryption workload is repeated (with the same plaintext and key for encryption) for many iterations. On the same thread, the measurement code measures the aggregated execution time of the victim using time stamp counter and logs it a single trace. The number of iterations is calibrated on each system such that every trace spans approximately 45ms (i.e., \( T_b=45ms \)). To boost SNR, multiple instances of the same victim workload are executed in parallel on the other cores.

For experimental evaluations, we considered three Intel systems: E3-1230V5, i7-1185G7, and Xeon Gold 6326 and one AMD system: Ryzen 5 5600G. Table 1 lists the details of different systems along with their corresponding PL2 (or PPT Fast for AMD system) values as adjusted in the configuration phase of the attack to introduce frequency throttling activity during workload execution. The reason behind selection of PL2 (PPT Fast for AMD system) is due to the lower default time window \( \tau \), which can be configured further to a shorter window of 2ms in an Intel system. Note that a lower \( \tau \) value reduces the minimal trace length and hence, reduces the MTD requirement as discussed in section 4.2.2. Also, note that since Xeon Gold 6326 is a 2-socket server system with power limits being defined independently per socket, we run the victim workload on socket 0 and adjust only PL2 corresponding to socket 0.

We first report the experimental outcomes of TVLA tests to highlight potential side-channel information leakage arising from frequency throttling activity. Then, we present the results of a CPA attack to demonstrate how an attacker can successfully recover the secret key by collecting timing side-channel traces of the AES implementation. We first test the victim code outside a TEE to
Table 1: Information and configurations of the systems under test.

| Processor Number       | # of physical cores | Max Turbo frequency | SMT | PL2/PPT Fast limit value | PL2 τ |
|------------------------|---------------------|---------------------|-----|--------------------------|-------|
| Intel E3-1230V5        | 4                   | 3.8 GHz             | disabled | 10W                      | 2ms   |
| Intel i7-1185G7        | 2                   | 4.1 GHz             | disabled | 8W                       | 2ms   |
| Intel Xeon Gold 6326   | 8/socket            | 3.5 GHz             | disabled | 50W                      | 2ms   |
| AMD Ryzen 5 5600G      | 6                   | 3.2 GHz             | disabled | 15W                      | -     |

Table 2: Pairwise t-score (absolute value) among All_zero, All_one, and Random traces. T-score greater than 4.5 are marked in bold and indicates the set of data are statistically distinguishable.

| All_zero_2 | All_one_2 | Random_2 | Intel E3-1230V5 | All_zero_2 | All_one_2 | Random_2 | Intel i7-1185G7 | All_zero_2 | All_one_2 | Random_2 | Intel Xeon Gold 6326 | All_zero_2 | All_one_2 | Random_2 |
|------------|-----------|----------|-----------------|------------|-----------|----------|-----------------|------------|-----------|----------|----------------------|------------|-----------|----------|
| 1.02       | 41.02     | 26.20    | 0.23            | 10.57      | 5.32      | 0.45     | 19.82           | 12.51      |           |          |                      |            |           |          |
| 38.42      | 41.02     | 26.20    | 12.58           | 3.02       | 8.08      | 19.74    | 0.53            | 7.57       |           |          |                      |            |           |          |
| 24.07      | 14.28     | 2.36     | 1.32            | 9.23       | 3.84      | 11.27    | 7.72            | 0.68       |           |          |                      |            |           |          |

Table 3: Converged Guessing Entropy (GE) on different systems with different leakage models. Lower GE implies more key bytes are recovered.

| System        | Intel E3 | Intel i7 | Intel Xeon | AMD Ryzen |
|---------------|----------|----------|------------|-----------|
| Round0-HW     | 17.5     | 27.5     | 2.6        | 2.0       |
| Round10-HW    | 85.7     | 73.3     | 86.0       | 3.16      |
| Round10-HD    | 0        | 27.3     | 81.2       | 35.8      |
| Round10-HW+HD | 0        | 21.4     | 72.7       | 1.5       |

On each of the Intel systems, we collected 8 million timing traces of the PoC code (with a fixed key) by providing randomly generated plaintexts. The trace collection process took about 100 hours on average across different systems. After the trace collection phase, we computed the median μ of the collected traces and discarded the outliers of [0.95μ, 1.05μ]. Subsequently, we applied the CPA attack on the filtered trace dataset, targeting the round keys k₀ and k₁₀.

In Figure 4, we present the GE trends (corresponding to different execution time estimate models) versus the number of timing traces considered for the CPA attack across multiple systems. Based on the data, we make the following observations:

- **The general trend** is that GE converges gradually when increasing number of traces are used for analysis. This is because a larger number of traces helps to reduce the effect of noise in the collected traces. Such GE trends highlight the fact that all the execution time estimate models considered correlate with the actual execution times of the PoC code. Also, it can be observed that in all cases, GE values start from somewhere around 112. This is because the expected value of the initial rank of correct key byte (without parsing any side-channel traces) is 128 among the 256 possible key byte guesses. Therefore, the expected value of initial GE value is $E(\text{GE}) = \sum_{i=0}^{127} \log_2(128) = 112$.

- **Round0-HW model** appears to be effective on all the three systems: GE converges to 17.5 on E3-1230V5, 27.5 on i7-1185G7, and 2.6 on Xeon Gold 6326. Especially, on Xeon Gold 6326, with this execution time estimate model, we successfully recovered **14 out of the 16 bytes of the correct key**. The ranks of the remaining two key bytes are 2 and 3.

- **Round10-HW model** converges the slowest among all the models tested. On both E3-1230V5 and Xeon Gold 6326 systems, even after analyzing with 8M traces the GE values remain above 80, signifying that the CPA attack was unsuccessful in these cases. The lowest GE value obtained was 73.3 on i7-1185G7 system.

- **Round10-HD model** shows distinctly different behaviors on different systems. On E3-1230V5 system, for example, GE converges to 0 (all 16 key bytes recovered) with less than 2M traces. Also, on i7-1185G7 system, for this model GE converges to 27.3, similar to Round0-HW model. But in the case of the Xeon Gold 6326 system, for this model the GE value reduces to only 81.2.

- **Round10-HW+HD model** results in consistently lower GE values compared to the Round10-HW model across all the three
systems. However, compared to the Round10-HD model, for this model the GE value converges slower on E3-1230V5 systems whereas the GE values converge faster on i7-1185G7 and Xeon Gold 6326 systems.

Note that for a given execution time estimate model, the difference in behavior of GE trends on different systems is likely due to variations in the underlying hardware micro-architecture designs and the fabrication technologies used. Table 3 summarizes the outcomes of the CPA attack corresponding to different execution time estimate models across systems. These results demonstrate the fact that power-limit induced frequency throttling activity can be successfully leveraged by an attacker to extract secret information from cryptographic workloads.

4.3.4 CPA Attack Results with Current Limit. We also repeated the CPA test on the i7-1185G7 system with VR-TDC limit set to 7 Amperes to trigger frequency throttling. All other configurations were kept the same as used for the power-limit induced frequency throttling experiments in the previous subsection. The GE trends for different execution time estimate models are shown in Figure 5. Similar to the power-limit experiments, the GE value corresponding to the Round10-HW model converges the slowest amongst all the models tested. The GE values for both Round0-HW and Round10-HD models converge to around 20 after analyzing with 8M traces. The GE value corresponding to Round10-HW+HD model converges to the lowest value (around 10) for the CPA attack with current limit. These observations confirm the fact that VR-TDC limit can also be leveraged by an attacker to mount the frequency throttling side-channel attack.

4.3.5 CPA Attack Results on AMD Ryzen 5. We also repeated the CPA test on an AMD Ryzen 5 5600G system with PPT Fast Limit set to 15W to trigger frequency throttling. The victim AES workload was executed using the configuration mentioned in last row of Table 1 and the number of iterations of the workload was calibrated such that every trace spans approximately 50ms (i.e., $T_{δ}=50$ms). We collected 4.5M traces with trace collection time of about 63 hours.

Figure 6 shows the trend in GE against the number of traces collected for CPA analysis across different execution timing estimate models. From the figure, we can observe that GE converges much faster with Round0-HW model as compared to other execution timing estimate models. The GE value converges to almost zero for approximately 1 million traces (in 16 hours) with Round-0 HW model, recovering 14 out of the 16 secret key bytes. A similar trend in GE was observed for other models as well; the GE values converged to (a) almost zero for approximately 3 million traces with Round10-HW and Round10-HW+HD models and (b) about 40 for approximately 4.5 million traces with Round10-HD model.
Table 3 summarizes the final converged GE values with different execution time estimate models on the systems we tested.

### 4.4 Attacking AES-NI inside Intel® SGX enclave

We also evaluated an AES-NI based AES implementation from Intel’s Integrated Performance Primitives (Intel IPP) [29] as the victim workload, executed inside an Intel SGX enclave. The victim takes a 16-byte plaintext as the input from Enclave Call (ECALL) and encrypts it using a secret key owned by the enclave. Similar to the experiment setup in section 4.3, the victim workload repeatedly encrypts the same plaintext many iterations to boost SNR: ippsAESencryptedECB is invoked 10000 times per trace, and each invocation encrypts 1024 16-bytes of the same plaintext. In entirety, 160 MB of data is encrypted in each ECALL. Ciphertext is returned to the caller of the enclave after encryption. Also, to boost SNR, we invoke multiple enclave instances, executing on multiple cores in parallel with the same plaintext as input. Only the execution time for one enclave is recorded as timing traces.

We performed the experimental evaluation on an Intel E3-1230V5 system, with PL2 limit and \( r \) set to 20W and 2ms, respectively. We followed TVLA test methodology as described in section 4.2.3 and collected 10000 timing traces corresponding to the encryption of each of the plaintexts (All\(_\text{one}\), All\(_\text{zero}\), and Random). The pairwise t-scores are presented in Table 4. We observed that the t-score values between timing traces corresponding to different plaintexts are greater than 4.5, while the t-score values between timing traces corresponding to the same plaintext are lower than 4.5, indicating data-dependent leakage in the time domain, due to PL-induced throttling activity. The only exception is Random\(_2\) vs. All\(_\text{zero}_1\), which shows a t-score value less than 4.5. Upon comparing the TVLA results on the same system (E3-1230V5) for the victim workload outside an SGX enclave (Table 2), we observe the magnitude of the t-scores (in most cases) for the victim executing inside an SGX enclave is lower. This is due to the additional noise introduced during enclave transitions, as well as IPP crypto function calls.

**Table 4: Pairwise t-score (absolute value) among All\(_\text{zero}\), All\(_\text{one}\), and Random traces, test on E3-1230V5 with victim workload inside Intel SGX enclave.**

| E3-1230V5 (Intel SGX victim workload) | All\(_\text{zero}_1\) | All\(_\text{one}_1\) | Random\(_1\) |
|--------------------------------------|----------------------|-------------------|------------|
| All\(_\text{zero}_1\)                 | 1.19                 | 29.19             | 24.31      |
| All\(_\text{one}_1\)                 | 33.12                | 3.65              | 2.20       |
| Random\(_1\)                        | 26.47                | 6.17              | 0.96       |

In a CPA test, we collected 8 million traces with \( T_5=45\) ms per trace, which took about 100 hours in total. The traces are analyzed with different leakage models and the results are shown in Figure 7. With Round10-HD model, guessing entropy converges to 6 (14 out of 16 key bytes recovered) with the 8 million traces, confirming that information is observable through the throttling side-channel for the given victim. Compared to the previous CPA result on E3-1230V5 system (Figure 4(a)), the additional noise results in lower SNR, and hence slower guessing entropy convergence (less key bytes being revealed with the same amount of traces) for all the leakage models. For example, in the previous test on the same system (Figure 4(a)), a full key can be recovered from a victim outside an SGX enclave with less than 2 million traces (25 hours).

### 4.5 User-Space Attack

We studied the feasibility of a user-space attack following the threat model assumed in Attack Scenario 2 (see Section 3.2.1). A user-space attacker also follows the attack methodology as presented in section 3.2.2. However, unlike a privileged attacker, a user-space attacker does not have the privilege to configure the reactive limits and hence, has to utilize the existing reactive limit settings. This results in two implications: first, for most of the time, the attacker can only leverage the PL1 limit (or PPT limit on AMD system) to trigger frequency throttling as the default PL1 limit is typically set lower than the other reactive limits. However, PL1 limit usually has a much larger default \( r \) window (in the order of tens of seconds) compared to that of PL2 limit, and hence, trace collection time due to PL1 limit-induced throttling will be significantly longer as well (see section 4.2.2). Second, it is possible that the power consumption of a victim workload does not exceed even the PL1 limit, thus failing to trigger any throttling activity, requiring the adversary to compensate.

In order to overcome the limitations of the second implication, the user-space attacker can execute a suitable stressor code in parallel with the victim workload to boost the cumulative power consumption \( P \) such that it exceeds a reactive limit of the system. According to Algorithm 1 (line 8), a significant boost in \( P \) will lead to a reduction of the available power budget \( \Delta \) below a certain threshold, which in turn will trigger frequency throttling activity. Stressor code selection requires the following careful considerations: first, power consumption of the stressor code should be as low as possible, so that it does not introduce significant additional noise in the collected side-channel traces. Third, the stressor code should have minimal resource contention (e.g., contention for ports or execution units) with the victim workload, to further reduce noise. Additionally, the execution of the stressor code should not cause the system temperature to exceed the thermal limit, since in that case the collected side-channel traces will be affected by noise introduced due to thermal throttling. Therefore, as evident from the above requirements, the selection procedure of a suitable...
stressor code for a given victim workload and system under test could be a challenging task for the user-space attacker.

We performed experimental evaluations for the user-space attack scenario on an Intel i7-10700K system using its available 8 physical cores/16 logical cores (with SMT enabled). At first, we profiled the power consumption $P_{victim}$ of victim workload (AES-NI based AES implementation) by simultaneously executing multiple instances of it on 8 different physical cores and observed that $P_{victim}$ is about 83W. Next, we considered the following four test cases by assuming the default PL1 limit at different levels (but with the same $r$ window of about 56s):

1. PL1 limit set to 80W. Only victim workload is executed.
2. PL1 limit set to 110W. Only victim workload is executed.
3. PL1 limit set to 110W. Stressor and victim workloads executed.
4. PL1 limit set to 140W. Stressor and victim workloads executed.

For all the above cases, we performed TVLA tests, by collecting 1,000 timing side-channel traces (with $T_b = 1s$) corresponding to the encryption of each of the plaintext sets as considered previously. Note that in these tests, we set $T_b$ to a much larger value (compared to 45ms as used in privileged attacker scenario) due to the high default value of PL1 $r$ window. Additionally, for cases (3) and (4), a stressor code consisted of repeated execution of MOVB instructions across 6 different threads was running in parallel with the victim.

The results of the test cases are reported in Table 5 from left to right. For test case (1), when PL1=80W and is lower than $P_{victim}$, we observe high t-score values between different pairs of plaintext sets, signifying significant throttling side-channel leakage from the victim workload execution even without stressor code. For test case (2), when PL1=110W and without any stressor code, we do not observe any leakage after analyzing the collected timing traces corresponding to the execution of victim workload. This is an expected outcome, since in this case the limit is higher and $P_{victim}$ fails to trigger PL1-induced frequency throttling activity.

This was the reason for introducing stressor code. For test case (3), when the stressor code was executed in parallel to the victim workload, the cumulative system power consumption $P$ hit the PL1 limit, leading to throttling side-channel leakage, as evident from the corresponding high t-score values in the third column. This shows that the stressor code is effective in inducing throttling side-channel leakage. For test case (4), when PL1=140W, we observed that the simultaneous execution of the victim and stressor workloads caused system temperature to rise to 100°C, thus triggering thermal throttling before triggering PL1-based throttling. Thermal throttling degraded the SNR of collected timing traces, thus leading to low t-score values as reported in the last column of Table 5.

In this paper, for the user-space attack scenario, we limited our experimental evaluations to TVLA tests, as it was infeasible to perform a CPA attack against an AES-NI based AES implementation, because of its very high MTD requirements for collecting millions of telemetry side-channel traces. Importantly, in case of side-channel analysis of cryptosystems which require low number of traces, a user-space attack exploiting frequency throttling activity can be realized with a reasonable MTD. For example, in [54], the authors demonstrate how a Ring 3 attacker utilizes the throttling side-channel information to extract keys from a post-quantum key encapsulation scheme within a few days, exploiting a corner case in the algorithm implementation.

5 MITIGATION

In this section, we discuss different countermeasures to safeguard a victim workload from being susceptible to frequency throttling side-channel attacks. Before going to the details of the mitigation strategies, we first summarize the conditions that must be satisfied to mount such an attack.

- **Condition 1 (Secret Dependency):** The victim code processes a secret asset that is vulnerable to a power side-channel attack. This requires (i) the victim software implementation to be vulnerable to traditional physical side-channel attacks and (ii) the underlying hardware system to exhibit variation in power consumption profiles for processing different data.

- **Condition 2 (Controller Actuation):** One of the reactive limits of the system is being hit during victim code execution. This will cause the power management architecture to trigger frequency throttling activity based on the available power budget (see Algorithm 1 for details).

- **Condition 3 (Observability):** The attacker can monitor the execution time (wall clock time) of the victim code with sufficiently high resolution, or else an equivalent quantity.

In order to thwart side-channel information leakage due to frequency throttling activity, the designer should consider targeting the above-mentioned necessary conditions. Next, we present different potential countermeasure options along with their respective advantages and disadvantages.

5.1 Analysis of Secret Dependency

5.1.1 Necessary conditions of Secret Dependency. Since power side-channel is the fundamental root cause of frequency throttling side-channel, the necessary conditions for the physical power side-channel attack also need to be satisfied for throttling side-channel (except for the physical access capability to measure power). First, the victim application needs to process a secret asset (e.g., cryptographic key) with a confidentiality requirement. Second, power consumption of the underlying hardware processing the secret needs to correlate with the asset. Third, the implementation of the victim application is susceptible to power side-channel attack. For example, the victim application provides the capability for the adversary to repeatedly initiate cryptographic operations with the same sensitive key to collect enough data. Also, for block ciphers,
the adversary should have the ability to read input/output or inter-round state of the block cipher primitives. Please note that the input/output is not necessarily the plaintext or ciphertext. One example is the counter (CTR) mode of operation for block ciphers, where the input to the block cipher is the concatenation of the nonce and the counter instead of a plaintext.

5.1.2 Mitigations. Most of the existing countermeasures against traditional power side-channel will be as effective against a frequency throttling side-channel. For example, software-based masking [47] that splits a secret asset into multiple random shares will randomize the power consumption of the hardware, and will be useful against a frequency throttling side-channel. There are several noteworthy exceptions. For example, shuffling-based countermeasures that randomize instruction execution order, while being effective in making trace alignment and identification of points of interest harder for physical power side-channel attacks, are less effective in mitigating a frequency throttling side-channel. This is because reordering instructions at the cycle granularity is less likely to impact average power consumption during the time window \( r \) in the order of milliseconds or longer. Also, since an adversary does not need to physically access the hardware, any protection that physically isolates the system will not be sufficient to prevent a frequency throttling side-channel attack.

For cryptographic applications based on existing cryptographic libraries, an example of a generic countermeasure against power side-channel is key refresh. One of the necessary conditions for power side-channel is amplification, or the ability to repeatedly kick off cryptographic operations with the same sensitive key to collect a sufficient amount of traces. If the secret key is refreshed before enough traces can be collected, it will be harder for the attacker to fully deduce the secret. One important design factor is how frequency the key should be refreshed, which could be based on timing (e.g., refresh per several hours) or data volume (e.g., the volume of data being encrypted with the same key). If the designer is uncertain of the threshold to use, the lowest threshold that meets performance and design requirements should be selected. Naturally, the practicality of key refresh depends on the specific cryptographic use case (e.g., key refresh is typically not applicable to disk encryption).

From a hardware perspective, secret dependency is satisfied for almost all modern CPUs since power consumption difference due to circuit switching behavior is an inherent property of CMOS circuits. Making the entire SoC power-constant would of course address this condition, but is difficult to achieve, if not impossible. A more feasible option is making specific security-sensitive hardware components (e.g., hardware cryptography accelerator) power-constant.

### 5.2 Analysis of Controller Actuation

This condition allows conversion from power differences to timing differences during an attack. As described in Algorithm 1, the new frequency limit after throttling \( \hat{f}_{max} \) is a function of the power budget, which is the difference between the power limit \( PL \) and the measured average power consumption \( \hat{P} \). A mitigation may target one of the components in this conversion process: the control algorithm, \( PL \), or \( \hat{P} \).

#### 5.2.1 Mitigations targeting the control algorithm. Since the purpose of reactive limits is to restrict the system from consuming power or current beyond the limit while maximizing system performance, a control algorithm is typically designed to select the highest possible frequency limit that satisfies the reactive limits. A straightforward mitigation option to change the control algorithm is to only allow the system to run at the lowest frequency when reactive limits are hit. While it prevents data-dependent frequency change, system performance is severely impacted. Another option is to fully disable reactive limit based throttling, which is usually not acceptable, since it is a critical power management feature and is required for safety. An option to trade-off between security and functionality is to reduce sensitivity of the control algorithm so that the switching of frequency limit would be less correlated with the input.

#### 5.2.2 Mitigations targeting reactive limits. Similarly, a firmware or system software may take a straightforward approach to either configure the limit to a value too high to hit, or keep it very low so that the system always runs at the lowest frequency. However, these changes have severe negative impact on performance or functionality. One alternative solution is to randomly “fuzz” the reactive limit. For example, instead of configuring a static reactive limit to \( PL \), firmware or system software may define a range \( [PL_{low}, PL_{high}] \), and randomly select a value in the range, dynamically and routinely configuring the reactive limit. By doing so, randomness will be introduced in the power budget, as well as CPU frequency.

As discussed, interfaces (e.g., MSRs) to configure reactive limits, if accessible, could be utilized by an adversary to reduce the limits and trigger the throttling side-channel attack. A cloud service provider (CSP) or system software could prevent these interfaces from being exposed to untrusted guest VMs or ring-3 software, and be aware of the risk if the interfaces have to be exposed.

#### 5.2.3 Mitigations targeting average power. The processor may decouple the calculated average power consumption from the actual power consumption. One approach is to utilize modelled power consumption instead of the actual power reading in the algorithm. If the model is selected to exclude information of instruction operands, then the average power will be independent of any secret data consumed by the victim application. Another approach is for the
processor to “fuzz” the average power consumption by adding noise to the value before the control algorithm uses it to compute the power budget. This is equivalent to the idea of fuzzing the reactive limit, since power budget is the difference between reactive limits and the average power. Please note that although fuzzing the power reading will not directly change power consumption, it will alter $f_{\text{max}}$ and indirectly impact power consumption and performance.

5.3 Analysis of Observability
One of the common countermeasures against side-channel attacks is to jam the channel with noise to prevent the attacker from deducing the secret. As the side-channel in this attack is frequency and timing information, noise can be injected into the frequency transition or timing information. One method is to leverage inherent noise during cryptographic application calls. As the cryptographic library provider or cryptographic application provider, one may restrict the maximal size allowed of processed data per API invocation, so that more invocations of the API are needed to process the same amount of data, and larger intrinsic noise will be introduced. Besides that, a cryptography implementer may proactively inject random noise to cryptographic operations to increase timing variation. To implement this countermeasure, the developer may add dummy instructions that introduce sufficient power or latency variation. The dummy instructions should be independent of the secret data used in the cryptographic function. For example, timing variation can be introduced using a loop of instructions with random iterations. In addition to that, any power variation induced by the dummy instructions may also increase the entropy of the frequency transition. To ensure randomness is introduced for every frequency transition, it is recommended that some noise is injected during every time window $\tau$ of the reactive limits that the attacker would target. One possible way to trade-off security and performance impact is to combine this scheme with a key refresh countermeasure, to increase the time needed to perform a successful attack to a key lifetime that is acceptable.

5.4 Summary of Mitigation Options
A summary of the mitigation options is listed in Table 6, categorized based on the condition to address, the layer(s) to apply, the security effectiveness in mitigating the frequency throttling side-channel, and the performance or functional impact. As can be seen, options that fully resolve the security issue (e.g., #2 and #6) bring high performance or functional impact, while options that partially reduce the security risk have low to medium impact. Depending on the layer in which the mitigation is applied, different options might be selected. For example, the developer of a user-space cryptography implementation may consider options #1 and #8, which are the options available to Ring 3 software.

6 RELATED WORK
Related work has demonstrated the vulnerability of software accessible energy and power telemetry information to side-channel analysis attacks. In [57], the authors highlighted the use of software-accessible battery data of an Android phone to extract sensitive information from multiple applications. It has been shown in [16] that energy meter readings can be used to infer control flow dependency as well as cache hit/miss patterns for a program. [41] demonstrated the utilization of energy meter readings to distinguish keys of different Hamming weights for an RSA implementation.

In addition to the above, several recent works have targeted a processor’s energy consumption information (as exposed by RAPL interfaces in both Intel and AMD processors) to perform side-channel analysis attacks. In [38], the authors demonstrate software-based power side-channel attacks called Platypus to extract a key from a secure enclave, to break kernel address space layout randomization (KASLR), and to establish a timing-independent covert channel. In [39], the authors present a methodology to perform side-channel risk assessment of different software-accessible telemetry including RAPL energy, CPU frequency, voltage, and temperature data.

Concurrent to our work, Wang et al. [54] also discovered the frequency throttling side-channel and named the attack Hertzbleed. Wang et al. highlight the concept of conversion of power side-channel information to timing-side-channel information and exploit it to recover a key from the SIKE post-quantum key encapsulation algorithm. Compared to Hertzbleed, this paper introduces and comprehensively explains the underlying mechanism and reasoning behind the frequency throttling side-channel leakage. We demonstrate key recovery by performing correlation power analysis on the widely used AES-NI based AES implementation and further elaborate on the privileged software attack scenario (sections 4.3 and 4.4), showing how reactive limit configuration helps coerce information leakage. We discuss the unprivileged attack scenario, which the Hertzbleed paper focuses on, showing that such an attack is comparatively harder to achieve (section 4.5). In addition, this paper provides a thorough discussion of mitigation options to thwart such frequency throttling side-channel attacks. Wang et al. propose to disable Turbo Boost or to disable SpeedStep and HWP from the BIOS, as a workload independent mitigation, with the presumed intent of minimizing DVFS transitions. While this has the effect of indirectly reducing power consumption, such a mitigation does not affect the enforcement of reactive limits nor the underlying behavior of Algorithm 1. Thus, if a reactive limit is hit (e.g., as in the privileged attack scenario, by an adversary sufficiently lowering the reactive limit), then information is still expected to leak.

7 CONCLUSION
In this paper, we present a novel frequency throttling side-channel analysis attack. The root cause of such a side-channel is a power side-channel, which is converted to a timing side-channel by the power management architecture when reactive limits are triggered. We demonstrate the threat posed by frequency throttling side-channel attacks by showing that the cryptographic key can be successfully extracted from a constant-cycle implementation of AES by measuring the executing time of cryptographic operations and apply correlation power analysis. Finally, we present a set of options to thwart such throttling side-channel analysis attacks, with analysis of pros and cons. These mitigation options provide insights into the necessary conditions for throttling side-channel information leakage and how to develop effective countermeasures.
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