GaN power devices: current status and future challenges

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Received December 30, 2018; accepted March 19, 2019; published online May 28, 2019

The status and challenges in the development of GaN power devices are reviewed. At present, normally-off gate injection transistors (GITs) on Si are commercially available. The updated structure known as a hybrid-drain-embedded GIT provides superior reliability that contributes to the stable operation of compact power switching systems with high efficiency. The fabricated vertical GaN transistor on GaN as a future challenge demonstrates extremely low specific on-state resistance and high breakdown voltage. Metal-insulator-semiconductor-gate GaN transistor is also a technical challenge for faster switching, since it would give greater freedom of gate driving as a result of both high threshold voltage and widened gate voltage swing. Normally-off operation free from hysteresis in the current–voltage characteristics is confirmed in a recessed-gate AlGaN/GaN heterojunction field effect transistor using AlON as a gate insulator. Fast switching characteristics are experimentally confirmed for both of the newly developed GaN devices, indicating their great potential for practical use.

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1. Introduction

Gallium Nitride (GaN) has been widely investigated for power switching applications owing to the material’s superior properties. The successful demonstration of the epitaxial growth of GaN on large diameter Si substrates has seen the GaN power transistor emerge as a viable alternative with the expectation of low-cost fabrication. The use of AlGaN/GaN heterojunction as the current channel is one of the most notable features of the GaN transistor. 2-dimensional electron gas (2DEG) with extremely high carrier concentration originated from the polarization-induced electric fields and the high electron mobility significantly reduced the on-state resistances. Lateral GaN transistors with the heterojunction formed on the insulating buffer layers exhibit extremely low parasitic capacitances as well. These features of the GaN transistor enable high-frequency switching with low operating losses. Thus, GaN transistors can make power switching systems highly efficient and very compact by increasing the switching frequencies. Although achieving normally-off operation and taking advantage of the high carrier concentration of the 2DEG has been the most critical issue for the practical use of GaN transistors, gate injection transistors (GITs) with p-type gate fabricated on Si substrates has successfully demonstrated the normally-off operations with stable operation. This new operating principle enables low on-state resistances, maintaining the normally-off operation. Highly efficient performances of switching systems have been demonstrated so far, through current commercially available GITs.

In this paper, the current status and future challenges of the GaN power devices are reviewed. Here, the updated structure of the GIT known as a hybrid-drain-embedded GIT (HD-GIT) is described. The HD-GITs demonstrate superior reliability to that of conventional GITs at higher operating voltages. After describing compact power switching systems by using GITs, further technical challenges in GaN power devices are reviewed by demonstrating new device structures. The challenges include vertical GaN transistors on GaN substrates as well as metal-insulator-semiconductor (MIS)-gate GaN transistors. The vertical GaN transistor demonstrates extremely low specific on-state resistance and high breakdown voltage, which would overcome the limitation of increasing the operating current and voltage by lateral GaN transistor. MIS-gate GaN transistor is expected to enable faster switching than p-gate GITs due to both high threshold voltage and widened gate voltage swing. The new GaN power devices as future challenges would extend the potential application of GaN from those of GITs.

2. GaN power devices on Si: current status

2.1. Update of GIT

GITs with p-type gate have demonstrated low on-state resistance utilizing conductivity modulation, in which injected holes at the on-state from the p-type gate produce equal numbers of electrons at the channel, as shown in Fig. 1. Although superior DC and switching performances have been confirmed even by conventional GITs, it is apparent that the switching reliability needs to be further improved under more severe switching conditions. Figure 2 shows the switching test circuits using a resistive load and an inductive load that can be applied to GaN transistors. The two loci of the switching imply that the inductive load switching is more severe, since both high current and voltage are applied to the transistor during the switching. Based on the extensive characterization of the power switching systems, it is understood that sufficient reliability under the severe...
inductive load switching should be achieved for practical applications. It has also been revealed that the switching reliability can be improved by the suppression of so-called current collapse, where the on-state resistance is increased during the switching due to the trapping states of the carriers. The HD-GIT, of which the schematic cross-section is shown in Fig. 3, is proposed to ensure sufficient reliability free from current collapse.10–12 In the HD-GIT, holes are injected from the p-type region formed as a part of the drain at the off-state. The holes from the drain region effectively control the capture and emission process of the carriers, which suppresses current collapse even at higher drain voltages up to 850 V. The p-GaN gate needs to be formed over a groove in AlGaN in the HD-GIT, while the p-GaN as a part of the drain is formed on the thick AlGaN to serve the above-mentioned operation.10,11 The introduction of the epitaxial regrowth of p-GaN/AlGaN successfully reduces the variation of the threshold voltage over the wafer, compared with that by the regrowth of p-GaN over a groove in the AlGaN.12 The total thickness of AlGaN in the vicinity of the source and drain is increased in the HD-GIT from that of conventional GIT, which reduces the series resistance, resulting in low on-state resistance.

It is also noted that sufficiently long lifetime by high-temperature reverse bias (HTRB) tests is confirmed in the HD-GITs. High drain voltages up to 750 V are applied at the off-states varying the temperature up to 150 °C for the HTRB test of the HD-GITs. Changes in the off-state leakage current as well as the threshold voltage are measured to examine the stability of the breakdown characteristics. By using the acceleration factors in the HTRB tests by the drain voltages and temperatures, the lifetime of the HTRB test at 480 V/80 °C is extracted to be 1000 years. In addition to the HTRB test, the HD-GIT has passed all of the reliability test standards by JEDEC that were originally specified for Si power transistors.

Switching lifetime tests using an inductive load called a dynamic high-temperature operating life (D-HTOL) test are proposed as the severe reliability test for the HD-GITs considering the practical application of GaN transistors.15,16 The test circuit for the inductive load switching shown in Fig. 2(b) is used for the D-HTOL test. The HD-GITs ensure sufficiently long lifetime under the D-HTOL test, as shown in Fig. 4, in which the waveform of the gate driving is also

![Fig. 2.](Color online) Test circuits for GaN power transistors and their switching loci using (a) a resistive load and (b) an inductive load.

![Fig. 3.](Color online) Schematic cross-section of the proposed HD-GIT.

![Fig. 4.](Color online) Variation of dynamic $R_{on}$ normalized by static $R_{on}$ under D-HTOL test with a test circuit using an inductive load, in which the results of conventional GIT and proposed HD-GIT are compared.
shown. Here, the change in the dynamic on-state resistances from static values as an indicator of whether the current collapse is suppressed or not is measured. While the conventional GITs can survive only up to 10 min, HD-GITs maintain stable dynamic on-state resistances over 10 h, indicating the improved reliability of HD-GITs. By choosing suitable values of L and R of the inductive load switching circuit, as shown in Fig. 2(b), only the voltage can be varied, maintaining the peak drain current constant under the D-HTOL tests. The peak drain current can be varied, maintaining the constant drain–source voltage as well. Figure 5 is a summary of the reliability tests by using Weibull plots, varying the stress voltages and currents. A number of HD-GITs are examined by the D-HTOL tests and the failure rate F is measured as a function of the testing time. Here, the semi-log plot of the measured \( \ln \ln \left(1/(1-F)\right) \) and the time shows a linear relationship with the slope \( m \) over 1, indicating that the failures are caused by the wear-out modes. The time at which the failure rate F is 50% is defined as the mean-time-to-failure (MTTF) of the D-HTOL tests. The measured values of the MTTF for various drain current and drain–source voltages reveal the acceleration factors by the current and the voltage to be \( \beta_c \) and \( \beta_v \), respectively, as shown in the inset figures of Fig. 5. An additional notable finding is that the MTTF for various temperatures is unchanged, although the detailed mechanism is still to be discussed. The estimated lifetime of the D-HTOL tests using the above-mentioned acceleration factors is as long as 6000 h at 400 V/27 A/95 °C. The operating lifetime of a GIT-based inverter, where high efficiencies are maintained even at lower output power, is confirmed.20) The inverter of the GITs can be compact and highly efficient, so that it can be directly attached to a motor.

Another promising application of GITs is various conversion circuits in power supplies. A totem-pole PFC circuit with high operating efficiency is demonstrated by using GITs with low on-state resistance and good recovery characteristics.21) The conversion efficiency is increased to 98.8% by the GITs. A resonant LLC converter with two inductors and a capacitor as an isolated DC-DC converter is also demonstrated using GITs, where high-frequency operation at 1 MHz with the conversion efficiency of 96.4% is confirmed.2) The totem-pole PFC and resonant LLC converters are assembled into a compact power supply, as shown in the photograph in Fig. 7. The power supply provides a maximum output power of 400 W and very high power density of 1.8 W cm\(^{-3}\). This superior performances of power switching systems demonstrate the great potential of the GITs for practical applications.

2.2. Application of GITs to power switching systems

The GITs on Si can be applied to various power switching systems, taking advantage of the superior performance and reliability. One suitable application of the GIT is an inverter for motor drive. The GIT is free from the voltage off-set in current–voltage characteristics for both forward and reverse direction, which is observed in conventional insulating gate bipolar transistors (IGBTs), resulting in significant reduction of the conduction loss. High operating efficiencies up to 99.3% are confirmed in a GIT-based inverter, where high efficiencies are maintained even at lower output power.20) The inverter of the GITs can be compact and highly efficient, so that it can be directly attached to a motor.

Figure 6 shows a schematic drawing as well as a photograph of a motor with an integrated inverter. This compact motor with an inverter can be applied to various advanced robotics, taking advantage of the elimination of AC cables between the inverter and motor.
3. Vertical GaN power transistors on GaN

3.1. Device structure

As described in the previous chapter, the lateral GITs on Si substrates with the rating blocking voltage of 600 V demonstrate highly efficient operation of power switching systems. Although the performances including the reliability are sufficient for practical use, increasing the total output power of the switching systems using the lateral GITs is limited to several kW. Increasing both the output current and breakdown voltage is necessary to enable higher output power, which has been difficult with the lateral device configuration. The surface area of the electrode as well as the spacing between the source and the drain are significantly large on the surface of the high-power devices. Vertical transistors can limit the device area, since the increase in the breakdown voltage is enabled just by increasing the thickness of the drift layer. Figure 8 summarizes the change in the device size by the increase of the breakdown voltage of both the vertical and lateral GaN transistors. Vertical transistors are advantageous for high-voltage application, maintaining the small device size. Since the vertical transistor needs to be formed on a conductive substrate with a thick drift layer, the use of GaN substrate is the practical choice. Although various structures of GaN vertical transistors have been presented so far, there still remain technical issues such as poor pinch-off characteristics and stability of the gate.

A new GaN vertical transistor on GaN substrate is proposed, of which the schematic cross-section is shown in Fig. 9. The device features epitaxially regrown p-GaN gate/AlGaN/GaN triple layers formed over the V-grooves at the surface of p-GaN well/n-GaN drift layers. Here, carbon-doped insulating GaN is formed on top of the p-GaN well layer to block the off-state leakage current, and the carbon-doped GaN/Mg-doped p-GaN double layer is referred to as the hybrid blocking layer (HBL). Figure 10 shows the calculated sheet carrier concentrations at AlGaN/GaN heterojunction and the threshold voltages as a function on the slanted angle from the c-plane, in which the schematic cross-section of the regrown AlGaN/GaN over the grooved GaN is also shown.

![Fig. 7](https://example.com/fig7.png)

**Fig. 7.** (Color online) Photograph of the fabricated compact power supply using GITs in which a totem-pole PFC and a resonant LLC DC-DC converter are connected in series.

![Fig. 8](https://example.com/fig8.png)

**Fig. 8.** (Color online) Change of device size by the increase in breakdown voltage: comparison between vertical and lateral transistors.

![Fig. 9](https://example.com/fig9.png)

**Fig. 9.** (Color online) Schematic cross-section of the proposed GaN vertical transistor on a GaN substrate.

![Fig. 10](https://example.com/fig10.png)

**Fig. 10.** (Color online) Calculated sheet carrier concentrations at AlGaN/GaN heterojunction and the threshold voltages as a function on the slanted angle from the c-plane, in which the schematic cross-section of the regrown AlGaN/GaN over the grooved GaN is also shown.

![Fig. 11](https://example.com/fig11.png)

**Fig. 11.** (Color online) $I_d-V_{gs}$ characteristics of the fabricated p-GaN/AlGaN/GaN gate over a semipolar plane, where those over the c-plane are also shown.
to increase the $V_{th}$. The change of $V_{th}$ is experimentally confirmed, as shown in Fig. 11. By forming the p-type gate on the slanted channel at the groove, the $V_{th}$ increases by 1.5 V from that on the c-plane surface. It is noted that regrowth of p-GaN/AlGaN/GaN triple layers instead of p-GaN/AlGaN double layers significantly increases the electron mobility at the AlGaN/GaN. Another feature of the proposed vertical GaN transistor is the insertion of a carbon-doped layer on top of the Mg-doped p-type well. Because of insufficient activation of the Mg-doped p-type well layer, relatively high electron concentrations exist between the source and drain at the off-state, resulting in punch-through current. Inserting the carbon-doped layer on top of the Mg-doped p-type well successfully blocks the current path as a result of its highly insulating nature. The improvement of the off-state characteristics is confirmed by the device simulation, as shown in Fig. 12. Figure 13 shows the cross-sectional image of the fabricated vertical GaN transistor by scanning electron microscope (SEM). The Si-doped drift layer is designed to provide a blocking voltage of 1.5 kV or more. Here, the slanted angle of the V-groove of the gate is measured to be 45°.

### 3.2. Device performances

Figure 14 shows the on-state and off-state $I_{ds}$-$V_{ds}$ characteristics of the fabricated vertical GaN transistor. The low specific on-state resistance $R_{onA}$ of 1.0 mΩ·cm² and the high breakdown voltage of 1.7 kV are experimentally confirmed. Note that the threshold voltage is as high as 2.5 V, enabling the normally-off operation. Suppression of the punch-through current by the HBL increases the breakdown voltage from 580 V to 1.7 kV. Figure 15 summarizes the performances of state-of-the-art vertical GaN transistors. The fabricated vertical GaN transistor exhibits the lowest $R_{onA}$ among the reported devices, while maintaining a high threshold voltage. The off-state bias stress test for the fabricated vertical GaN transistors confirms the very stable off-state leakage current.
and threshold voltage over 300 h at a stress bias of 400 V at 125 °C. Figure 16 shows a top-view photograph of the fabricated vertical GaN transistor designed to achieve high-current operation with a chip size of 1.1 × 1.2 mm². Fast switching at 400 V/15 A with a resistive load is confirmed by the large chip of GaN vertical transistor with the switching time of 40 ns or less. This indicates that the presented vertical transistor can be applied to practical switching systems.

4. MIS-Gate GaN power transistor using AlON-gate insulator

4.1. Device structure

So far, the introduction of p-type gate to GaN transistors has been very effective to provide stable operation of power switching systems. However, the positive value of the threshold voltage remains low and the applicable swing of the gate voltages is small as long as the p-type gate is employed. The low threshold voltages cause the undesired turn-on at the switching. In addition, the applicable small swing of the gate voltages requires special gate driving circuits for fast switching.21) The introduction of MIS-gate is expected to solve the above technical issues arising from the use of p-type gate. A modified design of the MIS-gate structure can increase the threshold voltage, which effectively suppresses the undesired turn-on. In addition, the applicable maximum gate voltage can be increased by the MIS-gate, resulting in wider swing of the gate voltages. Since the transient gate current to charge and discharge the parasitic capacitances is increased by the MIS-gate with the widened swing of the gate voltages, the device can provide faster switching, giving more freedom to the design of gate driving. It is also noted that the gate driving circuit for the MIS-gate device can be compatible with that of conventional Si-based power devices. Figure 17 summarizes the expected improvement in current–voltage characteristics of the GaN transistor by MIS-gate, compared with those by the GIT with p-type gate.

Fig. 18 shows the schematic cross-section of the proposed AlGaN/GaN MIS-gate HFET on Si substrates enabling normally-off operation with stable gate characteristics.19) Reccessed-gate structure is introduced to reduce the series resistances of the device. AlGaN thin layer is epitaxially regrown over the grooved structure of AlGaN/GaN by MOCVD. The regrowth at high temperature removes the processing damage caused by the dry etching of AlGaN/GaN heterostructure that had affected the stability of the gate. AlON is formed over the regrown surface by atomic layer deposition, Fig. 18.
which gives better uniformity, fully eliminating the processing damage compared with the conventional sputtering. Figure 19 shows the cross-sectional transmission electron microscope (TEM) image of the fabricated MIS-HFET with AlION-gate. The gate length $L_g$ and gate–drain spacing $L_{gd}$ are designed to be 2 and 10 $\mu$m, respectively, to achieve a breakdown voltage over 600 V.

### 4.2. Interfacial properties of MIS-gate

Al$_2$O$_3$ has been commonly examined so far as the gate insulator of AlGaN/GaN HFET, since it exhibits relatively small hysteresis in the gate-transfer current–voltage characteristics. The high permittivity helps to provide better reliability of the gate by increasing the insulator thickness, maintaining the high transconductance. However, hysteresis in the gate-transfer characteristics has been a technical issue for the use of Al$_2$O$_3$ considering the practical switching applications. The hysteresis increases as the applied maximum gate voltage increases, so that the increase in gate voltage swing is limited. The use of AlION by introducing nitrogen into the Al$_2$O$_3$ has been proposed as the gate insulator, by which the hysteresis is successfully reduced by the elimination of the number of fixed charges and electron traps in the insulator. Figure 20 shows the $I_{ds}$-$V_{gs}$ transfer characteristics of the fabricated MIS-gate formed over AlGaN/GaN heterojunction. Although the use of AlION reduces the hysteresis, the as-deposited AlION shows the negative threshold voltage $V_{th}$. Here, O$_2$ annealing after the deposition is introduced based on the assumption that the negative shift of the $V_{th}$ is caused by the positive charges originated from the dangling bonds of Al or/and Ga at the AlION/AlGaN interface. As shown in Fig. 20, the $V_{th}$ shifts to the positive side by 2 V after the O$_2$ annealing of AlION, resulting in normally-off operation with the $V_{th}$ of 1.4 V. Thus, the AlION annealed in O$_2$ achieves the normally-off operation free from the hysteresis over the AlGaN/GaN HFETs. Figure 21 shows the gate-transfer characteristics of the AlGaN/GaN MIS-HFET using AlION-gate insulator, varying the maximum gate voltage $V_{gs}$. The curves are unchanged even after increasing the $V_{gs}$ to 10 V, indicating that high-speed switching would be possible by the presented MIS-HFET by applying a wider swing of the gate voltage.

Capacitance–voltage ($C$–$V$) measurements for the MIS-gate reveal that the interface trap densities $D_{it}$ at the insulator/AlGaN interface are reduced by the use of AlION. The $D_{it}$ at the mid gap is reduced to those in the order of $10^{11}$ eV$^{-1}$ cm$^{-2}$ by AlION, while those by conventional Al$_2$O$_3$ remain in the order of $10^{12}$ eV$^{-1}$ cm$^{-2}$. These results indicate that the improved interfacial properties apparently help to reduce the hysteresis of the transfer characteristics.

### 4.3. Device performances

The above-mentioned processing and structure of the AlION-gate AlGaN/GaN HFET are applied to a high-current device.
with a gate width $W_g$ of 100 mm to examine the switching performance. Figure 22 shows a top-view photograph of the fabricated transistor with a chip size of $2.3 \times 2.3$ mm. The measured drain current–voltage ($I_{ds}$-$V_{ds}$) characteristics at both the on-state and off-state are shown in Fig. 23. The maximum drain current reaches 20 A at a gate voltage $V_{gs}$ of 10 V. The off-state leakage current is successfully reduced and the breakdown voltage reaches 730 V. The on-state resistance $R_{on}$ is as low as 270 m$\Omega$.

The switching performances are measured for the fabricated 20 A/730 V transistors with an off-state drain voltage of 400 V and an inductive load. Very fast switching is experimentally confirmed, where the measured $dV/dt$ for turn-on and turn-off are as small as 78 and 169 V ns$^{-1}$, respectively. Table I is a comparison of the performances among those obtained by the reported GaN insulating gate transistors and by the GIT with p-type gate.$^{10,21,30-32}$ The performances of commercially available Si super-junction (SJ) MOSFET is also shown. The presented switching performances are the best values for GaN-based MIS-HFET with a switching current of 10 A or more, indicating the great potential of the AlON-gate MIS-HFET for practical applications.

5. Conclusions

State-of-the-art technologies of GaN power devices are reviewed. A novel normally-off transistor known as GIT on Si demonstrates low on-state resistance together with sufficient reliability, especially by the updated structure of HD-GIT. Compact inverters and power supplies with high operating efficiencies are demonstrated by the 600 V GITs that are commercially available at present.$^{33}$ The development of vertical GaN transistors is a technical challenge for future widespread use of GaN, since the vertical device easily achieves high-current and high-voltage operations. A new structure of the vertical GaN transistor is proposed, where the p-type gate is formed over the V-groove of the GaN drift layers. Low specific on-state resistance of 1.0 m$\Omega$ cm$^2$ and high breakdown voltage of 1.7 kV are confirmed in the vertical device. As a future challenge, MIS-gate GaN transistor is demonstrated using AlON as a gate insulator. Hysteresis in the transfer current–voltage characteristics is fully eliminated and high gate voltage up to 10 V can be applied, which is advantageous for high-speed switching. Both the challenging GaN power devices exhibit high-speed switching under high-current/voltage switching conditions, indicating their superior potential for practical switching applications.

Acknowledgments

The author would like to thank members of the Panasonic Corporation working for the research and development of GaN power devices for their valuable help and advice. The work on GITs was partially supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan, under the Strategic Development of Energy Saving Innovative Technology Development Project. The work on vertical GaN transistors was partially supported by the Ministry of the Environment, Government of Japan. The author would like to thank the Scioci Co., Ltd. for providing the GaN epitaxial layers and substrates in this work. The work on MIS-gate GaN transistors was partially supported by the Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation

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**Table I.** Comparison of the performances between the presented MIS-HFET, reported MIS-HFET and commercially available normally-off devices by GaN and Si.

| Substrate | Device structure | Rating off-state voltage [V] | Rating drain current [A] | On-state resistance $R_{on}$ [m$\Omega$] | Threshold voltage $V_{th}$ [V] | Turn-on time [ns] | Turn-off time [ns] |
|-----------|-----------------|--------------------------|------------------------|---------------------------------|-------------------|------------------|------------------|
| Si        | Lateral         | 400                      | 10                     | 270                             | 1.4               | 4.1              | 1.9              |
| GaN       | Vertical        | 400                      | 2.5                    | 350                             | 1.3               | 1.2              | N/A              |
| Si        | Lateral         | 400                      | 10                     | 15                              | 3.5               | 19               | 1.9              |
| Si        | Vertical        | 400                      | 76                     | 150                             | 1.2               | 1.9              | 1.6              |
| Si SJ-MOS | Vertical        | 104                      | 104                    | 104                             | 3.5               | 10               | 8.0              |

Fig. 23. (Color online) $I_{ds}$-$V_{ds}$ characteristics of the fabricated AlON-gate GaN transistor for (a) on-state and (b) off-state.
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