Three dimensional fast tracker for central drift chamber based level 1 trigger system in the Belle II experiment

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The Belle II detector at the SuperKEKB accelerator has a level 1 trigger implemented in field-programmable gate arrays. Due to the high luminosity of the beam, a trigger that effectively rejects beam induced background is required. A three dimensional tracking algorithm for the level 1 trigger that uses the Belle II central drift chamber detector response is being developed to reduce the recorded beam background while having a high efficiency for physics of interest. In this paper, we describe the three dimensional track trigger that finds and fits track parameters which we developed.

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I. INTRODUCTION

The Belle II detector [1] is located at the asymmetric-energy electron positron collider SuperKEKB [2]. The high luminosity of SuperKEKB will open the possibility to a new panorama of measurements in heavy flavor physics [1]. In order to take advantage of the high luminosity, the trigger is required to have a high efficiency for physics of interest while suppressing other physics processes such as the beam-wall background that are not originated near the interaction point (IP). Also due to the hardware limits of the vertex detectors, the level 1 trigger is required to provide a trigger within 5 µs. Due to these requirements, the level 1 trigger is being developed with boards which have large field-programmable gate arrays (FPGAs) and high speed optical transceivers [3].

The level 1 trigger will utilize the sub-detector responses where the main sub-detectors are the central drift chamber (CDC) [4] and electric calorimeter. The CDC will provide information for charged particles. It consists of nine super-layers (SLs) of wires where five of them have wires arranged parallel to the beam axis (axial) and four of them have finite shift in the phi direction at the end plates (stereo). The CDC readout electronic system will send information to the level 1 trigger by optical transmission. By utilizing this information, the level 1 trigger will be able to reconstruct the trajectories of the charged particles in three dimensions.

The level 1 CDC trigger [5] is made up of six modules which are the merger, track segment finder (TSF), event time finder (ETF), two dimensional finder (2DF), neural network tracker (NNT) [6], and three dimensional tracker (3DT). The merger boards combine the information from the CDC readout boards and send the information to the TSF boards. The TSF finds parts of the particle trajectory called track segments (TS) using pattern matching. The TS information is then sent to the rest of the system which are the ETF, 2DF, NNT, and 3DT. The ETF determines the event timing which is sent to the NNT and 3DT. The 2DF finds the two dimensional track using Hough transformation [7] and sends the results to the NNT and 3DT. The NNT uses a feed-forward neural network to determine the track parameters and sends the information to the later stage of the level 1 trigger. The 3DT does geometric transformations and applies linear regressions to determine the track parameters which are sign of the electric charge, transverse momentum ($p_T$), incident angle ($\phi_i$), polar angle ($\theta$), and distance of track origin from the IP respect to the z axis ($z_0$). These information are sent to the later stages of the level 1 trigger.

In this paper, the 3DT we developed will be described. The algorithms of four modules in the 3DT will be explained which are the TS map maker, stereo TS finder, and $z_0$ fitter.

II. DESIGN

The 3DT extracts track parameters (sign of electric charge, $p_T$, $\phi_i$, $\theta$, and $z_0$) from the input data which consists of TSF, ETF, and 2DF data that changes every 32 ns. The TSF data has four components which are the TS ID, left right identification number (LR), priority layer identification number (PR), and “raw” TDC which is relative to the revolution of the beam. The ETF data has the event time relative to the revolution of the beam. The 2DF data has five axial TS information related to a found track.

The 3DT consists of multiple modules where the main modules are the TS map maker, stereo TS finder and $z_0$ fitter which can be seen in Fig. 1. The TS map maker integrates the TSF data over a certain amount of time.
A. TS map maker

Since the drift time for the CDC can be over than 500 ns, the TSF data that changes every 32 ns should be stored and combined for a certain amount of time. The TSF data consists of 10 TS information for each 32 ns interval. This information is transformed to an array of TS information where the index is the TS ID which we call TS map. The structure of the input TS and output TS map can be seen in Fig. 2. The TS map is then sent to a module which stores and combines the TS information. When new TS information for a certain index enters the module, a counter which counts how long the TS information has been saved is reset. When the counter reaches a certain amount of time, the TS information is erased.

Four stereo TSF data which cover half of the CDC enter the 3DT, so that there are four of these TS map makers. Each TSF has a different number of possible TS IDs, which are 80, 112, 144, and 176, so that the number of indices of the TS maps follow these numbers.

A VHDL [8] testbench was developed to test the developed firmware for the TS map maker. It was shown that the TS map maker works well as can be seen in Fig. 3. The ISim results and firmware results recorded with Chipscope [10] were compared. The timing and values of the results were found to be the same.
Figure 4. Logic flow of the stereo TS finder. This figure shows the detail of how the related TS to a 2D track is found. Using the 2D information the possible TSs are calculated. The TSs within the possible TSs are selected. The TS which is hit and is near the middle is chosen to be the related stereo TS.

(a) Chipscope results

(b) TSIM results

Figure 5. Comparison between firmware test bench indicated as Chipscope (a) and TSIM (b). The figures show the chosen related stereo TS for each stereo SL. The TSIM results and firmware results match perfectly.

B. Stereo TS finder

After a track is found by the 2DF, related stereo TSs should be found. By using the two dimensional track information, the geometrically possible stereo TSs are calculated where a framework that automatically generates VHDL was used for development [11]. Between the hit TSs for the possible TSs, the TS which is near the middle is selected. The flow of the logic can be seen in Fig. 4.

To calculate the geometrically possible stereo TSs, the location where the track would pass if the stereo SL was an axial SL is calculated. This location is calculated using the following equation according to the sign of the electric charge,

\[ \phi_{\text{ax}} = \pm \arccos \left( \frac{r \rho}{2} \right) + \phi_i \mp \pi, \]

where the radius of the CDC wire layer is \( r \) and the curvature and incident angle of the found track are \( \rho \) and \( \phi_i \). This calculated phi location is transformed to the according TS ID by multiplying a constant which depends on the SL. Since the geometrically possible stereo TSs should be within ten TSs from the ID calculated above, an array of 10 TSs is made. Between the hit TSs in the array, the TS which corresponds to the closest point to the IP is selected.

The firmware was tested with a VHDL testbench where data was generated from trigger simulation (TSIM). The results between TSIM and the firmware output recorded with Chipscope were found to be exactly the same for the stereo TS finder in each SL which can be seen in Fig. 5.

C. \( z_0 \) fitter

The related stereo TS information is transformed to a geometric representation and then fitted to get track parameters. We first find TDC for each stereo TS by subtracting the “raw” TDC of each stereo TS with “raw” event time. The TDC is converted to a length dimension which we call drift length using a look-up table that has the x-t curve of the CDC. Using the LR information from the TSF, the drift length is added or subtracted to the TS phi position which we call fine phi position. Using two dimensional track parameters and related stereo TS fine phi positions, the \( z \) location for each stereo TS is calculated with the following equation,

\[ z = \frac{z_{\text{endplate}} - 2r \sin \left( \frac{\phi_{\text{ax}} - \phi_{\text{st}}}{2} \right)}{\tan \theta_{\text{st}}}, \]

where \( z_{\text{endplate}} \) is the distance from the IP to the end-plate of the CDC, \( \theta_{\text{st}} \) is the angle of the stereo wires, and \( \phi_{\text{st}} \) is the fine phi position the stereo TS. The geometric representation of this equation can be seen in Fig. 6. The arc length of the track in the two dimensional \((x, y)\) plane for the radius of each stereo SL is calculated with the following equation,

\[ s = \arcsin \left( \frac{r \rho}{2} \right), \]
where $s$ is the arc length. The track of charge particles in an uniform magnetic field is a helix, so that the two dimensional arc length and $z$ of stereo TSs should have a linear relationship. We construct a $\chi^2$ as below to fit the $z_0$ and $\cot \theta$ using the geometric representation of the stereo TSs,

$$\chi^2 = \sum_i \frac{[z_i - (\cot \theta \times s_i + z_0)]^2}{\sigma_i^2},$$

where $\sigma_i$ is the error of $z_i$. The $\cot \theta$ and $z_0$ which minimize the $\chi^2$ can be found analytically as below

$$\begin{bmatrix} \cot \theta \\ z_0 \end{bmatrix} = \begin{bmatrix} \sum_i (\frac{s_i^2}{\sigma_i^2}) & -\sum_i (\frac{s_i}{\sigma_i^2}) \\ -\sum_i (\frac{s_i}{\sigma_i^2}) & \sum_i (\frac{1}{\sigma_i^2}) \end{bmatrix} \begin{bmatrix} \sum_i (\frac{s_i^2 z_i}{\sigma_i^2}) - \sum_i (\frac{s_i^2 z_0}{\sigma_i^2}) \\ -\sum_i (\frac{s_i^2 z_i}{\sigma_i^2}) + \sum_i (\frac{s_i^2 z_0}{\sigma_i^2}) \end{bmatrix}.$$

The algorithm was developed using a framework that automatically generates VHDL and validated using TSIM. The resolution of $z_0$ was found to be 1.35 cm which can be seen in Fig. 7. A VHDL testbench was developed for the firmware. The firmware output and TSIM were found to be exactly the same [11].

III. CONCLUSIONS

We have developed firmware that extracts track parameters from the input of the 3DT. The logic we developed that stores the input, finds related TS to a track, transforms the stereo TS to geometric representations, and does linear regression has been shown. Using the extracted track parameters, beam induced backgrounds which do not originate near the IP can be effectively rejected.

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