Modified LUO High Gain DC-DC Converter With Minimal Capacitor Stress for Electric Vehicle Application

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ABSTRACT
The vigorous growth of electric vehicles in the field of automobile paves the way for the development of dc-dc converter. A novel high gain super Luo dc-dc converter is proposed in this article. A modification is suggested in the topology when the converters are cascaded for high gain. This suggested modification can be applied to any topology for reliable capacitor. The presented converter adds boosting (voltage multiplier) cell before the load to expand the voltage conversion ratio. This converter renders remarkable features like extended voltage gain, low voltage stress on power switches, minimal capacitor stress and less component count. The operating principle and steady-state analysis of the proposed topology is presented. The main feature of the proposed topology is reduced capacitor stress which is evaluated by reliability study with military handbook MIL-HDBK-217F. The significance of minimal capacitor stress with the failure of the capacitor is elaborated. Simulation on the derived topology is carried out with Matlab/Simulink and it validates the theoretical results. Furthermore, the proposed topology is extended with dual output which makes the restructured converter suitable for Electric vehicle application and the simulation of the dual output topology is performed and studied. The experimental results obtained from the 50 W prototype validate the complete steady-state analysis performed on the proposed topology.

INDEX TERMS
High gain, voltage stress, reliability, boosting, failure rate.

I. INTRODUCTION
The number of conventional vehicles utilized over the world tends to produce harmful problems for both humans and the environment. The rate of depletion of fuels is rapidly...
increasing over a period of time. The earth’s temperature rises and liberation of certain gases associated with global warming are also increasing day by day. A perfect solution for the above-said issues is replacing the conventional vehicle with either electric vehicles (EVs), hybrid electric vehicles (HEVs), or fuel cell vehicles [1]–[3]. In EVs, the traction motor is supplied by the electric sources such as batteries, ultra-capacitors or fuel cells via a high voltage DC bus link as depicted in Figure 1. The main components of a hybrid electric vehicle are illustrated in Figure 1 (a). Non-isolated dc-dc converters are recurrently used in electric vehicle for medium and high-power applications. DC-DC converters are required to power several vehicular loads which require various voltage levels. Both unidirectional and bidirectional dc-dc converters occupy their own place and role in electric vehicles. Figure 1(b) depicts the blocks representing the usage of unidirectional bidirectional dc-dc converter in hybrid electric vehicle. More efficient and cost-effective high-power dc-dc converters are recently researched, developed, and implemented to study their performance. An inverter is used to supply the power to drive the motor (electric traction) and other utility loads like air conditioning system etc.

Figure 2 shows a comparison of different energy storage systems [4], [5]. Generally, propulsion sources are highly subjected to unregulated voltages due to the transient nature of the driving patterns [6]–[8]. There is a significant challenge among the researchers while integrating the power train traction motor with the supply devices. It is observed that each of the sources must require a specifically designed dc-dc power converter to integrate it with the DC bus link. The sources like batteries and supercapacitor subject to voltage fluctuation during operation.

Similarly, fuel cell faces high voltage drop during a transition in the dynamic response. These unregulated sources in electric vehicles can be compensated by integrating a dc-dc converter between the source and the load. In this application, apart from the efficiency, power density, cost and stresses across the components, the dynamic study on the converter needs to be carried out. According to the standard regulation, there is a need to investigate Electro Magnetic Interference (EMI). The efficiency of the converter is studied by making an investigation on the component selection and its switching. Many results from the literature reveal a lesser number of power switches are highly preferred in EVs to decrease the transition time intervals among the charging and discharging modes [9]–[11]. It is also essential to have less current and voltage stresses in to improvise the lifetime of the storage systems [12].

Although various common characteristics are considered in dc-dc topologies in literature, high voltage gain for delivering a wider voltage range seeks more attention [13]–[15].

For a low and medium powered vehicle, non-isolated power converters like interleaved boost and interleaved bidirectional buck–boost types are frequently utilized [16], [17]. They possess promising advantages like simpler architecture, least cost and also better controllability. Four-phase interleaved dc-dc converter has been proposed to improvise the voltage gain [10], [18]–[20]. There is also a rapid increasing study on quasi – Z-source power converters. Input current seems to be continuous all the time with the least stresses on the components. Several techniques such as voltage multiplier, voltage lift, coupled inductor,
switched inductor offers a similar characteristic among which switched inductor and capacitor are common [21]–[25]. In the case of the switched inductor, high current stresses are notified whereas in switched capacitor, high voltage stresses are present [26]. The issues arise in switched inductor and capacitor can be overcome by the coupled inductor. In addition to the increased number of components used in each converter circuitry, coupled inductors possess very low leakage inductor, resulting in a pulsating input current with decreased efficiency [27]–[30]. In this article, the major intent is to highlight the unique feature of the derived topology obtained by modifying the super-lift Luo converter. The lower stress on the components with less component count and extended boosting ability increases the performance, efficiency and reliability of the converter which is intended for solar energy application.

II. CIRCUIT CONFIGURATION

In this section, the derivation of Modified Luo high gain dc-dc converter (MLHGC) is discussed. Figure 3 (a) illustrates the modification carried out in existing super-lift Luo converter i.e., shifting the output part (diode and capacitor) to the input terminal which reduces the stress across the output capacitor. This advantage can be combined by integrating the converter with traditional boost converter with switched-capacitor (diode and capacitor) circuit to expand the voltage gain of the converter. There are three basic blocks in the converter configuration such as modified super-lift, boosting cell and output filter with the load. Figure 3(b) depicts the basic circuit of the proposed topology. It composed of two power switches (S₁ and S₂), three inductors (L₁, L₂ and L₀), four capacitors (C₁, C₂, C₃ and C₀) and two diodes (D₁ and D₂) with boosting cell made up of two diodes (Dᵇ₁ and Dᵇ₂) and two capacitors (Cᵇ₁ and Cᵇ₂). In a M (Number of boosting cell) stage, there are 2M capacitors and 2M diodes in the boosting cell.

A. PRINCIPLE OF OPERATION

Figures 4 (a) and (b) show the equivalent circuit of the derived topology operating in Continuous Conduction Mode (CCM). The characteristic waveforms of the derived topology are presented in Figure 5.

Mode I \([t₀ = 0 < t < t₁ = DTₛ]\): In this period, switches S₁ and S₂ are turned ON as illustrated in Figure 2 (a). The input voltage \(Vₕ\) charges the inductor L₁. Similarly, inductor L₂ is charged by the input voltage and capacitor voltage \(Vₕ₁\). The current through the inductors increases linearly. The diode D₁ is turned ON and diode D₂ is reverse biased due to the voltage across inductor L₂. Diodes (Dᵇ₁ and Dᵇ₂) in boosting cell are in reverse biased state due to the voltage across inductor L₀. The load voltage \(Vₒ\) is the summation of the voltage across output inductor L₀ and twice that of the voltage across the boosting capacitor.

Mode II \([t₁ = (1-D)TS < t < t₂ = TS]\): As shown in Figure 2 (b), switches S₁ and S₂ are in non-conducting state. The diode D₂ is forward biased due to the reverse polarity of the voltage across inductor L₂. The diode D₁ is turned ON and diode D₂ is reversed biased due to the voltage across inductor L₂. Diodes (Dᵇ₁ and Dᵇ₂) in boosting cell are in reverse biased state due to the negative polarity of the voltage across inductor L₀. The load voltage \(Vₒ\) is the summation of the voltage across output inductor L₀ and voltage across the boosting capacitor.

III. ANALYSIS OF CONVERTER

The following assumptions are considered to study the steady-state performance of the derived topology. (1) All
The components are considered as ideal. (2) The converter functions in Continuous Conduction Mode (CCM). (3) The converter output voltage is constant. The inductor voltages are obtained at ON and OFF condition.

ON: \[
\begin{align*}
V_{L1} &= V_{C2} = V_g \\
V_{L2} &= V_{C1} + V_g \\
V_{L0} &= 2V_{C3} - V_0
\end{align*}
\]

OFF: \[
\begin{align*}
V_{L1} &= V_{C2} - V_{C1} \\
V_{L2} &= V_g + V_{C1} - V_{Cb1} \\
V_{L0} &= V_{Cb1} - V_0
\end{align*}
\]

The following expressions are obtained by applying the volt-second balance principle on the above-mentioned inductors (L₁, L₂ and L₀) equations.

\[
\begin{align*}
V_{C1} &= \frac{V_g}{D} \quad (1) \\
V_{C2} &= V_g \quad (2)
\end{align*}
\]

Equations (1) and (2) present the voltage across the capacitors in the modified super lift converter.

The boosting capacitors (Cₜ₁, Cₜ₂) voltage is derived as

\[
V_{Ct1} = V_{Ct2} = \left(2-D\right)\frac{V_g}{D^2} \quad (3)
\]

The voltage gain expression is derived as

\[
G_v = \frac{V_0}{V_g} = \frac{(2-D)(1+D)}{D^2} \quad (4)
\]

If the boosting cell, M is even, then the general voltage conversion ratio of the proposed topology is

\[
G_{v-EVEN} = \frac{V_0}{V_g} = \frac{(2-D)[(M+1) - D]}{D^2} \quad (5)
\]

Similarly, for an odd M boosting cell, the general expression for voltage conversion ratio is obtained as

\[
G_{v-ODD} = \frac{V_0}{V_g} = \frac{(2-D)(M + D)}{D^2} \quad (6)
\]

A. VOLTAGE AND CURRENT STRESSES

The power semiconductor switches’ voltage stress is determined as

\[
\begin{align*}
V_{S1} &= \frac{V_g}{D} \quad (7) \\
V_{S2} &= \frac{(2-D)V_g}{D^2} \quad (8)
\end{align*}
\]

The Switch Utilization Factor (SUF) of the suggested converter is determined by

\[
SUF = \frac{V_0I_0}{V_{S1}I_{S1\text{(rms)}} + V_{S2}I_{S2\text{(rms)}}} \quad (9)
\]

Using the equation (9), the SUF of MLHG converter is calculated as

\[
SUF_{MLHGC} = \frac{G_vD}{2D[2-D] + \sqrt{D}[1+D]} \quad (10)
\]

From the equations (7), (8) and (10), it is observed that the stress on the power switches (S₁ and S₂) is low compared to few converters reported in the literature whose switch voltage stress is equivalent to the load voltage. Usually, it is recommended to design a converter with low stress which reduces the R_ds(on) of the MOSFET and also the cost of the topology. According to Figures 2 (a) and (b), the stresses on the semiconductor diodes are determined. The stress on the diodes and capacitors is tabulated in Table 1.

The average and RMS current through the components are presented in Table 2. The current stress on semiconductor devices is studied with Table 2. For efficiency calculation, currents through the components in Table 2 are used.
**TABLE 1.** Voltage stress across the diodes and capacitors-MLHG converter.

| Proposed converter-MLHG | voltage stress | voltage stress | voltage stress | voltage stress | voltage stress | voltage stress |
|-------------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| \( V_{b1} \)            | \( V_{b2} \)    | \( V_{b3} \)    | \( V_{b4} \)    | \( V_{c1} \)    | \( V_{c2} \)    | \( V_{c3} \)    | \( V_{c4} \)    |
| \( V_{b1} \)            | \( V_{b2} \)    | \( V_{b3} \)    | \( V_{b4} \)    | \( V_{c1} \)    | \( V_{c2} \)    | \( V_{c3} \)    | \( V_{c4} \)    |

**TABLE 2.** Current through the components of MLHG converter.

| Proposed converter-MLHG | current through components | current through components | current through components | current through components | current through components |
|-------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| \( I_{l1} \)            | \( I_{l2} \)              | \( I_{l3} \)              | \( I_{l4} \)              | \( I_{l5} \)              | \( I_{l6} \)              |

**B. BOUNDARY CONDUCTION MODE OF MLHG CONVERTER**

The voltage gain remains same in CCM and DCM, when the MLHG converter operates in Boundary Conduction Mode (BCM). The critical inductance \( K_{cric} \) value for the inductors \( (L_1, L_2 \) and \( L_0 \)) is obtained as follows:

\[
I_{L1} \geq \Delta I_{L1} \quad \text{CCM} \quad (11)
\]

Using the inductor \( (L1) \) current from table 2 and steady state equations at ON conditions, the following expression is obtained.

\[
\frac{(1 + D)I_0}{D^2} \geq \frac{V_gDT_s}{2L_1} \quad (12)
\]

Simplifying the above expression \( K_{cric(L1)} \) is acquired.

\[
\frac{2L_1f_s}{R_0} \geq \frac{(2 - D)D}{G_{cric(L1)}} \quad (13)
\]

where

\[
K_{L1} = \frac{2L_1f_s}{R_0} ; \quad K_{cric(L1)} = \frac{(2 - D)D}{G_{cric(L1)}} \quad (14)
\]

Similarly, the critical inductance of the inductors \( (L_2 \) and \( L_0 \) ) is derived as follows

\[
\frac{2L_2f_s}{R_0} \geq \frac{(2 - D)D}{G_{cric(L2)}} \quad (15)
\]

\[
\frac{2L_0f_s}{R_0} \geq \frac{(1 - D)D}{G_{cric(L0)}} \quad (17)
\]

Using equations (13), (15) and (17), the dependence of duty cycle on \( K_{cric} \) is analyzed with the graphical comparison presented in Figure 6.

**C. MLHG CONVERTER DESIGN CONSIDERATION**

The discussion on the component’s design of the MLHG converter is carried out in this section. The converter is designed to operate in CCM. In order to achieve this condition, the inductor current’s average value should be greater than 1/2 of its ripple.

The minimum value of inductors \( (L_1, L_2 \) and \( L_0) \) for the derived MLHGC to operate in CCM are obtained as

\[
L_1 \geq \frac{R_0[1 - D]^4D}{2(2 - D)(1 + D)^2f_s} \quad (19)
\]

\[
L_2 \geq \frac{R_0[1 - D]^2D}{2(1 + D)^2f_s} \quad (20)
\]

\[
L_3 \geq \frac{R_0[2 - D(3 - D)]D}{2[2D - D(1 + D)f_s]} \quad (21)
\]

To operate the converter in CCM, the equations (19) - (21) are used to determine the minimum value of inductors.

By considering the voltage ripple of the capacitor and disregarding the ESR of the capacitor, the capacitor values are found. The current waveform the capacitor \( C_1 \) is observed and presented in Fig 5 (b) for ripple voltage analysis. The maximum peak to peak value of capacitor \( C_1 \) current is

\[
I_{C1pp} = I_{D2max} \geq \frac{(1 + D\max)V_0D_{\max}}{(1 - D_{max})R_0minC_{minf}} \quad (22)
\]

\[
V_{C1pp} = \frac{\Delta Q}{C_{min}} = \frac{\Delta Q}{(1 - D_{max})R_0minC_{minf}} \quad (23)
\]

**D. EFFICIENCY ANALYSIS**

The \( \eta \) analysis of the derived MLHGC is carried out by determining the losses incurred in the passive element and semiconductor devices of the converter.

Inductors winding loss, \( P_{LW} \) in the converter is obtained as

\[
P_{LW} = \left[ \frac{(1 + D)I_0}{D^2} \right]^2 R_{L1} + \left[ \frac{(1 + D)I_0}{D^2} \right]^2 R_{L2} + I_0^2 R_{L0} \quad (24)
\]

Furthermore, core loss of the inductor is determined as

\[
P_{LC} = K_f^x B^y V_c \quad (25)
\]

where \( V_c \) = volume of the core, \( B = \) flux density, \( f = \) frequency, \( K = \) core materials’ constant, \( x \) and \( y \) are the exponent of flux density and frequency respectively.
The conduction and switching loss of the $S_1$ and $S_2$ are determined as

$$P_{S_{1+S_2}} = \left[ \frac{(1+D)\sqrt{D}I_0}{D^2} \right]^2 R_{ds1} + \left[ \frac{2I_0D\sqrt{D}}{D^2} \right]^2 R_{ds2}$$

$$+ \frac{f_s}{2} \left\{ (t_r1 + t_f1) I_{S1(avg)} V_{S1(max)} \right\} + (t_r2 + t_f2) I_{S1(avg)} V_{S1(max)} \right\} \right)$$

(26)

The total diode losses, $P_D$ of the MLHG are obtained as

$$P_D = \left[ \frac{2}{4} \left( \frac{(1+D)I_0}{D'} \right) + 4I_0D \right] V_f$$

$$+ \left\{ \frac{2}{4} \left[ \frac{1+D}{D'} \sqrt{1-D} \right] + 2 \left[ \frac{2I_0D}{V_f} \right]^2 \right\} R_f$$

(27)

Diode’s turn OFF loss is obtained by considering switching frequency ($f_s$), blocking voltage ($V_r$) and reverse recovery charge ($Q_{rr}$). Turn-On loss is observed to be very small and it can be neglected.

$$P_{DS} = Q_{rr} * \frac{V_r}{f_s} \frac{f_s}{2} \frac{(t_r1 + t_f1) I_{S1(avg)} V_{S1(max)}}{V_r}$$

(28)

Similarly, the loss in the capacitor, $P_C$ is determined by

$$P_C = \left\{ 2 \left[ \frac{(1+D)I_0}{D'} \right] + 2 \left[ \frac{2I_0D}{\sqrt{D'}} \right]^2 \right\} R_{C(ESR)}$$

(29)

Using the equations (24)-(29), the total losses in the MLHG converter are determined to estimate the converter’s efficiency. The total losses in the converter are calculated using the specification in Table 5 and it is observed to be 5.4 W. The most predominant loss in MLHG converter is diode loss since the number of diodes is four. The theoretical efficiency of MLHG converter for the chosen rating is 90.2%.

**IV. RELIABILITY ANALYSIS**

To perform the reliability analysis, the ratings of the components in the converters are identified. Number of components in MLHG converter is illustrated in Figure 7(a). To highlight the components considered for reliability study is presented in Figure 7(a). The reliability evaluation is carried out according to the steps described in Figure 7(b). Figure 7(b) depicts the flowchart of the procedure to determine the reliability of the high gain dc-dc converters. Reliability is the probability that a system will perform as necessitated under normal operating and environmental condition. The device performance not only depends on the manufacturing process and material but it indirectly relies on the working environment. Power electronic engineers need to work out on the materials to meet the several environmental situations. MTTF is estimated for the environmental condition for the derived topologies using military handbook. Diverse environmental situations change components’ failure rates. The failure rate of the components is different according to the environmental conditions whether it is used in ground or space. As a result, the consequence of the environmental condition on failure rate will be incorporated by environmental factor $\pi_E$. According to MIL-HDBK-217F, failure rate of electronic components [31] is evaluated by

$$\lambda_{component} = \lambda_b \prod_{i=1}^{k} \pi_k$$

(30)

where $k$ is the number of $\pi$ factors that persuade the component failure rate. Failure rate is the frequency with which an element fails and symbolized by the Greek letter $\lambda$. It is expressed in failures per unit of time. It is mainly used in reliability engineering. In this section, the failure rate of each component in the converters is estimated and its influencing factors are also discussed. Table 3 gives the failure rate specifications of the components to perform the failure rate analysis.
TABLE 3. Specification of the components in the converter for reliability analysis.

| Components | MLHG Converter |
|------------|----------------|
| Switch     | IRF 630, [200V, 10A] | [θJC = 1.7°C/w, Rds(on)= 0.4 Ω, output capacitance = 240 pF] |
|            | IRF 520, [100V, 10A] | [θJC = 2.5°C/w, Rds(on)= 0.27 Ω, output capacitance = 150 pF] |
| Diode      | MBR 10 100CT, [100V, 5A] | [θJC = 4°C/w, R= 0.15 Ω] |
|            | MBR 10 2000CT, [200V, 5A] | [θJC = 4°C/w, R= 0.17 Ω] |
| Inductor   | 5/0 μH, 6.3 A (τc = 23 mΩ) | 200 μH, 6 A (τc = 350 mΩ) |
|            | 500 μH, 2 A (τc = 361 mΩ) | |
| Capacitor  | Fixed, Electrolytic, Solid aluminium |
|            | [100V, 5A]; 10-20 μF; Res≈ 0.2 to 0.5 Ω |
|            | [200V, 5A]; 1-10 μF; Res≈ 1 Ω |

Most of the failure rate of the components can also be given in general form as

\[
λ_F = λ_b π_T π_Q π_E \text{ Failures/}10^6\text{hrs} \tag{31}
\]

where \(λ_b\) is the base failure rate which is usually expressed by a model relating the influence of temperature and electrical stresses on the components. The \(π\) factors such as \(π_T\), \(π_Q\) and \(π_E\) represent the stresses due to thermal, quality and environment respectively. A bottom-up approach is incorporated to estimate the reliability of the derived topologies. Temperature factor depends on hot spot temperature in inductors and junction temperature for semiconductor devices.

The failure rate not only depends on the temperature but also on application (\(π_A\)) and quality factor (\(π_Q\)). The quality of materials used in manufacturing of the devices affects the failure rate. In most of the reliability analysis in literature, environmental factor (\(π_E\)) is taken as 1. However, in this work, environmental factors for all parts are considered according to the chosen applications. Temperature effect on each part is determined by investigating power loss effect in the components of the converters. Hence, temperature is a significant factor which persuades the component’s failure rate. The effect of temperature on part’s failure rate is expressed by temperature factor (\(π_T\)) which is a function of part’s junction temperature, \(T_j\) for semiconductor devices or hot-spot temperature, \(T_{HS}\) for magnetic element.

**A. FAILURE RATE OF SEMICONDUCTOR SWITCH**

The switch failure rate is given as

\[
λ_{SW} = λ_b π_T π_A π_Q π_E \text{ Failures/}10^6\text{hrs} \tag{32}
\]

where \(π_A\) is the application factor. It gives the usage of the device for an application and its power rating. In this case, it is a switching device with a power rating less than 50 W. The quality factor (\(π_Q\)) depends upon the class and level of screening executed on the devices. Depending on the power conditioning and qualification tests, the values are specified in the handbook. The effect of environmental stresses on the device in the practical environment can be accommodated through an environmental factor, \(π_E\). Environmental symbols used for this analysis is \(G_M\). \(G_M\) represents the environment in which the devices are mounted in wheeled vehicles.

The thermal stress on the device is computed using

\[
π_T = \exp \left( -1925 \frac{1}{T_j + 273} - \frac{1}{298} \right) \tag{33}
\]

where \(T_j\) is the junction temperature which is determined by

\[
T_j = T_C + \theta_{JC}.P_{SW} \tag{34}
\]

In the above equation, \(T_C\) is the case temperature which is obtained from the default case temperature value for all environments available in the handbook. \(P_{SW}\) is the total power loss (Conduction + Switching loss) of the semiconductor switch and it is presented in equation (26). \(θ_{JC}\) is the junction to case temperature of the switch which is found from the datasheet of the semiconductor switch.

The power losses (\(P_{SW}\)) in the switch for various derived topologies are estimated as per the equation (26). Specification of the switch in converters is given in Table 3. According to the specification of the model chosen, the losses of the switch are calculated and it is used to estimate the junction temperature. With the junction temperature, the thermal stress on the power switch is calculated. If the losses on the switch are less, then the thermal stress is reduced.

**B. FAILURE RATE OF DIODES**

The failure rate of the diode is expressed as

\[
λ_D = λ_b π_T π_S π_Q π_E π_C \text{ Failures/}10^6\text{hrs} \tag{35}
\]

where \(π_S\) is the electrical stress factor which is obtained by calculating the voltage stress ratio. The voltage stress ratio is the ratio between voltage applied and rated voltage. Total voltage stress ratios for each topology are calculated and its corresponding electrical stress factor, \(π_S\) is chosen from the handbook. \(π_C\) is the contact construction factor depending on the type of bonding required for making contact.
in printed circuit board. Metallurgical bonding is selected for this device since it is superior and cost-effective. The result of the physical contact set up with the diode on the printed circuit board is found by the contact construction factor ($\pi_C$). This factor is unity for metallurgically bonded contacts.

If the diode is used as the switching device, then the temperature factor is given as

$$\pi_T = \exp\left(-3091\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right)$$  \hspace{1cm} (36)

where $T_j$ is the junction temperature which is determined by $T_j = T_{AC} + \theta_{jc}P_D$. The losses in the diode are denoted as $P_D$. $\pi_T$ factor is estimated similar to MOSFET as in the previous section. The power losses in the diodes are obtained by the equation (27).

**C. FAILURE RATE OF INDUCTORS**

The initial step in calculating the inductor’s failure rate is to select the inductor type. The failure rate of inductors is expressed as

$$\lambda_I = \lambda_b \cdot \pi_Q \cdot \pi_E \cdot \pi_C \quad \text{Failures}/10^6\text{hrs}$$  \hspace{1cm} (37)

Since fixed inductor is selected, the construction factor $\pi_C$ is one.

The value base failure rate of inductor is given as $\lambda_b = 0.00035 \exp\left(\frac{2500 + 273}{407}\right)^{10}$ for class C insulation. Class C insulation is preferred for the application operating beyond the $125\degree C$ temperature. Where $T_{HS}$ represents the hot spot temperature. The two factors to be considered for the hot spot temperature analysis in inductor are radiating surface area and power loss incurred in the inductor. This is given by

$$T_{HS} = T_A + 1.1(\Delta T)$$  \hspace{1cm} (38)

where $T_A$ is the inductive device ambient operating temperature ($\degree C$) and $\Delta T$ is the average temperature rise above ambient $\Delta T = \frac{125WL}{A}$; $W_L$ is the power loss in case radiating surface area ($A$). Power loss related to inductors is obtained by the equation (24).

**D. FAILURE RATE OF CAPACITORS**

The failure rate of capacitors is given by

$$\lambda_C = \lambda_b \cdot \pi_{CV} \cdot \pi_Q \cdot \pi_E \quad \text{Failures}/10^6\text{hrs}$$  \hspace{1cm} (39)

The base failure rate is generally influenced by the temperature and voltage stresses on the components. $\pi_{CV}$ is the capacitance factor depends on the value of capacitance used in the converters and it mainly depends on the dielectric material of the capacitors. It is determined by 0.34$C^{0.18}$. The failure rate of capacitor is also calculated similarly to other components of the converters. The equation for the base failure rate of the capacitors is given by

$$\lambda_b = 0.00254 \left(\left(\frac{S}{0.5}\right)^3 + 1\right) \exp\left(5.09 \left(\frac{T + 273}{358}\right)^5\right)$$  \hspace{1cm} (40)

where $S$ is the ratio of working to rated voltage and $T$ is the ambient temperature in $\degree C$.

**E. RELIABILITY ASSESSMENT BASED ON FAILURE RATE OF COMPONENTS**

From the above evaluation of reliability analysis, the mean time to failure (MTTF) of MLHG topology is obtained using the failure rate of the component [32]. Entire analysis is performed by considering the environmental condition of electric vehicle application. Figure 8 (a) and (b) depict the circuit configurations which highlights the modification made in the position of the capacitor to reduce its voltage stress. Figure 8 (c) illustrates that the increase in temperature and voltage stress ratio (applied voltage/rated voltage) increases the failure rate of the capacitor.

Table 4 presents the failure rate of the components in MLHG converter. Furthermore, the MTTF is also obtained and represented in kilohours. From Fig 8(c), it is noted that the stress ratio and temperature have greater impact on the base failure rate of the capacitor. According to Figure 8(a), the stress across the capacitor $C_1$ is $(2-D) \frac{V_g}{(1-D)}$. However, with the modification made in Figure 8(b), the stress across the capacitor $C_1$ is reduced to $V_g/(1-D)$. This reduction in voltage stress creates greater impact on the failure rate of the capacitor $C_1$. Figure 8 (c) depicts the significance of both temperature and stress ratio on the base failure rate of the capacitor. The importance of voltage stress on the capacitor relating to the reliability of the components is illustrated in Fig 8 (d). It is observed that with lesser voltage stress on the capacitor ($C_1/C_2$) increases the reliability of the passive component. To highlight the derivation of the modified Luo converter, a comparative study is performed with MLHG converter and the cascaded version of elementary Luo converter with traditional boost converter as depicted in Figure 3(a).

**F. RELIABILITY ASSESSMENT OF CAPACITOR WITH VARIATION IN SWITCHING FREQUENCY**

In this section, the further analysis on reliability of capacitor is extended by varying the switching frequency of the converter. The failure rate of the capacitor $C_1$ and the impact of switching frequency is analyzed with the following expression.

The failure rate of the capacitor is inversely proportional to the switching frequency and the expression is given as

$$\lambda_C \propto 0.34 \left[\frac{f_D(1 + D)D}{f_S \Delta V_g}\right]^{0.18}$$  \hspace{1cm} (41)
The impact of switching frequency on the failure rate is observed and depicted in Figure 8 (f). According to this Figure, it is noted that the failure rate of the capacitor is higher for low switching frequency.

The main contributions and the need for the derivation of the topology are listed as

1. The most vulnerable components in the power converters are capacitor and semiconductor. Hence, it is always recommended to design a topology by considering the stresses on these vulnerable components. In this MLHG converter, the capacitor stress is reduced by modifying the topology as depicted in Fig 8 (b).

2. The failure rate of the capacitor has cubic dependence on voltage stress of the capacitor. With increase in stress ratio and temperature, the reliability of capacitor is reduced which is depicted in Fig 8(c). This motivates us to derive this topology.

3. If the capacitor C1 is connected as illustrated in Fig 8 (a), the reliability of C1 is get reduced which is analyzed and represented in Fig 8 (e).

4. This modified version of capacitor and diode can be applied to any topology to be derived for high gain. This feature helps the researchers to avoid the idea of cascading of two converters for high gain application.
5. The impact of switching frequency on the reliability of the capacitor is analyzed and the result is presented in Fig 8 (f) which will help in design of the power converter.

V. SENSITIVITY ANALYSIS
It is also recommended to design a converter which depicts small in the voltage gain for the variation of duty cycle and the internal parasitic resistance of passive components. In this section, sensitivity analysis is analyzed to observe the variation in voltage gain for the change in duty cycle [37]. The voltage gain of the proposed topology by considering the internal resistance of inductor is

\[ G_V = \frac{(2 - D)(1 - D)}{(1 - D)^2 + \frac{(1 + D)^2 R_L}{R_O(1 - D)^2} + \frac{(1 + D)^2 R_{L2}}{R_O(1 - D)^2} + \frac{R_{L3}}{R_O}} \] (42)

where \( R_L \) is the internal parasitic resistance of the inductor. \( G_V \) denotes the voltage gain and \( R_O \) is the load resistance. To simplify the analysis, the internal resistance is considered as same for all the inductor and the voltage gain expression is simplified as

\[ G_V = \frac{R_O(2 - D)(1 - D)(1 - D)^2}{R_O(1 - D)^4 + (3 - D)^2 R_L} \] (43)

This analysis is performed by differentiating (43) with respect to \( D \). The final expression yielded after the mathematical manipulation is (44), as shown at the bottom of the page.

The change in non-ideal voltage gain of the MLHG converter is observed to be high for the duty cycle greater than 0.5 for all the value of the internal resistance of the inductor, \( R_L \) which is illustrated in Fig 9.

VI. ENERGY VOLUME OF CAPACITOR
The energy stored in the capacitor is obtained by multiplying the energy density by the volume between the plates. It is measured in joules and it is directly proportional to the voltage stress across the capacitor. In this section, the expression for the energy volume of the capacitor is obtained and analyzed.

The energy stored in the capacitor \( C_1 \) in elementary Luo converter is

\[ E_{C1V} = \frac{1}{2} \left( \frac{(1 + D)(2 - D)DV_g}{(1 - D)^2 R_{OFS} \Delta V_{C1}} \right) \left( \frac{(2 - D)V_g}{1 - D} \right)^2 \] (45)

The energy stored in the capacitor \( C_1 \) in modified Luo converter is

\[ E_{C1V} = \frac{1}{2} \left( \frac{(1 + D)(2 - D)DV_g}{(1 - D)^2 R_{OFS} \Delta V_{C1}} \right) \left( \frac{V_g}{1 - D} \right)^2 \] (46)

Using (45) and (46), surf plot is obtained from Matlab for the comparative study and the plot is depicted in Fig 9(b).

It is observed from the Figure that the maximum voltage across the capacitor has significant impact on the energy volume of the capacitor. This Figure depicts the advantage of modified structure compared to the conventional topology.

VII. COMPARISON RESULTS
The proposed converter and recently reported converters in literature are compared and discussed in this section. This converter is derived with minimal capacitor stress with high boosting capability. The comparison of the proposed converter with other converters taken for the study is presented in Table 5. The specification taken for comparison is also mentioned in Table 5. This analysis is done for all the capacitors in the converters excluding the output (filter) capacitor. Since the maximum voltage stress on the capacitor \( C_0 \) is equal to the load voltage for all the dc-dc converters. From this analysis, it is observed that the derived topology
In addition to that, the comparison is further extended by comparing the suggested topology with other topologies in the literature concerning the voltage gain and total component count. The voltage conversion ratio of the MLHG converter is compared with and without boosting cell. This comparison is depicted in Figure 10 (a). From the observation, it is noted that the voltage gain of derived topology is high compared to other topologies. The proposed converter has minimal capacitor stress which increases the reliability of this passive component and also reduces the cost of the converter.

### TABLE 5. Comparison of MLHG converter with other converters in literature.

| Converter                                      | Gain                         | No of SW | No of Diode | No of Inductor | No of Capacitor | Duty cycle | Capacitor Voltage stress |
|------------------------------------------------|------------------------------|----------|-------------|----------------|-----------------|------------|--------------------------|
| Proposed                                       | \( \frac{2 - D}{D} \frac{1 + D}{2 + D} \) | 2        | 4           | 3              | 5               | 0.6        | 12 V, 24 V               |
| Interleaved boost converter [18]               |                              | 3        | 3           | 3              | 3               | 0.7        | 17 V, 34V (2)            |
| Interleaved bidirectional converter [19]       |                              | 8        | --          | 5              | 4               | 0.55       | 81 V, 54 V               |
| Quasi-Z-source network DC–DC converter [22]    |                              | 1        | 6           | 2              | 7               | 0.47       | 40 V, 28V (3)            |
| High gain converter with switched inductor cell [23] | \( \frac{1 - 2D}{D} \) \text{[N = 1]} | 3        | 11          | 6              | 1               | 0.57       | NIL                      |
| High gain converter with coupled inductor [21] | \( \frac{1 + 5D}{D} \) \text{[M = 1]} | 1        | 4           | 2              | 5               | 0.55       | 27V, 29V (3)             |

Note: M= Number of boosting cell; N= number of turns in coupled inductor

Figure 10. (a) Voltage conversion ratio of the proposed topology and few topologies reported in the literature (b) Total component counts of derived topology and the topologies reported in [18], [19], [22]–[24] (c) Comparison of switch voltage of derived topology and the topologies reported in [33]–[36].
FIGURE 11. Results from simulation (a) Output voltage for $D = 0.5$ (b) Switch voltage stress ($S_1$ & $S_2$) (c) Diode voltages ($D_{11}, D_{21}, D_{b1}$ & $D_{b2}$) (d) Capacitor voltage ($C_1, C_2, V_{Cb1}$ & $V_{Cb2}$) (e) Inductor current ($L_1, L_2, L_o$) (f) Dual output modified Luo high gain dc-dc converter (g) Simulation results for two different output voltage level (h) Simulation results for same output voltage level.
to converters taken for comparison with the voltage gain of 9. Figure 10 (b) presents the comparison of the total component count of the converters. From this figure, it is viewed that the proposed converter has the least component count compared to other converters except the converters reported in [18]. However, the voltage gain of the converters is observed to be less compared to the proposed converter for the selected rating. It is also observed that the duty cycle of the converter in [22] is very less compared to the MLHG converter. However, it achieves this gain with very high component count of 16 and this converter can operate only for the duty cycle less than 0.5. The converter in [23] has no capacitor but it achieves this high gain with many inductors. Furthermore, the voltage stress on the switches on the MLHG converter is not equal to the output voltage as conventional boost converter. This feature is highlighted by comparing the switch voltage stress of MLHG converter with similar two switch converter in the literature. Fig 10 (c) depicts that MLHG converter has lesser switch voltage stress for the duty cycle less than 0.5 duty cycle compared the converter reported in the literature [34] [36]. However, it shows lesser switch voltage stress for all the value of voltage gain (4-25 times).
TABLE 6. Comparison of semiconductor voltage stress on MLHG converter with converters in literature.

| Converter               | Switch voltage stress | Output/ VM diode voltage stress |
|-------------------------|-----------------------|--------------------------------|
| Proposed                | $\frac{V_s}{D^2}$ [2 - D]$V_d$ | $\frac{2 - D}{D^2}$ $V_d$ |
| Quadratic boost         | $\frac{V_s}{D^2}$     | $\frac{V_d}{D^2}$              |
| Modified Sepic [34]     | $\frac{V_s}{D^2}$     | $\frac{V_d}{D^2}$              |
| A-SI/P-SC converter [35]| $V_{s1} = V_{s2} = \frac{V_d}{1 - D}$ | $\frac{2V_d}{1 - D}$ |
| mSiBC [36]              | $V_{s1} = V_{s2} = \frac{V_d}{1 - D}$ | $\frac{1 + D}{1 - D} V_s$ |
| Noncoupled Sepic [37]   | $V_{s1} = V_{s2} = \frac{V_d}{1 - D}$ | $\frac{2V_d}{1 - D}$ |

compared to the converters in [33], [35] and quadratic boost converter. Table 6 presents the comparison of switch and diode voltage stress of MLHG converter with the converters reported in [33]–[36].

VIII. SIMULATION AND EXPERIMENTAL RESULTS

In this section, with Matlab/Simulink, the MLHG converter is simulated and the results are discussed. Figures 11 (a)-(e) present the simulated results. From these simulated results, it is observed that the theoretical results closely match with the simulated results.

In addition to the simulation of modified Luo high gain dc-dc converter, the proposed topology is restructured to dual output converter which is more required for suggested Electric vehicle application. The restructured dual output topology depicted in Fig 11 (f) is simulated in Matlab and the results are presented in Fig 11 (g) and (h). Different voltage levels are essential for more than one electronic auxiliary load in an electric vehicle. For this application, the proposed converter is more appropriate with multioutput capability. In this section, the dual output nature of the converter is discussed, and similarly, it can be extended to multi-output depending on the requirement. The two outputs obtained from this modified Luo converter can be easily interfaced with an electric vehicle, as shown in the schematic diagram. Electric vehicle dc power supply has to satisfy the demand for more than a load with different voltage levels and the same voltage from other load points. In the converter, the output voltage $V_{01}$ is regulated through switch $S_{01}$, and output voltage $V_{02}$ is regulated through switch $S_{02}$. The simulation results obtained validate the dual output operation of the proposed converter. The converter exhibits two different voltage levels and two outputs with the same voltage levels in this simulation.

To validate the performance of the derived topology, a prototype is implemented to analyze the MLHG converter. The power rating is 50 W and the input voltage is chosen as 12 V as shown in Figure 12 (a)-(k). The digital storage oscilloscope DSOX2002A is used to record the necessary waveforms for the validation. Figure 12 (a) presents the picture of the proposed topology. The photograph of the complete setup is presented in Figure 12 (b). Figure 12 (c) and (d) illustrates the input and output voltage of the topology with 0.25 duty cycle as presented in Figure 12 (e).

Voltage across the switches and diodes are observed and presented in Figure 12 (f) - (i). Voltage across the capacitor and current through the inductors are depicted in Figure 12 (j) and (k) respectively. According to figures, the results obtained matches closely with the simulated and theoretical results. Table 7 and 8 present the component details and validation of the results obtained respectively. From the Table 8, it is observed that hardware results have excellent accordance with the theoretical and simulation results.

IX. CONCLUSION

A novel modified Luo high gain converter for electric vehicles is considered and analyzed in this article. The detailed steady-state analysis of the proposed topology is presented in this article. Since the capacitors are more prone to failures in most of the converters, designing a converter with low stress on the capacitor is recommended. The unique features of the suggested topology are
• Minimal capacitor stress compared to others considered for comparison which in turn increases the reliability of the capacitors. This advantage is validated by evaluating the failure rate of the capacitor and analyzing its performance with the stress ratio and temperature.
• The derived converter has an extended voltage conversion ratio with minimal capacitor stress and component count.
• The voltage conversion ratio of the proposed converter is high with a very low duty cycle compared to a few converters reported in the literature.
• The suggested modification can be applied to any topology for high gain conversion.
• A methodology is proposed for the derivation of high gain converter without cascading.
• The stresses on the switches are significantly less compared to other converters.

Finally, 50 W prototype of the presented topology is implemented to validate the theoretical and simulated results. The results acquired validate the capacitor and switches stresses in the derived topology. As a future scope, the dynamic analysis of the suggested topology and EMI issue will be carried out.

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