Quantum Carry Lookahead Adders for NISQ and Quantum Image Processing

Himanshu Thapliyal, Edgard Muñoz-Coreas and Vladislav Khalus
Department of Electrical and Computer Engineering
University of Kentucky, Lexington, KY, USA
Email: hthapliyal@ieee.org

Abstract—Progress in quantum hardware design is progressing toward machines of sufficient size to begin realizing quantum algorithms in disciplines such as encryption and physics. Quantum circuits for addition are crucial to realize many quantum algorithms on these machines. Ideally, quantum circuits based on fault-tolerant gates and error-correcting codes should be used as they tolerant environmental noise. However, current machines called Noisy Intermediate Scale Quantum (NISQ) machines cannot support the overhead associated with fault-tolerant design. In response, low depth circuits such as quantum carry lookahead adders (QCLA)s have caught the attention of researchers. The risk for noise errors and decoherence increase as the number of gate layers (or depth) in the circuit increases. This work presents an out-of-place QCLA based on Clifford+T gates. The QCLAs optimized for T gate count and make use of a novel uncomputation gate to save T gates. We base our QCLAs on Clifford+T gates because they can eventually be made fault-tolerant with error-correcting codes once quantum hardware that can support fault-tolerant designs becomes available. We focus on T gate cost as the T gate is significantly more costly to make fault-tolerant than the other Clifford+T gates. The proposed QCLAs are compared and shown to be superior to existing works in terms of T-count and therefore the total number of quantum gates. Finally, we illustrate the application of the proposed QCLAs in quantum image processing by presenting quantum circuits for bilinear interpolation.

I. INTRODUCTION

Quantum computing offers significant speedups for algorithms for encryption, searching and scientific computations [1] [2]. Arithmetic units such as adders are needed to implementing many of these quantum algorithms. Thus, researchers proposed adders for quantum computers [3] [4].

Existing quantum computers (Noisy Intermediate Scale Quantum (NISQ) machines) are plagued by noise errors [5] [6]. Computations can fail due to quantum operation errors and quantum coherence errors [5]. To reduce impact from coherence errors, the depth (number of gate layers) should be minimized.

Thus, low depth arithmetic circuits (such as quantum carry lookahead (QCLA) adders) have been proposed (see [2] [3] [4]). Out-of-place QCLAs (both inputs restored and sum on ancillae) such as [3] [4] and [3] and in-place QCLAs (one input restored and sum replaces other input) such as [4] [3] and [7] are proposed. However, these works suffer from overhead in terms of T gates and qubits. The fault-tolerant implementation cost of the T gate is higher compared to other quantum gates (such as Clifford gates) [6] [9]. By using recent developments such as improved Toffoli gate implementations (see [2]) we can design QCLAs with low T gate and/or qubit overhead.

To overcome shortcomings in existing works, this work proposes a novel QCLA for NISQ and fault-tolerant machines. In-place QCLA and out-of-place QCLA implementations for the design are shown. Both designs enjoy reduced T gate cost and qubit cost compared to the existing works. The proposed QCLAs use a proposed uncomputation gate with a T-count of 3. The proposed uncomputation gate allows the QCLAs to be used on NISQ machines. The proposed QCLA designs are based on the NOT gate, CNOT gate, Toffoli gate, logical AND gate and the novel uncomputation gate. The logical AND gate depicted in Figure 1 is presented in [9]. The existing designs in [4] are based solely on CNOT, NOT and Toffoli gates.

The proposed work modifies the design methodologies in [4] by replacing Toffoli gate with logical-AND gate and uncomputation gate pairs into the design where possible. The proposed uncomputation gate is used to avoid the measurement operation required by the uncomputation gate proposed in [9]. We seek to avoid the measurement operation because (i) the errors associated with the operation (such as SPAM errors) and (ii) the increased length of time to perform measurement compared to gates on NISQ machines. In consequence, the number of T gates thereby the total number of quantum gates used in the proposed design is significantly reduced compared to existing work.

Further, quantum computing has been applied to image orientation problems and image pattern recognition [10] [11]. To implement quantum image processing algorithms, images must be encoded on quantum hardware and circuits to manipulate image representations must be designed. In this work, we illustrate an example of a quantum circuit for quantum image processing by presenting quantum circuits for bilinear interpolation based on the proposed QCLAs.

II. PROPOSED DESIGN OF OUT-OF-PLACE QCLA CIRCUIT

The 8 step methodology to implement proposed out-of-place QCLA is generic and can be used to implement a QCLA circuit of any size. The methodology is a modified version of the design methodology presented in [4]. An example of the proposed QCLA is shown in Figure 2. The proposed QCLA
ancillae. The steps to implement QCLA are shown along with qubits can be set to computational basis values for reuse as

\[ \sum_{y=1}^{w(n)} \leq n \]

At the end of computation, \( A \) and \( B \) will contain the sum of the addition of \( a \) and \( b \). The QCLA will restore \( Z \) to \( \frac{1}{\sqrt{2}} \left( |0\rangle + e^{i\pi/4} |1\rangle \right) \). The QCLA will restore \( X \) to \( \frac{1}{\sqrt{2}} \left( |0\rangle + e^{i\pi/4} |1\rangle \right) \).

Fig. 3: In-place QCLA for the case of adding two 4 bit values \( a \) and \( b \).

TABLE I: Cost Comparison of Out-of-place QCLAs

| Design                  | T-count Equation |
|-------------------------|------------------|
| Draper et al. ([4])     | \( 35n - 21w(n) - 21\lfloor \log(n) \rfloor - 7 \) |
| Thapliyal et al. ([3])  | \( 35n - 14 \) |
| Babu et. al. ([8]*     | \( 54 \cdot n \) |
| Proposed                | \( 25n - 14w(n) - 14\lfloor \log(n) \rfloor - 7 \) |

* Circuits modified to remove garbage output. We use the methodology in [12] to remove the garbage output.

Table I indicates the proposed out-of-place QCLA has T-count cost of order \( O(n) \). The proposed QCLA requires
TABLE II: Cost Comparison of In-Place QCLAs

| Design             | T-count Equation |
|--------------------|------------------|
| Draper et al. (13) | $70n - 21w(n) - 21\lfloor \log(n) \rfloor - 21w(n-1) - 21\lfloor \log(n-1) \rfloor - 49$ |
| Thapliyal et al. (15) | $\frac{203}{2}n - 28$ |
| Cheng et al. (17)  | $\frac{14}{7}n^3 + \frac{21}{7}n^2 - \frac{49}{7}n$ |
| Proposed           | $46n - 14w(n) - 14\lfloor \log(n) \rfloor - 14w(n-1) - 14\lfloor \log(n-1) \rfloor - 36$ |

$w(n) = n - \sum_{y=1}^{\infty} \left\lfloor \frac{y}{2^n} \right\rfloor$

53.70% fewer T gates than the design by Babu et al., 28.57% fewer T gates than the designs by Draper et al. and Thapliyal et al.

Table II indicates that the proposed in-place QCLA has a T-count cost of order $O(n)$. The proposed in-place QCLA requires 34.29% fewer T gates than the designs by Draper et al., 9.36% fewer T gates than the designs by Thapliyal et al. and has a polynomial factor improvement over the work in Cheng et al.

V. APPLICATION IN QUANTUM IMAGE PROCESSING

We will now illustrate how the proposed QCLAs can be used to implement a quantum circuit for bilinear interpolation. Interpolation is of interest because it is used in image processing operations such as zooming, rotations, and resampling [13] [14]. Bilinear interpolation is a well-established method for scaling images [15]. Bilinear interpolation uses linear interpolation to sequentially perform interpolation for each pixel location variable $x$ and $y$. Figure 4a shows an example coordinate mapping of a bilinear interpolated pixel at original location $(X, Y)$. Further details about bilinear interpolation can be found in [15].

The QCLA circuits can be used to implement quantum circuits for bilinear interpolation. We can build quantum circuits for scaling down and for scaling up an image by an integer $n$. Scaling up by $n$ will increase an image by $2^n$ and scaling down by $n$ will decrease an image by $2^n$. We show the complete quantum bilinear interpolation circuit for the scale down operation in Figure 4b. Both quantum bilinear interpolation use (i) quantum adder, (ii) quantum subtractor and (iii) quantum multiplier. The required block of quantum adder, quantum subtractor and quantum multiplier can be easily designed from the proposed quantum carry lookahead adders [16]. As an illustrative example, we have shown a quantum integer multiplication circuit that is optimized for T-count and qubits [17]. The building blocks of the quantum integer multiplication circuit are (i) quantum Ctrl-Add circuit and (ii) arrays of Toffoli gates. The quantum Ctrl-Add circuit is based on a resource efficient quantum carry look-ahead adders presented in this work. Figure 5 shows an example of the proposed multiplier for the case of multiplying two 6 bit integers. In Figure 5 quantum registers $|A\rangle$ and $|B\rangle$ contain the inputs $a$ and $b$ to be multiplied. The proposed quantum integer multiplication circuit implements the shift and add multiplication algorithm. The placement of the Ctrl-Add circuits eliminates the need for gates to implement the shifting operation (see Figure 5). To reduce gate cost Ctrl-Add circuits are replaced by Toffoli gate arrays where possible.

We follow the procedures in [16] to implement both quantum bilinear interpolation circuits. Both circuits take the original pixel’s position $|Y\rangle$, $|X\rangle$ and color information $|C_{Y,X}\rangle$ as inputs. The color information for pixels at locations $(y+1,x)$, $(y,x+1)$ and $(y+1,x+1)$ are also inputs. The circuitry outputs the scaled pixel’s location $|\hat{Y}\rangle$ and $|\hat{X}\rangle$ and its color.
We determine the location information for the scaled pixel without gates by either appending ancillae or truncating the input location values. The quantum bilinear interpolation circuit to scale down an image evaluates expression [1] for the scaled color value:

$$
(2^n - \tilde{Y}) \cdot (2^n - \tilde{X}) \cdot C_{Y,X} + \begin{vmatrix} |Y \rangle \cdot (2^n - \tilde{X}) \cdot C_{Y,X+1} \\ \tilde{Y} \cdot (2^n - \tilde{X}) \cdot C_{Y,X+1} \\ \tilde{Y} \cdot \tilde{X} \cdot C_{Y,X+1} + 1 \\ \frac{C_{Y,X}}{2^{2^n}} \end{vmatrix} + 2^{2^n} \tag{1}
$$

Where $\tilde{Y} = Y_{n-1:0}$ and $\tilde{X} = X_{n-1:0}$. The quantum bilinear interpolation circuit to scale up an image evaluates expression [2] for the scaled color value:

$$
(2^n - \tilde{Y}) \cdot (2^n - \tilde{X}) \cdot C_{Y,X} + \begin{vmatrix} 2^n - \tilde{Y} \cdot (2^n - \tilde{X}) \cdot C_{Y,X+1} \\ \tilde{Y} \cdot (2^n - \tilde{X}) \cdot C_{Y,X+1} \\ \tilde{Y} \cdot \tilde{X} \cdot C_{Y,X+1} + 1 \\ \frac{C_{Y,X}}{2^{2^n}} \end{vmatrix} + 2^{2^n} \tag{2}
$$

Where $\tilde{Y} = Y_{m+n-L-1:0}$ and $\tilde{X} = X_{m+n-L-1:0}$.

Details of the design of the quantum bilinear interpolation circuits for the scale down operation and for the scale up operation are illustrated in [10]. We determine $C_{Y,X}$ for both circuits without division by truncating the quantum register containing the result of computation (see Figure 4b).

VI. CONCLUSION

In this work, we propose quantum circuits for carry look-ahead addition for NISQ machines. We propose designs for an in-place QCLA and out-of-place QCLA. The proposed QCLAs are optimized for low T gate cost. The proposed QCLAs are based on the NOT gate, the CNOT gate, the Toffoli gate, the logical AND gate and the proposed uncomputation gate. These designs are compared and shown to have reduced T gate and therefore total number of quantum gates compared to the existing work. The proposed QCLAs also enjoy qubit cost savings compared to existing work. We conclude that the proposed in-place QCLA and out-of-place QCLA can be used in larger quantum data-path circuits in NISQ machines or when fault-tolerant quantum circuit design is not possible. We also illustrate the application of the proposed QCLAs in image processing through the example of circuits for quantum bilinear interpolation.

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