Effect of Wafer Tilt During Ion Implantation on the Performance of a Silicon Traveling-Wave Mach-Zehnder Modulator

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ABSTRACT This paper reports a study of the effect of wafer tilt during dopant implantation on the performance of silicon PN phase shifter and traveling-wave Mach-Zehnder modulator. The PN phase shifter is designed and process simulated to include the effects of different fabrication processes in the device performance. The wafer tilt during implantation is varied from 0° to 3°, 5°, and 7°. The resulting crystal damage during dopant implantation to form the PN junction and the active concentration profile upon annealing, along with the formation of dopant–defect clusters, are discussed. Compared to 0° tilt, 7° tilt results in 1.58 × higher phase shift and better modulation efficiency. The overall phase shifter performance is improved using 5° wafer tilt for implantation resulting in 1.23 × lower absorption, 1.45 × better modulation efficiency, and 3.14 × higher 3 dB RC modulation bandwidth for lumped-driven phase shifter. A traveling-wave electrode to enhance the modulation bandwidth is used, and the modulator performance for non-return-to-zero on-off-keying modulation with –2.5 V bias and 2.5 Vpp drive signal across each arm is evaluated using a dual-arm push-pull drive. The sample with 5° tilt shows better traveling-wave and modulator high-speed characteristics compared to the other samples. Among the four samples with different wafer tilts, the sample with 0° tilt shows the worst phase shifter performance, and the sample with 3° tilt shows the worst modulator characteristics. The best overall performance is obtained for the sample with 5° tilt. Compared to the modulator with implantation at 0° tilt, the 5° tilted sample shows 2.3 × higher 6.4 dB electrical bandwidth and 1.36 × higher 3 dB electro-optic bandwidth at –2.5 V using a traveling-wave electrode with 1.48 × lower energy-per-bit for 5 km transmission at the KP4-forward-error-correction bit-error-rate threshold. The comparison of the effect of wafer tilt angles on various device metrics is presented and discussed.

INDEX TERMS Mach-Zehnder modulator, process simulation, silicon photonics, traveling-wave electrode.

I. INTRODUCTION

With rapid rate of increase in data traffic, there is a need to realize high link capacities and high-speed data integration. Optical modulators play an important role in integrating data into the light for free-space as well as fiber-optic communications. The global market for optical modulators has an expected growth of USD 8.14 billion for a forecast period 2021–2025 with a compound annual growth rate of 7.13% [1]. On-chip integrated silicon optical modulators have gained much popularity in recent years due to their compact size and low cost. Mach-Zehnder modulators (MZMs), as compared to ring modulators, have greater fabrication and temperature tolerance at the cost of having a larger footprint. Many studies have been done over the years to enhance the silicon modulator performance and mitigate various tradeoffs. The main component of an MZM is the phase shifter, which in silicon is realized through junction devices using the free-carrier plasma dispersion (FCPD) effect [2].

The modulator performance can be enhanced by using device-level and system-level engineering techniques. System-level engineering techniques include using higher-order modulation formats and different driving configurations to increase the modulation speed. Low bandwidth modulators can be used for high-speed operation...
using higher-order modulation formats like pulse amplitude modulation (PAM) [3], quadrature amplitude modulation (QAM) [4], etc. Generating higher-order modulation signals in the electrical domain leads to increased power consumption due to digital-to-analog converters [5]. Samani et al. presented different MZM architectures for generating PAM-4 signal in the optical domain using on-off keying (OOK) electrical signals [6]. Ding et al. used four MZMs driven by four electrical binary signals to generate a 16-QAM signal in the optical domain [7].

Device-level engineering techniques involve ways to enhance the FCPD effect and the modulation bandwidth. Sorianello et al. reported the intensity and phase modulation efficiency of single and double-layer graphene capacitive modulators on silicon for up to 50 Gbps operation [8]. Passoni et al. showed enhanced modulation efficiency in the range 0.1–0.5 V.cm in slow-light silicon MZM with interleaved PN junctions with waveguide grating structure [9]. He et al. demonstrated hybrid silicon/lithium niobate MZM with > 70 GHz bandwidth and 100 Gbps OOK modulation with 5 dB dynamic extinction ratio [10]. The authors have previously shown the effectiveness of using germanium in enhancing the performance of silicon modulators [11], [12]. Although multiple studies on improving modulator performance have been reported over the years, very few have reported on ways to improve the modulator performance of pure silicon modulators using device-level engineering techniques without using different materials and hybrid integration techniques. Yong et al. demonstrated U-shaped silicon PN phase shifters with improved modulation efficiency to realize power-efficient modulators [13]. Li et al. proposed a substrate removing technique to improve the modulation bandwidth of silicon MZM [14]. The authors have recently shown the dependency of the phase shifter metrics on pre-amorphization and annealing temperature and time [15]. The modulator performance can be optimized by adjusting various process parameters. A process simulation study can be used to emulate a fabricated device and to observe the effects of various process parameters on device metrics.

In this paper, the effects of wafer tilt during dopant implantation on the phase shifter and MZM performance are evaluated. To the authors’ knowledge, this is the first comprehensive study that covers the effect of wafer tilt angles on MZM metrics viz., modulation bandwidth, bit-error-rate (BER) performance, extinction ratio (ER), fiber transmission length, fiber dispersion tolerance, and energy-per-bit. The phase shifter design is given in section II. Section III presents the process study and discusses the implantation damage profile, active dopant concentrations, and dopant-defect cluster formation for different wafer tilt angles during implantation. The phase shifter metrics, along with the lumped element analysis, are given in section IV. Section V presents and discusses the traveling-wave electrode and modulator characteristics along with a comparison of various device metrics for different wafer tilts. Lastly, section VI concludes the paper.

II. PHASE SHIFTER STRUCTURE

The PN phase shifter cross-section is shown in Fig. 1(a). A <100> silicon-on-insulator wafer with 0.22 µm top silicon height (\(H\)), 2 µm buried silicon dioxide thickness (\(T_{BOX}\)), and 500 µm bottom silicon (not shown in figure) is used. The waveguide width (\(W\)) is 0.5 µm with 0.1 µm slab (\(h\)). The PN junction is at the middle of the rib with the highly doped contact regions 1.75 µm from the junction on either side (\(W_s = 1.5 \mu m\)). The top cladding (pre-metal dielectric) has a thickness (\(T_{PMO}\)) of 1.7 µm. The electrode dimension (\(W_t \times H_t\)) is 5.0 µm x 1.8 µm. The waveguide height and width are along the \(x\) and \(y\) axes with light propagation along the \(z\) axis. The wafer tilt angle (\(\theta\)) is shown in Fig. 1(b) and is defined as the angle between the ion beam and the normal to the wafer.

III. PROCESS SIMULATION

The phase shifter is designed using the process simulator, Silvaco® Athena. The Monte Carlo implant module based on the binary collision approximation (BCA) is used for dopant implantation with 5000 ion trajectories at room temperature (300 K). BCA is used to simulate the interaction of dopant atoms with the host material and is based on a series of
two-body interactions [16]. A brief history of different ion implantation models and the efficiency of BCA code can be seen in [17]. The wafer tilt angle, $\theta$, is varied from 0° to 3°, 5°, and 7°. The beam divergence is 1°. To form the P and N regions, boron and phosphorus are used with a dose of $5 \times 10^{13}$ cm$^{-2}$ and $2 \times 10^{13}$ cm$^{-2}$ at an energy of 17 keV and 30 keV respectively. A dose of $1 \times 10^{15}$ cm$^{-2}$ each of boron and phosphorus is used at an energy of 17 keV and 30 keV to form the P$^{++}$ and N$^{++}$ regions. Each implantation step is followed by rapid thermal annealing at 1100°C for 10 seconds in nitrogen ambient. An anisotropic uniform etch of 120 nm is done to form the P and N slab regions of thickness 100 nm. Oxide is deposited to form the upper cladding (PMD) layer. Vias are created to form the contact electrodes, and aluminum is deposited.

Implantation results in the dopant atoms taking interstitial sites and damaging the crystal order depending on the dopant dose and implantation energy. High-dose implants can lead to the formation of amorphous pockets in the crystal lattice. The amorphization threshold dose of boron and phosphorus in silicon is $> 10^{14}$ cm$^{-2}$ and occurs when the defect density is $> 10\%$ of the atomic density [18]. In this study, subamorphization doses of boron and phosphorus have been used to form the P and N regions. Annealing is done to recrystallize the damaged lattice and activate the dopant atoms, i.e. the interstitial dopant atoms substitutes a host atom [19]. Dopant implantation results in a Gaussian-like profile, the shape of which depends on the wafer tilt angles. For a $<100>$ oriented wafer, considerable ion channeling will occur along the crystallographic axes. Tilting the wafer reduces the degree of ion channeling [20]. Initial annealing results in greater diffusion of the implanted dopant Gaussian tail relative to the high concentration Gaussian peak, known as transient enhanced diffusion [21]. Dopant diffusion is aided by silicon interstitials and vacancies that are created during the dopant implantation step [22]. During annealing, defect recombination and defect clustering occur. Also, dopant-defect clusters may form, leading to $A_mV_n$ or $A_mI_n$ pairs, where $A$ is the dopant atom, and $V$ and $I$ represents vacancies and interstitials, respectively. Detailed defect reactions can be found in [18].

The lattice implant damage upon boron and phosphorus implantation is shown in Fig. 2(a) and (b) for different $\theta$. At higher tilt angles, due to lower ion channeling, the damage concentration increases near the surface as few atoms channel towards the bottom silicon-oxide interface. As $\theta$ increases, most of the interstitial dopant atoms occupy the top half of the waveguide at a distance of 0.11 $\mu$m from the surface. The active boron and active phosphorus concentration upon annealing is shown in Fig. 2(c) and
is given as \[24\] the carrier concentration at 1550 nm wavelength of operation \(n_1^{\alpha}\) and absorption \(\alpha\) with increase of depletion width. The corresponding change in the junction leads to majority carrier extraction, resulting in the carrier distribution in the waveguide and is given as \[25\]

\[
\begin{align*}
n_{\text{eff}} &= \int \int \Delta n(x, y) |E(x, y)|^2 \, dx \, dy \\
\alpha_{\text{eff}} &= \int \int [\alpha(x, y) - \Delta \alpha(x, y)] |E(x, y)|^2 \, dx \, dy
\end{align*}
\]

where \(|E|^2\) is the normalized mode power in the rib waveguide.

The phase shift (\(\Delta \phi\)) is calculated as \[2\]

\[
\Delta \phi = \frac{2\pi n_{\text{eff}} L}{\lambda}
\]

where \(L\) is the phase shifter length and \(\lambda\) is the free-space wavelength of light.

The surface plot of the free-carrier concentration at 0 V bias across the waveguide rib for \(\theta = 0^\circ, 3^\circ, 5^\circ\) and 7° is shown in Fig. 3(a)–(d), respectively. The cross-sectional mode intensity profile from Silvaco® Atlas simulation at 1550 nm wavelength is shown in the figure inset with the PN junction outlined. Atlas solves the 2D vector Helmholtz equation to determine the effective refractive index and effective absorption of each mode \[26\]. The difference in the modal distribution across the waveguide with \(\theta\) is negligible. However, the carrier distribution across the rib waveguide changes as \(\theta\) varies. The free-carrier concentration decreases with waveguide height at higher \(\theta\), which can also be seen from Fig. 2(e)–(h). In the waveguide rib, the P region becomes wider compared to the N region as \(\theta\) increases. This can be visualized from Fig. 1(b). Also, the enhanced boron diffusion along the tail of the implanted profile leads to a right shift of the PN junction near the bottom of the waveguide. This leads to a larger modal overlap with the P region compared to the N region as \(\theta\) increases.

The phase shift and absorption loss as a function of the reverse bias voltage are shown in Fig. 4(a) and 4(b), respectively. The positive voltage in Fig. 4(a)–(d) is the voltage applied to the cathode of the PN phase shifter, making it reverse biased. The phase shift increases with voltage as the depletion width widens, causing a larger change in the free carrier concentration across the PN junction. The phase shift increases with \(\theta\), and a larger change can be observed from 3° to 5° tilt from Fig. 4(a). This is due to the larger overlap of the mode field with the P depletion region. Holes lead to a larger change in the refractive index compared to electrons, as evident from (1a). The phase shift at 5 V reverse bias for 7° tilted wafer is \(\sim 67^\circ\)mm compared to \(\sim 42^\circ\)mm phase shift for 0° tilt, showing an improvement of 1.6×. The absorption loss shown in Fig. 4(b) decreases with an increase in the reverse bias voltage as the free carriers concentration decreases with a widening depletion region. The absorption depends on the modal overlap with the free carriers, and the carrier distribution in the waveguide rib determines the effective loss. The absorption loss is highest and lowest for \(\theta = 0^\circ\) and \(\theta = 5^\circ\), respectively. The slope in the absorption loss for different values of \(\theta\) is
similar to the corresponding slope of the phase shift curves. The $5^\circ$ and $7^\circ$ tilts have a higher slope for both phase shift and absorption loss compared to $0^\circ$ and $3^\circ$ tilts. The depletion region becomes longer at higher tilts as the PN junction becomes two-dimensional, as can be observed from Fig. 3(a)-(d). The absorption loss at $-5$ V of the $5^\circ$ tilted phase shifter is $\sim 1.64$ dB/mm compared to $\sim 2.02$ dB/mm of the $0^\circ$ tilted phase shifter, showing an improvement by a factor of 1.23. The square root dependency of the depletion width on the voltage leads to the non-linear phase-voltage and absorption-voltage curves.

For light extinction in an MZM, the relative phase difference between the two arms should be an odd multiple of $180^\circ$ or $\pi$ radians. The length of the phase shifter required to attain $\pi$ phase shift is denoted by $L_\pi$ and is calculated to be $4.24$ mm, $4.16$ mm, $2.92$ mm, and $2.68$ mm for $\theta = 0^\circ$, $3^\circ$, $5^\circ$, and $7^\circ$, respectively at $-5$ V operation. The modulation efficiency is the product of the voltage and length for $\pi$ shift and is $2.12$ V.cm, $2.08$ V.cm, $1.46$ V.cm, and $1.34$ V.cm for $\theta = 0^\circ$, $3^\circ$, $5^\circ$, and $7^\circ$ at $|V| = 5$ V. The phase shifter created with $\theta = 7^\circ$ has the best modulation efficiency, while that with $\theta = 0^\circ$ the poorest. Another figure of merit taking both phase shift and absorption loss into effect is the $\alpha V L_\pi$ product which gives the total loss ($\alpha L_\pi$) at the voltage required for light extinction. For $\theta = 0^\circ$, $3^\circ$, $5^\circ$, and $7^\circ$, $\alpha V L_\pi$ is $42.88$ V-dB, $38.03$ V-dB, $23.95$ V-dB, and $24.32$ V-dB, respectively. Although $\theta = 7^\circ$ shows the best modulation efficiency, $\theta = 5^\circ$ has better overall phase shifter performance.

The phase shifter resistance and capacitance determine the $RC$ modulation bandwidth when the MZM is driven as a lumped element. The small-signal analysis is done to determine the phase shifter admittance matrix, from which the frequency normalized impedance is calculated. The phase

FIGURE 3. Surface plot of the carrier distribution across the waveguide rib for (a) $0^\circ$ tilt, (b) $3^\circ$ tilt, (c) $5^\circ$ tilt, and (d) $7^\circ$ tilt. The mode profile is shown in the inset denoting the PN junction.

FIGURE 4. Phase shifter metrics as a function of the reverse bias voltage for different wafer tilt angles: (a) phase shift per unit length, (b) absorption loss per unit length, (c) capacitance per unit length, and (d) resistance.
shifter capacitance \((C_{pn})\) and resistance \((R_{pn})\) at different reverse bias voltages are shown in Fig. 4(c) and 4(d), respectively. \(C_{pn}\) and \(R_{pn}\) have units of \(\text{pF/cm}\) and \(\Omega\cdot\text{cm}\) respectively. The large depletion width at higher reverse voltages leads to lower capacitance. The different carrier distribution across the waveguide for different \(\theta\) leads to different capacitance and resistance curves. \(C_{pn}\) reduces and \(R_{pn}\) increases as \(\theta\) becomes large. In addition to the 1D diode capacitance, the total capacitance has multiple components due to the fringing electric field and widened depletion near the silicon–oxide interfaces [27]. The 1D diode capacitance per unit length depends on the depletion width and the length over which the depletion occurs. With large \(\theta\), the depletion width narrows along the top and widens along the bottom of the waveguide due to the high and low carrier concentration at the top and bottom, respectively. The phase shifter capacitances at \(-5\) V for \(\theta = 0^\circ\), \(3^\circ\), \(5^\circ\), and \(7^\circ\) tilts are 903 fF, 800 fF, 276 fF, and 310 fF, respectively. The resistivity depends on the doping concentration and the carrier mobility. As \(\theta\) increases, the P rib width increases, which leads to larger resistance as the hole mobility is lower than the electron mobility. Also, the slab resistance has a larger contribution to the overall phase shifter resistance since the slab height is much lower than the slab width. At larger \(\theta\), the slab resistance increases due to a reduction in the carrier concentration. The resistance is much larger for \(\theta = 7^\circ\) compared to \(\theta = 0^\circ\), \(3^\circ\), and \(5^\circ\). This can be attributed to multiple reasons – the P region is much larger than the N region in the waveguide rib, and the carrier concentration is lower in the slab region.

The equivalent electrical circuit for lumped analysis is shown in Fig. 5 with a source resistance \((R_s)\) and termination resistance \((R_t)\) of 50 \(\Omega\) each [28]. The 3 dB \(RC\) bandwidth \((f_3\ dB)\) for the lumped element is calculated as

\[
f_3\ dB = \frac{1}{2\pi R_{eq} C_{pn} L_\pi}
\]

where \(R_{eq}\) is the equivalent resistance seen from the right side of Fig. 5. Using \(R_{pn}\) and \(C_{pn}\) to determine \(f_3\ dB\) results in a much larger value of the intrinsic \(RC\) bandwidth and is independent of the phase shifter length. However, the source resistance of the electrical driver and the on-chip termination resistance results in a length dependence of \(f_3\ dB\), whereby \(R_{eq}\) is given as

\[
R_{eq} = \frac{R_s R_t L_\pi + (R_s + R_t) R_{pn}}{(R_s + R_t) L_\pi}
\]

The 3 dB \(RC\) bandwidth at \(-5\) V for the circuit of Fig. 5 is 6.94 GHz, 7.62 GHz, 21.78 GHz, and 17.68 GHz for \(\theta = 0^\circ\), \(3^\circ\), \(5^\circ\), and \(7^\circ\). The 3 dB lumped element bandwidth is highest for \(\theta = 5^\circ\) and lowest for \(\theta = 0^\circ\) showing an increase of more than 3×. The phase shifter device simulation shows that among the wafer tilt angles taken, the \(5^\circ\) tilt shows the best performance in terms of the \(\alpha V_{\pi}\) product and 3 dB \(RC\) bandwidth. Varying the tilt angle during dopant implantation can be used to tailor the carrier distribution in order to enhance the phase shifter performance.

**V. TRAVELING-WAVE MZM CHARACTERISTICS**

On-off keying modulation is used with a dual-arm push-pull operation to drive the modulator. Each PN phase shifter arm has a length of 4.24 mm, 4.16 mm, 2.92 mm, and 2.68 mm for \(\theta = 0^\circ\), \(3^\circ\), \(5^\circ\), and \(7^\circ\) with a \(V_{\pi} = -5\) V. The phase shifters are biased at \(-2.5\) V, and a \(2.5\) V pp radio-frequency (RF) signal is applied to both arms to obtain \(\pi\) phase shift. The limitation in the modulation bandwidth when driven as a lumped element is overcome by using a traveling-wave electrode (TWE) structure. The TWE configuration is shown in Fig. 6. The TWE is treated as a transmission line driven as a lumped element.

The transmission line impedance \((Z_{tl})\) and admittance \((Y_{tl})\) can be calculated as

\[
Z_{tl} = R_{tl} + j\omega L_{tl}
\]

\[
Y_{tl} = G_{tl} + j\omega C_{tl}
\]

where \(\omega\) is the microwave angular frequency, and \(R_{tl}, L_{tl}, G_{tl},\) and \(C_{tl}\) are the transmission line resistance per unit length, inductance per unit length, conductance per unit length, and capacitance per unit length, respectively. \(R_{tl}\) and \(L_{tl}\) is same for all values of \(\theta\), whereas \(G_{tl}\) and \(C_{tl}\) varies with \(\theta\) due to
different $R_{pm}$ and $C_{pm}$. The transmission line admittance,

$$Y_{tl} = f \left( \frac{1}{R_{pm} - \frac{C_{pm}}{\omega}} \right)$$

(7)

where $f(X)$ denotes function of $X$. With $G_{tl} = \text{Re}(Y_{tl})$ and $C_{tl} = \text{Im}(Y_{tl})/\omega$,

$$G_{tl} = f \left( \frac{\omega^2 R_{pm} C_{pm}^2}{\omega^2 R_{pm} C_{pm}^2 + 1} \right)$$

(8a)

$$C_{tl} = f \left( \frac{C_{pm}}{1 + \frac{C_{pm} \omega^2}{\omega^2 R_{pm} C_{pm}^2 + 1}} \right)$$

(8b)

For all $\theta$, $\omega^2 R_{pm} C_{pm}^2 < 1$. As $\omega$ increases, $G_{tl}$ increases and $C_{tl}$ decreases. The characteristic impedance ($Z_0$) and propagation constant ($\gamma$) of the transmission line can be calculated as [33]

$$Z_0 = \sqrt{\frac{Z_{tl}}{Y_{tl}}} = \sqrt{\frac{G_{tl} + j\omega L_{tl}}{G_{tl} + j\omega C_{tl}}}$$

(9a)

$$\gamma = \sqrt{Z_{tl} Y_{tl}} = \sqrt{(R_{tl} + j\omega L_{tl})(G_{tl} + j\omega C_{tl})}$$

(9b)

$Z_0$ should ideally be equal to $R_s$ and $R_t$ so that back reflection does not occur. The microwave signal attenuation ($\alpha_{TWE}$) as it travels through the electrode can be calculated from $\gamma$ as [33]

$$\alpha_{TWE} = 20 \log e^{\text{Re}(\gamma)L_{tn}}$$

(10)

$Z_0$ and $\alpha_{TWE}$ for different tilt angles are shown in Fig. 7(a) and 7(b), respectively. Since $R_{tl}$ and $L_{tl}$ are same for all $\theta$, $Z_0$ and $\alpha_{TWE}$ is determined by $G_{tl}$ and $C_{tl}$. In all the cases, $\omega C_{tl} = G_{tl}$, and $Z_0$ follows $C_{tl}$. The power dissipation in the TWE follows $G_{tl}$. For the $5^\circ$ tilt, the impedance matching is better as well as the TWE attenuation is low. The worst-case occurs for $3^\circ$ tilt with $> 19$ dB signal loss at $45$ GHz compared to $\sim 6$ dB loss in case of $5^\circ$ tilt.

The electro-electro (EE) S-parameters are used to evaluate the TWE performance. EE $S_{11}$ gives a measure of the back reflection, and EE $S_{21}$, the measure of the signal transmission loss. The EE S-parameters are calculated as [33]

$$S_{11} = \frac{\Gamma (1 - e^{-2\gamma L})}{1 - \Gamma e^{-2\gamma L}}$$

(11a)

$$S_{21} = \frac{(1 - \Gamma^2) e^{-\gamma L}}{1 - \Gamma e^{-\gamma L}}$$

(11b)

where the voltage reflection coefficient,

$$\Gamma = \frac{Z_0 - R_s}{Z_0 + R_s}$$

(12)

when $R_s = R_t$.

The EE S-parameters of the designed TWE for different values of $\theta$ are shown in Fig. 7(c) and follows the trend of Fig. 7(a) and 7(b). The lowest back reflection (EE $S_{11}$) occurs for $5^\circ$ tilt and is $\sim 16$ dB over $45$ GHz range. The highest back reflection is $-11.1$ dB for $0^\circ$ tilt at $\sim 3.8$ GHz. Another important TWE metric is the microwave index which should be matched to the optical group index. This indicates that both the high-frequency microwave voltage signal and the optical mode travels at the same group velocity. In the absence of velocity mismatch, the $3$ dB electro-optic (EO) bandwidth can be determined from the $6.4$ dB EE $S_{21}$ point. It can be observed from Fig. 7(c) that the $6.4$ dB EE bandwidth is largest for $\theta = 5^\circ$, which is $> 45$ GHz. The lowest bandwidth is for $3^\circ$ tilt at $\sim 16$ GHz. Velocity mismatch between the microwave and optical group index leads to a $3$ dB EO bandwidth different from the $6.4$ dB EE bandwidth and is shown in Fig. 7(d). The $3$ dB EO bandwidth is highest for $5^\circ$ tilt ($\sim 41$ GHz) and lowest for $3^\circ$ tilt ($\sim 22$ GHz), showing an improvement of $19$ GHz. Compared with $0^\circ$ tilt, the $6.4$ dB EE bandwidth and the $3$ dB EO bandwidth for $5^\circ$ tilt are $2.3 \times$ and $1.37 \times$ higher, respectively.

The block diagram representation of the system-level simulation setup is shown in Fig. 8. A $10$ mW continuous-wave (CW) laser with $10$ kHz linewidth operating at $1550$ nm wavelength is used as the light source. A single-mode fiber (SMF) with $0.2$ dB/km attenuation, $16.75$ ps/nm/km dispersion, $0.075$ ps/nm$^{-2}$ km$^{-1}$ dispersion slope, $0.2$ ps/km differential group delay, and $80$ $\mu$m$^2$ effective area is connected between the modulator and receiver. The receiver is a photodiode (PD) with a responsivity of $0.7$ A/W, $50$ nA dark current, thermal power density of $10^{-22}$ W/Hz, Gaussian shot noise distribution, and $30$ GHz modulation bandwidth. A pseudo-random binary bit stream of order 13 is generated by a bit-error-rate (BER) test set, whose outputs are mapped to the driving voltage levels by an NRZ generator. S-parameter filters are used to include TWE data [34]. A clock recovery block is used at the output of the PD with a reference signal from the NRZ generator to compensate for the time delay in the received.
signal. The data recovery block maps the electrical signal amplitude to a binary stream that is fed back to the BER test set. The eye viewer is used to generate the eye diagram. Multiple visualizers not shown in the picture are used to see electrical and optical time-varying signals and power levels. Generic data files containing the phase and absorption loss data at different voltages are imported in the MZM model. The system-level simulation is done using OptiSystem v17.1. With –2.5 V DC bias across the phase shifters in each MZM arm, a push-pull operation is used where one arm undergoes +2.5 V and the other arm –2.5 V. The maximum voltage difference is 5 V leading to a phase shift of π.

The SMF length is varied from 1 km to 5 km, and the effect of θ on the BER and the extinction ratio (ER) is shown in Fig. 9(a) and 9(b), respectively at 40 Gbps transmission. The BER is a measure of the number of error bits received relative to the total bits transmitted. BER ranges from 0 to 1, 0 being the best and 1 being the worst. The fiber dispersion leads to broadening of the data pulse, as a result of which the BER increases with fiber length. It can be seen from Fig. 9(a) that best performance is obtained for θ = 5°. The 3° tilt represents the worst case among the four samples. For error-free operation (BER = 10^-12), the transmission distance at 40 Gbps for θ = 0°, 3°, 5°, and 7° are < 1 km, ~ 0 km, ~ 3.7 km, and ~ 2.5 km, respectively. The ER represents the ratio of light intensities for representing bit ‘1’ and ‘0’. The maximum DC ER is > 25 dB for all the four tilt angles. The change in the dynamic ER with fiber length for 40 Gbps transmission is shown in Fig. 9(b). High dynamic ER implies low BER and vice-versa. The ER curve follows the BER curve with 5° tilt having the highest ER and 3° the lowest for any fiber length. Similar to the BER, the difference in ER reduces among different samples with an increase in fiber length. The BER and ER curves for different θ follow the TWE bandwidth curves of Fig. 7(c) and 7(d). Since the bandwidth is large for θ = 5°, the BER is low and ER is large for the same data speed and fiber length compared to the other samples.

The BER as a function of the modulation speed is shown in Fig. 10 for 5 km SMF transmission. As the speed increases, the bit period decreases, due to which the effect of dispersion is more pronounced, leading to high BER and low ER. The BER increase as the speed is varied from 35 Gbps to 50 Gbps. For KP4-forward-error-correction threshold (BER = 2.2 × 10^-4), the speed for θ = 0°, 3°, 5°, and 7° is limited to 38.5 Gbps, 36.5 Gbps, 43.8 Gbps, and 41 Gbps, respectively. Again, the sample with θ = 5° can reach higher speeds for the same BER compared to others due to its large 3 dB bandwidth.

The BER and ER for different θ follow the TWE bandwidth curves of Fig. 7(c) and 7(d). Since the bandwidth is large for θ = 5°, the BER is low and ER is large for the same data speed and fiber length compared to the other samples.
observed for 5° tilt. The asymmetry of the eye is due to the non-linear phase-voltage relation in silicon phase shifters as +2.5 V push and −2.5 V pull in the two arms do not lead to the same amount of phase shift. The effect of fiber dispersion on the BER and ER of the four MZMs are simulated and shown in Fig. 12(a) and 12(b), respectively. The BER and ER response to the change in fiber dispersion is similar to the change in fiber length. At any BER, the 5° (3°) tilt MZM has the highest (lowest) dispersion tolerance. Also, the ER is largest for the 5° tilt within the simulated dispersion range.

The energy-per-bit ($E_b$) of a modulator represents the electrical energy required to send an optical bit and is given as [35]

$$E_b = \frac{V_{TWE}^2}{4Z_0 BR}$$

where $V_{TWE}$ is the RF voltage across the TWE, and $BR$ represents the bit rate. Considering a KP4-FEC threshold at the receiver for 5 km SMF transmission, the modulation speed is different for different tilt angles (Fig. 10). $Z_0$ at the modulation frequency for 0°, 3°, 5°, and 7° tilts are 34.08–0.74 i, 34.69+0.83 i, 44.23–1.02 i, and 41.20+3.22 i, respectively. The corresponding total power consumption is 91.7 mW, 90.1 mW, 70.7 mW, and 75.8 mW. $E_b$ for 0°, 3°, 5°, and 7° tilt angles are 2.38 pJ/bit, 2.47 pJ/bit, 1.61 pJ/bit, and 1.84 pJ/bit, respectively.

So far in the system-level simulation study, the phase shifters are biased at −2.5 V and the voltage applied across the MZM arms are +/-2.5 V for $|V_{\pi}| = 5 $V. Due to the non-linear phase-voltage relation of silicon PN phase shifters, −2.5 V bias doesn’t bias the MZM at quadrature. Also, for different samples, the same bias point results in different phase points keeping the $|V_{\pi}|$ same with different $L_{\pi}$. Also, 2.5 V push-pull drive results in different corresponding phase shifts in different samples. For comparison, the DC bias and the RF voltage are kept the same for all samples. The variation of BER with the RF drive voltage is shown in Fig. 13 for different tilt angles. The RF voltage across each TWE arm is varied from 1 V to 2.5 V for 3 km 40 Gbps SMF transmission. It can be observed from Fig. 13 that the sample...
TABLE 1. Comparison of phase shifter and MZM metrics between samples having different wafer tilts during dopant implantation ("blue" and "red" indicates best and worst values respectively).

| θ  | Δφ† (°/mm) | α† (dB/mm) | V/Lα† (V/cm) | αV/Lα† (V-dB) | f3 dB† (GHz) | EE S11† (dB) | 6.4 dB EE‡ (BW (GHz)) | 3 dB EO‡ (BW (GHz)) | BER⊥ | ER⊥ (dB) | E0⊥ (pJ/bit) |
|----|------------|------------|---------------|---------------|--------------|------------|-------------------|------------------|------|--------|----------|
| 0° | 42.45      | 2.02       | 2.12          | 42.88         | 6.94         | <-11.1     | 20.67             | 29.98            | 6.47×10⁻⁴ | 8.11   | 2.38   |
| 3° | 43.32      | 1.83       | 2.08          | 38.03         | 7.62         | <-11.3     | 15.97             | 22.22            | 3.83×10⁻³ | 8.02   | 2.47   |
| 5° | 61.60      | 1.64       | 1.46          | 23.95         | 21.78        | <-16.8     | 47.40             | 40.89            | 3.07×10⁻⁶ | 8.76   | 1.61   |
| 7° | 67.16      | 1.81       | 1.34          | 24.32         | 17.68        | <-14.9     | 24.88             | 28.98            | 1.36×10⁻⁴ | 8.48   | 1.84   |

† –5 V.
‡ 5 km SMF transmission at 40 Gbps with −2.5 V bias and 2.5 V drive voltage across each arm.
§ KP4-PEC threshold at 3 km SMF transmission with −2.5 V bias and 2.5 V drive voltage across each arm.

with 5° tilt has a much larger BER tolerance to the RF voltage amplitude compared to the other samples. The sample with 3° tilt exhibits the worst performance followed by 0° tilt. The BER improves as the RF voltage increases, as expected.

A comparison of the different phase shifter and modulator metrics for the four samples with different values of θ is given in Table 1. The best case is marked by ‘blue’ and the worst by ‘red.’ It can be seen that for the phase shifter performance, the 7° tilt shows better phase shift and modulation efficiency whereas, lower absorption and higher 3 dB RC bandwidth of a lumped phase shifter is obtained for the 5° tilt. In all the metrics, the 0° tilt showed the worst performance. The best TWE and MZM performance is obtained for the 5° tilt with the 3° tilt representing the worst-case, followed by the sample with 0° tilt. The sample with 5° tilted implantation shows overall better performance compared to the other samples.

VI. CONCLUSION

A silicon PN phase shifter is process simulated, and the wafer tilt angles during dopant implantation are varied from 0° to 7°. The corresponding effect of the wafer tilts on the lattice damage, dopant concentration, and formation of dopant–defect clusters are investigated. The four samples with different wafer tilt angles are used in an MZM with traveling-wave architecture for on-off keying modulation. The TWE characteristics and high-speed characteristics for different samples are presented and discussed. The overall best performance is exhibited by the sample with 5° tilt with 1.45× higher phase shift and modulation efficiency, 1.23× lower absorption, and 3.14× higher 3 dB bandwidth for lumped MZM at −5 V bias compared to 0° tilt. For a 2.5 V push-pull operation at −2.5 V bias with a traveling-wave arm, the sample with 5° tilt has 2.29× (2.97×) higher EE bandwidth, 1.36× (1.84×) higher EO bandwidth, and 1.48× (1.53×) lower energy-per-bit compared to the sample with 0° (3°) tilt. A 5° tilt during implantation shows better performance compared to other samples with 0°, 3°, and 7° tilt and has larger dispersion and drive voltage tolerance. Adjusting the wafer tilt during implantation can be used to tailor the carrier distribution across the waveguide resulting in enhanced phase shifter and modulator performance in pure silicon modulators.

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