WSe₂/SnSe₂ vdW heterojunction Tunnel FET with subthermionic characteristic and MOSFET co-integrated on same WSe₂ flake

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Two-dimensional/two-dimensional (2D/2D) heterojunctions form one of the most versatile technological solutions for building tunneling field effect transistors because of the sharp and potentially clean interfaces resulting from van der Waals assembly. Several evidences of room temperature band-to-band tunneling (BTBT) have been recently reported, but only few tunneling devices have been proven to break the Boltzmann limit of the minimum subthreshold slope, 60 mV per decade at 300 K. Here, we report the fabrication and characterization of a vertical p-type Tunnel FET (TFET) co-integrated on the same flake with a p-type MOSFET in a WSe₂/SnSe₂ material system platform. Due to the selected beneficial band alignment and to a van der Waals device architecture having an excellent heterostructure 2D–2D interface, the reported tunneling devices have a sub-thermionic point swing, reaching a value of 35 mV per decade, while maintaining excellent ON/OFF current ratio in excess of 10⁵ at VDS = 500 mV. The TFET characteristics are directly compared with the ones of a WSe₂, MOSFET realized on the very same flake used in the heterojunction. The tunneling device clearly outperforms the 2D MOSFET in the subthreshold region, crossing its characteristic over several orders of magnitude of the output current and providing better digital and analog figures of merit.

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the junction obtained by density functional theory (DFT) calculations. We then discuss the possible BTBT mechanism matching our experimental findings. Finally, we provide a direct comparison of the heterojunction TFET and the built-in WSe$_2$ MOSFET in terms of both digital and analog figures of merit of the out best device. We show that the WSe$_2$/SnSe$_2$ TFET outperforms its WSe$_2$ counterpart over several orders of magnitude of the output current both for analog and digital applications.

RESULTS AND DISCUSSION
Heterojunction band diagram
The structure of the fabricated WSe$_2$/SnSe$_2$ heterojunction devices is shown in Fig. 1. In order to accurately model the band alignment of the heterostructure, VASP$^{29}$, a density functional theory tool, is employed. A supercell containing six layers of each material is constructed by applying a relative rotation of 30° and a small strain of 0.22 % to both layers, resulting in a hexagonal cell material is constructed by applying a relative rotation of 30° and a total energy difference smaller than 10$^{-3}$ eV. The resulting three-dimensional schematic view of the final heterojunction device is shown in Fig. 1a, which consists of a back gated WSe$_2$/SnSe$_2$ heterojunction with Pd Schottky contacts deposited on each side of the junction. The first fabrication step is the deposition of atomic layer deposition (ALD) of 50 nm layer of hafnium oxide (HfO$_2$) on a Si wafer. The bottom gate electrode is then defined by electron beam lithography (EBL) on a MMA/PMMA bilayer and lift-off of 50 nm of tungsten (W). The gate stack is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ flakes have been mechanically exfoliated directly on the patterned substrate starting from commercially available bulk samples. In order to form the junction, SnSe$_2$ flakes were first exfoliated on a poly(dimethylsiloxane) (PDMS) transparent substrate and then deterministically transferred on previously selected WSe$_2$ samples$^{32,33}$. The source and drain contacts were deposited by lift-off of a Cr/Pd stack (5/50 nm) after a second EBL deposition by atomic layer deposition (ALD) of 50 nm layer of HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$.

Figure 1d represents a qualitative band diagram of the WSe$_2$/SnSe$_2$ heterojunction obtained starting from reported results on similar heterostructures assembled with multilayer WSe$_2$ and thicker SnSe$_2$ flakes$^{13}$. As confirmed by our DFT calculations, at the equilibrium the band alignment is of type III, resulting in a non-zero energy overlap between SnSe$_2$ conduction band and WSe$_2$ valence band. By applying a positive drain bias to the WSe$_2$ contact, electrons can tunnel from SnSe$_2$ to WSe$_2$ providing a BTBT conduction path. A negative bottom gate voltage determines an upward shift of WSe$_2$ bands, resulting in an increase of the energy overlap and an enhanced tunneling current. Therefore, we expect our three terminal heterojunction devices to exhibit a tunneling current at positive drain to source voltage with negative bottom gate bias.

Device fabrication
The three-dimensional schematic view of the final heterojunction device is shown in Fig. 1a, which consists of a back gated WSe$_2$/SnSe$_2$ heterojunction with Pd Schottky contacts deposited on each side of the junction. The first fabrication step is the deposition by atomic layer deposition (ALD) of 50 nm layer of hafnium oxide (HfO$_2$) on a Si wafer. The bottom gate electrode is then defined by electron beam lithography (EBL) on a MMA/PMMA bilayer and lift-off of 50 nm of tungsten (W). The gate stack is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ flakes have been mechanically exfoliated directly on the patterned substrate starting from commercially available bulk samples. In order to form the junction, SnSe$_2$ flakes were first exfoliated on a poly(dimethylsiloxane) (PDMS) transparent substrate and then deterministically transferred on previously selected WSe$_2$ samples$^{32,33}$. The source and drain contacts were deposited by lift-off of a Cr/Pd stack (5/50 nm) after a second EBL deposition by atomic layer deposition (ALD) of 50 nm layer of HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$. WSe$_2$ is then completed by a second ALD deposition of 10-nm-thick HfO$_2$.

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\text{Fig. 1 Structure and expected band alignment of the fabricated WSe}_2/\text{SnSe}_2\text{ heterojunction. a Three-dimensional schematic of the final device structure, consisting in a back g} \]


Electrical characterization

All the electrical measurements have been performed at room temperature and ambient conditions. The WSe2 contact is always biased as the drain of the heterojunction device.

As a first step, we characterized the electrical properties of individual SnSe2 and WSe2 flakes. The double-sweep transfer characteristic, drain current versus the gate voltage, \( I_D-V_G \), and the output characteristic, drain current versus the drain voltage, \( I_D-V_D \), of a representative SnSe2 FET is reported in Supplementary Fig. 1. As expected, given the degenerate n doping typical of this 2D material, the gate bias has a very limited capability of modulating the conduction in the channel\(^{27,34}\), that cannot be depleted of electrons for the investigated range of voltages resulting in a ON/OFF current ratio larger than 50 nm. The atomic force microscopy (AFM) profile of a typical WSe2 flake (taken measuring along the red cutline in Fig. 2b) is reported in Fig. 2c.

Fig. 2 Optical and scanning electron microscopy imaging. a Optical image of two fabricated WSe2/SnSe2 devices. It is possible to distinguish the two flakes for each junction, the overlap region and the Pd contacts to the two sides of the heterostructure. For flakes sufficiently large it is possible to deposit four contacts, so to be able to characterize both the internal WSe2 FET and the heterojunction device. b SEM image of a final device with highlighted cutline for thickness estimation. c AFM profile of the WSe2 flake taken along the red cutline shown in the SEM image. The presented devices have been fabricated with 10-nm-thick WSe2 flakes.

The transfer characteristic, drain current versus gate voltage, \( I_D-V_G \), of a representative WSe2 FET measured at different drain biases is reported in Fig. 3a. The device, whose channel is 2 µm wide, exhibits p-type polarity with ON/OFF current ratio larger than 10\(^5\). The hole mobility can be extracted applying the Y function method (see Supplementary Fig. 2)\(^ {35,36} \). At \( V_D = 500 \text{ mV} \), the carrier mobility is 1.8 cm\(^2\) V\(^{-1}\) s\(^{-1}\), comparable to reported results on similar devices\(^ {23} \). The inset in Fig. 3a shows the transconductance of the device, \( g_m \), which saturates upon reaching the maximum value. The ratio of the gate transconductance and the drain current gives the transconductance efficiency, plotted in Fig. 3b for three values of the drain voltage. \( g_m/I_D \) is a fundamental parameter to evaluate the potential of a technology platform for analog applications\(^ {37} \). Indeed, high transconductance efficiency values are fundamental for the design of high performance, low power consumption differential couples. In a MOSFET, the maximum value of the transconductance efficiency is physically constrained to be lower than 40 V\(^{-1}\) and the maximum value can be achieved operating the device in its weak inversion regime\(^ {18} \). As shown in Fig. 3b, our WSe2 pMOSFET achieves a \( g_m/I_D \) value comprised between 25 and 30 V\(^{-1}\), comparable to advanced bulk Si FET\(^ {39-43} \).

The potential of a technology to realize energy efficient, low voltage digital switches can be evaluated considering its subthreshold slope. A steep turn-on characteristic is fundamental to scale down the power supply, or to achieve higher current at lower gate voltage and, therefore, faster switching for the same gate bias. Figure 3c shows the subthreshold slope as a function of the output current for the three investigated drain biases. The minimum point value is 80 mV per decade and point slopes around 100 mV per decade are maintained also at \( V_D = 500 \text{ mV} \). Such results are better or comparable with the best reported back gated WSe2 FETs\(^ {23,24,44-46} \). Figure 3d–f collects the corresponding results obtained measuring the WSe2/SnSe2 heterojunction TFET based on the very same WSe2 flake characterized as MOSFET. Comparing the transfer characteristics of the two devices (Fig. 3a, d) under the same drain bias, it is clear that the heterojunction TFET exhibits lower \( I_{ON} \), lower \( I_{OFF} \), more negative threshold voltage and steeper turn-on characteristic than its built-in WSe2 MOSFET. The OFF state current is limited by the gate leakage, while the relatively large tunneling resistance at the heterojunction interface likely fixes the current level in the ON state. The inset of Fig. 3d shows the transconductance of the heterojunction FET, from which it is possible to derive the transconductance efficiency curve, represented in Fig. 3e as a function of the drain current. The WSe2/SnSe2 TFET exceeds, at room temperature, the \((kT/q)^{-1} \approx 40 \text{ V}^{-1}\) fundamental limit of MOSFET \(g_{m}/I_D\) analog figure of merit, for all the considered drain biases. Similarly, the subthreshold slope plotted as a function of the drain current shown in Fig. 3f exhibits point swing below the 60 mV per decade Boltzmann limit for all the three drain biases. In order to evaluate the impact of the gate leakage current on the estimation of the subthreshold slope, in particular for current levels close to the leakage floor as in our case, it is important to consider both drain and source transfer characteristics, and their relative subthreshold swings. Supplementary Fig. 3 reports the \( I_D-V_G \) and \( I_S-V_G \) characteristics, demonstrating that the numerical derivatives of both source and drain measured currents versus the gate voltage result in subthermionic values of the turn-on subthreshold slopes at room temperature.
in Supplementary Fig. 4. As discussed in our IEDM paper, the output characteristic of this WSe₂/SnSe₂ TFET shows a clear, gate decade. As expected, the WSe₂ FET maintains a larger minimum point subthreshold slope for the TFET is 35 mV per almost three orders of magnitude of the output current. The at low current levels and indeed outperforming the MOSFET over the BTBT conduction path schematically described in Fig. 1d. The WSe₂/SnSe₂ heterojunction device shows a more positive threshold voltage and steeper turn-on characteristic with respect to the WSe₂ FET, while the turn-on slope is improved. Inset: transconductance as a function of the gate bias. e) Heterojunction FET transconductance efficiency as a function of the device output current. For all the investigated drain to source biases, the peak transconductance efficiency exceeds the fundamental 40 V⁻¹ limit characterizing MOSFET devices. f) Subthreshold slope vs drain current for the TFET, showing room temperature subthermionic point swing for all the applied drain biases.

The transfer characteristics of a second couple of devices, again a WSe₂ MOSFET and its same flake WSe₂/SnSe₂ TFET are reported in Supplementary Fig. 4. As discussed in our IEDM paper, the output characteristic of this WSe₂/SnSe₂ TFET shows a clear, gate tunable NDR region, that together with the measured subthermionic subthreshold slopes contributes to demonstrate the onset of the BTBT conduction path schematically described in Fig. 1d.

In order to discuss in more details the differences between the WSe₂ and the heterojunction FET, it is useful to directly compare the relative transfer characteristics. Figure 4a collects the curves of our reference TFET and its built-in MOSFET, both measured applying VDS = 500 mV. The TFET threshold voltage has been shifted so to match the MOSFET one and provide an easier correlation. The WSe₂/SnSe₂ heterojunction device has both a lower IOFF current and steeper turn-on characteristic with respect to the WSe₂ FET (see the inset in Fig. 4a), crossing its characteristic at low current levels and indeed outperforming the MOSFET over almost three orders of magnitude of the output current. The WSe₂/SnSe₂ heterojunction TFET not only overcomes the 40 V⁻¹ analog efficiency limit at low current levels, but it consistently outperforms the WSe₂ FET, whose performance is comparable to long channel Si bulk MOSFETs over the entire subthreshold region. Conversely, for large drain current the MOSFET transconductance is larger, reflecting the higher ION granted by the thermionic injection mechanism.

The reported results demonstrate the best reported experimental minimum subthreshold slope for 2D/2D heterojunction devices, while maintaining an ON/OFF current ratio larger than five orders of magnitude and co-integrating on the same flake both the heterojunction tunneling device and the WSe₂ MOSFET.

The co-integration of MOSFET and TFET on the same flake paves the way for the realization of hybrid devices with dual transport mechanism that combine the advantages of each of these devices while not requiring any additional lithography and production steps. The possibility of co-integrating TFET and MOSFET in the same material system and technology platform has been explored thoroughly for silicon and III–V based devices, but not yet in a true 2D/2D material system. Here, in Fig. 5a, we propose a new steep slope hybrid device, named dual transport (DT) FET consisting in the parallel connection of a WSe₂/SnSe₂ heterojunction TFET and its built-in WSe₂ MOSFET. Such device could inherit

Fig. 3 Electrical characterization at room temperature (T = 300 K) of a representative WSe₂ FET and the WSe₂/SnSe₂ heterojunction device fabricated on the very same flake. a) Transfer characteristic in semilogarithmic scale of the WSe₂ FET for increasing values of the drain bias. The ON/OFF current ratio is larger than 10⁶ and the minimum subthreshold slope ranges from 80 to 110 mV per decade. b) WSe₂ transconductance efficiency as a function of the device output current. c) Subthreshold slope vs drain current for the MOSFET under different applied drain to source bias. The width of the WSe₂ FET is 2 µm. d) Transfer characteristic in semilogarithmic scale of the WSe₂/SnSe₂ Tunnel FET for increasing values of the drain bias. The threshold voltage is shifted to more negative values with respect to the WSe₂ FET, while the turn-on slope is improved. Inset: transconductance as a function of the gate bias. e) Heterojunction FET transconductance efficiency as a function of the device output current. For all the investigated drain to source biases, the peak transconductance efficiency exceeds the fundamental 40 V⁻¹ limit characterizing MOSFET devices. f) Subthreshold slope vs drain current for the TFET, showing room temperature subthermionic point swing for all the applied drain biases.
the best figures of merit of a Tunnel FET and a MOSFET, a subthermionic subthreshold slope (dictated by a BTBT current) and a high on current (dictated by a thermionic current), respectively. The qualitative transfer characteristic of such a device is shown in red in Fig. 5a. In order to achieve such unique behavior, it is required that the TFET and MOSFET threshold voltages fulfill a particular condition, with the turn-on of the TFET before the MOSFET. In absolute values, $|V_{\text{Th,TFET}}| < |V_{\text{Th,MOSFET}}|$ for p-type devices. Here, for simplicity, we consider the TFET threshold voltage extracted as the gate bias corresponding to the 60 mV per decade slope in the transfer characteristics, called the $I_{60}$ drain current. More precise engineering of this design condition, for the optimization of the DT FET figures of merit by taking the best of its composing device parts, would need the development of a physics-based compact model for such hybrid device, which was not the purpose of this work. For p-type devices, operated at negative gate voltages, enforcing this condition would grant that the p-type TFET controls the turn-on of the DT FET, while the pMOSFET intervenes for more negative back gate voltages providing the higher ON current. For our fabricated devices, as discussed both in Fig. 3 and Supplementary Fig. 4, such condition is not fulfilled correctly, preventing us to match the condition for making an ideal dual-transport experimental device. Supplementary Fig. 5 shows the measured characteristic of the first experimental implementation of our DT FET based on the WSe$_2$/SnSe$_2$ TFET and WSe$_2$ FET devices whose characteristic are collected in Supplementary Fig. 4. Because of the non-ideal relationship between the devices threshold voltages, the combined transfer characteristic follows more dominantly the MOSFET rather than the TFET at the turn-on.

In order to provide an estimation of the performance of such a device in an optimal design, we used the measured experimental transfer characteristic presented in Fig. 3 and we artificially shifted the TFET threshold voltage, as potentially possible by the use of metal contacts with different work functions. The resulting transfer curve is shown in Fig. 5b. As expected, provided that $|V_{\text{Th,TFET}}| < |V_{\text{Th,MOSFET}}|$, the DT FET turns on following the heterojunction tunneling curve and inherits both a steep transition and the higher thermionic $I_{\text{ON}}$ current of the MOSFET. Consequently, the proposed device exhibits better analog and digital figures of merit of the constituting devices. Figure 5c collects the transconductance efficiency of the three FETs: while not achieving the peak value obtained by the TFET, the DT FET exhibits a transconductance efficiency larger than the MOSFET one for the entire range of the output current, outperforming also the TFET at large drain currents. The evolution of the subthreshold slope follows a similar trend, as reported in Fig. 5d. Even if the DT FET proposed device does not reach a point subthreshold slope as small as the heterojunction TFET, it exhibits a much steeper turn on than the MOSFET and it outperforms the TFET at large current values.

The practical engineering of the WSe$_2$ MOSFET and WSe$_2$/SnSe$_2$ threshold voltages can be obtained experimentally either by (i) changing the contact metal used for one of the two devices or (ii) depositing a top dielectric and top gate contact on the WSe$_2$ channel\cite{24}. This second solution, while more challenging and cumbersome from a fabrication viewpoint, it would enable the
possibility of programming on the fly the threshold voltage of the WSe$_2$ FET so to obtain the desired condition.

**DISCUSSION**

In this work, we reported co-integrated subthermionic 2D/2D WSe$_2$/SnSe$_2$ tunnel FET and WSe$_2$ MOSFET realized on the very same flake. The device is fabricated by deterministic assembly of the van der Waals heterojunction on top of a tungsten/HfO$_2$ bottom gate stack. DFT calculations confirm that this heterojunction presents an optimal broken gap band alignment, resulting in room temperature subthermionic subthreshold slope and sizeable, gate tunable negative differential resistance observable in the output characteristic. A record low point subthreshold slope of 35 mV per decade at $V_{DS} = 500$ mV has been demonstrated, while $I_{OFF} < 0.1$ pA $\mu$m$^{-2}$ and an excellent ON/OFF current ratio exceeding $10^5$. The fabricated pTFET clearly outperforms the built-in WSe$_2$ MOSFET, crossing its characteristic over several orders of magnitude of the drain current and providing better digital and analog performance in the subthreshold region. The demonstrated heterojunction device provides a new insight in the potential of 2D/2D systems for the realization of high performance steep-slope devices. Moreover, the possibility of co-integrating on the same flake both MOSFET and TFET with no increase in the process flow complexity paves the way to new hybrid device, such as the proposed DT FET, and circuit topologies able to harvest the steep TFET turn-on characteristic granted by the band to band tunneling conduction mechanism and the high MOSFET thermionic ON current.

**METHODS**

Fabrication of WSe$_2$/SnSe$_2$ bottom gated heterojunction devices

The starting substrate is a p doped silicon wafer. An insulation 50-nm-thick layer of HfO$_2$ is deposited by atomic layer deposition (ALD). The bottom gate is obtained by the lift-off in acetone of 50 nm of sputtered tungsten after an electron beam lithography (EBL) step performed on a MMA/PMMA bilayer. The structure of the bottom gate is then completed by ALD of 10 nm of HfO$_2$. The bulk WSe$_2$ and SnSe$_2$ crystals were purchased respectively from hq graphene and 2D semiconductors. WSe$_2$ flakes are directly exfoliated by scotch taping on the final substrate, and flakes with desired geometry, thickness and position are identified by optical microscopy. SnSe$_2$ is first exfoliated on a PDMS stamp that is then used.
in combination with a micromanipulator and an optical microscope to deterministically transfer SnSe2 flakes on the previously selected WSe2 flakes. The contacts to the heterojunction devices are obtained by evaporation and lift-off of a Cr/Pd stack (5/50 nm) after a second EBL step on MMA/PDMA bilayer resist. A third EBL step is performed to pattern a PMMA mask for the low power ion beam etching of the gate dielectric in selected areas in order to gain electrical access to the bottom gate contact.

Electrical measurements

All the reported electrical measurements have been performed at room temperature and ambient conditions using conventional semiconductor parameter analyzers and electrical probes. The WSe2 contact is always biased as the drain of the heterojunction device.

Metrology

AFM in contact mode for accurate thickness estimation and SEM have been performed after the electrical characterization, so to avoid contamination of the devices.

DATA AVAILABILITY

The raw data used in this study are available upon reasonable request to the corresponding author.

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AUTHOR CONTRIBUTIONS
N.O. and A.M.I. developed the device principle and the fabrication process flow. N.O. and L.C. worked on device fabrication. J.B. and M.L. modeled and derived the heterojunction band diagram from first principle studies. M.C. performed AFM measurements. N.O. performed electrical measurements and the data analysis. N.O., J.B., L.C., M.L. and A.M.I. wrote the manuscript.

COMPETING INTERESTS
The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION
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