Scalable Contact-Capacitive MEMS Switches With High Capacitance Ratio for Millimeter-Wave Applications

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\textbf{ABSTRACT} This paper proposes a series of optimized scalable contact-capacitive radio frequency micro-electro-mechanical systems (RF MEMS) switches for millimeter wave applications. Due to the contact-capacitive topology, the ON-state and OFF-state of the switch can be designed separately to obtain smaller $C_{ON}$ and larger $C_{OFF}$, which results in high capacitance ratio ($C_r$). The $C_{ON}$ is defined by capacitance of the contacts, and it is optimized for low insertion loss ($IL_{ON}$). The $C_{OFF}$ is defined by the metal-insulator-metal (MIM) capacitor, and it is designed for working band and scalable performance. The measurements of the fabricated devices show acceptable agreements with design and simulation. The optimized switches perform well with $IL_{ON}$ better than 1.5dB and capacitive ratio about 124. The switches follow scaling rules from 20GHz to 110GHz. Linearity (IIP3) of the switches are tested to be higher than 60dBm, and calculated to be higher than 80dBm. Performances of the switch can be further improved and optimized in the future study.

\textbf{INDEX TERMS} RF MEMS, contact-capacitive switch, scalable, high capacitance ratio, high linearity.

I. INTRODUCTION

Millimeter wave (mmW) is attracting more and more attentions because of its wide application prospect in radio frequency (RF) systems, including future mobile communication (5G, 6G and Beyond), automotive radar and satellite communication [1], [2]. RF devices with excellent performances are necessary to achieve satisfactory system. Owing to their low insertion loss (IL), high isolation (Iso), high linearity, wide band, the RF micro-electro-mechanical systems (MEMS) switches, especially capacitive RF MEMS switches, are regarded as promising candidate technology to meet the mmW requirements [3], [4].

For the extremely broad band in mmW, it is hard to cover the whole bands by a single device. Scalable design is a commonly used method to cover different frequency bands [5]. In this study, a scalable metal-insulator-metal (MIM) capacitor design is proposed for different bands switch from 20GHz to 110GHz. Meanwhile, because of the more and more crowded frequency bands, the intermodulation distortions (IMD) in RF systems become very complex. In this case, devices with high linearity are urgently needed. On the basis of the previous studies [6]–[8], we propose an optimized small $C_{ON}$ design to obtain switches with excellent linearity performance.

Generally, it is the capacitance at ON-state ($C_{ON}$) and capacitance at OFF-state ($C_{OFF}$) that affect the RF performance. The capacitance ratio ($C_r = C_{OFF}/C_{ON}$) is an important factor to characterize the performance of the switch. Efforts have been made in the past to realize high capacitance ratio, including high-k materials [9], [10], larger gap, and curly beams [11], [12]. But, the introduction of these methods above will bring in some disadvantages, such as complex fabrication process, complex parasitical parameters, and so on.

Series connection of different structures is another method to improve the performances of the switches. Combination of a shunt capacitive switch and a metal-air-metal (MAM) capacitor is introduced in [13] and [14], which aims at high-Q design. Contact-capacitive structures are introduced in [15]–[17], which are composed of contact type RF-MEMS.
In this paper, we propose a series of optimized scalable RF MEMS switches. The contact-capacitive structures are used to realize separate design of ON-state and OFF-state, in which the contacts are located at sides of the MIM capacitor. The $C_{ON}$ is defined by capacitance of the contacts, while the $C_{OFF}$ is defined by the MIM capacitor. The switches are optimized carefully for RF performances. High $C_r$, scalable performance and low insertion loss are realized in mmW bands, from 20GHz to 110GHz. Electrical and mechanical design, modeling, optimization, analysis and simulation are conducted in Section II. And, the devices are fabricated using surface manufacturing process in Section III. Then, the electronic and mechanical performances of the switches are tested in Section IV. Finally, we conclude this paper with several further studies presented to improve the performances in Section V.

II. DESIGN AND MODELING OF THE SWITCHES

A. DESCRIPTION OF THE SWITCHES

The schematic views of the switch are illustrated in Fig. 1, with overview of the whole device and close-view of the cantilevers. The top view and cross-sectional view of the switch are shown in Fig. 2 with detailed parameters marked. The device consists of several parts: quartz substrate, coplanar waveguide transmission line (CPW TML), MIM capacitor, cantilevers, contacts, actuators and so on. Contacts and cantilevers are located at sides of the MIM capacitor, which is aimed at low $C_{ON}$, low insertion loss ($IL_{ON}$) and high linearity design. When the driving voltage is applied to the actuators, the cantilevers are actuated with the contacts contacted. Then the RF signal couples to the ground through the MIM capacitor and cantilevers, which is called OFF-state. When the driving voltage is removed, the cantilevers return back to the original position. Then RF signal passes through the device directly, which is called ON-state.

The equivalent circuit of the switches is shown in Fig. 3. The equivalent circuit consists of four parts: transmission line, MIM capacitor, contact and cantilever, just like the topology of the device. The switch between $C_c$ and $R_c$ defines the working states. These parameters influence the performances of the devices significantly, which should be designed carefully.
B. RF PERFORMANCE ANALYSIS

Because of the negligible influence of the series inductor \( L_s \), the insertion loss \( \text{IL}_{\text{ON}} \) and return loss \( \text{RL}_{\text{ON}} \) at ON-state are mainly defined by the \( C_{\text{ON}} \), as shown in (1) and (2). And, \( C_{\text{ON}} \) is mainly affected by \( C_c \). At ON state, \( C_{\text{ON}} = 1/(1/C_{\text{MIM}} + 1/C_c) \approx C_c \), since \( C_c \ll C_{\text{MIM}} \) for different values of \( I_{\text{MIM}} \). According to (1)(2) and the roughly equal \( C_{\text{ON}} \) for switches with different \( I_{\text{MIM}} \), \( \text{IL}_{\text{ON}} \) of the devices are almost same.

\[
\text{IL}_{\text{ON}} \approx \frac{2}{2 + j\omega C_{\text{ON}} Z_0} \tag{1}
\]

\[
\text{RL}_{\text{ON}} \approx -\frac{j\omega C_{\text{ON}} Z_0}{2 + j\omega C_{\text{ON}} Z_0} \tag{2}
\]

At OFF-state, the isolation \( (\text{ISO}_{\text{OFF}}) \) and return loss \( (\text{RL}_{\text{OFF}}) \) are determined by the CLR circuit in Fig. 3. There is an LC resonance in the equivalent circuit, which defines the working bands of the switch. The resonance frequency \( (f_0) \) of the switch can be calculated by (3).

\[
f_0 \approx \frac{1}{2\pi \sqrt{(L_{\text{MIM}} + L_{\text{canteilever}}) C_{\text{MIM}}}} \tag{3}
\]

The \( \text{ISO}_{\text{OFF}} \) and \( \text{RL}_{\text{OFF}} \) can be designed by (4) and (5), in which \( L_{\text{OFF}} = L_{\text{MIM}} + L_{\text{canteilever}} \), \( R_{\text{OFF}} = R_c + R_{\text{MIM}} + R_{\text{canteilever}} \). Generally, the \( \text{ISO}_{\text{OFF}} \) is better than \(-30\)dB at \( f_0 \), due to the small \( R_{\text{OFF}} \).

\[
\text{ISO}_{\text{OFF}} \approx \frac{2 \left( j\omega L_{\text{OFF}} + 1/j\omega C_{\text{MIM}} + R_{\text{OFF}} \right)}{2 \left( j\omega L_{\text{OFF}} + 1/j\omega C_{\text{MIM}} + R_{\text{OFF}} \right) + Z_0} \tag{4}
\]

\[
\text{RL}_{\text{OFF}} \approx \frac{2 \left( j\omega L_{\text{OFF}} + 1/j\omega C_{\text{MIM}} + R_{\text{OFF}} \right)}{2 \left( j\omega L_{\text{OFF}} + 1/j\omega C_{\text{MIM}} + R_{\text{OFF}} \right) + Z_0} \tag{5}
\]

When a two-tone signal passes through the switch at ON-state, the cantilevers will vibrate with the envelope. The \( C_{\text{ON}} \) is dependent on the vibration of the cantilevers, which results in changes of the \( \text{IL}_{\text{ON}} \). Then, the device shows out nonlinearity performance. Referring to the previous studies [6]–[8], the third-order input intercept point (IIP3) can be designed and calculated by (6), where \( k \) is the spring constant, \( g \) is the gap, \( \omega \) is the angular frequency in radians, \( Z_0 \) is the characteristic impedance.

\[
\text{IIP3} = \frac{4kg^2}{\omega^2 C_{\text{ON}}^2 Z_0^2} \tag{6}
\]

Equation (6) is based on the situation in which the envelope frequency \( (f_{\text{en}}) \) of the two-tone signal is smaller than mechanical resonance frequency \( (f_m) \). When \( f_{\text{en}} \) is higher than \( f_m \) \( (f_{\text{en}} > f_m) \), the intermodulation will decrease by 40dB per decade, and the IIP3 will increase by 20dB per decade. In this paper, the method of extremely small \( C_{\text{ON}} \) is used for high linearity switch design.

According to the analysis above, it is easy to design the device just as shown in Fig. 4. And, with the consideration of the RF system application, the design goals of IIP3 is set to be 80dBm, and the \( \text{IL}_{\text{ON}} \) is set to be \(-1\)dB, and the \( \text{ISO}_{\text{OFF}} \) is set to be \(-30\)dB. As the result, the \( C_{\text{ON}} \) needs to be less than 30fF to realize the \( \text{IL}_{\text{ON}} \) better than \(-1\)dB at 110GHz. Meanwhile, the \( C_{\text{ON}} \) needs to be less than 20fF to realize the IIP3 better than 80dBm when \( f_{\text{en}} \) is 100kHz. The \( R_c \) needs to be less than 0.8\( \Omega \) for \( \text{ISO}_{\text{OFF}} \) better than \(-30\)dB. With these performances above considered, the contact number per cantilever is set to 2, just as shown in the schematic views in Fig. 1 and Fig. 2. Additionally, the \( k \) dimension of contact are set to be 5.2\( \mu \)m, \( 8 \times 8 \mu m^2 \) as preconditions in the design and optimization.

C. C-V ANALYSIS

The C-V simulation is conducted using CoventorWare [18], for \( l_{\alpha} = 209\mu m \) and \( l_{\text{MIM}} = 120\mu m \). The C-V curves are plotted in Fig. 5. The pull-in and lift-off voltages are simulated to be 23V and 14V, respectively. \( C \) is the capacitance.
Y. Zhang et al.: Scalable Contact-Capacitive MEMS Switches With High Capacitance Ratio

FIGURE 5. (a) Simulated capacitance between signal line and ground line versus actuation voltage, with \(V_{\text{pull-in}}, V_{\text{lift-off}}, C_{\text{ON}}\) and \(C_{\text{OFF}}\) marked. (b–c) The simulated deformation of the cantilever at \(V_{\text{pull-in}}\) and \(V_{\text{lift-off}}\). Length of the MIM capacitor (\(l_{\text{MIM}}\)) in the simulated switch is set to be 120 \(\mu\)m (CS11).

TABLE 1. Parameters and dimensions of the proposed switches.

| Parts       | Parameters                | Value, \(\mu\)m |
|-------------|---------------------------|-----------------|
| CPW TML     | Width of signal line, \(S\) | 120             |
|             | CPW spacing, \(G_{\text{CPW}}\) | 16              |
|             | Thickness of CPW, \(t_{\text{CPW}}\) | 2.5            |
| Cantilever  | Width of cantilever, \(w_{\text{ct}}\) | 120            |
|             | Length of cantilever, \(l_{\text{ct}}\) | 209            |
|             | Thickness of cantilever, \(t_{\text{ct}}\) | 2.5            |
|             | Gap between cantilever and actuator, \(\text{gap}\) | 3.5            |
| MIM Capacitor | Thickness of upper plate, \(t_{\text{up}}\) | 2.5            |
|             | Thickness of dielectric, \(t_{\text{d}}\) | 0.45           |
|             | Thickness of bottom plate, \(t_{\text{bottom}}\) | 0.5           |
|             | Length and width of the MIM cap, \(l_{\text{MIM}}\) | 30-120         |
| Contact     | Length and width of contact, \(l_{\text{contact}}\) | 8              |
|             | Thickness of the contact, \(t_{\text{contact}}\) | 0.4            |

between the signal line (S) and ground line (G) of the CPW. When the voltage is higher than \(V_{\text{pull-in}}\), \(C_{\text{OFF}}\) is the capacitance of OFF-state. \(C_{\text{OFF}}\) is defined by the MIM capacitor. When the voltage is lower than \(V_{\text{lift-off}}\), \(C_{\text{ON}}\) is the capacitance of ON-state. \(C_{\text{ON}}\) is mainly determined by capacitances of contacts and their fringe capacitance. According to the C-V simulation in Fig. 5, the \(C_{\text{r}}\) of the simulated switch is about 330. Generally, the tested \(C_{\text{ON}}\) and RF simulated \(C_{\text{ON}}\) are bigger than the DC simulated results in Fig. 5, due to the RF parasitic effect. So, the tested \(C_{\text{r}}\) and RF simulated \(C_{\text{r}}\) will be smaller than 330.

D. SCALABILITY

The parameters and dimensions of the proposed switches are listed in Table 1. As a variable parameter, \(l_{\text{MIM}}\) is designed to be 30-120\(\mu\)m, which is important for the scalability.

The switches are named on the basis of length of the MIM capacitor (\(l_{\text{MIM}}\)), just as listed in Table 2. RF performances, especially S-Parameters, are simulated using High Frequency Structure Simulator (HFSS) [19] and fitted by Advanced Design System (ADS) [20]. The simulated \(C_{\text{MIM}}, C_{\text{r}}\) and \(f_{0}\) are also listed in Table 2.

The simulations predict the scalability of the switches, mainly including \(C_{\text{MIM}}\) and \(f_{0}\). The scaling parameter (\(K_{s}\)) is defined as

\[
K_{s} = \frac{l_{\text{MIMi}}}{l_{\text{MIM1}}} \tag{7}
\]

The letter \(i\) denotes the considered switches, such as \(i = 1\) for CS11, 2 for CS12, 3 for CS13, and so on.

The simulated capacitance of MIM capacitor (\(C_{\text{MIM}}\)) and resonance frequency (\(f_{0}\)) versus scaling parameter (\(K_{s}\)) are plotted in Fig. 6. As shown in Fig. 6, the \(C_{\text{MIM}}\) scales according to (8), and the \(f_{0}\) scales according to (9).

\[
C_{\text{MIM}} \approx C_{\text{MIM1}} K_{s}^{2} \tag{8}
\]

\[
f_{0} \approx \frac{f_{01}}{K_{s}} \tag{9}
\]

III. FABRICATION

The switches are fabricated by the Tsinghua University metal-contact switch process [21], [22] as shown in Fig. 7. The switches are fabricated on a 4-inch quartz substrate. Detailed fabrication process is illustrated as follows.

(a) A 100-nm SiO\(_2\) layer is deposited as a buffer layer. A 500-nm polysilicon layer is deposited, injected, annealed and patterned to form dimples and bias resistors;

(b) A 500-nm Al layer is sputtered and patterned as actuators and bottom plates of MIM capacitors. A 400° C annealing process is conducted to realize ohmic contact between Al and polysilicon;

(c) A 450-nm Si\(_3\)N\(_4\) layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) as dielectric layer with several holes etched to exposed the Al, which is used to form Al-Au contacts;

(d) A 100-nm Au layer is sputtered as electroplating seed layer. Then a 6-\(\mu\)m photore sist (PR) is coated and patterned as electroplating mold;

(e) A 2.5-\(\mu\)m Au layer is electroplated to form CPW TML. PR mold and seed layer are removed;

TABLE 2. Simulated results of the proposed switches with different dimensions.

| Name | \(l_{\text{MIM}}\) (\(\mu\)m) | \(K_{s}\) | \(C_{\text{MIM}}\) (pF) | \(f_{0}\) (GHz) | \(C_{r}\) |
|------|----------------|--------|----------------------|--------|--------|
| CS11 | 120           | 1      | 1.98                 | 30     | 124    |
| CS12 | 100           | 0.833  | 1.38                 | 36     | 86     |
| CS13 | 80            | 0.667  | 0.890                | 43     | 56     |
| CS14 | 60            | 0.500  | 0.550                | 55     | 34     |
| CS15 | 40            | 0.333  | 0.255                | 76     | 16     |
| CS16 | 35            | 0.292  | 0.2                  | 84     | 12.5   |
| CS17 | 30            | 0.250  | 0.15                 | 92     | 9.4    |
(f) A 3-µm polyimide (PI) layer is coated, baked and patterned as a sacrificial layer;
(g) A 100-nm Au layer is sputtered as electroplating seed layer for the second electroplating. A 6-µm PR is coated and patterned as cantilever mold;
(h) A 2.5-µm Au layer is electroplated to form cantilevers. PR mold and seed layer are removed;
(i) The PI sacrificial layer is removed by O₂-plasma etching.

We obtain a series of switches through the process. The scanning electron microscope (SEM) photographs of the contact-capacitive switches are shown in Fig. 8, with overviews of the devices and close views of MIM capacitor, cantilever and Au-Al contact.

The optical microscope (OM) photograph is shown in Fig. 9, with surface height plotted at line A-A’. The cantilevers in the switches warp slightly, which is caused by the low-stress electroplating and dry etching process. The slight warping makes the \( V_{\text{pull-in}} \) higher than design, and it is beneficial for long term stability. The gap at contacts is about 3.7µm.

IV. MEASUREMENTS AND ANALYSIS

Measurements of the contact-capacitive switches are carried out. The devices are tested to obtain \( k, C_{\text{OFF}}, V_{\text{pull-in}}, V_{\text{lift-off}} \) firstly. After that, the S-Parameters measurement and linearity analysis of the switches are conducted. Then the scalability is analyzed.

A. MECHANICAL MEASUREMENT

The elastic coefficient (\( k \)) of the cantilever is tested by Agilent Nano Indenter G200. The indenter is put on the tip point as shown in Fig. 10. Responses of the cantilever and the CPW TML on substrate are also recorded and plotted in Fig. 10, in which they show different performances. In the initial displacement (from 0nm to 200nm), response of the cantilever follows Hooke’s Law. And, it is reasonable to ignore the inserting depth of the indenter on cantilever. The cantilever can be regarded as a spring. The \( k \) of the spring (~7.5N/m) is higher than the theoretical and design value (~5.2N/m), which is caused by the residual stress of the cantilever and variation of the fabrication process.

B. CAPACITANCE MEASUREMENT

As an important part of the switch, MIM capacitor is tested byFocused Ion Beam (FIB) to expose the section. The MIM capacitor is formed by 486nm-Al layer, 459nm-Si₃N₄ layer, and 2.5µm-Au layer, just as shown in Fig. 11(a-c).
FIGURE 8. SEM photographs of the fabricated contact-capacitive switches: (a) Overview of the switch with 120µm MIM (CS11); (b) Overview of the switch with 80µm MIM (CS13); (c) Close view of the MIM capacitor and contacts of CS13; (d) Close view of the cantilevers of the switch with 60µm MIM (CS14); (e) Close view of the Au-Al-contact of the switch with 30µm MIM (CS17).

FIGURE 9. OM photograph of switch CS13 (upper) and surface height of the device at line A-A’ (bottom).

FIGURE 10. Measured results of the elastic coefficient (k) of the cantilever when the force is put on end of the cantilever, with the indenter tip point and measured force versus displacement.

Some dummy capacitors with different areas are also tested. Measured capacitance versus area in Fig.11(d) shows a good linearity, which verifies the stability of the capacitance performance. The relative dielectric constant (εr) of the PECVD Si3N4 in MIM capacitor is tested to be 7.5.

Fig. 12 shows the measured capacitance versus actuation voltage by using the test machines (Cascade 150 and Agilent B1505A). The tested capacitance consists of two parts: one is capacitance between signal line (S) and ground line (G) in CPW, and the other one is C_{ON}/C_{OFF}. The V_{pull-in} and V_{lift-off} are marked in the figure. The C_{ON} is not marked because of the limitation of the capacitance floor (∼100fF) which is caused by the space between signal line and ground line. C_{ON} cannot be tested by this method; instead, we use fitting S-Parameters method to obtain C_{ON}, as shown in next part.

The measured V_{pull-in} and V_{lift-off} are 32.6V and 13.6V, respectively, which are slightly different with simulation. And, this is caused by warping and adhering of the cantilever.

TABLE 3. Fitted parameters of the switches using ADS based on measured S-Parameters.

| Parameters | CS11 | CS12 | CS13 | CS14 | CS15 | CS16 | CS17 |
|------------|------|------|------|------|------|------|------|
| L_{pull} / μm | 120  | 100  | 80   | 60   | 40   | 35   | 30   |
| C_{MIM} / pF  | 1.98 | 1.37 | 0.869| 0.5  | 0.225| 0.180| 0.125|
| L_{OFF} / pH  | 13   | 12.9 | 13.3 | 13.3 | 15.5 | 17   | 21.5 |
| R_{OFF} / Ω   | 0.425| 0.35 | 0.825| 0.475| 0.675| 0.375| 1.00 |
| C_{OFF} / pF  | 16   | 16   | 16   | 16   | 16   | 16   | 16   |
| f_{S} / GHz   | 29   | 37.9 | 46.7 | 61.6 | 86.9 | 91.0 | 97.3 |

* L_{OFF} is the sum of L_{OFF1} and L_{OFF2}.
C. S-PARAMETERS MEASUREMENT

The S-Parameters of the switches are measured with the help of probe station (Cascade Summit 12000M) and PNA-X Microwave Network Analyzer (Keysight N5290A). The S-Parameters are plotted in Fig. 13, with $I_{ON}$, $R_{ON}$ at ON-state and $I_{OFF}$, $R_{OFF}$ at OFF-state. The fitted results by using equivalent circuit in Fig. 3 and ADS are also plotted in Fig. 13. The $I_{ON}$s are better than $-1.5$dB, and the $R_{ON}$s are better than $-10$dB, from DC to 110GHz. The $I_{ON}$ can be further optimized by impedance matching. Meanwhile, $f_0$s of the switches vary from 29 to 97GHz. The fitted parameters are summarized in Table 3. The $C_{MIM}$ of the switches vary from 8 to 124. And, the $C_r$ can be improved by high-k materials and thinner layer to enhance the performance of the switch. The switches show scalability on some parameters, which will be discussed later.

D. LINEARITY MEASUREMENT AND CALCULATION

The typical linearity test system with RF sources, 3dB coupler, and spectrum analyzer just like in [11] is used for IIP3 measurement. But, the ability of the test system we use is about 60dBm, which is much lower than the proposed devices. The test result is illustrated in Fig. 14. Limited by the test bench performance, it is difficult to extract the intermodulation signal generated by the switch directly with the non-negligible influence of test system. So, we use indirect test method to calculate the linearity of the device, according to (6).

On the basis of (6), previous studies [15]–[17] and the tested $k$, $g$, $C_{ON}$, $f_0$ ($\omega_0$), it is easy to obtain the IIP3 of the switches. The IIP3s of CS11 and CS17 are plotted in Fig. 15. The $f_0$s of CS11 and CS17 are 29GHz and 97.3GHz, respectively. When the $f_{en}$ is higher than 100kHz, the IIP3 will be higher than 80dBm, which can reach the requirement of future communication system.

E. SCALABILITY

The scalability of the switches is illustrated in Fig. 16, in which the dependencies of $C_{MIM}$ and $f_0$ on $K_s$ are described. Fig. 16(a) shows the capacitance of MIM capacitors ($C_{MIM}$) versus scaling parameter ($K_s$), which agrees
TABLE 4. State-of-the-Art of different capacitive MEMS switches.

| Switches | [9] | [10] | [11] | [12] | [16] | [17] | [6] | [7-8] | This work |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Description | High-k Materials | Curly Beam | Contact-capacitive | Linearity Analysis | Scalable Design | Contact-capacitive Design |
| $f_0$ (GHz) | 23 | >40 | ~10 | 45 | 15 | ~10 | - | - | 20 | 60 | 94 | 29 | 61.6 | 97.3 |
| Dielectric | TaX | AlN | SiN | SiO | SiO | SiN | SiN | Air | SiN | SiN |
| $C_{eq}$ (pF) | 1.32 | 1.55 | 10 | 2.6 | 5 | 26.8 | - | - | 2.155 | 0.525 | 0.265 | 1.98 | 0.5 | 0.125 |
| $C_0$ | 19 | 38 | 168 | 108 | 78.5 | 237 | - | - | - | 27 | - | 124 | 26 | 5.5 |
| IL (dBm)* | - | - | - | - | - | - | >50 | >41 | - | - | - | - | - | >80 |

*The IL is tested or calculated under situation that $f_{on}$=100kHz.

Figure 16. Measured (a) Capacitance of MIM capacitor ($C_{MIM}$) and (b) resonance frequency ($f_0$) versus scaling parameter ($K_s$).

Table 4 shows the state-of-the-art of different capacitive MEMS switches. The proposed switches combine the contact-capacitive design and scalable design, which is the main advantage and the reason of the well performances. The switches show almost the widest frequency bands. And they perform the highest linearity, owing to the small capacitance at ON-state. The capacitance ratio $C_r$ is higher than 120, and it can be improved to a higher value by high-k materials and thinner dielectric layer.

**V. CONCLUSION**

This paper presents design, modeling, optimization, fabrication and measurements of a series of scalable contact-capacitive switches for mmW applications. The contact-capacitive topology makes it feasible to design ON-state and OFF-state separately. The proposed switches show good scalable performance, whose working bands vary from 20GHz to 110GHz. $I_{LON}$ of the switches are better than 1.5dB, and the $I_{SOFF}$s are better than 30dB. Linearity (IIP3) of the switches are tested to be higher than 60dBm, and calculated to be higher than 80dBm. The capacitance ratio ($C_r$) of CS11 reaches 124, which can be improved in the future studies.

Further studies on direct linearity test, package, reliability and application of these devices should be conducted.

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