**Abstract:** Slew-rate enhancement (SRE) techniques assist the charge transfer process in OTA-based switched-capacitor circuits. Parallel-type slew-rate enhancement circuits, i.e., circuits that provide a feed-forward path external to the main OTA, are attractive solutions, since they introduce a further degree of freedom in the speed/power consumption design space without affecting other specifications regarding the main OTA. This technique lends itself to be employed jointly with advanced OTA topologies in order to compose a highly energy efficient OTA/SRE system. However, insights in design choices such as power optimization are still missing for such systems. Here we discuss system level choices with the help of a simple model. Using precise electrical simulations, we demonstrate energy savings greater than 30% for different OTA/SRE systems implemented in a standard 180-nm CMOS technology.

**Keywords:** energy efficiency; switched-capacitors amplifier; switched-capacitors integrator; auxiliary slew-rate enhancer; slew-rate assisted single-stage otas

### 1. Introduction

The settling behaviour of Switched-Capacitor (SC) stages, as the one depicted in Figure 1a, has been conveniently described by a simplified model [1–8]. This model breaks down the charge-transfer operation in a SC stage, whether a SC amplifier or a SC integrator, into two phases, corresponding to the idealized operating regions of the OTA: slew and linear regions. Hence, the total settling time, \( t_S \), is then given by two contributions \( t_1 \) (slew-time) and \( t_2 \) (linear time) as:

\[
\begin{align*}
  t_S &= t_1 + t_2, \\
  t_1 &= \left( \Delta V_l(0^+) - V_{d\text{max}} \right) \frac{C_r'}{I_{\text{omax}}}, \\
  t_2 &= \tau \cdot \ln \left( \frac{V_{\text{dmax}}}{V_{\text{line}}} \right),
\end{align*}
\]

where: \( \Delta V_l(0^+) \) is the initial step seen at the OTA’s input due to the charge redistribution at \( t = 0 \), proportional to \( \Delta V_S \) through the attenuation factor \( C_S / [C_S + C_P + C_F C_L / (C_F + C_L)] \); \( I_{\text{omax}} \) is the OTA’s maximum output current; \( C_r' = (C_S + C_P)(1 + C_L / C_F) + C_L \); \( V_{d\text{max}} \) discriminates the OTA’s operation region (slew rate for \( |V_l| \geq V_{d\text{max}} \), linear for \( |V_l| < V_{d\text{max}} \); \( V_{\text{line}} = \epsilon R \Delta V_S C_S / (C_S + C_P + C_F) \); where \( \epsilon R \) is the relative error on the output voltage step and finally \( \tau = C_r' / G_m \) is the time constant in the linear transient of a single-pole OTA, being \( G_m \) the OTA’s transconductance.

As shown in Figure 1a, we are interested in the case of large voltage steps which trigger the OTA to operate initially in its slewing region. This leads us to point out that both \( t_1 \) and \( t_2 \) depends on \( \Delta V_S \) respectively through \( \Delta V_l(0^+) \) and \( V_{\text{line}} \). On the other hand, Equation (1) explicitly shows how \( V_{d\text{max}} \) which is a design parameter, influences the settling time, both in the \( t_1 \) and \( t_2 \) terms also. For a Class-A OTA, like the common folded-cascode (FC) OTA, \( V_{d\text{max}} \) can be identified with the range of operation of the input.
differential pair. When sized to operate in weak inversion to achieve the maximum current efficiency \([9]\), \(V_{dmax} = 2nU_T\), being \(n\) the sub-threshold slope and \(U_T\) the thermal voltage \((\approx 25.7 \text{ mV at } 25 ^\circ\text{C})\).

Figure 1b shows the relative impact of \(t_1\) on the overall settling as a function of the input voltage step assuming the conventional FC OTA modeled from (1). For this OTA, a simple linear relationship between its \(G_m\) (weak inversion operation of input devices) and \(I_{omax}\) exists, which can be easily shown to be: \(\tau I_{omax} = 2nU_TC_S'\). This fact allows us to eliminate all the transistor-level design parameters from \(t_1/t_S\). The design space, for this particular case, can be represented as a family of curves parameterized for a given capacitive network \((C_S, C_F, C_L, C_P)\) and the relative error \(\epsilon_R\). In Figure 1b two design cases, named "high-resolution" and "low-resolution", are shown. They correspond to the respective parameters sets in the inset table. These are typical values, mainly derived from \(kT/C\)-noise specifications, that can be found in high-resolution (\(\geq 16\) bits) and low-resolution (12 bits or less) systems. Marginally, specific transistor-level design choices (sizing of input devices) affect \(C_P\), but as long as \(C_P\) is sufficiently smaller than \(C_S\), the model accuracy is not compromised. The main OTA, depending on the specific application case, follows design optimization taking into account many other aspects, such as offset, low-frequency noise. Using a parallel-type SRE, the speed/power-consumption trade-off can be targeted without affecting other design parameters.

\begin{table}[h]
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Case & \(C_S\) (pF) & \(C_F\) (pF) & \(C_P\) (pF) & \(C_L\) (pF) & \(\epsilon_R\) (ppm) \\
\hline
high resolution & 6.00 & 24.00 & 0.32 & 1.00 & 25 \\
low resolution & 0.375 & 1.50 & 0.32 & 1.00 & 400 \\
\hline
\end{tabular}
\end{table}

Figure 1. SC circuit and its relevant waveforms under the charge transfer process for a stimulus of \(\Delta V_S\) (a); Slew-rate time over total settling time as function input voltage step \(\Delta V_S\) considering a folded-cascode OTA with input pair working in weak inversion \((V_{dmax} = 2nU_T)\) (b). Colored bands correspond to voltage supply \((V_{dd})\) regions considering \(n\) ranging from 1.5 and 2.0, room temperature conditions. The numerical values of the circuit parameters for high-resolution and low-resolution cases are indicated in table.
In order to achieve the best signal-to-noise ratio, \( \Delta V_S \) is set equal to the maximum magnitude of the input step voltage that we assume to be the supply voltage \( V_{dd} \). Moving from one technological node to another, distinct supply voltage domains are given. In Figure 1b, the \( V_{dd} \) regions for 1.2 V, 1.8 V, 3.3 V can be associated to the 65-nm, 180-nm and 350-nm CMOS processes, respectively. As expected, the lower \( V_{dd} \) the lower is the impact of \( t_S \) on \( t_f \). However, even for the 1.2-V/low-resolution case \( t_1 \) is approximately the 75% of \( t_S \), justifying the need for power-efficient circuit techniques to reduce \( t_f \). For example, by reducing \( t_1 \) to one third of its original value, \( t_S \) would be halved. Intuitively this \( t_S \) reduction can be translated to a design situation where \( t_S \) is maintained, but the total power consumption is scaled down. We recently proposed a capacitive-boosted slew-rate enhancer (SRE) technique fit to this purpose \cite{10} based on Nagaraj’s SRE \cite{11,12}. Nevertheless, a systematic study of this technique to provide clear system-level design insight is still missing.

Here we want to address this issue by analyzing the performances of the SRE technique when combined with more advanced OTA configurations, such as the recycling folded cascode (RFC) \cite{13}. The remainder of this paper is organized as follows: Section 2 develops the settling-time model for power-aware system-level choices; Section 3 introduces energy metrics to evaluate the performances of different OTA/SRE systems by the means of accurate electrical simulations; Section 4 concludes this work by stating the major findings.

2. Extended Settling-Time Model

2.1. System-Level Settling Model

We recently introduced an extension of model in (1) concerning system-level parameters \cite{10}. This model is useful to describe the settling behaviour of the SC stage in Figure 1a whether it employs a single-stage OTA, or a OTA/SRE system:

\[
\frac{t_S}{t_X} = \frac{1}{k_{AB}} \left( c_1 - \frac{V_{dmax}}{\Delta V_S} \right) + \frac{1}{k_G} \frac{V_{dmax}}{\Delta V_S} \ln \left( \frac{c_2 \frac{V_{dmax}}{\Delta V_S} + 1}{\epsilon R} \right)
\]

(2)

The two addends in the right hand side of (2) correspond to \( t_1 \) and \( t_2 \) of (1) respectively, normalized by the time \( t_X \). Indeed, Equation (2) descends from Equation (1), once the following identities are defined:

\[
t_X = \frac{C'_S \Delta V_S}{I_{sup}}; \quad c_1 = \frac{C_S}{C_S + C_F} \left( 1 - \frac{C_L}{C'_S} \right); \quad c_2 = 1 + \frac{C_F + C_P}{C_S}; \quad k_{AB} = \frac{I_{dmax}}{I_{sup}}; \quad k_G = \frac{G_m V_{dmax}}{I_{sup}}.
\]

(3)

As evident from (3), the model of (2) emphasizes the role of the quiescent current \( I_{sup} \) drawn by the circuit from the supply rail. The parameters in (2) have the following meaning:

- \( t_X \) acts as a normalizing unit for \( t_S \) taking into account system-level specifications regarding the capacitive load \( C'_S \), the input step amplitude \( \Delta V_S \), and the current consumption \( I_{sup} \).
- \( c_1 \) and \( c_2 \); both parameters mainly depend on the capacitive feedback network \( C_S, C_F, C_L \) and the OTA’s input parasitic capacitance \( C_P \).
- \( k_{AB} \) expresses the efficiency by which the OTA uses the given \( I_{sup} \) to produce its output current when operating in slew-rate region.
- \( k_G \) expresses the efficiency by which the OTA uses the given \( I_{sup} \) to produce large transconductance when operating in linear region.

By applying the following transformation:

\[
\frac{t_S}{t_X} = \frac{t_S I_{sup}}{C'_S \Delta V_S} = \frac{I_{sup}}{I_X}, \quad \text{where} \quad I_X = \frac{C'_S \Delta V_S}{t_S}.
\]

(4)

We observe that the same expression in (2) can be used to estimate the static current consumption \( I_{sup} \) needed for a given \( t_S \), while maintaining the rest of the constraints.
The normalizing current $I_X$, similarly to $t_X$, takes into account only system-level specifications.

### 2.2. Model Extension to OTA/SRE Systems

Figure 2a shows a typical Fully-Differential SC integrator configuration. It is possible to demonstrate its equivalence in terms of settling time with the single-ended circuit in Figure 1a, considering voltages and currents of the single-ended model representing the total differential-mode components of the fully-differential circuit in Figure 2a. It can be easily shown that the only transformation that has to be applied regards the input capacitance of the OTA in the equivalent circuit, $C_P$ in Figure 1a, that should be set to twice the input capacitance of the fully-differential OTA. Considering Figure 2a, the other capacitances of the circuit are simply replicated in the single-ended equivalent, i.e., $C_S = C_{S1} = C_{S2}, C_T = C_{F1} = C_{F2}, C_L = C_{L1} = C_{L2}$.

The SRE of [10] provides a parallel signal path in order to assist the OTA during the charge transfer process; its transistor-level schematic is also shown in Figure 2a. The SRE delivers non-zero output currents only during the slew rate time $t_{s1}$, while mirrors Mm1-Mm8 are ideally turned off afterwards. This behaviour is achieved thanks to the current comparison occurring at nodes A-A’ and B-B’ under the action of Mb1-Mb2 and Mb3-Mb4 transistors which are set to subtract a fixed amount of current $I_{th}$, determining the turn-on/off threshold of the SRE. For large input differential voltage ($> V_{dmax}$), the SRE provides an amount of current equal in magnitude to $I_{omax,SRE}$.

The introduction of the SRE adds a static current consumption indicated with $I_{sup,SRE} = 2I_{tail}$. Its maximum output current capability is then measured by:

$$k_{AB,SRE} = \frac{I_{omax,SRE}}{I_{sup,SRE}} = k \left( 1 - \frac{I_{th}}{I_{tail}} \right),$$

(5)

since the SRE is statically biased by $2I_{tail}$ (bias chain not included) and, by considering a robust sizing with $I_{th} = 3I_{tail}/4$, it is capable to deliver $kI_{tail}/4$ at the output under maximum unbalanced condition. Actually, SREs with large values of $k$ together with low $I_{tail}$, which would represent an optimum design choice for the SRE, show a degradation of their effectiveness. The capacitive-boosting proposed in [10] and implemented by the capacitor $C_B$ shown in Figure 2a solves this issue and has been adopted in this work.

From the design point of view, the SRE input commutation threshold is designed to coincide with voltage $V_{dmax}$, that defines the boundary between the input regions where the OTA behaves in a linear and non-linear (saturated) fashion. The threshold-conditioned behaviour of the SRE is similar to that of comparator-based SC circuits introduced in [14]. Ideally, comparator-based SC circuits has a null linear settling time ($t_2 = 0$ corresponding to $V_{dmax} = 0$) making $I_S = I_{s1}$. This condition is extremely beneficial from the power-efficiency point of view since the current drawn from the supply rail is almost entirely used to charge directly the load. In practice, the absence of virtual ground prevents comparator-based SC solutions to be used in medium/high resolution applications. In our case the SRE always operates in parallel with an OTA in order to ensure precise virtual ground settling and thus circumventing the linearity limitations typical of comparator-based SC circuits.

From the system point of view, the overall static current consumption is now composed by the OTA’s contribution $I_{sup,OTA}$ and the SRE’s contribution $I_{sup,SRE}$; this can be accounted for by defining the $\eta$ parameter such that:

$$\eta = \frac{I_{sup,SRE}}{I_{sup,OTA}} \quad \text{and} \quad I_{sup} = I_{sup,OTA} + I_{sup,SRE} = (1 + \eta)I_{sup,OTA}.$$  

(6)

As already stated, the settling time model in (2) is valid also for OTA/SRE system, with due attention to the expressions of $k_{AB}$ and $k_G$. The former, being related to the maximum output current, is given by the combined action of the OTA and SRE, while the
latter is strictly related to the $G_m$ of the OTA alone which is now biased by a portion of the total supply current, namely $I_{sup}/(1+\eta)$:

$$k_{AB} = \frac{I_{omax,OTA} + I_{omax,SRE}}{I_{sup}} = \frac{k_{AB,OTA} + \eta k_{AB,SRE}}{1+\eta}; \quad k_G = \frac{k_{G,OTA}}{1+\eta}. \tag{7}$$

Figure 2b shows the settling time $t_S$ and $I_{sup}$ while increasing the $k_{AB}$ of the OTA/SRE system for both the FC and RFC OTA topologies. Solid traces show the possible reduction in $t_S/t_X$ or $I_{sup}/I_X$ when using an ideal SRE (no static power) to increase the $k_{AB}$. A more realistic prediction is shown by the dotted traces, which account for a $\eta = 10\%$ budget. In any case, substantial benefit of the SRE action is predicted by the model. Detailed discussion on RFC vs. FC parameters ($k_{AB}$, $k_G$ and $V_{dmax}$) is presented in the following section.

![Figure 2](image)

**Figure 2.** SC integrator with OTA/SRE combination: (a) topology of the parallel-type SRE employing capacitive boosting. (b) Plot of $t_S/t_X$ as a function of $k_{AB}$ for two different OTA topologies combined with an ideal (no power consumption) and real ($\eta = 10\%$) SRE. Note that different $k_{AB}$ values correspond to different design choices for the SRE. The relative settling time $t_S/t_X$ can be converted to a relative supply current consumption $I_{sup}/I_X$ through (4).

### 2.3. Model Extension to Advanced OTA Topologies

The validity of the model in (2) for advanced single-stage OTA architectures, such as RFC [13], Super-Class AB [15], VMA [16] has not been yet demonstrated. The model in (1) and hence (2) hinges on a piece-wise linear approximation of OTA’s characteristic of the output differential current as function of input differential voltage, i.e., $I_{od}(V_{id})$. A hard threshold, $V_{dmax}$, is set between large-signal and small-signal regions. Within
the $V_{d_{\text{max}}}$ range, i.e., $|V_{id}| < V_{d_{\text{max}}}$, the model considers the linear small-signal circuit approximation. Outside the $V_{d_{\text{max}}}$ range, i.e., $|V_{id}| \geq V_{d_{\text{max}}}$, the model considers perfect saturation of currents to the $I_{o_{\text{max}}}$ value. This highly simplified model is intrinsically prone to inaccuracy [2,3] and cannot be used to fine tune any final design, for which accurate electrical simulations are still needed [17]. Nevertheless it provides a uniform and simple analytic tool useful to compare different OTAs and OTA/SRE architectures, as will be shown in the following discussion.

Here we will discuss the RFC topology [13] as exemplary case study for mapping advanced single-stage OTAs to the model in (2). Although the methodology is of general applicability, exhaustive mapping of other advanced OTA families, as those stemming from [15,16], are beyond the scope of this paper.

Figure 3a shows a conceptual schematic of folded cascode architectures formed by a current-steering core and an output section. The current-steering core is in charge to provide the differential voltage to differential current conversion and to properly bias the rest of the circuit. The output section provides low-impedance inputs for the differential current (through Mc1-Mc2) and high-impedance output of the whole OTA.

The FC and the RFC OTAs are obtained when the current-steering core is implemented as the standard and the current-recycling core, respectively, as shown in Figure 3a. The RFC core is obtained by equally splitting the input devices to create an auxiliary current path. Thanks to the action of mirrors Mm1-Mm2 and Mm3-Mm4, both the $G_m$ and the $I_{o_{\text{max}}}$ are enhanced with respect to the FC. Theoretically, in the case of $k_R = 3$, $G_m$ is multiplied by 2 and $I_{o_{\text{max}}}$ is multiplied by 3. This enhancement comes without any static power penalty [13].

Considering now the piecewise approximation, since no discontinuities are present, the relationship $I_{o_{\text{max}}} = G_m V_{d_{\text{max}}}$ is set for both the FC and the RFC OTA. Since in the RFC architecture $I_{o_{\text{max}}}$ and $G_m$ scale differently, the $V_{d_{\text{max}}}$ parameter needs to scale accordingly, i.e., $V_{d_{\text{max}},\text{RFC}} = \frac{3}{2} V_{d_{\text{max}},\text{FC}}$. From the circuit point of view, the wider $V_{d_{\text{max}}}$ is due to the
mires Mm1-Mm2 and Mm3-Mm4 which provide both biasing and signal propagation, differently from what happens in the standard core where the NMOS section only provides biasing currents.

Electrical simulations confirm the theoretical behaviour as shown in Figure 3b where the $I_{od}(V_{id})$ characteristics are shown for both the FC and RFC. The inset shows the actual FC and RFC characteristics, resulting in $I_{od,max, RFC}/I_{od,max, FC} = 3.13$ and $G_{m, RFC}/G_{m, FC} = 1.97$. The main plot is normalized to the maximum output current for each topology. The relative piecewise asymptotes are also reported for comparison. The extracted $V_{dmax}$ parameters are found to be 97.0 mV and 154.0 mV for the FC and the RFC, respectively, which are in good agreement with the expected scaling factor. The normalized $I_{od}$ values for $V_{id} = V_{dmax}$ are 77.6% (FC) and 77.2% (RFC) indicating that the impact of non-linearities on the model prediction accuracy is very close, and that, in both cases, the analytical techniques proposed in [2,3] would be equally effective to mitigate inaccuracy.

3. Energy Efficiency of OTA/SRE Systems

The transient of the SC circuit in Figure 1a implies a quantity of charge delivered to the effective load capacitance $C'_L$ seen at OTA’s output:

$$C'_L = C_L + \frac{C_F (C_S + C_P)}{C_S + C_P + C_F}. \quad (8)$$

The magnitude of the total charge delivered from the OTA to $C'_L$ depends on the total voltage swing at the output node, $\Delta V_{oL}$:

$$\Delta V_{oL} = |\Delta V_o(0^+)| + (1 - \epsilon_R)|\Delta V_o(\infty)| \approx |\Delta V_o(0^+)| + |\Delta V_o(\infty)|, \quad (9)$$

where the $\Delta V_o(0^+)$ and the $\Delta V_o(\infty)$ are easily calculated from the initial charge redistribution and the asymptotic value for an ideally infinite open-loop gain OTA:

$$\Delta V_o(0^+) = \frac{C_S (C_F + C_L)}{(C_S + C_P)(C_F + C_L) + C_F C_L} \Delta V_S; \quad \Delta V_o(\infty) = - \frac{C_S}{C_F} \Delta V_S. \quad (10)$$

Under the action of the fully-differential OTA (or OTA/SRE system), the power supply delivers the charge $Q_L$, given by:

$$Q_L = \frac{1}{2} C'_L \Delta V_{oL}. \quad (11)$$

Note that in differential-circuits the $\Delta V_{oL}$ variation is equally distributed between the output nodes ($V_{op}$ and $V_{on}$ in Figure 2a) around the common mode of the OTA. For the sake of clarity, let us assume that $V_{op}$ and $V_{on}$ undergo a variation of $+\frac{1}{2} \Delta V_{oL}$ and $-\frac{1}{2} \Delta V_{oL}$, respectively. Discharge at $V_{on}$ node occurs due to charge flow to the ground rail, so $Q_L$ is only given by the charge variation at $V_{op}$ node. This fact accounts for the 1/2 factor in (11). Finally, the energy $E_L$ needed for the charge transfer is calculated considering (8)–(11):

$$E_L = Q_L \cdot V_{dd} = \frac{1}{2} C'_L \Delta V_{oL} \cdot V_{dd}. \quad (12)$$

It is important to observe that $E_L$ is proportional to $\Delta V_S$ (see (10)) through a rather complex function of the capacitor network. While $C_S$, $C_F$ and $C_L$ values derive directly from system-level specifications, $C_P$ is the result of a specific OTA design. First-hand estimation of $E_L$, prior any OTA design, can be done neglecting $C_P$ in (8), (10) and asserting the condition $C_P \ll C_S$ in the aftermath.

In a system where the stochastic or pseudo-stochastic characteristics $\Delta V_S$ are known, like in a SC $\Delta \Sigma$ modulator [18], $E_L$ can be used to estimate the energy needed for signal processing purposes, regardless of the overheads due to the employment of actual circuits. A simple electrical testbench can be employed to numerically calculate the actual energy,
$E_{sup}$, drawn from the supply rail by the OTA or OTA/SRE for a single transition step ($\Delta V_S$). The normalized $E_{sup}/E_L$ quantity may be employed as a useful indicator to optimize the OTA or OTA/SRE system tailored to its final application. In such testbench different OTA/(SRE) topologies can be tested for efficiency comparison aiding the search for power optimization among different topological solutions.

As exemplary design cases, specifications in Table 1 are assumed. We will discuss the application of the SRE technique in both a FC and RFC topologies in comparison with the FC and RFC alone aiming to fulfill the same settling speed and precision ($t_S = 15$ ns, $\epsilon_R = 100$ ppm). Regular NMOS and PMOS devices from the UMC 180-nm CMOS process under 1.8-V supply condition are assumed. The comparison methodology starts by designing a FC OTA (FC1) compliant with the specifications in Table 1. The next step is to consider the FC/SRE system, for $\eta = 10\%$, $C_B = 500$ fF and $k = 30$ which are a valid set of parameters for nearly optimum behaviour of the SRE [10]. For this configuration the FC biasing currents and its input devices are scaled to maintain the same current density in the input devices and to attain to the same settling time (FC2). A further step is to consider the RFC topology (RFC1) which embeds power-efficient class-AB behaviour. Finally, the RFC/SRE system is considered, with the correspondent current and input devices scaling (RFC2). Since the SRE is completely turned off in the last part of the settling, the noise, offset and gain properties of the original OTA are left unchanged.

Actual transistor parameters and biasing currents are also reported in Table 1. The $I_{tail}$ current predicted by the model Equations (2), (4) and (7), together with the mirror ratios $k = 30$ for the RFC, $k_R = 3$ for the RFC and $\eta = 10\%$ are: 375 $\mu$A for FC1, 195 $\mu$A for FC2, 152 $\mu$A for RFC1 and 96 $\mu$A for RFC2. The FC-OTA parameters are $k_{AB,FC} = k_{G,FC} = 0.5$, while the RFC-OTA parameters are $k_{AB,FC} = k_{G,FC} = 1.5$, calculated applying the definitions in (3). The input devices are biased in weak inversion operation in all cases, so that $V_{dmax,FC} = 98.8$ mV and $V_{dmax,RFC} = 148.2$ mV. Note that the SRE commutation threshold has been kept around $V_{dmax,FC}$ in both cases for the sake of simplicity; further optimization can be achieved in the SRE/RFC2 design. $k_{AB,SRE}$ has been estimated from the electrical simulations, due to the lack of a proper description of the capacitive-boosting technique effects in the modeling approach. As discussed in [10], the relation (5) is valid only neglecting the turn-on and turn-off transients of the SRE circuit. The actual $k_{AB,SRE}$, calculated through electrical simulations, is found to be 41.5.

The $I_{tail}$ estimation is quite accurate for FC1 and FC2, while the evident underestimation for RFC1 and RFC2 can be ascribed to the simplistic modeling. More specifically, it derives from the phase-margin degradation of the RFC topology due to the non-dominant pole determined by the current mirrors Mm1-Mm2 and Mm3-Mm4 (see Figure 3a). In such condition the single-pole OTA approximation used in Equation (1) is not accurate, reinforcing the need for more refined models to abstract circuit behaviour including the presence of non-dominant singularities in the OTA frequency response [8].

Table 2 lists the results from electrical simulation using Spectre/Cadence. As expected, the use of the SRE greatly enhances the $E_{sup}/E_L$ figure of merit in both cases, i.e., FC1 vs. FC2 + SRE and RFC1 vs. RFC2 + SRE, which in the second case showed to be even more beneficial than in the first case. Interestingly, the use of the SRE coupled to the standard FC showed to surpass the efficiency performances of the RFC alone, proving to be a quite effective and versatile technique. In absolute terms, the energy reduction enabled by the SRE is 34% for both the FC and the RFC topology. The $t_1/t_S$ has been also estimated using the model with the $k_G$ corrected values. In the first case, a reduction of almost 1/5 is obtained, while in the second case the slew-rate time is approximately divided by three. As already mentioned, offset and noise performances are not affected by the action of the SRE, with respect to the OTAs considered individually. For this reason we do not report comparative figures in Table 2.
| Specifications |  |
|----------------|---|
| $t_S$          | 15 ns |
| $\Delta V_S$   | 1.8 V  |
| $C_S$          | 1.5 pF |
| $C_F$          | 6.0 pF |
| $C_L$          | 1.0 pF |
| $\epsilon_R$   | 100 ppm|

**SRE, $I_{tail} = 20 \mu A$, $C_B = 500 fF$.**

| L (nm) | W (µm) |
|--------|--------|
| Mi1-2  | 180    | 1.50   |
| Mi3-4  | 180    | 4.50   |
| Mm1, Mm3 | 180 | 1.62   |
| Mm2, Mm4 | 180 | 48.60  |
| Mm5, Mm7 | 180 | 0.54   |
| Mm6, Mm8 | 180 | 16.20  |
| Mtn     | 1000   | 2.88   |
| Mtp     | 1000   | 0.96   |
| Mb1-2   | 1000   | 2.16   |
| Mb3-4   | 1000   | 0.72   |

| L (nm) | W (µm) |
|--------|--------|
| Mi1-2  | 180    | 480    |
| Mm1-2  | 400    | 32     |
| Mc1-2  | 180    | 72     |
| Mc3-4  | 180    | 288    |
| Mb1-2  | 400    | 73     |
| Mt1    | 400    | 146    |
| Mt2    | 180    | 576    |

| L (nm) | W (µm) |
|--------|--------|
| Mi1-2  | 180    | 240    |
| Mm1-2  | 400    | 32     |
| Mc1-2  | 180    | 72     |
| Mc3-4  | 180    | 288    |
| Mb1-2  | 400    | 73     |
| Mt1    | 400    | 146    |
| Mt2    | 180    | 576    |

| L (nm) | W (µm) |
|--------|--------|
| Mi1′-1′′-2′-2′′ | 180 | 156 |
| Mm1-3  | 400    | 16     |
| Mm2-4  | 400    | 48     |
| Mc5-6  | 180    | 36     |
| Mc1-2  | 180    | 72     |
| Mc3-4  | 180    | 28     |
| Mb1-2  | 400    | 73     |
| Mt1    | 400    | 146    |
| Mt2    | 180    | 72     |
Table 1. Cont.

| Specifications | L (nm) | W (µm) |
|---------------|--------|--------|
| Mi1-1’-2’-2”  | 180    | 78     |
| Mm1-3         | 400    | 16     |
| Mm2-4         | 400    | 48     |
| Mc5-6         | 180    | 36     |
| Mc1-2         | 180    | 72     |
| Mc3-4         | 180    | 28     |
| Mb1-2         | 400    | 73     |
| Mt1           | 400    | 146    |
| Mt2           | 180    | 72     |

Table 2. Electrical simulation results and impact of slew-rate time on the overall settling time \((t_1/t_S)^\star\) estimated by means of the proposed model.

|                          | FC1     | FC2 + SRE | RFC1     | RFC2 + SRE |
|--------------------------|---------|-----------|-----------|------------|
| \(t_S\) (ns)            | 14.98   | 14.69     | 14.64     | 14.61      |
| \(E_{sup}\) (pJ)        | 21.93   | 14.49     | 15.52     | 10.3       |
| \(C_P\) (fF)            | 701     | 358       | 528       | 270        |
| \(E_L\) (pJ)            | 3.13    | 3.14      | 3.13      | 3.15       |
| \(E_{sup}/E_L\)         | 7.00    | 4.61      | 4.95      | 3.27       |
| \((t_1/t_S)^\star\) (%) | 49.8    | 10.5      | 38.8      | 11.9       |

4. Conclusions

This work discusses energy efficiency optimization by using parallel-type SRE circuits to assist single-stage OTAs in the charge transfer process. Detailed electrical simulations demonstrated that power savings greater than 30% are achieved both when using standard Class-A OTAs and more advanced OTA topologies like the recycling folded cascode topology. The optimization process is aided by a simple model useful to fairly compare different OTA topologies. Model accuracy limitations, when used to predict absolute power figures, are also discussed.

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