Optimization of CNOT circuits under topological constraints

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Abstract

CNOT circuit is the key gadget for entangling qubits in quantum computing systems. However, the qubit connectivity of noisy intermediate-scale quantum (NISQ) devices is constrained by their topological structures. To improve the performance of CNOT circuits on NISQ devices, we investigate the optimization of the size/depth of CNOT circuits under topological constraints. We firstly present a method that can optimize the size of any $n$-qubit CNOT circuit to less than $2n^2$ on any connected graph, which is optimal for sparsely connected structures. The simulation experiment shows that our method performs better than state-of-the-art results. Specifically, we present two detailed examples to illustrate the applicability of our algorithm. Furthermore, for the future device with a denser structure, we give a better optimization method that achieves $O(n^2/\log \delta)$ size on a graph with the minimum degree $\delta$, which is optimal on the regular graph. Secondly, for the grid structure, which is commonly used in current quantum devices, we demonstrate that the depth of any $n$-qubit CNOT circuit can be optimized to be linear in $n$ with certain ancillary qubits (ancillas). Our experimental results indicate this method has significant improvements compared with all of the existing methods. We further implement the two circuits commonly used in quantum variational algorithms and quantum chemistry on the 5-qubit IBMQ devices by leverage of our optimization algorithm, the experimental results show the optimized circuit has far less error when there exists noise compared to IBM mapping method.

1 Introduction

Quantum circuit synthesis is a process to construct a quantum circuit that implements a desired unitary operator and optimizes its size/depth in terms of a given gate set, which is an important task in the field of quantum computation and quantum information [1, 2, 3]. There are two key limitations of the current intermediate-scale quantum devices. First, the performance and reliability of quantum devices heavily depend on the length of time that the underlying quantum states can remain coherent. Hence it is natural to design

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the algorithm with less coherent time and environmental noise [4, 5], which in other
words, with smaller size and/or lower depth. The second limitation is that the state-of-
art quantum devices do not support to place 2-qubit gates (usually the CNOT gates) in
arbitrary pairs of qubits. The 2-qubit gates are only allowed to place between the adjacent
qubits [6, 7, 5]. We denote a qubit as a vertex, and use an edge between two vertices to
represent a 2-qubit gate can be performed on these two qubits. Then the limitations of
the qubit connection can be represented as a topological constraint graph. The near term
devices usually use grid-style graph to be their constrained graphs [6, 7, 4]. Meanwhile, d
dimensional grid is also a good candidate of constrained graph for quantum supremacy by
Harrow et al. [8]. There are a large number of work aim to map a quantum circuit to real
quantum superconducting devices restricted to a constrained graph [9, 10, 11, 12, 13].

CNOT circuits, in which there are only CNOT gates, are indispensable for quantum
circuit synthesis to construct general circuits [14, 15, 16, 2], since people often use CNOT
gates with some single qubit gates to construct universal quantum computing [17, 18, 19].
The optimization of the size/depth of CNOT circuits shed some light on more general
problem of arbitrary circuit mapping. CNOT circuits also dominate stabilizer circuits,
which plays an important role in quantum error correction [3] and quantum fault-tolerant
computations [20]. Aaronson et al. [14] proved that any stabilizer circuit has a canonical
form, i.e., H-C-P-C-P-C-H-C-P-C-P-C, where H and P are one layer of Hadamard gates and
Phase gates respectively, and C is a block of CNOT gates only. Hence, optimization of
CNOT circuits can be directly applied to optimization of stabilizer circuit.

There are many researchers aiming at reducing the size/depth of CNOT circuits without
topological constraints [21, 22, 15]. For instance, Moore and Nilsson [21] proposed
an algorithm to parallelize any CNOT circuits to $O(\log n)$ depth with $O(n^2)$ ancillas, in
which the depth matches the lower bound $\Omega(\log n)$. However, these work can not be
directly applied to near-term quantum devices with topological constraints.

There are several size optimization algorithms for CNOT circuits under topological
constraint graph. Kissinger et al. [23] proposed an algorithm that gives a $2n^2$-size equivalent
circuit for any CNOT circuits if the constrained graph contains a Hamiltonian path.
Unfortunately, their optimized size is $O(n^3)$ for the constrained graph without a Hamiltonian
path. Nash et al. [24] proposed a similar algorithm simultaneously which gives a
$4n^2$-size equivalent CNOT circuit for any CNOT circuits on any connected graph. There
arises the following question: Given any CNOT circuit, how can we implement it on the
state-of-art quantum devices with smallest size of quantum gates and/or lowest circuit
depth?

In this paper, we consider how to optimize the size/depth of CNOT circuits under
topological structure constraints, without or with limited ancillas. We firstly propose
an algorithm that can optimize the size of any given CNOT circuit to $2n^2$ on any
connected graph. This bound is tight for the constrained graph with maximum degree $O(1)$.
We further give an algorithm that can optimize the size of any given CNOT circuit to
$O\left(\frac{n^2}{\log \delta}\right)$ on a constrained graph with minimum degree $\delta$. We also prove this bound is
asymptotically tight for a regular graph. We simulate our size optimization algorithm on
some particular graphs in near-term quantum devices, and the simulation experimental
results show our optimized size is smaller than the existing results [23, 24].

Secondly, based on the rapid decoherence of quantum system and the grid constriction
of the recent quantum devices [5, 4], we propose an algorithm which can optimize the depth
of any given CNOT circuit to $O\left(\min\left\{n, \frac{n^2}{m_1 m_2}\right\}\right)$ with $3n \leq m_1 m_2 \leq n^2$ qubits on $m_1 \times m_2$
grid. The optimized depth is asymptotically tight when $m_1 m_2 = n^2$. We generalize the
result to any constant $d$ dimensional grid. We also give the experimental result of the
depth optimization algorithm on an $n \times n$ grid. As the number of qubits grows, the
optimized depth has significant advantages over the existing size optimization algorithms.
Figure 1: 3-qubit CNOT circuit with topological constraint graph. (a) A circuit which cannot be performed in topological constraint (c); (b) A circuit which can be performed in topological constraint (c); (c) topological constraint of a 3-qubit quantum devices.

In the rest of the manuscript, we cover the basic notation of this manuscript, and the basic preliminaries of CNOT circuit and its properties in Sec. 2. In Sec. 3 we introduce our size optimization algorithms, the lower bound and also give an experimental comparison of our algorithms and existing algorithms. Next, we introduce our depth optimization and the experimental results in Sec. 4. In Sec. 5, we implement the optimized CNOT circuit on IBMQ device. The experimental results show less measurement errors compared to the original circuit on the IBMQ noisy device. Finally, we give an discussion in Sec. 6.

2 Preliminary

Notations. We use $[n]$ to denote $\{1, 2, \ldots, n\}$, $\mathbb{F}_q$ to denote field with $q$ elements, $\oplus$ to denote addition under $\mathbb{F}_2$, $\text{GL}(n, 2)$ to denote set of all $n \times n$ invertible matrix over $\mathbb{F}_2$, $\textbf{I}$ to denote identity matrix. Let $e_j$ be the $j$-th coordinate basis vector with all zeros but a 1 in the $j$-th position. In the later sections, with a little abuse of symbols, we use a decimal number to represent the ceiling of this number when it needs to be an integer.

CNOT/SWAP Gate and Circuit. A CNOT gate, with control qubit $q_i$ and target qubit $q_j$, maps $(q_i, q_j)$ to $(q_i, q_j \oplus q_i)$. A SWAP gate, operating on two qubits $q_i$ and $q_j$, swaps $(q_i, q_j)$ to $(q_j, q_i)$. A CNOT/SWAP circuits is a circuit only contains CNOT/SWAP gates. We call a CNOT circuit with size $s$, which means the number of CNOT gates equals $s$ in this CNOT circuit.

Circuit with topological constraint. We use graph $G(V, E)$ to represent the topological constraint of two-qubit gates (CNOT gate) in the circuit. A vertex in $G$ represents a qubit, and the two-qubit gate (CNOT gate) can only operate on two qubits that are connected in $G$. We say a circuit $C$ is under constrained graph $G$ if all two-qubit gates in $C$ satisfy the constraints. Fig. 1 gives an example for the constrained circuit. CNOT circuit in Fig. 1 (a) cannot be performed directly on a 3-qubit quantum device with topological constraint in 1 (c). In contrast, CNOT circuit in Fig. 1 (b) can be performed directly on it.

Circuit with ancillas. We say a CNOT circuit $C_{n,m-n}$ with $n$-qubit inputs and $(m - n)$-qubit ancillas implements an $n$-qubit circuit $C$, if for any input $|x\rangle$ with ancillas $|0\rangle^{(m-n)}$, the results of $C_{n,m-n}$ is $C|x\rangle \otimes |0\rangle^{(m-n)}$. We say two circuits (with or without ancillas) are equivalent if they implement the same circuit $C$.

Matrix representation of CNOT circuit [21]. We use $\text{CNOT}_{i,j}$ to denote CNOT gate with control qubit $q_i$ and target qubit $q_j$. The CNOT gate is an invertible linear map $\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ over $\mathbb{F}_2$. It is easy to check, a CNOT gate $\text{CNOT}_{i,j}$ is equivalent to the row operation which adds the $i$-th row to $j$-th row over $\mathbb{F}_2$ in the corresponding invertible matrix. By the linearity property of CNOT circuits, we can represent an $n$-qubit CNOT circuit $C$ as an invertible matrix $M \in \text{GL}(n, 2)$ [21, 15], and the $j$-th column of $M$ equals $C e_j$. We use $R(i, j)$ to denote such row adding operation in the matrix, and call the $\{i, j\}$ its index set. We take a 3-qubit CNOT circuit as an example for the matrix representation as
shown in Fig. 2. A sequence of row adding operations that transform \(M\) to \(I\) correspond to a CNOT circuit represented by \(M^{-1}\). The size optimization of CNOT circuit \(C\) is equivalent to optimizing a parameter \(t\) such that there exist index pairs \((i_1, j_1), \ldots, (i_t, j_t)\) satisfy \(M = \prod_{k=1}^{t} R(i_k, j_k)\). The summation for the input qubits is under module 2 in Sec. 3 and 4.

**Grid Graph.** In a \(d\) dimensional grid graph \(G(V, E)\) with the size of each dimension be \(m_i\). A vertex in this \(m_1 \times \cdots \times m_d\) grid can be represented as a \(d\) dimensional integer vector \((p_1, p_2, \ldots, p_d)\), where \(p_i \in [m_i]\). An \(n\)-qubit CNOT circuit is under \(m_1 \times \cdots \times m_d\) grid, which means the number of ancillas is \(m_1 \cdots m_d - n\), where \(m_1 \cdots m_d \geq n\), and the initial input \(x \in \{0, 1\}^n\) is located on any \(n\) vertices of the grid.

**Parallelized row-addition Matrices [22].** We say a matrix \(R\) is a parallelized row-addition matrix if there exists \(t \in [n], i \in [n]^t, j \in [n]^t\) such that \(i_k, j_k\)'s are \(2t\) different indices and \(R = \prod_{k=1}^{t} R(i_k, j_k)\). A parallelized row-addition matrix corresponds to a CNOT circuit with depth 1. Hence optimizing the depth of a CNOT circuit \(C\) is equivalent to optimizing a parameter \(t\) such that there exists \(t\) parallelized row-addition matrices \(R_1, \ldots, R_t\) and \(M = \prod_{k=1}^{t} R_k\).

**Several concept in graph theory.** The degree of a vertex is the number of edges that are incident to the vertex. In graph \(G\), \(\Delta\) and \(\delta\) denote its maximum and minimum degree of its vertices respectively. A graph is regular if \(\Delta = \delta\). The Steiner tree with terminals set \(S \subseteq V\), is a connected sub-graph of \(G\) with a minimum number of edges that contain all vertices in \(S\). A cut vertex is a vertex whose removal will make the connected graph disconnected.

### 3 Size optimization of a CNOT circuit

Since the quantum device is sensitive to the error and easy to be disturbed by the environment, we consider the size optimization of CNOT circuits on any connected constrained graph. We present two results for size optimization process. The first result is aiming at the near-term quantum devices under a sparse constrained graph, while the second result has a great advantage over the quantum devices with a larger number of input qubits and the denser topological structure. We then give the lower bound for the size of CNOT circuits under topological constraint. We give an experimental comparison of our size optimization algorithms and other existing algorithms in the end of this section.

#### 3.1 Size optimization algorithm for the near-term quantum devices

For the “elimination process” that transforms a matrix to identity by row operations under a constrained graph, we cannot add a row to another if their corresponding vertices are not adjacent. Given the constrained graph \(G\) and the matrix \(M \in \text{GL}(n, 2)\) corresponding to a CNOT circuit. The algorithms of Kissinger et al. [23] and Nash et al. [24] both firstly transform a given invertible matrix into an upper triangular matrix, and then transform
the triangular matrix into identity. In contrast, we propose an algorithm that eliminates
the $i$-th row and $i$-th column simultaneously for vertex $i \in V$ which is not a cut vertex.
The optimized size of the algorithm achieves $2n^2$ in the worst case on any connected
topological structure, as stated in the following theorem.

**Theorem 1.** The size of any $n$-qubit CNOT circuit can be optimized to $2n^2$ under a
connected graph $G(V, E)$ as the topological constraint.

We give a size optimization algorithm, as Algorithm ROWCOL in this section, to en-
sure the correctness of Theorem 1. Theorem 1 is more applicable for near-term quantum
devices since it has a smaller factor than the existing algorithms [23, 24].

In Algorithm ROWCOL, Steps (3-6) aim to transform the $i$-th column into $e_i$ and
Steps (7-10) aim to transform the $i$-th row into $e_i^T$. All arithmetic operations are over
the binary field $\mathbb{F}_2$. An illustrative example is shown in Example 1. The topological
constrained graph for the CNOT circuit in Example 1 is depicted in Fig. 5. The optimized
CNOT circuit for this inevitable matrix is the inverse of the joint circuit generated from
step (1) to (8).

**Algorithm 1: (ROWCOL) Near-term size optimization algorithm**

```
input : Integer $n$, matrix $M \in \mathbb{F}_2^{n \times s}$, graph $G(V, E)$ where $|V| = n$.
output: Row additions to transform $M$ into $I$.

1. for $i \in V$ which is not a cut vertex do
2.   $S = \{j|M_{ij} \neq 0\} \cup \{i\}$;
3.   Find a tree $T$ containing $S \subseteq V$ in graph $G$;
4.   Postorder traverse $T$ from $i$. When reaching $j$ with parent $k$, add row $j$ to row $k$ if
5.     $M_{ji} = 1$ and $M_{ki} = 0$;
6.   Postorder traverse $T$ from $i$, add every row to its children when reached;
7.   Let $S' \subseteq V$ that $\sum_{j \in S'} M_j = M_i + e_i$;
8.   Find a tree $T'$ containing $S' \cup i$;
9.   Preorder traverse $T'$ from $i$. When reaching $j \notin S'$, add the $j$-th row to its parent;
10.  Postorder traverse $T'$ from $i$, add every row to its parent when reached;
11.  Delete $i$ from graph $G$;
```

When we perform CNOT gates in Steps (2-3, 5-6), the number of CNOT gates is less
than the number of remaining nodes, hence the total size is at most $4(n - 1) + 4(n - 2) +
\cdots + 4 \times 1 \leq 2n^2$.

Since a connected graph must have a vertex which is not a cut vertex and the graph
keeps connected after that vertex deleted, this algorithm can be applied to any connected
graph. We can BFS (Breadth First Search) starting from any vertex in the graph and
apply the above algorithm in the BFS tree, then we delete a leaf node each time.

3.2 Size optimization algorithm for general topological graph

In this subsection, we propose an algorithm aiming at optimizing the size of CNOT circuits
for quantum system on denser constrained graph, as shown in Theorem 2.

**Theorem 2.** The size of any $n$-qubit CNOT circuit can be optimized to $O\left(\frac{n^2}{\log \delta}\right)$ under
a connected graph with minimum degree $\delta$ as the topological constraint.

**Proof.** Let $k = n/\delta$ in Theorem 3, where $\delta$ is the minimum degree of graph $G(V, E)$. It is
easy to check the summation of the degree of any $k$ vertices are greater than $n$, and thus
we have a $O\left(\frac{n^2}{\log \delta}\right)$-size CNOT circuit. 

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Example 1: An illustration of Algorithm ROWCOL. In each block, we eliminate the red row or column on the left by leverage of the right side of CNOT circuit.
This theorem is the generalization of Patel et al. [15], which optimizes the size of CNOT circuits on the complete graph and gives the optimized size of $O\left(\frac{n^2}{\log n}\right)$. The most significant difference between the techniques of Theorem 2 and the algorithms in Refs. [23, 24] is that here we eliminate several columns simultaneously instead of eliminating a single column each iteration.

It follows that the optimized size in Theorem 2 is asymptotically tight for a nearly regular graph in which all vertices have the same order of degree by Lemma 4.

Algorithm 2: (SBE) Eliminate the first $s$ columns of the given invertible matrix.

**input**: Integers $n, s$, where $s \leq \log n/2$, matrix $M \in \mathbb{F}_2^{n \times s}$, graph $G(V,E)$ where $|V| = n$.

**output**: Row additions to transform $M$ into $[e_1, \ldots, e_s]$.

1. Let $M^{(1)}$ be the first $s$ rows of $M$ and $M^{(2)}$ be the rest rows, and $T$ be the 2-approximate minimum Steiner tree for vertices $\{V_1, \ldots, V_s\}$ in $G$;
2. for $j \leftarrow 1$ to $s$ do
3.   Eliminate the $j$-th column of $M^{(1)}$ to $e_j$ under graph $T$ with Lemma 2;
4.   $l := \arg \max_{s<j \leq n} \deg(V_j)$;
5. for $j \leftarrow 1$ to $s$ do
6.   Eliminate $(l, j)$-th element $M_{l,j}$ to 0 with the $j$-th row of $M^{(1)}$ under the minimum path of the vertices $V_j$ and $V_l$ with Lemma 2;
7. $k := n/2^s$;
8. for $i \leftarrow 1$ to $2^s$ do
9.   Let $\text{Gray}(i) := i \oplus \lfloor i/2 \rfloor$ be the Gray code of $i$;
10. Let $S$ be the set containing all the rows in $M^{(2)}$ with Gray code equals $\text{Gray}(i)$;
11. Transform the binary string of row $l$ to $\text{Gray}(i)$ by adding one of the rows in $M^{(1)}$ to row $l$ under the minimum path between the vertices of these two rows with Lemma 2;
12. while $|S| \neq \emptyset$ do
13.   Let set $S'$ be random $k$ rows of $S$, and let set $R$ be the vertices of these rows in $S'$;
14.   Eliminate rows in $S'$ to 0 by row $l$ under the 2-approximate minimum Steiner tree of set $R$ in $G$ with Lemma 2;

We give an explicit algorithm to show the upper bound in Theorem 2. Recall that the construction of CNOT circuit is equivalent to construct an invertable matrix with row addition operations. Algorithm SBE (size block elimination) gives the row additions for the first $s$ columns of the invertible matrix under graph $G(V,E)$. In the algorithm, we use vertex $V_i$ to represent row $i$, also qubit $q_i$. The $i$-th row can be added to the $j$-th row means vertex $V_i$ is connected to $V_j$. We also depict the process in Fig. 3.

Let $k$ be a number such that the summation of degree of any $k$ vertices in $G(V,E)$ are greater than the total number of qubits $n$. Algorithm SBE gives a better optimized size $O\left(\frac{n^2}{\log(n/k)}\right)$ as stated in Theorem 3. Theorem 3 is the generalization of Theorem 2, here we consider the first $k$ minimum degrees of the graph instead of only one minimum degree.

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1. The Gray code for row $i$ equals $\text{Gray}(i)$. 

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Theorem 3. For any \( n \)-qubit CNOT circuit and connected graph \( G(V, E) \) as the topological structure of quantum system, for any integer \( k \) such that the summation of the degree of any \( k \) vertices are greater than \( n \), there exists an algorithm that outputs an equivalent \( O\left(\frac{n^2}{\log(n/k)}\right) \) size CNOT circuit on the constrained graph \( G \).

Proof. Theorem 3 holds by Lemma 1 and Lemma 3.

Lemma 1 ensures the efficiency of our optimization algorithm, by which we can eliminate one row in one step on average.

Lemma 1. Given connected graph \( G(V, E) \), for any integer \( k \) such that the summation of the degree of any \( k \) vertices are greater than \( n \), the minimum Steiner tree for any \( k \) vertices in \( G \) is less than \( 5k \).

This Lemma can be obtained directly by applying the technique in Theorem 2.4 of Ali et al. [25]. The detailed proof of this lemma is in Appendix A. The core idea of the proof is that two vertices share no common neighbors if the distance between them equals three. This lemma needs exponential cost to give a minimum Steiner tree, hence we replace it by the 2-approximate minimum Steiner tree in Algorithm SBE, as stated in the following corollary.

Corollary 1. Given connected graph \( G(V, E) \), for any integer \( k \) such that the summation of the degree of any \( k \) vertices are greater than \( n \), the 2-approximate minimum Steiner tree for any \( n \) vertices in \( G \) is less than \( 10k \).

The following lemma serves for Lemma 3. This lemma can be obtained directly from the optimization process of Nash et al. [24], by which we can add the value of a qubit to the target qubits and keep the values of the other qubits the same.

Lemma 2. [24] For \( S \subseteq [n - 1], y \in \{0, 1\}^n \), where \( y_j = x_j + x_n \) if \( j \in S \), and \( y_j = x_j \) otherwise. The transformation \( |x_1\rangle \cdots |x_n\rangle \rightarrow |y_1\rangle \cdots |y_n\rangle \) on any connected graph can be implemented by CNOT gates with size \( O(n) \).

By this lemma, we can eliminate one column of the matrix with \( O(n) \) row additions.

Lemma 3. There is a polynomial time algorithm where for any CNOT circuits and integer \( k \leq n \), connected graph \( G(V, E) \) with \( O(k) \)-size 2-approximate Steiner tree of any \( k \)-vertex set, the algorithm outputs an equivalent CNOT circuit with \( O\left(\frac{n^2}{\log(n/k)}\right) \) size on constrained graph \( G \).

Proof. Let \( s = \log(n/k)/2 \). Given \( n \)-qubit CNOT circuit \( M \in \text{GL}(n, 2) \), the following algorithm uses \( O(n^2/s) \) row additions to transform \( M \) to \( I \) and thus gives an equivalent \( O(n^2/s) \) size CNOT circuit. The algorithm starts with dividing \( M \) into \( n/s \) blocks \( [M_1 \cdots M_{n/s}] \), where \( M_i \in \mathbb{F}_2^{n \times s} \). Similarly let \( I = [I_1 \cdots I_{n/s}] \). Next transform \( M_j \) to \( I_j \) for all of \( j \in [n/s] \).

Algorithm SBE states how to transform \( M_1 \) to \( I_1 \) with row additions. The process of transforming \( M_j \) to \( I_j \) for \( j > 1 \) are almost the same with the process of transforming \( M_1 \) to \( I_1 \), except in step (1), we set \( M^{(1)} \) be the \((j - 1)s + 1\)-th to \( js \)-th rows for input matrix \( M_j \), and \( M^{(2)} \) be the rest rows.

Now we prove the row additions is indeed \( O(n^2/s) \). Since any \( k \) vertices has a \( O(k) \)-size 2-approximate minimum Steiner tree, the number of vertices in 2-approximate minimum Steiner trees in Steps (2) and (17) in Algorithm SBE are both \( O(k) \). Hence the number of row additions is less than

\[
\frac{O(s \cdot k)}{\text{Steps (3-5)}} + \frac{O(s \cdot k)}{\text{Steps (7-9)}} + \frac{O(2^s \cdot k)}{\text{Step (14)}} + \frac{O(n)}{\text{Step (17)}} = O(n)
\]

for \( k \leq n \). Thus we need in total \( n/s \times O(n) = O\left(\frac{n^2}{s}\right) \) row additions.
The optimized size in Theorem 3 is asymptotically tight when \( k = n^\varepsilon \) for \( 0 \leq \varepsilon < 1 \) since \( \Omega \left( \frac{n^2}{\log n} \right) \) is the lower bound for any constrained graph by Theorem 4.

### 3.3 Lower bound for size optimization

The best lower bound of unrestricted CNOT circuit synthesis is \( \Omega \left( \frac{n^2}{\log n} \right) \) size by Patel et al. [15]. This lower bound is obtained by counting the number of distinct CNOT circuit with the given number of CNOT gates, which also implies the same lower bound \( \Omega \left( \frac{n^2}{\log n} \right) \) for CNOT circuit synthesis on a constrained graph. We say the quantum circuit \( \hat{U} \in \mathbb{C}^{2^n \times 2^n} \) is an \( \varepsilon \)-approximation for the quantum circuit \( U \in \mathbb{C}^{2^n \times 2^n} \) if \( \| \hat{U} - U \|_2 \leq \varepsilon \).

Here we prove a tighter lower bound as stated in Theorem 4. Note that what we are discussing here is a lower bound for general circuits. The technique of the proof is inspired by the counting method from Christofides [26] and Jiang et al. [22].

Before giving a lower bound for general 2-qubit circuit, we firstly give the same lower bound for “CNOT circuit” in Lemma 4. Next we generalize the “equivalent CNOT circuit” into any 2-qubit gates with \( \varepsilon < \frac{1}{\sqrt{2}} \) approximation as in Theorem 4.

**Lemma 4.** For any connected graph \( G(V, E) \) as the topological structure of quantum system, there exists some \( n \)-qubit CNOT circuits that any equivalent CNOT circuits need \( \Omega \left( \frac{n^2}{\log \Delta} \right) \) size of CNOT gates on graph \( G \), where \( \Delta \) is the maximum degree of the constrained graph.

Before giving the proof of Lemma 4, we first define the canonical CNOT circuit.

**Definition 1** (Canonical CNOT circuit). For any \( n \)-qubit CNOT circuits with \( k \) CNOT gates, which can be represented as a sequence of elementary row operations, \( R_1, R_2, \ldots, R_k \). We say it is canonical if and only if the sequence can be partitioned into several non-empty blocks \( G_1, G_2, \ldots, G_s \) and these blocks satisfies the following properties,

1. For \( 1 \leq i \leq s \), the index set of matrix in block \( G_i \) is disjoint with each other;
2. For \( 2 \leq i \leq s \), for every matrix in the block \( G_i \), there exists at least one element of its index set belonging to the index set of some matrix in the previous block \( G_{i-1} \).

Intuitively, the canonicity means that CNOT gates in the same block can be executed simultaneously and no CNOT gate can be put into the previous block. It is not hard to prove any CNOT circuit can be transformed into an equivalent canonical CNOT circuits within finite steps and the readers can refer to [26] for specific proof. Next, we will show the upper bound of the number of distinct canonical CNOT circuits as stated in 5.

**Lemma 5.** Given the constrained graph \( G(V, E) \), there are at most \( 8k^4 \Delta^k 2^n \log n \) different canonical \( n \)-qubit CNOT circuits with \( k \) CNOT gates, where \( \Delta \) is the maximum degree of the graph.
Proof. For any $n$-qubit CNOT circuits with $k$ gates $R_1, R_2, \ldots, R_k$, we denote its canonical form by $\{G_1, G_2, \ldots, G_s\}$, in which the length of the blocks are respectively $r_1, r_2, \ldots, r_s$. We first consider the number of different partitioning ways, i.e., different choices of $r_1, r_2, \ldots, r_s$. It’s not hard to see the number is $2^{k-1}$ for any combination from set $[k-1]$ being a partition of set $[k]$.

Next, we derive the upper bound of the number of distinct canonical forms, given the specific partitioning $r_1, r_2, \ldots, r_s$.

For block 1, the index set of each matrix are required to be disjoint. Thus, there are at most $\binom{n}{r_1}$ different combinations of $r_1$ indices and there are at most $\Delta$ choices for another index of a matrix since the CNOT gates can only act on the nearest neighbour qubits and the maximum degree of the graph is $\Delta$. All this leaves for block 1 at most $(2\Delta)^{r_1}\binom{n}{r_1}$ possible combination, where the factor 2 is due to the different order of the indices.

Subsequently, for block 2, each index set of matrix has at least one element intersect with that of block 1, so we need to choose $r_2$ index from the index set of block 1. The number of possible combination is $\binom{2r_1}{r_2}$. Similar to block 1, there are at most $(2\Delta)^{r_2}\binom{2r_1}{r_2}$ possible combinations.

For the same reason, block $i$ has at most $(2\Delta)^{r_i}\binom{2r_{i-1}}{r_i}$ possible combinations. In all, the number of distinct canonical forms is at most

$$2^k \Delta^k \binom{n}{r_1} \binom{2r_1}{r_2} \cdots \binom{2r_{s-1}}{r_s}. \tag{1}$$

Since $\binom{n}{r_1} < n^{r_1}/r_1! < 2^{n\log n}/r_1!$, and $\binom{2r_i}{r_{i+1}} < 2^{r_{i+1}}r_{i+1}/r_{i+1}!$, we can relax the upper bound to

$$4^k \Delta^k 2^{n\log n} r_1!r_2!\cdots r_s! \tag{2}.$$

From the Stirling formula, the following inequality holds

$$r_1!r_2!\cdots r_s! \geq \left(\frac{r_1}{e}\right)^{r_1} \left(\frac{r_2}{e}\right)^{r_2} \cdots \left(\frac{r_s}{e}\right)^{r_s}. \tag{3}$$

And then applying the rearrangement inequality to obtain

$$r_1^{r_1}r_2^{r_2}\cdots r_s^{r_s} \geq r_1^{r_1}r_2^{r_2}\cdots r_s^{r_s} \geq r_1^{r_1}r_2^{r_2}\cdots r_{s-1}^{r_{s-1}}. \tag{4}$$

The last inequality holds for $r_s \geq 1$ and $r_1 \geq 1$. Combining Eq. (3) and (4), we have the following inequality,

$$r_1!r_2!\cdots r_s! \geq e^{-k} r_1^{r_1}r_2^{r_2}\cdots r_{s-1}^{r_{s-1}}. \tag{5}$$

Therefore, we can obtain the desired upper bound by multiplying the number of different partitioning ways.

$$8^k e^k 2^{n\log n}. \tag{6}$$

In the following, we give the proof of Lemma 4.

Proof of Lemma 4. Since the number of $n$-qubit CNOT circuits equals the number of invertible matrix $M \in \text{GL}(n, 2)$, there are at least $2^{n(n-1)/2}$ distinct $n$-qubit CNOT circuits. And by Lemma 5, the upper bound of the number of distinct $n$-qubit CNOT circuits with
$k$ CNOT gates is at most $8^k e^k \Delta^k 2^{n \log n}$. Thus if we want to construct all of the $n$-qubit CNOT circuits, $k$ must satisfies

$$k \geq \frac{n(n-1)/2 - n \log n}{\log \Delta + 3 + \log e}.$$  \hspace{1cm} (7)

In other words, there exists some $n$-qubit CNOT circuit, any equivalent CNOT circuit need $\Omega \left( \frac{n^2}{\log \Delta} \right)$ size of CNOT gates.

We can generalize the lower bound of Lemma 4 to any two qubit circuits, as the following theorem.

**Theorem 4.** For any connected graph $G(V,E)$ as the topological structure of quantum system, there exists some $n$-qubit CNOT circuits that any $\varepsilon < 1/\sqrt{2}$-approximation 2-qubit circuits need $\Omega \left( \frac{n^2}{\log \Delta} \right)$ size of CNOT gates on graph $G$, where $\Delta$ is the maximum degree of the constrained graph.

**Proof.** For a real number $a \in [-1,1]$, let the $\eta$ discretization of $a$ be $a^\eta = \eta \lfloor a \eta \rfloor$. Then there are in total $\frac{\eta}{\eta}$ different $\eta$ discretizations for all the continuous number $a$ in the interval $[-1,1]$ with $|a^\eta - a| \leq \eta$. Hence there are in total $\left( \frac{\eta}{\eta} \right)^{32}$ different $\eta$ discretizations for all the 2-qubit unitaries $U$ in $\mathbb{C}^{4 \times 4}$, and the error $\|U^\eta - U\| \leq 2\eta$.

In the following we prove that when $\eta = \frac{\varepsilon}{2\eta}$ and $\varepsilon < \frac{1}{\sqrt{2}}$, the $\eta$ discretizations of any two different CNOT circuits with size $k$ are different. Since for any two different CNOT circuits $U_f, U_g$ with size $k$ such that

$$U_f \ket{x} \neq U_g \ket{x},$$

we have

$$\|U_f \ket{x} - U_g \ket{x}\|_2 = \sqrt{2}.$$

By the definition of $U_f^\eta$, we have

$$\left\| \left( U_f^\eta - U_f \right) \ket{x} \right\|_2 \leq 2k\eta \leq \varepsilon.$$

Similarly we have $\| \left( U_g^\eta - U_g \right) \ket{x} \|_2 \leq \varepsilon$. Since our approximation needs to be $\varepsilon < \frac{1}{\sqrt{2}}$ close to the original solution, which implies

$$U_f^\eta \ket{x} \neq U_g^\eta \ket{x}.$$  \hspace{1cm} (8)

Hence we have an upper bound for the number of 2-qubit circuit with $\varepsilon < \frac{1}{\sqrt{2}}$ approximation to the all of the possible $k$ CNOT gates

$$8^k e^k \Delta^k 2^{n \log n} \left( \frac{2}{\eta} \right)^{32k}$$

with error $2k\eta$. Since Eq. (8) is greater than all possible CNOT circuits, which is greater than $2^{n(n-1)/2}$, then we have $k = \Omega \left( \frac{n^2}{\log \Delta} \right)$. \qed
3.4 Experimental results of Algorithm ROWCOL

In this subsection, we give the comparison of the experimental simulation of Algorithm ROWCOL and algorithms in Refs. [23, 24]. The simulation are ran under IBM Q20 graph and T-like graph (T20). The topological structure of IBMQ20 and T20 are depicted in Fig. 4. We choose different size of original circuits, from 20 to 800 in the experiment, where the number of qubit is 20. For each input size of original circuit, 200 CNOT circuits are random sampled. All these three algorithm, ROWCOL and algorithms in [23, 24], are used to optimize these CNOT circuit. The average optimized size of 200 random CNOT circuits are used to determine the quality of the algorithm. Since we want to show our algorithm performs well in most kinds of CNOT circuits, not only for some specific kinds, we randomly sample CNOT circuits. To give a more explicit comparison, we simulate these algorithms on two specific CNOT circuits. The simulation results of our algorithm are superior to the other algorithms in both cases. In this subsection, we sample a random CNOT circuit by randomly sampling two adjacent qubits and adding a CNOT gate until the size meets the requirement. The result shows that our algorithm can generate the smallest CNOT circuit in 82.3% of the input circuits.

In Fig. 6, we compare the optimized size of Algorithm ROWCOL with algorithms in Refs. [23, 24]. The y axis shows the average optimized size of the 200 random circuits with the same input size after performing these algorithms. The experimental result of Algorithm ROWCOL is significantly superior to the algorithm of Nash et al. for all of physical devices, which fit the analysis since their algorithm has a larger factor. Our algorithm also performs better in most generated random circuits than the algorithm of Kissinger et al. for the constrained graph with a Hamiltonian path, as shown in Fig 6 (a). In particular, we have a better optimized size for 82.3% random circuits on IBMQ20, 99.9% random circuits on T20. When the graph does not have a Hamiltonian path, our algorithm has obvious advantages than Kissinger et al. [23] (as in Fig. 6 (b)).

The above optimized result for the random generated CNOT circuits shows the great advantages of Algorithm ROWCOL for general CNOT circuits. In the following, we perform Algorithm ROWCOL and Algs. in Refs. [23, 24] on two specific CNOT circuits to show the applicability of our algorithm. The comparison results are coincident with
The size of the original circuit

Optimized size

(a) IBMQ20

(b) T20

Figure 6: The experimental results of Algorithm ROWCOL, algorithms in [24] and [23] under topological constraint graphs: (a) IBM Q20 and (b) T20. As a contrast, we also draw the curve $y = x$ in the figure.

The first example is a staircase CNOT circuit (as shown in Fig. 5 (a)). The staircase CNOT circuit is a crucial part in the quantum circuits of error detection and correction [27, 28, 29], simulation of quantum chemistry [30, 31], Hamiltonian simulation [32] and near-term variational algorithms [33]. Here we simulate Algorithm ROWCOL for the particular staircase CNOT circuit in Fig. 5 (a) under the topological constraint in Fig. 5 (b). Fig. 7 gives a comparison of the optimized circuit between Algorithm ROWCOL and Algorithms in Refs. [23, 24]. The optimized size of Algorithm ROWCOL is 3, however, algorithms in Ref. [23] and Ref. [24] need 7 and 15 CNOT gates respectively.

The second example is a SWAP circuit (as shown in Fig. 5 (b)), which is widely used in quantum circuit implementation of general unitaries. Fig. 8 gives the optimized circuits of Algorithm ROWCOL and algorithms in Ref. [23, 24] for the SWAP circuit in Fig. 5 (b) under the constrained graph in Fig. 5 (c).

Figure 7: Optimized circuits for the staircase CNOT circuit in Fig. 5 (a) under the constrained graph in Fig. 5 (c). The optimized size of Algorithm ROWCOL, Refs. [23] and [24] are 3, 7 and 15 respectively, as shown in (a), (b) and (c).

4 Depth optimization of a CNOT circuit

Due to decoherence in the near-term quantum devices, the quantum computing task should be finished in a short time. Although Algorithm ROWCOL can also be used to optimize the depth of any given CNOT circuit, the depth of the optimized circuit is almost the same as the size. To our knowledge, the ancillas can reduce the depth of a circuit to a great extent. A bunch of work aimed to reduce the depth of CNOT circuits
via designing optimized circuits with some ancillas [21, 22, 34]. In this section, we first propose a depth optimization algorithm under grid with limited ancillas, and then show the great improvements of the optimized depth compared to other existing algorithms by numerical experiment.

### 4.1 Depth optimization algorithm for the near-term quantum devices

Here we optimize the depth of CNOT circuits via bringing in limited ancillas on a 2 dimensional grid. We then generalize the result to any constant $d$ dimensional grid.

**Theorem 5.** Given $m_1 m_2 - n$ ancillas, the depth of any $n$-qubit CNOT circuit can be optimized to $O \left( \frac{n^2}{\min\{m_1, m_2\}} \right)$ under the $m_1 \times m_2$ grid where $3n \leq m_1 m_2 \leq n^2$.

This theorem gives a trade-off of depth and ancillas for CNOT circuits under grid topological structure. The depth can be optimized to $O(n)$ when $m_1 = m_2 = n$. It is easy to check there exists a CNOT circuit, the optimized depth is $\Omega(n)$ on $n \times n$ grid. Hence our optimized depth is asymptotically tight in this case. The main idea for Theorem 5 is to divide the output of CNOT circuit into several intermediate results conserving in the ancillas. Then combine the intermediate results to generate the output and restore the ancillas.

Before giving the algorithm to show the correctness of Theorem 5, we would like to cast two lemmas which show how to copy and add inputs under the $d$ dimensional grid, and one can easily check the lower bound for these operation on $(m_1 \times m_2 \times \cdots \times m_d)$ grid is also $\Omega \left( \sum_{j=1}^d m_j \right)$.

**Lemma 6.** Let $i \in [m]$, integer $m > 1$ and $\prod_{i=1}^d m_i = m$. The copy operation $|0\rangle^\otimes(i-1)|x\rangle|0\rangle \rightarrow |x\rangle^m$ on $(m_1 \times m_2 \times \cdots \times m_d)$ grid with $m$ vertices can be implemented by CNOT gates with depth at most $O \left( \sum_{j=1}^d m_j \right)$, where $x \in \{0, 1\}$.

The following lemma gives a tight $O \left( dm^{1/d} \right)$ depth construction for addition operation on $d$ dimensional grid.

**Lemma 7.** Let $S \subseteq [m-1]$, integer $m > 1$, $y = \sum_{i \in S} x_i \mod 2$, and $\prod_{i=1}^d m_i = m$. The addition operation $|x_1\rangle \cdots |x_{m-1}\rangle|0\rangle \rightarrow |x_1\rangle \cdots |x_{m-1}\rangle|y\rangle$ on the above grid can be implemented by CNOT gates with depth at most $O \left( \sum_{i=1}^d m_i \right)$, where $x_i \in \{0, 1\}$ and $|y\rangle$ can be arbitrary vertex in the grid.

We prove this lemma by constructing a tree rooted at vertex $y$ with depth $O(\sum_{i=1}^d m_i)$ in the $d$ dimensional grid, then we divide the tree into some disjoint path to parallelize the CNOT gates. See Appendix B for the proofs of Lemmas 6,7.
In the following, we give the algorithm for Theorem 5. Let \( y := y_1 \cdots y_n \in \{0, 1\}^n \) be the output, then \( y_i = \sum_{j} M_{ij} x_j \). We first divide the summation into several parts. Let \( z_{ij} := \sum_{k=(j-1)m_1+1}^{jm_1} M_{ik} x_k \) where \( i \in [n] \) and \( j \in [n/m_1] \) (Here we suppose \( n/m_1 \) is an integer. It is easy to generalize it to the general case.). It is easy to check that the \( i \)-th output qubit \( y_i = \sum_j z_{ij} \). Let \( s := m_2 - 2n/m_1 \). Let the coordinate \((i, j)\) represent the \( i \)-th row and \( j \)-th column of the \( m_1 \times m_2 \) grid.

Algorithm \textbf{DepAncGrid} implements the transformation

\[
(x, 0^{\otimes(m-2n)}, 0^{\otimes n}) \xrightarrow{U_M} (x, 0^{\otimes(m-2n)}, Mx).
\]

Hence, the transformation \((x, 0^{\otimes(m-n)}) \rightarrow (Mx, 0^{\otimes(m-n)})\) can be implemented by first performing

\[
(x, 0^{m-2n}, 0^n) \xrightarrow{U_M} (x, 0^{m-2n}, Mx),
\]

and then performing

\[
(x, 0^{m-2n}, Mx) \xrightarrow{U_{M^{-1}}} (x \otimes M^{-1} Mx, 0^{m-2n}, Mx) = (0^{m-n}, y).
\]

Finally, move \( y_j \) to the first \( n/m_1 \) columns for all \( j \) by SWAP gates. Hence we have an equivalent paralleled CNOT circuit for any given CNOT circuit. We depict this process in Fig. 9.

The total number of paralleled operations in Algorithm \textbf{DepAncGrid} equals

\[
c \frac{n}{m_1} \left( \frac{n}{s} (m_1 + m_2) \right) = O \left( \frac{n^2}{\min(m_1, m_2)} \right),
\]

for a suitable constant \( c \).

Theorem 5 can be generalized to constant \( d \) dimensional grid. In specific, the depth of any CNOT circuit can be optimized to \( O \left( \frac{n^2}{\min(m_1, \cdots, m_d)} \right) \) under \( m_1 \times \cdots \times m_d \) grid, where \( d \) is a constant and \( 3n \leq m_1 \cdots m_d \leq n^2 \). Let \( m \) be the third largest value of \( \{m_1, \cdots, m_d\} \).

4.2 Experimental results of Algorithm \textbf{DepAncGrid}

In this subsection, we give the experimental simulation of Algorithm \textbf{DepAncGrid}. We compare the optimized depth of Algorithm \textbf{DepAncGrid} with all of existing size optimization algorithms on grid graph mentioned previously. To show the performance of...
Algorithm 2: DepAncGrid: Depth optimization algorithm under $m_1 \times m_2$ grid

**input**: Matrix $M \in \{0, 1\}^{n \times n}$, $m_1 \times m_2$ grid, $s := m_2 - 2n/m_1$.

**output**: Optimized CNOT circuit.

1. Place input $x_1, \ldots, x_n$ in the first $n/m_1$ columns sequentially of the grid;
   
   // $x_1, \ldots, x_{m_1}$ in the first column, and so on, as in Fig. 9

2. for $l \leftarrow 1$ to $n/m_1$
do
   
   3. Copy all of $x_i$ in the $l$-th column to the columns $j$ for $n/m_1 + 1 \leq j \leq n/m_1 + s$ in the same row as $x_i$;

   4. for $j \leftarrow s$ down to 2 do

   5. if $M_{j,i}$ equals 0 then

   6. Perform CNOT$_{a,b}$, where qubit $a$ is in coordinate $(i, n/m_1 + j - 1)$ and $b$ is in coordinate $(i, n/m_1 + j)$ for $i \in [m_1]$ in parallel;

   7. for $1 \leq j \leq n/s$ do

   8. Add all values of each column $k$ to the last row to generate $z_{k,1}$ in the coordinate $(m_1, n/m_1 + k)$;

   9. Add $z_{(j-1)s+1,1}, \ldots, z_{js,1}$ to the mirror symmetric coordinate;

10. Restore the ancillas in columns $j$ for $n/m_1 + 1 \leq j \leq n/m_1 + s$;

these algorithms, different size of $n \times n$ dimensional grids ranging from 4 to 11 are selected in this experiment. For one grid, we firstly randomly sample 200 different CNOT circuits, and then run all these algorithms under this condition. The method to sample a random CNOT circuit here is: (1). Randomly sample an $n \times n$ 0-1 matrix by randomly selecting a “0” or “1” in each position; (2). Determine whether the matrix sampled in (1) is invertible, if not, return to (1), otherwise accept the matrix as a random CNOT circuit.

The comparison results is depicted in Fig. 10, including the optimized depth of Algorithms ROWCOL, DepAncGrid, and algorithms in Refs. [23, 24] on grid graph. In particular, here Algorithm DepAncGrid needs $n^2$ qubits and other algorithms only need $n$ qubits. The $y$ axis shows the average depth of the optimized circuit. In consideration of reducing the impact of the different Hamiltonian paths chosen in Ref. [23], we choose two different Hamiltonian paths to synthesis the same CNOT circuit. The comparison results show Algorithm DepAncGrid has a significant improvement for the optimized depth as the number of qubits increasing. Theoretical, the depth of CNOT circuit generated by Algorithm DepAncGrid equals $O(n)$, while $O(n^2)$ for other algorithms.

This experimental result shows that the depth of CNOT circuit can be greatly reduced for the ancillas free quantum system.

## 5 Experimental result on IBMQ

In this section, we test the performance of our optimized CNOT circuits on IBM devices. We implement a staircase CNOT circuit and an Add CNOT circuit, which have wide applications in error correction [3], variational algorithms [3, 35] and quantum chemistry [36, 37].

We leverage IBMQ devices (ibmq_athens and ibmq_5_yorktown) as the topological constrained graphs [38], as shown in Fig. 14 of the Appendix. In Fig. 12 (a), we give the staircase circuit without considering the topological constrained graph, with input $|\phi\rangle = \frac{|0\rangle + |1\rangle}{\sqrt{2}} |0\rangle$ and $\frac{|0\rangle + |1\rangle}{\sqrt{2}} |0\rangle$. We perform the circuit on IBMQ with the mapping CNOT circuit provided by the ROWCOL algorithm in Fig. 12 (b). There is a layer of $H$ gates
Figure 10: The comparison of optimized depth of these algorithms in the grid graph. We compare the performance of different synthesis algorithms in $n \times n$ grid. We use two different numbering of the grid: (a) numbering row by row from the first row to the last row, (b) numbering from the inside to the outside in the form of a grid.

6 Discussion and outlook

Optimization of size/depth of the quantum circuit with topological constraints is one of the main challenges in near-term quantum computing [39, 40, 41]. In this paper, we propose two main size/depth optimization algorithms on the topological constrained graph. The experimental results show our algorithms have better performances compared to the existing optimization algorithms.

In specific, we can optimize any CNOT circuits to $2n^2$ size on any connected graph, the order is tight when the constrained graph is a simple path. We also give an algorithm that takes more features of the graph into accounts and gives a better upper bound for the specific class of graphs. In specific, for the connected graph which has minimum degree $\delta$, any $n$-qubit CNOT circuits can be optimized to $O\left(\frac{n^2}{\log \delta}\right)$ size on such graph.
**Figure 11:** The comparison of the ROWCOL algorithm, IBM optimization algorithm on IBM devices, and the classical simulation result. (a) For the CNOT circuit in Fig. 12 (a) under ibmq_athens device. (b) For the CNOT circuit in Fig. 13 (a) under ibmq_5_yorktown device.

**Figure 12:** Mapping the staircase CNOT circuit to the topological 1D grid graph. (a) Staircase CNOT circuit with input state $|0\rangle + |1\rangle \sqrt{2}$ $|0\rangle |0\rangle + |1\rangle |1\rangle$. (b) A layer of $H$ gates, followed by a block of CNOT circuit, which is equivalent to the CNOT circuit of (a), and can be performed on the ibmq_athens device (a 1D grid). The input state in (b) equals $|0\rangle ^{\otimes 5}$.

**Figure 13:** Mapping the CNOT Add circuit to ibmq_5_yorktown device. (a) CNOT Add circuit with input state $|0\rangle + |1\rangle \sqrt{2}$ $|0\rangle + |1\rangle \sqrt{2}$ $|0\rangle |0\rangle + |1\rangle |1\rangle$. (b) A layer of $H$ gates, followed by a block of CNOT circuit, which is equivalent to the CNOT circuit of (a), and can be performed on the ibmq_5_yorktown device. The input state in (b) equals $|0\rangle ^{\otimes 5}$.
We also prove the order is tight for a regular graph. Algorithm SBE further indicates the size of any \( n \)-qubit CNOT circuits can be optimized to \( O\left(\frac{n^2}{\log(n/k)}\right) = O\left(\frac{n^2}{\log \delta}\right) \) on the constrained graph where the average degree of any \( k \) vertex set is greater than \( n/k \) for the constrained graph. The maximum degree of the vertices equals 4 for current quantum superconducting devices \([38, 5, 4]\), hence the optimized size equals \( O(n^2) \). The lower bound of the size is in the same order for these grid-type devices. In the end, we consider a special constrained graph \( m_1 \times m_2 \) grid. We show that any \( n \)-qubit CNOT circuits can be optimized to \( O\left(\frac{n^2(m_1 + m_2)}{m_1 \cdot m_2}\right) \) depth on this grid, where \( 3n \leq m_1 \cdots m_d \leq n^2 \). This optimized result can be easily generalized to any constant \( d \) dimensional grid. The dimensions for corresponding grid of current quantum superconducting devices \([38, 5, 4]\) are \( d \in \{1, 2\} \).

Note that the 65-qubit quantum superconducting devices proposed by IBMQ \([38]\) is not exactly a grid, nevertheless, it is a sub-graph of a grid. We can still perform Algorithm DepAncGrid on the expanded grid by leverage of SWAP gates to implement the CNOT gate for two vertices which are not connected in the sub-graph. Another avenue is to construct a new virtual 2D grid, and convert the single CNOT gate in the virtual grid to a series of CNOT gates in the real devices. We can ensure the additional cost of CNOT gates to be bounded to a constant factor of the original one due to its sub-grid structure.

We list two open problems for the optimization of CNOT circuits on the constrained graph. (1) Is there any improved size optimization algorithm for some more specific structure under the constrained graph? (2) If there are no ancillas, can we give some better results for the depth optimization of CNOT circuits on \( m_1 \times \cdots \times m_d \) grid for constant \( d \)?

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A Proof of Lemma 1

Proof of Lemma 1. Denote $T_k(G) = \max_{|S|=k,S \subseteq V} T_G(S)$, where $T_G(S)$ is the size (the number of vertices) of the minimum Steiner tree for vertex set $S$ in $G$.

Let $S = \{u_1, \cdots, u_k\} \subseteq V$ and $A$ be an empty set. In a connected graph $G(V, E)$, let the distance between two vertices be the number of edges in a shortest path that connect them. Let $d(i,j)$ denote the distance between vertex $i$ and $j$ in Graph $G$, $d(A,v)$ denote the minimum distance between vertex $v$ and set $A$.

Firstly put $u_1$ into set $A$, and then put all of $v \in V$ such that $d(A,v) = 3$ into $A$. That is,

- $d(v_i, v_j) \geq 3$ if $v_i, v_j \in A$.
- $d(A,v_i) \leq 2$ if $v_i \notin A$.

Let $A' = \{a_1, \cdots, a_k\}$ be a set such that the element $a_i \in A'$ is a vertex in set $A$ and closest to $u_i$ in $S$. By the construction of $A$, we have $T_G(\{a_1, \cdots, a_k\}) \leq 3(|A| - 1) + 1 \leq 3|A|$.

By the definition of $G$, for any $k$ vertex in $G$, the summation of their degrees are greater than $n$. On the other hand, since there are no common neighbors for any two vertex in set $A$, $\sum_{v \in A} d(v) + |A| \leq n$, thus we have $|A| < k$.

Therefore,

$$T_G(S) \leq T_G(\{a_1, \cdots, a_k\}) + \sum_{j=1}^{k} T_G(a_j, u_j)$$

$$\leq 3|A| + 2(k - 1)$$

$$\leq 5k$$

$\square$
B Algorithms for copy operation and add operation

Proof of Lemma 6. Each qubit in the hypergrid has a $d$ dimensional grid coordinate $(p_1, p_2, \ldots, p_d)$, $p_i \in [m^{1/d}]$. We may assume $q_1$ in $(1,1,\ldots,1)$ without loss of generality, otherwise $q_1$ can be moved to $(1,1,\ldots,1)$ by at most $dn^{1/d}$ SWAP gates, where every SWAP gate can be implemented by 3 CNOT gates. We can copy $q_1$ to all other vertices by following operations, we use ‘$\leftarrow$’ to denote CNOT from qubit at right coordinate to left coordinate.

1. for $k$ from 2 to $m_1$, $(k,1,\ldots,1) \leftarrow (k-1,1,\ldots,1),$
2. for every $p_1 \in [m_1]$, for $k$ from 2 to $m_2$, $(p_1,k,1,\ldots,1) \leftarrow (p_1,k-1,1,\ldots,1),$
3. for every $p_1 \in [m_1], p_2 \in [m_2]$, for $k$ from 2 to $m_3$, $(p_1,p_2,k,1,\ldots,1) \leftarrow (p_1,p_2,k-1,1,\ldots,1),$

\ldots

\textbf{d.} for every $p_i \in [m_i], 1 \leq i \leq d-1$, for $k$ from 2 to $m_d$, $(p_1,\ldots,p_d-1,k) \leftarrow (p_1,\ldots,p_d-1,k-1),$

we copy $q_1$ to all other vertices by above operations, operations in the $i$-th item can be parallelized to $m_i - 1$ depth, hence the total depth is $O(\sum_{i=1}^d m_i)$. \hfill\Box

Proof of Lemma 7. By the same argument in proof of Lemma 6, we may assume the $n$-th vertex in $(1,1,\ldots,1)$ without loss of generality. We can implement the addition operation as follows.

1. For $k$ from 2 to $m_1$, if $(k,1,\ldots,1) \notin S$, then $(k-1,1,\ldots,1) \leftarrow (k,1,\ldots,1),$
2. For every $p_1 \in [m_1]$, for $k$ from 2 to $m_2$, if $(p_1,k,1,\ldots,1) \notin S$, then $(p_1,k-1,1,\ldots,1) \leftarrow (p_1,k,1,\ldots,1),$
3. For every $p_1 \in [m_1], p_2 \in [m_2]$, for $k$ from 2 to $m_3$, if $(p_1,p_2,k,1,\ldots,1) \notin S$, then $(p_1,p_2,k-1,1,\ldots,1) \leftarrow (p_1,p_2,k,1,\ldots,1),$

\ldots

\textbf{d.} For every $p_i \in [m_i], 1 \leq i \leq d-1$, for $k$ from 2 to $m_d$, if $(p_1,p_2,\ldots,p_d-1,k) \notin S$, then $(p_1,p_2,\ldots,p_{d-1},k-1) \leftarrow (p_1,p_2,\ldots,p_{d-1},k),$

\textbf{d+1.} For every $p_i \in [m_i], 1 \leq i \leq d-1$, for $k$ from $m_d$ to 2, $(p_1,\ldots,p_d-1,k) \leftarrow (p_1,\ldots,p_d-1,k-1),$

\ldots

\textbf{2d-2.} For every $p_1 \in [m_1], p_2 \in [m_2]$, for $k$ from $m_3$ to 2, $(p_1,p_2,k-1,1,\ldots,1) \leftarrow (p_1,p_2,k,1,\ldots,1),$

\textbf{2d-1.} For every $p_1 \in [m_1]$, for $k$ from $m_2$ to 2, $(p_1,k-1,1,\ldots,1) \leftarrow (p_1,k,1,\ldots,1),$

\textbf{2d.} For $k$ from $m_1$ to 2, $(k-1,1,\ldots,1) \leftarrow (k,1,\ldots,1),$

we get the sum of all vertices, except the vertices not in $S$ added twice. The arithmetic operations are over $\mathbb{F}_2$, so $y = \sum_{i \in S} x_i$. We can recover $x_1, x_2, \ldots, x_{n-1}$ by reversing above operations which are not related to $(1,1,\ldots,1)$. The operations in the $i$-th item and $(2d + 1 - i)$-th item can be parallelized to $m_i - 1$ depth, where $1 \leq i \leq d$, hence the total depth is $O(\sum_{i=1}^d m_i).$ \hfill\Box

C The topological graphs for the IBM devices for our experiments

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Figure 14: The topological constrained graph for (a) ibmq_athens device, and (b) ibmq_5_yorktown device.