MF-Net: Compute-In-Memory SRAM for Multibit Precision Inference using Memory-immersed Data Conversion and Multiplication-free Operators

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Abstract—We propose a co-design approach for compute-in-memory inference for deep neural networks (DNN). We use multiplication-free function approximators based on $\ell_1$ norm along with a co-adapted processing array and compute flow. Using the approach, we overcome many deficiencies in the current art of in-SRAM DNN processing such as the need for digital-to-anaolog converters (DACs) at each operating SRAM row/column, the need for high precision analog-to-digital converters (ADCs), limited support for multi-bit precision weights, and limited vector-scale parallelism. Our co-adapted implementation seamlessly extends to multi-bit precision weights, it doesn’t require DACs, and it easily extends to higher vector-scale parallelism. We also propose an SRAM-immersed successive approximation ADC (SA-ADC), where we exploit the parasitic capacitance of bit lines of SRAM array as a capacitive DAC. Since the dominant area overhead in SA-ADC comes due to its capacitive DAC, by exploiting the intrinsic parasitic of SRAM array, our approach allows low area implementation of within-SRAM SA-ADC. Our $8\times62$ SRAM macro, which requires a 5-bit ADC, achieves $\sim105$ tera operations per second per Watt (TOPS/W) with 8-bit input/weight processing at 45 nm CMOS. Our $8\times30$ SRAM macro, which requires a 4-bit ADC, achieves $\sim84$ TOPS/W. SRAM macros that require lower ADC precision are more tolerant of process variability, however, have lower TOPS/W as well. We evaluated the accuracy and performance of our proposed network for MNIST, CIFAR10, and CIFAR100 datasets. We chose a network configuration which adaptively mixes multiplication-free and regular operators. The network configurations utilize the multiplication-free operator for more than 85% operations from the total. The selected configurations are 98.6% accurate for MNIST, 90.2% for CIFAR10, and 66.9% for CIFAR100. Since most of the operations in the considered configurations are based on proposed SRAM macros, our compute-in-memory’s efficiency benefits broadly translate to the system-level.

Index Terms—Deep neural networks; In-SRAM processing; MNIST; CIFAR10; CIFAR100.

I. INTRODUCTION

In many practical applications, deep neural networks (DNNs) have shown a remarkable prediction accuracy [1]–[3]. DNNs in these applications typically utilize thousands to millions of parameters (i.e., weights) and are trained over a huge number of example patterns [5]–[7]. Operating over such a large parametric space, which is carefully orchestrated over multiple abstraction levels (i.e., hidden layers), facilitates

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Figure 1: High-level overview of in-SRAM processing in the current art and key limitations. The figure considers CONV-SRAM [8] as a motivating example, however, the challenges are common to the most other designs.

DNNs with a superior generalization and learning capacity, but also presents critical inference constraints, especially when considering real-time and/or low power applications. For instance, when DNNs are mapped on a traditional computing engine, the inference performance is strangled by extensive memory accesses, and the high performance of the processing engine helps little.

A radical approach, gaining attention to address this performance challenge of DNN, is to design memory units that can not only store DNN weights but also locally process DNN layers. Therefore, using such ‘compute-in-memory’ high volume data traffic between processor and memory units is obviated, and the critical bottleneck can be alleviated. Moreover, a mixed-signal in-memory processing of DNN operands reduces necessary operations for DNN inference. For example, using charge/current-based representation of the operands, the accumulation of products simply reduces to current/charge summation over a wire. Therefore, dedicated modules and operation cycles for product summations are not necessary.

In recent years, several in-SRAM DNN implementations have been shown. However, many critical limitations remain, which inhibit the scalability of the processing. In Figure 1, using CONV-SRAM [8] as a motivating example, we highlight these limitations – notably, the challenges are common to most other in-SRAM applications too. To compute the inner product of $l$-element weight and input vectors $w$ and $x$, $l$-DACs and one ADC are required. Since DACs are concurrently active, they lead to both high area and power. With the increasing precision of operands, the design of DACs also becomes more
complex. In [9], time-domain DACs are used to handle this complexity; however, with increasing input precision, either operating time increases exponentially, or complex analog-domain voltage scaling is necessitated. In [10], DACs are obviated, but the operation is only limited to binary inputs and weights, which has low accuracy.

An ADC is needed to digitize the inner product of \( w \) and \( x \) vectors in Figure 1. If \( x \) is \( n \)-bit and ADC combines the output of \( l \) cells, the minimum necessary precision of the ADC is \( \approx n + \log_2(l) \) to avoid any quantization loss. Therefore, ADC precision requirement becomes more stringent with increasing input precision and the number of cells being summed. Moreover, scaled technology nodes of SRAM precludes analog-heavy ADCs embedded within SRAM. In [8], a charge-sharing-based ADC was integrated with SRAM. However, the worst-case comparison steps grow exponentially with ADC’s precision, limiting vector scale parallelism (i.e., the number of cells/products \( l \) that can be concurrently processed). In [11], ADC is avoided by using a comparator circuit, but this limits the implementation only to step function-based activation and doesn’t support the mapping of DNNs with larger weight matrices that cannot fit within an SRAM array.

Near-memory processing avoids the complexity of ADC/DAC by operating in the digital domain only. The schemes use the time-domain and frequency-domain summing of weight-input products. Unlike charge/current-based sum, however, time/frequency-domain summation is not instantaneous. A counter [12] or memory delay line (MDL) [13] can be used to accumulate weight-input products. With increasing vector-scale parallelism (length of input/weight vector \( l \)), the integration time of counter/MDL increases exponentially, which again limits parallelism and throughput.

Addressing the challenges of state-of-the-art, we propose the following core concepts:

1) We use a multiplication-free neural network operator that eliminates high-precision multiplications in input-weight correlation [14]–[16]. In the new operator, the correlation of weight \( w \) and input \( x \) is represented as

\[
w \oplus x = \sum_i \text{sign}(x_i) \cdot \text{abs}(w_i) + \text{sign}(w_i) \cdot \text{abs}(x_i) \quad (1)
\]

Here, \( \cdot \) is an element-wise multiplication operator, \( + \) is element-wise addition operator, and \( \sum \) is vector sum operator. \text{sign()} operator is \( \pm 1 \) and \text{abs()} operator produces absolute unsigned value of the operand. Therefore, in Eq. (1) the correlation operator is inherently designed to only multiply a one-bit element of \text{sign}(x) against full precision \( w \), and one-bit \text{sign}(w) against \( x \). By avoiding direct multiplications between full precision variables, DACs can be avoided in in-memory computing.

2) Additionally, we reformulate Eq. (1) as below to minimize the dynamic energy of computation:

\[
2 \times \sum_i \text{step}(w_i) \cdot \text{abs}(x_i) - \sum_i \text{abs}(x_i)
\]

In the above reformulation, \text{step()} \( \in [0, 1] \). The above reformulation allows processing with single product port of SRAM cells; thus, it can reduce dynamic energy. Compare this to current implementations [8], [9], [11] where operations with weights \( w \in [-1, 1] \) require product accumulation over both bit lines. SRAM design in [8] is \( 10T \) to support differential ended processing, while our SRAM is \( 8T \) due to single-ended processing. However, the above reformulation also has residue terms \( \sum \text{abs}(x_i) \) and \( \sum \text{abs}(w_i) \). The first term can be computed using a dummy row of weights, all storing ones. For a given input, this computation is referenced for all weight vectors; thus, computing overheads amortize. The second term is a weight statistics that can be pre-computed and can be looked-up during evaluation.

3) We also discuss that parasitic capacitance of bit lines of SRAM array can be exploited as a capacitive digital-to-analog converter (DAC) for successive approximation-based ADC (SA-ADC). In our architecture, when bit lines in one half of the array compute the weight-input correlation, bit lines in the other half implement binary search of SA-ADC to digitize the correlation output. Remarkably, the proposed DNN operator also helps reducing precision constraints on SA-ADC. With the proposed operator, each SRAM cell only performs 1-bit logic operation; thus, to digitize the output of \( l \) columns, ADC with \text{log}_2(l) \) precision is needed. Compare this to CONV-SRAM in Figure 1, where necessary ADC’s precision is \( n + \text{log}_2(l) \) since each SRAM cell processes \( n \)-bit DAC’s output. By simplifying data converters, our scheme can also achieve higher vector-scale parallelism, i.e., allows processing a higher number of parallel columns \( l \) with the same ADC complexity than in [8].

Sec. II introduces the co-adapted multiplication-free operators for the in-SRAM deep neural network. Sec. III characterizes the algorithmic accuracy of our framework. Sec. IV gives an overview of compute-in-memory macro based on multiplication-free operator. Sec. V discusses power/performance characterization of the proposed compute-in-SRAM macro. Sec. VI explores the concept of synergistic integration of digital and compute-in-memory processing for DNN. Sec. VII concludes.

II. CO-DESIGNED MULTIPLICATION-FREE NN OPERATOR

Multiplication-free DNN operator were presented in [17]. In this work, we expand on the potential of multiplication-free operators to considerably reduce the complexity of SRAM-based compute-in-memory design. Compared to [17], we adjusted the operator with \text{abs()} operation on operands \( w \) and \( x \) in Eq. (1) to further simplify compute-in-memory processing steps. Our later discussion will show that the adjusted operator also achieves high prediction accuracy on various benchmark
datasets. Note that a multiplication-free operator in Eq. (1) is based on the $\ell_1$ norm, since $x \oplus x = 2|x|_1$. In traditional neural networks, neurons perform inner products to compute the correlation between the input vector with the weights of the neuron. We define a new neuron by replacing the affine transform of a traditional neuron using co-designed NN operator as $\phi(\alpha(x \oplus w) + b)$ where $w \in R^d$, $\alpha,b \in R$ are weights, the scaling coefficient and the bias, respectively. Moreover, since the proposed NN operator is nonlinear itself, an additional nonlinear activation layer (e.g., ReLU) is not needed, i.e., $\phi()$ can be an identity function. Most neural network structures including multi-layer perceptrons (MLP), recurrent neural networks (RNN), and convolutional neural networks (CNN) can be easily converted into such an \textit{compute-in-memory compatible} network structures by just replacing ordinary neurons with the activation functions defined using $\oplus$ operations without modification of the topology and the general structure.

The above co-designed neural network can be trained using standard back-propagation and related optimization algorithms. The back-propagation algorithm computes derivatives with respect to the current values of parameters. However, the key training complexity for the operator is that the derivative of $\alpha(x \oplus w) + b$ with respect to $x$ and $w$ is undefined when $x_i$ and $w_i$ are zero. The partial derivative of $x \oplus w$ with respect to $x$ and $w$ can be expressed:

$$\frac{\partial (x \oplus w)}{\partial x_i} = \text{sign}(w_i) \text{sign}(x_i) + 2 \times \text{abs}(w_i) \delta(x_i),$$  

$$\frac{\partial (x \oplus w)}{\partial w_i} = \text{sign}(x_i) \text{sign}(w_i) + 2 \times \text{abs}(x_i) \delta(w_i).$$

Here, $\delta()$ is a Dirac-delta function. For gradient-descent steps, the discontinuity of sign function can be approximated by a steep hyperbolic tangent and the discontinuity of Dirac-delta function can be approximated by a steep zero-centered Gaussian function.

### III. Accuracy on Benchmark Datasets

In this section, we characterize the prediction accuracy of the proposed NN operator for MNIST [18], CIFAR10 [19] and CIFAR100 [20] data-sets. For MNIST, we simulate the LeNet-5 network [21]. The network consists of two convolution layers, two fully connected layers, and uses max-pooling layers. For CIFAR10, we use a convolutional neural network consisting of five convolution layers and two fully connected layers. DNN for CIFAR10 uses max-pooling layers and batch normalization layer. For CIFAR100 we choose MobileNetV2 [22]. Both MNIST and CIFAR-10 data sets consist of 60,000 images with 10 classes, whereas the CIFAR100 data set consists of 60,000 images with 100 classes. A test-set of 10,000 images is used to characterize the prediction accuracy.

Table I summarizes test-set accuracy for the data sets with conventional, multiplication-free, and binarized network operators. In Table 1, for CIFAR10 results, the convolution layers are binarized in BNN and made multiplication-free in the proposed network, respectively, while the fully-connected layers are implemented using regular multiplications. Accuracy results for MNIST are obtained by keeping only the last layer typical, and the other layers are binarized or multiplication-free. For CIFAR100 results, we make only the bottleneck (BN) layers of MobileNetV2 multiplication-free and keep the rest of the network with the typical operator. In Table I, we also compare the accuracy of the multiplication-free operator against the binarized weight operator using the above configuration on various datasets. While a binary neural network (BNN) simplifies the implementation at the cost of constrained learning space, the learning space of the multiplication-free operator is as extensive as the typical operator. Therefore, multiplication-free operator-based networks have much better accuracy than BNN. The accuracy of the multiplication-free operator is also quite competitive to the conventional operator on various datasets [14], [15]. Meanwhile, our later discussion will show that a multiplication-free operator significantly reduces implementation complexity compared to the typical operator. Figures 2(a-b) show the training curve for the multiplication-free operator compared to BNN under identical training conditions for MNIST and CIFAR10. In Figure 2(c),
the prediction accuracy of multiplication-free operator is also amenable to input/weight quantization. Operation with 8-bit fixed precision inputs/weights has equivalent accuracy to the floating-point precision cases on various datasets. Therefore, in the following discussion, we consider an 8-bit fixed-precision operation with the multiplication-free operator.

IV. OVERVIEW OF COMPUTE-IN-SRAM MACRO BASED ON MULTIPLICATION-FREE OPERATOR

A. Compute-in-SRAM macro based on µArrays/Channels

Figure 3(a) shows the proposed design of compute-in-SRAM macro for multiplication-free operator-based DNN inference. In the proposed design, an SRAM macro consists of µArrays and µChannels, as shown in the figure. Each µArray is dedicated to storing one weight channel. DNN weights are arranged across columns in a µArray where each bit plane of weights is arranged in a row. Therefore, an N-dimensional weight channel with m-bit precision weights will require m rows and N columns of SRAM cells in a µArray. Figure 3(b) shows the proposed 8T SRAM cell used for the in-SRAM processing of the operator. Extra transistors in the cell compared to a 6T cell decouple typical read/write operations to within cell product. The added transistors are selected by the row and column select lines (RL and CL) and operate on the product bit line (PL). The decoupling of read/write and product operations mitigates interference between the operations, reduces the impact of process variability, and allows operation in storage hold mode. Each µArray is augmented with a µChannel. µChannels convey digital inputs/outputs to/from µArrays. µChannels are essentially low overhead serial-in serial-out digital paths based on scan-registers. If a weight filter has many channels, µChannels also allow stitching of µArrays so that inputs can be shared among the µArrays. Figure 3(d) shows µChannel-based column merging between two µArrays. If two columns are merged, inputs are passed to the top array directly from the bottom array, and the loading of input bits is bypassed on the top column; therefore, overheads to load input feature-map are minimized. Figure 3(c) illustrates input/weight mapping to SRAM macro and operation sequence. For step(x) · abs(w) step in w ⊕ x, step(x) vector is loaded on the µChannel and operated against abs(w) rows of µArray. For step(w) · abs(x) step, bitplanes of abs(x) vector are sequentially loaded on the µChannel and operated against step(w) row of the µArray.

B. Operation cycles

In a µArray, to compute x ⊕ w, the operation proceeds by bit planes. If the left half computes the weight-input product, the right half digitizes. Both halves subsequently exchange their operating mode to process weights stored in the right half. When evaluating the inner product terms step(x) · abs(w), computations for ith weight vector bitplane are performed in one instruction cycle. At the start, the inverted logic values of step(x) bit vector is applied to CL through µChannels. PL is precharged. When clock switches, tri-state MUXes float PL. Compute-in-memory controller activates SRAM rows storing ith bit vector of w. In a column j, only if both wj,i and step(xj) are one, the corresponding PL segment discharges. To minimize the leakage power, we maintain SRAM cells in their hold mode and dedicate additional clock time to discharge PLs. The potential of all column lines is averaged on the sum-lines to determine the net multiply-average (MAV), i.e., ∑ 1/2(wj,i × step(xj)) for input vector and weight bit plane wj. Figure 3(e) shows the instruction sequence for the left half to compute MAV consisting of precharge, product, and average stages. Figure 4(b) shows the simulated transients in the left half to illustrate the execution sequence. step(w) · abs(x) is processed similarly by loading bitplanes of abs(x) to the µChannels.

C. SRAM-Immersed SA-ADC

Since MAV output at the sum line (SL) is charge-based, an analog-to-digital converter (ADC) is necessary to convert the output into digital bits. In Figure 5(a), the right half of the array implements an SRAM-immersed successive approximation (SA) data converter to digitize the output at the left sum line (SLL). Reference voltages for SA-based data conversion are generated by exploiting PL parasitic in the right half. Figure 5 describes the utilization of parasitic capacitance of the product lines for the DAC implementation of SA-ADC. The product lines of the right half are charged and discharged according to the SAR logic to produce the reference voltage at the right sum line (SLR). In the ith SA iteration, 2i capacitors are used to generate the reference voltage. Each half also uses a dummy PL of matching capacitance to complete SA. Although the capacitance of SL affects the MAV range, its effect nullifies during the digitization since the capacitor is a common mode to both ends of the comparator. Nonetheless, limited voltage swing range due to SL’s capacitance limits the number of parallel columns in a µArray that can be reliably operated.

Figure 3(e) also shows the instruction cycles for the data conversion consisting of precharge, average, compare, and SAR steps. One cycle of data conversion lasts two clock periods. For n-bit digitization, 2n clock cycles are needed. In a conversion cycle, at the start, PLs in the right half are charged based on initialization or SA output from the previous cycle. At the next clock transition, PLs are merged to average their voltage. Next, a comparator compares the potential at the left and right sum lines (SLL and SLR in Figure 3(a)). Subsequently, SA logic operates on the comparator’s output to update the digitization registers and produces the next precharge logic bits. Figure 4(b) shows the simulated transients in the right half and interplay with the left half.

The comparator in our design must accommodate rail-to-rail input voltages at SLL and SLR. Therefore, in Figure 4(a), we use a cross-coupled comparator consisting of n-type and p-type modules. The n-type module receives inputs at NMOS transistors while p-type receives at PMOS. Coupling transistors to integrate both modules are highlighted in Figure 4(a). If the input voltages are closer to zero, the p-type instance dominates. Otherwise, if the input voltages are close to VDD, the n-type instance dominates. Connections to coupling transistors in the figure ensure that n-type or p-type instances can be overridden at the appropriate voltage range. Figure 4(c) shows the comparator output transients.
D. Key advantages over the current compute-in-SRAM

Our multiplication-free inference framework using compute-in-SRAM μArrays and μChannels has many key advantages over the competitive designs [23]–[25]. First, a multiplication-free learning operator, obviates digital-to-analog converters (DAC) in SRAM macros. Meanwhile, DACs incur considerable area/power in the current competitive designs [26], [27]. Although overheads of DAC can be amortized by operating in parallel over many channels, the emerging trends on neural architectures, such as depth-wise convolutions in MobileNets [28], show that these opportunities may diminish. Comparatively, our DAC-free framework is much more efficient in handling even thin convolution layers by eliminating DACs; thereby, allowing fine-grained embedding of μChannels without considerable overheads. If the filter has many parallel channels, our architecture can also exploit input reuse opportunities by merging μChannels as we discussed earlier. Secondly, a multiplication-free operator, is also synergistic with the discussed bitplane-wise processing. Bitplane-wise processing followed in this work reduces the ADC’s precision demand in each cycle by limiting the dynamic range of MAV. Note that with bitplane-wise processing, for n column lines, MAV varies over 2^n levels. However, if such bitplane-wise processing is performed for the typical operator, an excessive O(n^2) operating cycles will be needed for n-bit precision. Meanwhile, a multiplication-free operator only requires O(2n) cycle. Lastly, we have discussed unique opportunities to exploit SRAM array parasitic for SRAM-immersed ADC. The proposed scheme obviates a major area overhead for SA-ADC. Therefore, the compute-in-SRAM macro can maintain a high memory density.
V. Power–Performance Characteristics of Compute-in-SRAM Macro

A. Simulation methodology

In this section, we discuss power–performance characteristics of compute-in-SRAM macro presented earlier. We use LeNET-5 for MNIST characterization as a running use-case to discuss various design and power optimization opportunities. The scalability of the proposed framework on more complex datasets and deeper networks will be discussed in the next section. The network weights for LeNET-5 are trained using TensorFlow. Convolutional layers in LeNET-5 and the next fully-connected layer are implemented using a multiplication-free operator. The last layer of LeNET-5 is implemented in a typical operator. Data transfer among SRAM arrays and post-processing of array’s output, such as applying max-pooling, is simulated functionally. Compute-in-SRAM operations are simulated using HSPICE in 45 nm CMOS technology using predictive technology models [29]. Each μArray in SRAM-macro has 8 rows and 62 columns. A μArray is split into halves, where each half stores a weighted channel by flattening it to one-dimensional. μArrays process 8-bit weights against 8-bit inputs. In each SA cycle in μArrays, MAV is digitized to 5-bit output. If the flattened filter width is more than 31, it is partitioned and mapped on more μArrays.

B. Power–performance characteristics

We summarize key power–performance characteristics of our compute-in-SRAM macros based on 45 nm CMOS simulations using PDK [30]. In Figure 6(a), reducing the hold voltage of SRAM cells reduces leakage current through the cells; however, also increases the PL discharge time during product computation. We chose the hold voltage to be 0.4 V since this represents an optimal balance of discharge time and leakage power. At this voltage, the worst case discharge time (considering slow-slow corner and 120°C temperature) is 50 ps. The average leakage power of a μArray is 0.97 nW at the typical corner. Figure 6(b) shows the distribution of power among various operations in a μArray. A μArray consumes ∼7.6 μW of active power to perform the MAV operation while operating at 1 GHz. MAV operation consumes 44% of the total energy, whereas digitization consumes 55% of the total energy, accounting for capacitive DAC, comparator, and SAR logic operations. The leakage power of SRAM accounts for <1% of the total. Since ADC’s power overhead are considerable, in the next section, we discuss techniques for dynamic precision scaling to mitigate the overhead.

C. Dynamic precision scaling

In Figure 7 we explore the design space of varying weight precision ($W_P$) and ADC precision ($A_P$) for predictions on MNIST dataset. Figure 7(a) shows a surface plot showing the prediction accuracy at varying $W_P$ and $A_P$. The prediction accuracy improves with higher $W_P$ and $A_P$. Figures 7(b-c) show surface plot for latency and energy for a unit $w⊕x$ operation on the μArray, respectively. The following determine the clock cycles ($T$) and average energy ($E$) for the unit operation

$$T = W_P \times (1 + 2A_P)$$

$$E = W_P \times \left( MC_{PL}V_{PCH}^2 + \sum_{i=0}^{A_P-1} E_C + E_{SAR} + 2C_{PL}V_{PCH}^2 \right)$$

Here, $C_{PL}$ is the product line (PL) capacitance. $V_{PCH}$ is the precharge voltage for processing. $E_C$ and $E_{SAR}$ are the average energy of unit operation for the comparator and SA register logic. $M$ is the number of columns in each half of μArray. Since MAV operation requires all PL to charge, the estimated dynamic energy is $MC_{PL}V_{PCH}^2$ per weight bit plane. Within a bit plane processing, SA-ADC operates comparator and SAR logic $A_P$ times. From our simulations in 45 nm CMOS, Figure 7(d) shows various parameters in the equation. For $C_{PL}$, we add a 20% overhead from the transistor capacitance to account for the interconnect parasitic.

From the surface plots, $W_P$ and $A_P$ have different sensitivity to latency and energy demand on computing in our scheme. Consider two iso-accuracy cases: Case-A ($W_P=8$-bit, $A_P=2$-bit) and Case-B ($W_P=4$-bit, $A_P=5$-bit) in the surface plot. For both cases, the prediction accuracy is ∼95%, but the cases are diametrically opposite in weight and ADC precision – Case-A has the maximum $W_P$ and Case-B has the maximum $A_P$. For the iso-accuracy cases, Case-A has ∼10% lower latency than
Case-B while requires ~30% more energy. Case-B has lower energy due to fewer MAV steps, thereby, fewer MAV and ADC cycles. Case-A has lower latency since each MAV cycle is much shorter than in Case-B. Interestingly, an optimal ADC cycles. Case-A has lower latency since each MAV cycle due to fewer MAV steps, thereby, fewer MAV and ∼

Estimating comparator’s variability by forcing it to metastable point and probability by discarding columns with high PL capacitor variability. (e) An on-chip scheme to estimate PL capacitor mismatch and contributing to the MAV numerator. (c) An on-chip scheme to estimate PL columns with extremely varying capacitance. (d) MAV crossover probability at varying PL capacitor mismatch and µArray sizes. Mitigating MAV crossover probability by discarding columns with high PL capacitor variability. (e) Estimating comparator’s variability by forcing it to metastable point and calibrating tail currents to mitigate process variability.

### D. Impact of process variability and on-chip calibration

In Figure 8(a), due to process variability among PL capacitors, MAV output levels will follow a Gaussian distribution. The distribution of MAV output levels arises both due to variability in PL capacitors as well as many combinations to obtain a MAV level. If MAV output levels crossover, the weight-input product from µArrays can be erroneous. In our scheme, the accuracy of MAVs is mainly affected by the PL capacitor’s mismatch. The effect of global variability among PL capacitors cancels out by bi-partitioning a µArray – generating MAVs in one half and reference voltages in the other half – so that the global variability of PL capacitors becomes common mode. Considering a Gaussian distribution of MAV output levels, Figure 8(d) shows the probability of MAV crossover (P\(F\)) in a µArray at varying capacitor mismatch and µArray size. P\(F\) increases with higher PL capacitor variability as well as with the increasing number of columns in a µArray. Therefore, the maximum number of columns in a µArray (i.e., its parallelism) is constrained.

In Figure 8(c), we discuss an on-chip scheme to self-determine the usable column width of a µArray based on its process variability. In the figure, the strength of a PL capacitor is measured on-chip by repeatedly charging the sum-line through it and counting the number of cycles to cross a set threshold. A smaller PL capacitor will require more charging cycles to cross the threshold. Most extreme PL capacitors are identified. If their process variability is more than an acceptable margin, these columns are not used [Figure 8(b)]. In our scheme, we avoid adding a switch to disconnect such columns, since it will considerably increase the area overhead of the on-chip calibration scheme. Note that the column disconnect switch and a memory cell to store the switch enable needs to be implemented for each column of µArray. Instead, we lessen the effect of columns with extreme C\(PL\) variation by writing one to all SRAM cells in the column and by applying the CL input signal to be one. Therefore, the column with extremely varying C\(PL\) always discharges and only contributes to the charge averaging step. The sensitivity of extremely varying C\(PL\) to MAV is thereby low since it only contributes to the denominator of MAV, where its effect averages out against other columns in µArray. Based on this scheme, the right of Figure 8(d) shows the MAV cross-over probability for 8×62 µArrays considering ±12% mismatch among PL capacitors and at varying C\(TH\) levels [Figure 8(b)]. By discarding only about 3% of columns, MAV cross-over probability can be sufficiently suppressed.

Similarly, process variability in the comparator constrains the minimum precharge voltage and the maximum number of columns in a µArray. In Figure 8(e), we use an on-chip calibration scheme to mitigate the comparator’s process variability. The scheme selects N- and P-type counterparts of the comparator in turn. The comparator is first set to a known initial condition and then forced to a metastable point by shorting both inputs. By repeatedly resetting and setting the comparator, its bias can be estimated from the output bit sequence. An unbiased comparator should have an equal probability of 0/1 under thermal noise. The tail currents in the left and right half of the comparator can be adjusted to minimize the comparator’s bias. Calibrating transistors for the comparator are shown in Figure 4(a). A counter monitors the comparator’s output and adds calibration transistors to the left or right half to minimize bias in the comparator. In the right of Figure 8(e), using a 2-bit calibration, the comparator’s mismatch can be reduced to ±12 mV from the initial ±45 mV.

### E. Comparisons to current art

Table II compares our results against the state-of-art on different data sets. For various datasets, our network configu-
Table II: Comparison against state-of-the-art

| Metric          | Our [23] 62 | [24] 65 mm | [25] 65 mm | [31] 28 nm |
|-----------------|-------------|------------|------------|-----------|
| Tech (nm)       | 45          | 28         | 65         | 7         |
| Weight bits     | 8-bit       | 8-bit      | 8-bit      | 8-bit     |
| Input bits      | 8-bit       | 8-bit      | 8-bit      | 8-bit     |
| Output bits     | 16-bit      | 20-bit     | 8-bit      | 4-bit     |
| Accuracy (%)    |             |            |            |           |
| MNIST           | 98.6%       | -          | 99.28%     | 98.2%     |
| CIFAR10         | 90.2%       | 91.9%      | 86.62%     | -         |
| CIFAR100        | 66.9%       | 67.8%      | -          | -         |

... an exponential reduction in the throughput with increasing precision. Meanwhile, in this work, we overcame the critical challenge using a novel co-design approach by adapting the DNN operator to in-memory processing constraints. In our multiplication-free compute-in-memory framework, the parameteric learning space expands, yet the implementation complexities are equivalent to a binarized neural network. Even so, the accuracy of multiplication-free operators is somewhat lower than the typical deep learning operator due to the non-differentiability of gradients.

Considering the above trade-offs, we find that the key to balance scalability with energy efficiency in DNN inference is through a synergistic integration of compute-in-memory with digital processing. In Figure 9 we discuss insights towards this. The figure shows a layer-wise distribution of weights and operations for the networks used for MNIST, CIFAR10, and CIFAR100. The network configurations were discussed earlier in Sec. II. Note that as the processing propagates through the networks, weights per layer increase, but the number of operations per weight reduces. This is, in fact, typical to any DNN due to shrinking input feature map dimensions, which reduces the weight reuse opportunities. Since the starting layers have much fewer parameters but much higher weight reuse, they are quite suited for compute-in-memory. The latter layers require many more parameters but have low weight reuse. Therefore, digital processing can minimize the excessive storage overheads of these layers with denser storage.

Using this strategy, the figure also shows a mixed mapping configuration that layer-wise combines compute-in-memory and digital processing. For example, in the mixed implementation of MobileNetV2, feature extraction layers with high weight reuse are mapped in compute-in-memory using an 8-bit multiplication-free operator. Regression layers and others with low weight reuse are mapped in digital using the typical operator. Remarkably, based on the synergistic mapping strategy, compute-in-memory only stores about a third of the total weights; yet, performs more than 85% of the total operations. Therefore, the synergistic mapping can optimally translate compute-in-memory’s energy-efficiency advantages to the overall system-level efficiency, and yet, limits its area overheads. The synergistic mapping also improves the prediction accuracy, since only critical layers are implemented with the energy-expensive typical operator while the remaining most of the network is operated with multiplication-free operators. The figure also shows similar mapping configurations for MNIST and CIFAR10 prediction networks. In the figure, we also project average macro-level energy efficiency in TOPs/W. For digital processing, we use 2.8 TOPs/W from [34]. For multiplication-free compute-in-memory processing, we use 105 TOPs/W from Table II. We, however, note that the macro-level energy efficiency doesn’t necessarily translate to system-level energy efficiency where overheads due to routing and control flow must also be accounted for. We plan to consider this characterization in future work.

VI. SYNERGISTIC INTEGRATION OF DIGITAL AND COMPUTE-IN-MEMORY PROCESSING FOR DNN

Compute-in-memory offers immense energy efficiency benefits over digital by eliminating weight movements. Mixed-signal processing of compute-in-memory also obviates processing overheads for adders by exploiting physics (Kirchoff’s law) to sum the operands over a wire. Note that additions are a significant portion of the total workload in a digital DNN inference. However, compute-in-memory is also inherently limited to only weight stationary processing. The advantages of stationary weight processing reduce if the filter has fewer channels or if the input has smaller dimensions. Compute-in-memory is also more area expensive compared to digital processing, which can leverage denser memory modules such as DRAM. On the other hand, the memory cells in compute-in-memory are larger to support both storage and computations within the same physical structure. Additionally, multibit precision DNN inference is complex using compute-in-memory. Therefore, many prior works [31, 32] utilize binary-weighted neural networks, which, however, constraints the learning space and reduces the prediction accuracy. Deep in-memory architecture (DIMA) in [33] considers multibit precision in-memory inference; however, the implementation suffers from
modulated to reduce prediction latency, and ADC’s precision can be controlled to reduce energy. Additionally, for deeper neural networks, we have discussed mapping configurations where high weight reuse layers can be implemented in our compute-in-SRAM framework, and parameter-intensive layers (such as fully-connected) can be implemented through digital accelerators. Our synergistic mapping strategy combining both multiplication-free and typical operator is promising to achieve both high energy efficiency and area efficiency in operating deeper neural networks.

REFERENCES

[1] K. Makantasis, K. Karantzalos, A. Doulamis, and N. Doulamis, “Deep supervised learning for hyperspectral data classification through convolutional neural networks,” in 2015 IEEE International Geoscience and Remote Sensing Symposium (IGARSS). IEEE, 2015, pp. 4959–4962.

[2] J. Liu, Y. Deng, T. Bai, Z. Wei, and C. Huang, “Targeting ultimate accuracy: Face recognition via deep embedding,” arXiv preprint arXiv:1506.07310, 2015.

[3] Y. Wei, Q. Yuan, H. Shen, and L. Zhang, “Boosting the accuracy of multispectral image pansharpening by learning a deep residual network,” IEEE Geoscience and Remote Sensing Letters, vol. 14, no. 10, pp. 1795–1799, 2017.

[4] J. Cho, K. Lee, E. Shin, G. Choy, and S. Do, “How much data is needed to train a medical image deep learning system to achieve necessary high accuracy?” arXiv preprint arXiv:1511.06348, 2015.

[5] H. Qassim, D. Feinizer, and A. Verma, “Residual squeeze vgg16,” arXiv preprint arXiv:1705.03004, 2017.

[6] T. Carvalho, E. R. De Rezende, M. T. Alves, F. K. Balieiro, and R. B. Sovat, “Exposing computer generated images by eye’s region classification via transfer learning of vgg19 cnn,” in 17th IEEE International Conference on Machine Learning and Applications (ICMLA). IEEE, 2017, pp. 866–870.

[7] C. Szegedy, S. Ioffe, V. Vanhoucke, and A. A. Alemi, “Inception-v4, inception-resnet and the impact of residual connections on learning,” in Thirty-First AAAI Conference on Artificial Intelligence, 2017.

[8] A. Biswas and A. P. Chandrakasan, “Conv-sram: An energy-efficient sram with in-memory dot-product computation for low-power convolutional neural networks,” IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 217–230, 2019.

[9] M. Kang, S. Lim, S. Gonugondla, and N. R. Shanbhag, “An in-memory vlsi architecture for convolutional neural networks,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 8, no. 3, pp. 494–505, 2018.

[10] Z. Jiang, S. Yin, J.-s. Seo, and M. Seok, “Xnor-sram: In-bitcell computing sram macro based on resistive computing mechanism,” in Proceedings of the 2019 on Great Lakes Symposium on VLSI. ACM, 2019, pp. 417–422.

[11] J. Zhang, Z. Wang, and N. Verma, “In-memory computation of a machine-learning classifier in a standard 6t sram array,” IEEE Journal of Solid-State Circuits, vol. 52, no. 4, pp. 915–924, 2017.

[12] A. Amaravati, S. B. Nasir, J. Ting, I. Yoon, and A. Raychowdhury, “A 55-nm, 1.0–0.4 v, 1.25-pj/mac time-domain mixed-signal neuromorphic accelerator with stochastic synapses for reinforcement learning in autonomous mobile robots,” IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 75–87, 2018.

[13] A. Sayal, S. T. Nitinanupudi, S. Fathima, and J. P. Kulkarni, “A 12.08-tops/w all-digital time-domain cnn engine using bi-directional memory delay lines for energy efficient edge computing,” IEEE Journal of Solid-State Circuits, 2019.

[14] H. Pan, D. Badawi, X. Zhang, and A. E. Çetin, “Additive neural network for forest fire detection,” Signal, Image and Video Processing, pp. 1–8, 2019.

[15] T. Ergen, A. H. Mirza, and S. S. Kozat, “Energy-efficient lstm networks for online learning,” IEEE Transactions on Neural Networks and Learning Systems, 2019.

[16] A. Afrasiyabi, D. Badawi, B. Nasir, O. Yildi, F. T. Y. Vural, and A. E. Çetin, “Non-euclidean vector product for neural networks,” in 2018 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP). IEEE, 2018, pp. 6862–6866.

[17] C. E. Akbaş, A. Bozkurt, A. E. Çetin, R. Çetin-Atalay, and A. Uner, “Multiplication-free neural networks,” in 2015 23rd Signal Processing
[18] Y. LeCun, C. Cortes, and C. Burges, “Mnist handwritten digit database,” ATT Labs [Online]. Available: http://yann.lecun.com/exdb/mnist, vol. 2, 2010.

[19] A. Krizhevsky, “Learning multiple layers of features from tiny images,” Tech. Rep., 2009.

[20] A. Krizhevsky, V. Nair, and G. Hinton, “Cifar-10 (canadian institute for advanced research).” [Online]. Available: http://www.cs.toronto.edu/~kriz/cifar.html.

[21] Y. Lecun, L. Bottou, Y. Bengio, and P. Haffner, “Gradient-based learning applied to document recognition,” Proceedings of the IEEE, vol. 86, no. 11, pp. 2278–2324, 1998.

[22] A. Krizhevsky, V. Nair, and G. Hinton, “Cifar-100 (canadian institute for advanced research).” [Online]. Available: http://www.cs.toronto.edu/~kriz/cifar.html.

[23] J. Su, X. Si, Y. Chou, T. Chang, W. Huang, Y. Tu, R. Liu, P. Lu, T. Liu, J. Wang, Z. Zhang, H. Jiang, S. Huang, C. Lo, R. Liu, C. Hsieh, K. Tang, S. Sheu, S. Li, H. Lee, S. Chang, S. Yu, and M. Chang, “15.2 a 28nm 64kb inference-training two-way transpose multibit 6t sram compute-in-memory macro for ai edge chips,” in 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 2020, pp. 240–242.

[24] J. Yue, Z. Yuan, X. Feng, Y. He, Z. Zhang, X. Si, R. Liu, M. Chang, X. Li, H. Yang, and Y. Liu, “14.3 a 65nm computing-in-memory-based cnn processor with 2.9-to-35.8tops/w system energy efficiency using dynamic-sparsity performance-scaling architecture and energy-efficient inter/intra-macro data reuse,” in 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 2020, pp. 234–236.

[25] Q. Dong, M. E. Sinangil, B. Erbagci, D. Sun, W. Khwa, H. Liao, Y. Wang, and J. Chang, “15.3 a 351tops/w and 372.4gops compute-in-memory sram macro in 7nm finfet cmos for machine-learning applications,” in 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 2020, pp. 242–244.

[26] A. Biswas and A. P. Chandrakasan, “Conv-sram: An energy-efficient sram with in-memory dot-product computation for low-power convolutional neural networks,” IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 217–230, 2019.