All-digital built-in self-test scheme for charge-pump phase-locked loops

Lanhua Xia | Jifei Tang

Abstract
Charge-pump phase-locked loop (CP-PLL) is widely used to generate timing signals in systems on chips (SoCs). However, the number of cores embedded in SoCs, the limited I/O port resources and the cost of external test equipment lead to the increase of test complexity and cost. An all-digital built-in self-test structure of CP-PLL especially suitable for low-cost production tests when I/O port resources are limited is proposed. The structure is simple and easily implemented with just a few DFFs, MUXs and some existing circuits in CP-PLL under test. It reduces the requirement of additional external test clocks and high-performance test equipment, which decreases the test cost of the whole integrated circuits. Combined with the proposed calibration technique, it eliminates the effect of uncertain initial value of voltage controlled oscillator input voltage on the fault coverage. Thus, the reliability of test results is also increased. Experiment results demonstrate the effectiveness of the proposed scheme with high fault coverage of 99.16%. In addition, the physical chip design is presented to show low area overhead of 1.37%.

1 | INTRODUCTION

With the rapidly growing of very large-scale integration (VLSI) industry, the mixed-signal testing plays an important role of shortening production cycle and reducing production cost of modern communication and electronic systems [1, 2]. However, as the feature sizes of transistors are scaled down constantly, more and more circuits of complex functions including analogue and digital modules were integrated on a single chip. It greatly increased the difficulty of testing such chips. Taking system-on-chips (SoCs) as an example, numbers of cores embedded in SoCs, the limited I/O port resources, the cost of external test equipment, and the limitation of data path lead to the increase of test complexity and cost.

Built-in self-test (BIST) method is an attractive testing solution proposed to solve the problem, which avoids high performance test instruments by adding extra test circuits and pins on chip. It is significantly important to save test cost and time. Although the applications of BIST technology for digital circuits have become quite mature, the research of BIST solution for mixed-signal circuits has just started. Especially the high test cost of mixed-signal modules is still a main obstacle in VLSI systems testing.

The test solution of charge-pump phase-locked loop (CP-PLL), which is a classical mixed-signal circuit, is studied. Compared with conventional PLL, CP-PLL has several key characteristics, such as low jitter, low power consumption, high stability, wide capture range, and easy integration. Thus, it gets extensive applications in electronic and communication production, such as wireless communication device, frequency synthesizer, and clock recovery circuit. However, as the only mixed-signal module in most of SoCs, high test cost of CP-PLL caused by its tight feedback and complex mixed-signal characteristics increases the production cost [3]. Thus, there are strong demands for a low cost efficient production test scheme of CP-PLL. To address this challenge, an all-digital BIST structure of CP-PLL which aims to achieve low-cost test solution is studied, which may also provide certain references for other mixed-signal circuits testing.

The paper is organised as follows: a review of some previous works on PLL testing is introduced in Section 2. Proposed BIST scheme is discussed in Section 3. Then, the
description and operation of proposed BIST structure is described in Section 4. Finally, the fault simulation and performance evaluation results are analysed in Section 5. The conclusions are summarised in Section 6.

2 | PREVIOUS WORKS

The recent works about BIST schemes of CP-PLL are introduced below. The main methods used are summarised.

1) Functional test

One or more PLL functionality is verified at some pre-specified test points, such as static phase offset [4, 5], locking time [6], locking frequency range, loop gain [7], capture frequency range, and jitter transfer function [8–10]. The accuracy of test results and the test cost are dependent on the selection of validated functional specifications. However, the tight feedback characteristic of PLL makes this solution less attractive because it is difficult to relate the specifications from the PLL level to the block level, which requires high-performance instruments with even unacceptable test cost.

2) On-chip jitter measurement [11–14].

It aims to measure the clock jitter of PLL output by additional BIST circuits on chip. Many different structures of time-to-digital converter have been used in the method, such as that based on the delay line, the Vernier ring oscillator, and the time-to-voltage converter. Though it achieves a very excellent time resolution, the additional test circuits are usually too complex with high area overhead.

3) Defect-oriented test (DOT) [15–22].

It focusses on the detection of structural faults caused by the physical defects occurred in PLLs. Since it is easily implemented with a little test area overhead, it is widely accepted as an alternative solution for PLL low-cost production test.

Thus, the DOT method is mainly discussed here. A BIST circuit for PLL fault detection is proposed in [15]. To instead break the loop by inserting a MUX, the author inserts a small loading capacitance at the inputs of the phase detector to measure phase offset. It avoids the effects of additional MUXs on the performance of circuit under test (CUT) and the measurement accuracy, but its resolution is limited by the target CUT rather than the capability of the BIST circuit. In [16], a BIST scheme to perform testing of both catastrophic and parameter faults in a PLL using low frequency ATE resources is suggested. The scheme is robust and is independent of the fabrication process corner and the operating conditions, but the fault coverage is relatively low. In [17], the technique uses an internal test signal for evaluating the test procedure instead of breaking the loop to include test circuit in the PLL design stage. It shows high fault coverage, but only focussed on voltage controlled oscillator (VCO) testing. The approaches adopted in [18–22], which have made further modifications of previous BIST structure, provide valuable basis for the low-cost all-digital strategy of CP-PLL testing. However, in most of these improved structures, there are too many external clocks introduced during testing, which increase the I/O ports needed for test.

An all-digital CP-PLL BIST structure especially suitable for low-cost production test when I/O port resources are limited is proposed. With the proposed structure, the area overhead and fault coverage are also improved.

3 | PROPOSED BIST SCHEME

This section analyses the effect of structural faults on CP-PLL performance, proposed BIST scheme, and fault model used for fault detection.

3.1 | The analysis of effect of structural faults on CP-PLL performance

CP-PLL is a negative feedback loop system which is used to synchronise an oscillator’s output signal with a reference signal in both frequency and phase. Any possible fault in CP-PLL is closely related with its structure. Thus, in order to fully understand the effects of structural faults on output signal of CP-PLL, the structure, operation and sensitivity of CP-PLL will be first studied.

Figure 1 shows a classical structure of CP-PLL [23, 24]. It consists of five functional blocks, including phase/frequency detector (PFD), charge-pump (CP), loop filter (LF), VCO and divide-by-N frequency divider (DBN). The PFD compares the phase or frequency difference between reference signal \( f_{RF} \) and output signal of DBN and converts it into two DC voltage signals, that is, \( U_P \) and \( D_N \), which is proportional to the difference. The DC voltage signals act on the next functional block and is amplified by the CP to charge and discharge the capacitance of LF. By the CP and LF, these digital signals are transformed into an analogue voltage \( V_{ctrl} \) for the VCO. Then, the frequency and phase of VCO output signal \( f_{OUT} \) are changed according to the control voltage transmitted. Finally, this output signal will be incorporated into the dynamic range of reference signal \( f_{RF} \) by the DBN.

This cycle is repeated until the loop is in locked state. At this point, the reference signal \( f_{RF} \) and the output signal of DBN are at the same frequency. There is only a small fixed error or alignment phase between them. The CP-PLL system

![FIGURE 1 A classical structure of CP-PLL.](image-url)
remains stable. Assuming the non-ideal effect of CP-PLL, such as the problems of the mismatch between \( U_P \) and \( D_N \) path in PFD, the mismatch of the current of CP, the charge injection, the charge leakage, the clock feed through, and the charge sharing is processed perfectly, the control voltage \( V_{\text{ctl}} \) of VCO will be a stable DC voltage within the normal voltage range. Thus, when CP-PLL is in locked state, the phase and frequency of its output signal will not be changed. This assumption is valid only when there is no fault in CP-PLL circuits. Otherwise any structural fault in CP-PLL may cause leakage, mismatches, or coupled noise. Due to the tight feedback and complex mixed-signal characteristic, the performance of CP-PLL is sensitive to these non-ideal effects. Thus structural faults may directly cause the degradation of CP-PLL performance, such as increasing the clock jitter, changing the centre frequency, affecting reference spurs, producing additional noise, extending the locking time or even making PLL unable to work. The proposed scheme focuses on the detection of structural faults in a PLL. By comparing the variation of CP-PLL performance, this scheme could almost detect any fault in PLL.

3.2 Proposed BIST scheme

A CP-PLL with open loop configuration is shown in Figure 2. After pre-treatment, the input signal \( In1 \) and signal \( In2 \) with a time difference \( \Delta T \) are input into the CP-PLL. The time difference \( \Delta T \) is detected by the PFD and then converted into a voltage variation \( \Delta V \) by the CP combined with LF existing in CP-PLL, as shown in the following equation: 1

\[
\Delta V = \frac{I_{CP}}{C_{LF}} \times \Delta T,
\]

where \( I_{CP} \) is the current of CP and \( C_{LF} \) is the equivalent capacitance of LF.

Then, the frequency of VCO and DBN is changed with the control voltage inputted to the VCO. The voltage variation \( \Delta V \) is transformed into a frequency value \( \Delta f \). Assuming the frequency of VCO is changed from \( f_0 \) to \( f_1 \), the variation \( \Delta f \) is calculated as in following the equation: 2

\[
\Delta f = \frac{f_1 - f_0}{N} = \frac{K_{VCO} \times \Delta V}{N},
\]

where \( K_{VCO} \) is the gain of VCO and \( N \) is the frequency division factor of DBN. Equations (1) and (2) yield the relationship between the frequency variation \( \Delta f \) and the time difference \( \Delta T \), as shown in the following equation: 3

\[
\Delta f = \frac{K_{VCO} \times I_{CP}}{N \times C_{LF}} \times \Delta T
\]

Supposed \( \Delta T \) is a fixed value, the frequency variation \( \Delta f \) is closely related with all key parameters of CP-PLL. Thus it can be used to reveal structural faults in any module of CP-PLL.

The logic state of output voltage of DBN will be measured to check its frequency variation for testing evaluation. The difference of logic state of DBN output from its normal state value indicates that there is a fault in CP-PLL. The output response feature of DBN can reflect faults in all blocks of CP-PLL.

3.3 Fault model

A widely accepted structural fault model of PLL [19–22] has been built to evaluate the fault coverage of proposed BIST scheme on low-cost production test of CP-PLL. As shown in Table 1, the structural fault types include the following Gate-to-drain short (GDS), Gate-to-source short (GSS), Gate-open (GO), Drain-to-source short (DSS), Capacitance-short (CS), Source-open (SO), Drain-open (DO), Resistor-short (RS) and Resistor-open (RO). During the test, a short fault model and an open fault model are usually simulated with a low resistance (1 Ω) and a high resistance (10 MΩ), respectively.

For each test, different single known faults will be preset in the CUT. The testing process will be repeated for all the possible faults to record the number of faults that can be detected. Then, the fault coverage can be got by calculating the ratio of this number to the total number of single fault that may occur in the CUT. Here, the CUT is an integer-64 CP-PLL, but the proposed scheme can also be applied to other types of CP-PLL. Based on the circuit, the circuit design and operation of the BIST structure, the performance evaluation and fault simulation will be analysed. Moreover, some conflicting issues in the research will be discussed.

4 PROPOSED BIST STRUCTURE DESCRIPTION AND OPERATION

This section provides the circuit description and operation of proposed BIST structure.

| Table 1 | Fault types |
|---------|-------------|
| GDS     | GSS         | GO   | DSS | DO | SO | RS | CS | RO |
| 1 Ω     | 10 MΩ       | 1 Ω  | 1 Ω | 1 MΩ | 100 Ω | 10 Ω | 10 MΩ |

**Figure 2** Fundamental theory of the proposed BIST scheme
4.1 | Circuit description of proposed BIST structure

The schematic of proposed structure is shown in Figure 3. A FAULT-TEST module, a AND gate, two MUXs and a DFF are added to the CP-PLL under test. The FAULT-TEST module is employed to pre-treat test stimulus and control the testing process on chip. The MUXs are used to deliver the corresponding stimulus signals to the CP-PLL to allow the switch of different operation modes. It will be inserted into the CP-PLL loops at design stage, so that the delay caused by the MUXs can be incorporated into the initial loop characteristics of CP-PLL. The DFF is used to check the frequency variation of DBN. It is reset when the signal Test and calibrate signal Cal are both set to logic 1. As explained above, the value of \( T_{\text{out}} \) at different faulty cases during test mode after calibration will be recorded to reveal structural faults in CP-PLL. Also, because the implementation of the calibration and trigger signal, the \( T_{\text{out}} \) signal is fixed for every specific fault type, so that to compare to reference patterns. In the structure, the only signal needed for test from external is the signal Test which is easily obtained by connecting to an enable switch outside the chip. Thus, the proposed structure is especially suitable for low-cost production test of CP-PLL when I/O port resources are limited.

The schematic of FAULT-TEST circuit is shown in Figure 4. It consists of just a few DFFs and logic gates, which is easily implemented. The DFF1, DFF2 and DFF3 are used to generate test stimulus signals with different phase, which will be delivered to the input of CP-PLL for test operation. The DFF4, DFF5… DFF(\( n + N +4 \)), DFF(\( n + N +5 \)) are used to provide control signals \( CT_n \), \( CT_N \), and Cal, which will be used to set the working mode of proposed BIST structure. The signals used are listed in Table 2. The period of signals \( CT_n \) and \( CT_N \) is \( n \) and \( N \) periods of reference signal, respectively. The signal Cal lags behind the signal \( CT_N \) \( N \) periods of reference signal \( f_{RF} \).

4.2 | Operation of the proposed BIST structure

The structure has two working modes, normal mode and test mode, which are set by the FAULT-TEST module combined

| Signal | Calibration | Structure faults test | Normal mode |
|--------|-------------|-----------------------|-------------|
| Test   | 1           | 1                     | 0           |
| \( CT_N \) | 0           | 1                     | -           |
| \( CT_n \) | 1           | 1                     | -           |
| Cal    | 0           | 1                     | -           |

**Table 2** Signals used in the proposed structure

| Signals | Introduction |
|---------|--------------|
| \( f_{RF} \) | Reference clock |
| \( In1, In2 \) | Input signals of the CP-PLL |
| \( f_{OUT} \) | Output signal of the CP-PLL |
| \( f_{DBN} \) | Output signal of divider |
| \( CT_n, CT_N \) | Control signals |
| Cal | Calibrate signal |

Abbreviation: Cal, calibrate signal; CP-PLL, charge-pump phase-locked loop; \( f_{RF} \); frequency difference between reference signal; \( f_{OUT} \), the frequency and phase of VCO output signal; \( In1, In2 \), input signal.

**Table 3** Operations of the proposed BIST structure

| Signal | Calibration | Charge test | Discharge test | Normal mode |
|--------|-------------|-------------|----------------|-------------|
| Test   | 1           | 1           | 1              | 0           |
| \( CT_N \) | 0           | 1           | -              | -           |
| \( CT_n \) | 1           | 1           | -              | -           |
| Cal    | 0           | 1           | 1              | -           |

**Figure 3** The schematic of proposed BIST structure

**Figure 4** The schematic of the FAULT-TEST circuit
with the test enabled switch. Table 3 lists the operations of proposed BIST method.

1) Normal mode

If the signal \( Test = '0' \), it works in normal mode. The MUXs are set to bypass the reference signal and feedback signal. The CP-PLL is used to provide clock signals.

2) Test mode

If the signal \( Test = '1' \), the test mode is started by opening the loop of CP-PLL, which includes calibration, charge, and discharge test operation. The test stimulus signal \( S_{test1} \) and \( S_{test2} \) with some time difference will be delivered into CP-PLL. First, the PFD detects the phase difference. The CP and LF transform it into a voltage variation. Then the VCO frequency is changed with the control voltage inputted to it. Finally, the logic state of output voltage of DBN will be measured by the additional DFF to check the frequency variation of DBN for testing evaluation. The difference of logic state of DBN output from its normal state value indicates that there is a fault in the CP-PLL.

To clarify the test operation of proposed BIST structure, the test procedure is illustrated in Figure 5. This procedure will be repeated for every possible fault in CP-PLL, until all of them are tested. The timing diagram of test procedure is shown in Figure 6. The further explanation of Figure 6 is described here.

1) Calibration

During test mode, the initial value of the control voltage inputted to VCO is not a constant value because of the random initial state of DFFs in FAULT-TEST circuit, the tracking ability of PLL, the interference of noises and so on. Thus, the frequency variation rate of VCO output signal, which is dependent on the control voltage, is different even with the same input phase difference and test time. It may have an effect on the logic state of voltage recorded at the output of DBN. To ensure the same initial state of VCO to increase the reliability of test results, there is a calibration mode before every test operation, as shown in Figure 5. In calibration mode, the CP-PLL will be discharged until the control voltage of VCO got the minimum value to keep the same initial state. Then the frequency variation of VCO output signal during the next charge test and discharge test operations will be recorded by the final test output \( T_{out} \).

The calibration operation will proceed when the calibrate signal \( Cal \) is set to logic 0. In this mode, the MUXs are set to deliver the reference signal \( f_{RF} \) and test stimulus signal \( S_{test2} \) which lags behind \( N + 1 \) period of signal \( f_{RF} \). The CP is discharged during the time of \( (N + 1) \times T \). Here, \( T \) is the period of reference signal. \( N \) is decided according to the calibration time which should be set to ensure the control voltage of VCO got the minimum value.

2) Charge Test Operation

The charge test operation starts when the calibrate signal \( Cal \) and the control signal \( CT_N \) are set to logic 1 and 0, respectively. During the process, the MUXs will select the signal \( S_{test1} \) and \( S_{test2} \) as input signals. As the test signal \( S_{test2} \) leads up signal \( S_{test1} \) with time \( T \), the charge pump operates in charge period. By the VCO, the output voltage of LF is converted into a frequency value and by the additional DFF, the logic state of output voltage of DBN will be scanned out for test evaluation.

3) Discharge Test Operation

The discharge test operation can be performed when both the calibrate signal \( Cal \) and control signal \( CT_N \) are set to logic 1.

In Figure 3, the MUXs select the test stimulus signal \( S_{test1} \) and \( S_{test2} \) as input signals. As the signal \( S_{test2} \) lags behind the signal \( S_{test1} \) with time \( T \), the charge pump operates in discharge period, which will drop the output voltage of LF. At this phase, the output voltage of LF is also transformed using the existing VCO and DBN. Then, the logic value of DBN output voltage will be also collected and delivered to the test output for evaluation.
This scheme reduces additional noises from external environment by avoiding the requirement of high-performance test equipment. It solves the loading problem for the sensitive analogue nodes by adding the extra test circuits only on the digital part of CP-PLL. The proposed structure is simple and easily implemented with just a few logic gates. The only additional test signal from external is easily obtained by connecting to an enable switch outside the chip. Employed with most of existing blocks in the CP-PLL as parts of test device, it reduces test area overhead and cuts the test cost. The additional circuits are all digital and the final test output from the DFF is a digital value which is easily extracted and processed. The robustness and practicability of proposed BIST structure is increased. Combined with proposed calibration technique on chip, the reliability of test results is also increased. Thus, it is especially suitable for low-cost production test of CP-PLL when I/O port resources are limited.

5 | CIRCUIT IMPLEMENTATION, FAULT SIMULATION AND PERFORMANCE EVALUATION

The proposed BIST structure was implemented using TSMC 0.13 μm one-poly, eight-metal CMOS technology. Figure 7 illustrates the physical chip design of proposed structure and the chip micrograph. The key parameters of implemented CP-PLL circuits are summarised in Table 4. The area overhead of the chip is approximately 540 × 580 μm² and the additional test circuit is 86 × 50 μm². Comparing the area occupied by the chip before and after adding the extra BIST circuits demonstrates that the area overhead is about 1.37%, which is acceptable for CP-PLL testing in engineering applications.

5.1 | Performance evaluation

The structure is first tested in normal mode to verify the functionality of CP-PLL. In traditional functional test, many parameters such as static phase off-set, locking-frequency range and loop gain need to be tested to determine whether a system functions as intended. It incurs increasingly high cost. Thus, we mainly go on a frequency lock test used in most cases [18–22].

After evaluation, it indicates that the CP-PLL can operate at correct frequency range. A Tektronix MSO712-54C mixed-signal oscilloscope is used to measure the timing jitter of CP-LL when it works in normal mode. As shown in Figure 8, the value of root mean square (RMS) jitter and peak-to-peak jitter is 4.679 and 28.75 ps, respectively. The locking times with and without additional BIST circuits are 2.8 and 2.6 μs, respectively. The results demonstrate that the additional test circuits have a little effect on the functionality of CP-PLL. The measured results of input response of VCO and CP-PLL in normal mode and test mode are shown in Figure 9. It verifies the operation described in Section 4.

5.2 | Fault simulation

In test mode, when the signal test and calibrate signal Cal are both set to logic 1, the DFF is reset. The logic state of output
The physical chip design. (b) The chip micrograph

Voltage of DBN will be measured at some preset observation points for fault evaluation. The value of $n$ and $N$ is decided by the time of charge/discharge test operation and calibration, which is according to the testing requirements. The value is set to be 10 and 20. The value of $T_{out}$ is decided by the scan clock and the number of selected time points, which has a big influence on the test time and the fault coverage. Thus, the number of observation points should be carefully decided. If it is not enough, some of the faults in CUT will not be detected. Generally, the observation points' number is calculated based on the testing accuracy requirements. For example, to the project actual demand, the fault coverage is expected to be above 99%. Since the output of DBN is a square wave, at each observation point, the probability of the logic state of DBN output being correct is $1/2$, therefore, the observation points' number $M$ is calculated as the following equation:

$$1 - \left( \frac{1}{2} \right)^M \geq 99\% \ (M \in Z) \Rightarrow M \geq 7. \hspace{1cm} (4)$$

Thus seven time points should at least be chosen. As too many observation points will extend the test time instead of greatly increasing the fault coverage, in the paper, seven time points ($t = 0.5, 1, 1.5, 2, 2.5, 3, \text{and} \ 3.5 \ \mu s$) are chosen for fault evaluation. The position of observation point can be selected randomly. But it must be ensured that the interval between two observation points is longer than several periods of reference signal $f_{ref}$, so that the change of output caused by fault can be detected more easily with the accumulation of time. In test mode, after calibration, when the CP-PLL works without structural fault, the normal value of $T_{out}$ at each observation point is “0000011”. Any difference between the test output and the normal value demonstrates the presence of fault. Figure 10 shows the value of final test output $T_{out}$ at each observation point, when there is fault free, a CS fault in LF, a DSS fault in VCO and a GDS fault in CP.

The three fault cases are analysed below:

1) CS fault in the LF

The capacitor in the LF is mainly used to transform the current from CP to the control voltage inputted to VCO. When it is shorted, the current will be leakage. A change in control voltage will cause the frequency variation of VCO output signal. This fault is detected at $1.5 \ \mu s$.

| Parameters                  | Value          |
|-----------------------------|----------------|
| Reference clock ($f_{ref}$) | 25 MHz         |
| CMOS technology             | 0.13 μm        |
| VDD                         | 1.8 V          |
| VCO frequency ($f_{out}$)   | 1.6 GHz        |
| Current of CP ($I_{CP}$)    | 120 μA         |
| Gain of VCO ($K_{VCO}$)     | 41.8 MHz/V     |
| Capacitance of LF ($C_{LF}$)| 85 pF          |
| Coefficient of DBN ($N$)    | 64             |
| Power consumption           | 14.7 mW        |
| Chip area                   | $540 \times 580 \ \mu m^2$ |
| BIST area                   | $86 \times 50 \ \mu m^2$ |
| Locking time                | 2.8 μs         |
| RMS jitter (normal mode)    | 4.679 ps       |
| Peak-to-peak jitter (normal mode) | 28.75 ps     |

Abbreviations: BIST, built-in self-test; LF, loop filter; RMS, root mean square; VCO, voltage controlled oscillator.
2) DSS Fault in the VCO

The catastrophic structural faults occurred in the analogue part of system will cause serious influence on its output signals. As shown in Figure 10, when there is a DSS fault in the VCO, it is detected at 0.5 μs.

3) GDS Fault in the CP

The CP in CP-PLL needs to be well designed to avoid the problem of charge injection, clock feed-through, charge leakage, charge sharing, and the mismatch of charge and discharge current. However, any fault occurred in the CP will aggravating the non-ideal effect of itself, which may change the output of PLL. The test results of a GDS fault occurred in the CP are shown in Figure 10. The target transistor is selected from the discharge circuit. Thus, the operation of CP is...
the fault is detected at 0.5 μs.

Abbreviations: DSS, Drain; GDS, Gate.

| TABLE 6 | Fault types and coverage results |
|---------|----------------------------------|
| Fault types | Coverage Results | Fault types | Coverage Results |
| GDS      | 117/117          | SO           | 117/117          |
| GSS      | 116/117          | RS           | 4/4              |
| GO       | 114/117          | CS           | 7/7              |
| DSS      | 115/117          | RO           | 4/4              |
| DO       | 117/117          | ALL          | 99.16%           |

Abbreviations: DSS, Drain-to-source short; DO, Drain-open; GDS, Gate-to-drain short; GO, Gate-open; GSS, Gate-to-source short.

abnormally during the discharge test period. Results show that the fault is detected at 0.5 μs.

In Table 5, it lists the value of $T_{out}$ at different faulty cases, including the fault-free state. Different types of faults in all modules of CP-PLL are contained. Based on the fault models described in Section 3.3, the total number of faults in the structure of CP-PLL is 717, which are all tested to calculate the fault coverage. The fault simulation results show that the total number of detected faults is 711. Thus, the fault coverage is 99.16% (711/717), which indicates the effectiveness of proposed BIST technique.

The coverage results by proposed method are shown in Table 6. Affected by the tracking ability of PLL and the interference of noises, some kinds of faults have not been all detected. That is because the appearance of these faults has little effect on the CP-PLL, which would not affect its regular work, so that the logic state of DBN output is not changed. In this case, the scheme of judging whether there is a fault in the CP-PLL by extracted the feature of its output response is infeasible, but it also shows that these faults are less important for the structural test of CP-PLL. Nevertheless, the proposed method is simple, convenient and efficient with promising prospect in engineering application. It has a relatively high fault coverage of 99.16% and low area overhead of 86 × 50 μm² in 0.13 μm CMOS technology.

The comparisons with other works are summarised in Table 7. The proposed all-digital production test scheme yields a better coverage with a smaller hardware cost. Especially, the number of additional pins needed for test is the least, which demonstrates the proposed structure is more suitable for low-cost production test of CP-PLL when I/O port resources are limited.

### 6 | CONCLUSIONS

An all-digital CP-PLL BIST structure especially suitable for low-cost production tests when I/O port resources are limited is proposed in the paper. It has four main merits:

1) The proposed structure is simple and easily implemented with just a few DFFs, MUXs and some existing circuits in CP-PLL under test. It reduces the requirement of additional external test clocks and high-performance test equipment, which decreases the test cost of whole integrated circuits.

2) Combined with the proposed calibration technique on chip, it eliminates the effect of uncertain initial value of VCO input voltage on the frequency variation rate of VCO output signal. Thus the reliability of fault coverage is increased.

3) The additional BIST structure is all digital circuits and the final test output is also a pure digital value, which is easily extracted and processed. Thus the robustness and practicability of proposed BIST structure is increased.

4) The experiment results demonstrate that the proposed structure yields a relatively better fault coverage (99.16%) with a smaller hardware cost (1.37%).

Thus, it is efficient for low-cost production tests of CP-PLL.

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