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Active Auto-Suppression Current Unbalance Technique for Parallel-Connected Silicon Carbide MOSFETs

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Abstract: Nowadays, medium- and high-power applications make use of silicon carbide (SiC) MOSFETs, and many times their parallelization is necessary. Unfortunately, this requirement causes an inevitable current unbalance between power devices, affecting the performance of power switches. Over the last decade, numerous studies have been conducted, proposing various techniques with the capability of mitigating current unbalance for a number of discrete parallel SiC MOSFETs. However, the realization of most methods requires knowledge of the technical characteristics of power devices, adding extra cost to the system, since screening is a time-consuming and costly process. This necessity reduces the possibilities of such a technique being implemented in power electronics applications, preventing the exploitation of the exceptional features of SiC MOSFETs. In addition, most of these techniques can suppress only the current unbalance, which occurs during turn-on and turn-off transitions. In this paper, an active auto-suppression current unbalance technique is proposed, requiring no device screening. The active method is a closed-loop system capable of sensing and eliminating the entire current unbalance between parallel SiC MOSFETs automatically, actively, and independently of the cause. Simulation results are presented to demonstrate the feasibility and effectiveness of the proposed technique.

Keywords: wide band gap (WBG) semiconductors; silicon carbide (SiC) semiconductors; active current balancing technique; parallel connected MOSFETs

1. Introduction

Nowadays, a significant portion of energy needs is covered with the use of renewable energy sources (RES), reducing the environmental impact. Due to this fact, power electronic applications are in a state of continuous development and evolution. The basic requirements of new technology power converters are maximizing efficiency, minimizing volume, as well as high reliability and durability to short-circuit/overvoltage conditions. Although silicon (Si) devices have been the main switching elements of these applications for decades, silicon semiconductors have reached their limits without being able to meet the energy demands of our time. On the other hand, wide band gap (WBG) semiconductors could fill the void due to their exceptional characteristics over silicon ones.

Among WBG semiconductors, SiC MOSFET is one of the most popular WBG semiconductor devices with the most probabilities of responding with reliability to the field of medium and high-power density applications, due to its more stable construction, comparatively lower cost and, relatively mature technology [1,2]. Additionally, the most important advantages of SiC MOSFET are the higher breakdown voltage, its capability of operating in increased temperature environments, the high thermal conductivity, its superior switching characteristics with short turn-on and turn-off transient times and reverse recovery charge, the use of gate drivers with low complexity, the normally-off characteristic, and lower on-state resistance. Moreover, due to its unipolar structure, SiC
MOSFET does not appear tail current enabling the reduction of switching losses and higher switching frequency [1,3,4].

Despite its superior features, SiC MOSFET has a smaller die size in comparison with Si devices due to the lower yield in the wafer and high thermal-mechanical stress in the device. This is attributed to the manufacturing process of SiC MOSFET being less mature compared with the Si devices, making commercially available SiC MOSFETs incapable of offering high current capability. However, this limitation can be overcome by paralleling a number of SiC MOSFETs, increasing the power density of a system [5–9].

On the other hand, due to parallelization, a current unbalance between power devices is always evident. This phenomenon causes unequal conduction and switching losses and unequal distribution of junction temperature between parallel-connected devices, which may even lead the power switch(es) to thermal runaway [10,11]. That aside, a risk of over-current and simultaneously overheat is also probable, stressing the parallel power switch which carries a current greater than its nominal value. In this case, if the current unbalance is not suppressed, the power switch may receive severe damage or even be destroyed [5,12].

One of the reasons which provoke this inevitable current unbalance is the mismatch between the technical characteristics of the parallel SiC MOSFETs. Current unbalance which occurs during steady-state, known as static current unbalance, is attributed to the mismatch of on-state resistance ($R_{DS\text{on}}$) between parallel power switches. Moreover, current unbalance which appears during turn-on and turn-off transients, known as dynamic current unbalance, is caused due to the mismatched threshold voltage ($V_{th}$) and trans-conductance ($g_m$) [5]. Another reason is the asymmetry of the PCB layout, which has a negative effect on the current sharing of the devices [13]. Moreover, different temperature rise and electromagnetic interference (EMI) between parallel devices are caused by both types of unbalances, reducing the reliability of devices and system [14].

In an effort to overcome this problem, many scientific studies have been conducted and published over the last decade, proposing numerous techniques with the ability to mitigate one or even both types of current unbalances for a number of discrete parallel SiC MOSFETs.

In a few studies [5,15,16], an active current balancing method uses current sensors with the purpose of sensing the dynamic current unbalance directly and actively. In the process, a current balancing controller receives the unbalance and generates the proper corrections which should be implemented to the gate of one of the parallel devices. Finally, an active gate driver synchronizes the switching trajectories of the parallel power devices, based on the instructions of the controller. In this way, dynamic current unbalance is eliminated in a closed-loop and independently of the cause. In [5], the turn-on current unbalance was eliminated, and in [15,16], dynamic current balance was achieved.

Most of the published studies have proposed methods using passive elements, suppressing static or/and dynamic current unbalance. In [12,17], dynamic current unbalance was mitigated by connecting external gate resistors of the same size and extra coupled inductance. In this way, a difference between the voltage control levels of SiC MOSFETs occurs only during dynamic transients, limiting the overall dynamic current unbalance. Similarly, ref. [18] suppresses dynamic unbalance by adding extra gate resistors of different sizes. In this way, the impedances of the gate loops are differentiated, suppressing the dynamic unbalance only during turn-on transient. In [14], an extra resistor to the gate of the parallel-connected SiC MOSFET with the lowest threshold is added. As a result, the charging process of $C_{iss}$ of this particular SiC MOSFET is delayed, suppressing the turn-on dynamic unbalance. In [9,19], with the aid of series resistors of the same size, inserted into the parallel branches, static current unbalance was suppressed. Additionally, in [9], with the incorporation of a differential mode choke (DMC) both unbalances were mitigated. According to [9], the choke is able to eliminate the unbalance by utilizing magnetic flux as a media to transfer current from one branch to the other. In [20,21], both types of current unbalance were suppressed with the application of a coupled inductor connected...
in series with the drains of the SiC MOSFETs. Based on \([20,21]\), the higher the coupling coefficient, as well as the inductance of the coupled inductor, the more the overall current unbalance, is reduced. Moreover, refs. \([22,23]\) apply the aforementioned method in alternative ways, in order to suppress the current unbalance in a better way while limiting the disadvantages created by using coupled inductor.

In \([1,24–28]\), novel screening methods are proposed, capable of discovering SiC MOSFETs with almost identical technical characteristics, such as threshold voltage and trans-conductance, with the goal of achieving an equal current sharing without the necessity of a current balancing method. According to \([11,29]\), the current unbalance, which is attributed to the PCB layout asymmetry, can be limited by suppressing the mismatches of the drain and power source parasitic inductances, resulting in a very close symmetrical layout. However, ref. \([30]\) addresses the unbalance caused by asymmetric PCB layout, connecting a common mode choke to the gate loops of each parallel SiC MOSFET. This technique is based on the assumption that the greater the mutual inductance of the choke, the smaller the current unbalance. Based on \([31]\), an optimal dynamic current sharing was achieved because the effect of the threshold voltage mismatch can become less significant in case the value of the gate driver resistance is reduced. This results in a reduction in the switching transitions of the power switches due to the increase in the gate current of SiC MOSFETs, reducing the dynamic unbalance.

In addition, ref. \([32]\) proposes a technique for suppressing dynamic unbalance by using an intelligent gate driver capable of generating driving pulses (PWMs) with different propagation delays for the parallel SiC MOSFETs. The proposed technique can impose driving pulses with a time resolution difference of picoseconds.

All the aforementioned techniques manage to limit static or/and dynamic current unbalance between a number of parallel-connected SiC MOSFETs in their own way and extent. However, most of these techniques lack the merit of easy implementation which has fundamental value in power electronics applications. The most important reason is that the knowledge of the actual technical characteristics of the parallel devices is required in order for these techniques to be implemented. This necessity adds extra cost to the system, as screening is a time-consuming and extremely costly process, preventing these techniques from being implemented in industry \([5]\). Additionally, none of the current balancing techniques can suppress both static and dynamic current unbalance combining the easy implementation merit.

One disadvantage between passive and active methods is that the latter requires a number of operating cycles, depending on the magnitude of unbalance until the current unbalance is eliminated. Nevertheless, active methods are an attractive solution because they do not only overcome the problem but also continuously inspect the current sharing state and guarantee its balance. Something similar to that is extremely important, as operating and temperature conditions vary during operation, severing current unbalance.

In this paper, an active auto-suppression current unbalance technique is proposed without requiring any information on the technical characteristics of the parallel devices. Additionally, the proposed method can mitigate both static and dynamic current unbalance during turn-on and turn-off transients automatically, actively, and irrelevantly of the cause. Additionally, the proposed method offers the ability to suppress the unbalance even from the first operating cycles. In Section 2, an analytical investigation on potential current balancing strategies is derived. In Section 3, the structure, capabilities, and design guidelines of the proposed method are described in detail. In Section 4, the performance of the proposed method against multiple impact factors is validated by a number of simulations under several parameter mismatch scenarios. In Section 5, an extension of the proposed suppression method is described. Finally, Section 6 sets out the conclusions of this research.
2. Investigation of Current Unbalance Suppression

In this section, an analysis of the parameters which provoke static and dynamic current unbalances is performed. Additionally, an investigation on strategies that may result in a balanced current sharing between devices is conducted.

2.1. Dynamic Unbalance Mitigation Strategies

As mentioned above, dynamic current unbalance may occur due to parameter mismatch of devices and deviation between parasitic elements of the power circuit. According to (1), turn-on delay \( t_{d(on)} \) depends on device parameters. As a result, during turn-on transition, \( t_{d(on)} \) mismatch, deriving from device parameter deviation, will lead to dynamic current unbalance [16].

\[
t_{d(on)} = R_G C_{iss} \ln \left( \frac{V_{CC}}{V_{CC} - V_{th}} \right) \quad (1)
\]

Additionally, during the turn-on transition and before drain-source voltage \( V(DS) \) across the device starts to decrease, the drain current of SiC MOSFET reaches its maximum [16]. During this interval, the device is in saturation mode and its drain current can be expressed by (2).

\[
\frac{dI_D}{dt} = \frac{V_{CC} - V_{th} - i_D/g_m}{L_S + R_G C_{iss}/g_m} \quad (2)
\]

where \( V_{CC} \) is the gate driver high-level output; \( V_{th}, g_m, \) and \( C_{iss} \) are the threshold voltage, the transconductance, and the input capacitance of the device, respectively; \( i_D \) is the drain current; \( L_S \) is the source inductance common to both gate and power loop; and \( R_G \) is the gate driver resistance. Based on (2), it is concluded that the slew rate of drain current depends on several factors and any mismatch of these factors between devices will also result in dynamic current unbalance. As for the turn-off transition, Equations (1) and (2) can be written in a similar way. In conclusion, Equations (1) and (2) indicate that \( t_s \) and \( di_D/dt \) depend on the magnitude of \( R_G \) [16].

When SiC MOSFET driver outputs \( V_{CC} \), the gate current \( (i_G) \) begins to charge the gate-drain capacitance \( (C_{GD}) \) and the gate-source capacitance \( (C_{GS}) \). Therefore, \( i_G \) is expressed as (3), where \( i_{GD} \) and \( i_{GS} \) are the charging currents of the \( C_{GD} \) and \( C_{GS} \), as shown in Figure 1. The parameters \( L_{D,int}, L_{S,int}, \) and \( L_{G,int} \) come from the pins of SiC MOSFET devices which are mainly caused by the production process and manufacturing technology.

\[
i_G = i_{GD} + i_{GS} \quad (3)
\]

When \( R_G \) is large enough, the effect of the parasitic inductance \( L_G \) of the gate loop on \( V_{GS} \) can be neglected. For the loop of the gate drive current \( i_G \), the Kirchhoff voltage equation can be written as

\[
i_G = \frac{V_{CC} - V_{GS}(t) - L_{S,int} \frac{di_{GS}(t)}{dt}}{R_G} \quad (4)
\]

Based on (4), the gate current \( (i_G) \) that charges and discharges \( C_{GS} \) capacitance depends on the \( R_G \) value, affecting the switching behavior of the device. Therefore, dynamic current unbalance suppression can be achieved by adjusting the magnitude of \( R_G \) with the purpose of modifying the gate current, affecting the \( di_{GS}/dt \) and \( i_G \) of both SiC MOSFETs.
Ref. [23] states that transient unbalance can be reduced by matching the time delays of the devices. This can be achieved by changing the firing angle and duty cycle of the driving pulse affecting $t_d$ directly. During turn-on transient, the device, carrying the largest current during this stage, turns on faster than the other power switch. Therefore, increasing the firing angle of the driving pulse which controls the fastest device will make it turn on slower, reducing turn-on unbalance between devices. In addition, during the turn-off transient, the device carrying the largest current during this interval turns off slower than the other one. In this way, reducing the duty cycle of the driving pulse which controls the slowest device will make it turn off faster suppressing turn-off unbalance between them. In conclusion, dynamic unbalance could be eliminated by properly adjusting the firing angle and duty cycle, synchronizing switching delays of devices. The switching time delay during turn-on and turn-off transients can be expressed as (5) and (6), where $t_{d,\text{angle}}$ and $t_{d,\text{DC}}$ are the times corresponding to the firing angle variation and duty cycle modification, respectively.

$$t_{d,\text{on,total}} = t_{d,\text{on}} + t_{d,\text{angle}}$$  \hspace{1cm} (5)

$$t_{d,\text{off,total}} = t_{d,\text{off}} - t_{d,\text{DC}}$$  \hspace{1cm} (6)

Based on [16], the current unbalance level between turn-on and turn-off transients cannot be the same due to different gate drive strength and current/voltage waveforms at the drain. As a result, to achieve a well-balanced current sharing, independent control for on and off transitions is necessary.

### 2.2. Static Unbalance Mitigation Strategies

Since $V_{DS}$ of SiC MOSFET becomes much smaller than gate-source voltage minus the threshold voltage ($V_{GS} - V_{th}$), SiC MOSFET can be equivalent to an on-resistance ($R_{DS-on}$), as shown in Figure 2. $L_D$ is the sum of the parasitic inductance in the drain terminal and the one deriving from the PCB layout or the wiring. Additionally, $L_S$ is attributed to the source terminal and has the same meaning as $L_D$.

As mentioned earlier, the main reason for static current unbalance is provoked by the $R_{DS-on}$ mismatch of devices. Similar to Si MOSFET, SiC MOSFET $R_{DS-on}$ also offers the positive temperature characteristic (PTC). Therefore, SiC MOSFET with the higher junction temperature will carry less of the total current because its $R_{DS-on}$ increases. This thermal capability of on-state resistance could be used for the suppression of static current unbalance. However, the thermal sensitivity of SiC MOSFET $R_{DS-on}$ is limited and is not common for all SiC MOSFET models [9]. Therefore, it would not be wise to rely on the positive...
temperature coefficient (PTC) character of SiC MOSFET $R_{DS-on}$ for suppressing static current unbalance.

![Figure 2. Equivalent circuit of parallel SiC MOSFETs in steady-state.](image)

Because SiC MOSFET is treated as resistance during steady-state, the drain current can be expressed as (7) and static current unbalance ($\Delta i_{DS,\text{static}}$) for two parallel-connected SiC MOSFETs can be calculated by (8).

$$i_{DS} = \frac{V_{DS}}{R_{DS-on}}$$  \hspace{1cm} (7)

$$\Delta i_{DS,\text{static}} = \frac{V_{DS} \Delta R_{DS-on}}{R_{DS-on,1} R_{DS-on,2}}$$  \hspace{1cm} (8)

Based on (8), static current unbalance becomes less when $R_{DS-on}$ mismatch ($\Delta R_{DS-on}$) between power devices decreases. Based on [33], the drain current of an N-channel FET in the linear region can be expressed as (9).

$$i_{D} = \mu_n C_{OX} \frac{W}{L} [(V_{GS} - V_{th}) V_{DS}] \text{ for } V_{DS} \ll (V_{GS} - V_{th})$$  \hspace{1cm} (9)

where $\mu_n$ is the electron mobility, $C_{OX}$ is the oxide capacitance, $W$ is the width of the gate, and $L$ is the length of the gate. Combining (7) and (9), on-state resistance can be written as (10).

$$R_{DS-on} = \frac{1}{\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{th})}$$  \hspace{1cm} (10)

According to (10), $R_{DS-on}$ depends on $V_{GS}$, and (7) states that drain current of SiC MOSFET during steady-state depends on $R_{DS-on}$. As a result, with the proper modification of the correct power switch $V_{GS}$, $\Delta i_{D,\text{static}}$ can be mitigated, offering a well-balanced current sharing during steady-state.

Except for static current unbalance, $V_{GS}$ modification influences dynamic unbalance as well. Based on [19], during the switching process of the device, $i_D$ satisfies the following relationship:

$$i_D = \begin{cases} 
0 & V_{GS} \leq V_{th} \\
\frac{g_m}{I_L} (V_{GS} - V_{th}) & V_{th} < V_{GS} < V_{GP} \\
V_{GS} > V_{GP} & \end{cases}$$  \hspace{1cm} (11)

where $V_{GP}$ is the plateau voltage generated by the Miller effect and $I_l$ is the load current.

Thus, the dynamic unbalance can be affected, as the gate–source voltage difference ($\Delta V_{GS}$) increases since the drain current depends on $V_{GS}$ during this stage. However, trying
to minimize the overall unbalance only by increasing $\Delta V_{GS}$ is not an efficient strategy because $\Delta V_{GS}$ does not have the same influence on both unbalances.

For this reason, static current unbalance should be minimized by increasing $\Delta V_{GS}$ and in the process, dynamic unbalance should be dealt with one or even with a combination of the aforementioned dynamic current balancing strategies.

3. Active Current Balancing Technique Design

Current unbalance is an unpredictable phenomenon that can be attributed to several impact factors. For this reason, static and dynamic current unbalances should be both actively inspected and suppressed. Additionally, a current balancing technique should require the least necessities for its realization, such as the requirement of knowing the deviation of the technical characteristics of parallel power switches.

In this section, the general structure and operation principle of the proposed method is introduced in detail. To solve the current unbalance problem, the proposed technique consists of three parts, as depicted in Figure 3.

1. Current sensors: For each SiC MOSFET, a current sensor is used and required to measure the level of the parallel currents, providing information about the magnitude of the current unbalance. Each current is sensed through a current sensing resistor. In the process, the sensed voltage across the resistor is amplified by a voltage amplifier, and the amplified voltage is sampled and digitalized through an Analog to Digital Converter (ADC) of high sampling capacity.

2. Digital controller: A digital controller is utilized to generate the driving pulses of the power switches. In addition, in each cycle, it samples the currents through the Analog to Digital Converters and estimates the current unbalances during steady and transient states. In the process, if current unbalance exists, the controller can impose the proper corrections to a number of parameters, such as $V_{GS}$, $R_G$, $t_{angle}$ and $t_{DC}$, minimizing both static and dynamic unbalance during turn-on and turn-off transients.

3. Gate driver circuits: Finally, for each power device, a gate driver circuit with the ability to control the SiC MOSFETs and actively modify $V_{GS}$ and $R_G$, based on the instructions of the digital controller, is mandatory.

The three parts form a negative feedback loop, which can actively inspect and suppress current unbalance regardless of the cause of it.

![Figure 3. Block diagram of the proposed technique.](image)

3.1. Structure and Characteristics of the Proposed Gate Driver

According to the above investigation, all parameters that affect current unbalance are related to the gate drivers controlling SiC MOSFETs and also to the source that generates their driving pulses. Therefore, a gate driver with the ability to modify these parameters during the operating process for balancing parallel currents is needed. In order for the proposed method to apply different changes to each SiC MOSFET control parameter, suppressing current unbalance, a gate driver is required for each parallel power switch.
3.1.1. Proposed Gate Driver Circuit Operation Principle

As shown in Figure 4, the proposed gate driver is derived by a driving circuit that activates and deactivates SiC MOSFET by applying the control voltages $V_{CC}$ and $V_{ee}$, respectively. The variation of the $V_{CC}$ is conducted with the aid of a forward converter which is inserted between the $V_{CC}$ power supply and the driving circuit, providing dc-dc voltage isolation, as well. In this way, the $V_{CC}$ of SiC MOSFET can be actively changed by varying the duty cycle of the PWM signal which controls the forward converter switch. The control of the duty cycle, as well as the driving pulse of the forward converter switch, is performed by the digital controller. In this way, static current balance can be achieved by the proper adjustment of the correct $V_{CC}$.

Figure 4. Proposed Gate Driver developed in the Matlab/Simulink.

As mentioned earlier, dynamic unbalance can be minimized under the condition of producing driving pulses with different firing angles and duty cycles of picosecond time resolution. Such time displacement is too small and cannot be achieved by all commercially available digital controllers. For this reason, most of the dynamic unbalance can be suppressed by varying firing angle and duty cycle, whereas the rest of the unbalance can be eliminated by adjusting the gate currents of the power switches. Additionally, this current unbalance suppression pattern makes the proposed method capable of mitigating any current unbalance, regardless of its magnitude.

Gate Driver Design

The gate current variation can occur by changing the magnitude of the gate resistance. As shown in Figure 4, the branch which is connected to the SiC MOSFET gate terminal comprises two sub-branches. The above branch consists of a fixed resistor ($R_{on}$) connected in series with an auxiliary low power silicon MOSFET ($M-on$) whose $R_{DS-on}$ depends on its control voltage. Therefore, by actively changing the control voltage of the auxiliary MOSFET, the overall resistance of the upper branch can be changed affecting the turn-on delay of the SiC MOSFET. The lower branch consists of the same elements as the upper one, with the difference that the control voltage variation of the auxiliary MOSFET ($M-off$) of the lower branch affects the discharging gate current and consequently the turn-off delay of the SiC MOSFET. Each of these branches includes a diode ($D_{g-on}$ and $D_{g-off}$), connected in series with their elements in order to control the charging and discharging currents independently. For the control voltage variations of the auxiliary MOSFETs, two forward converters are also used.

Therefore, by changing the duty cycle of each forward converter switch, the control voltage of the auxiliary MOSFETs can be actively changed. The control of the duty cycles along with the driving of the switches of the forward converters is performed by the digital controller. To control the power switch and the forward converter switches, the digital controller totally produces four different driving pulses (PWM).
Design Guidelines of the Forward Converter

The minimization of current unbalance depends on the magnitude of the maximum clock frequency of the digital controller. In order for the controller to generate each PWM signal, a step-up counter with reset ability is used. As shown in Figure 5, for each positive edge of the clock, the counter increases by one step and resets when its count reaches a certain value.

![Figure 5. Concept of PWM driving signal generation.](image)

Based on this function, the PWM frequency can be set, and the duty cycle can be adjusted. As shown in Figure 5, PWM is “high” when the counter ranges between two values (e.g., 0 to 5) and “low” whether it exceeds a specific value (e.g., higher than 5). The higher the clock frequency, the more times the counter can count in a certain time period. As a result, firing angle and duty cycle variations become smaller as clock frequency increases. In this way, minimizing dynamic unbalance by modifying the firing angle and the duty cycle becomes even more feasible and effective. In addition, the minimum variation step of the control voltages becomes even smaller, making the elimination of both static and dynamic unbalances even more possible. Therefore, the minimum control voltage modification step \( V_{\text{var,step}} \) can be calculated by (12), where \( V_{\text{out}} \) and \( f_{\text{sw}} \) are the output voltage and switching frequency of the forward converter, respectively. Additionally, \( f_{\text{clk}} \) is the utilized clock frequency for the counter behind PWM generation. Therefore, the minimum voltage output variation can be reduced by using a digital controller, operating at high \( f_{\text{clk}} \), and lowering \( f_{\text{sw}} \) of forward converter as much as possible. However, utilizing a digital controller with quite high fundamental \( f_{\text{clk}} \) capability is a costly solution. In conclusion, \( f_{\text{sw}} \) selection is quite important for both static and dynamic unbalance suppression, making the implementation of the proposed method more cost-efficient.

\[
V_{\text{var,step}} = \frac{V_{\text{out}}}{f_{\text{sw}}} \frac{f_{\text{sw}}}{f_{\text{clk}}}
\]  

Nonetheless, design of forward converter is also crucial for the output voltage ripple of the converter and especially for the \( V_{\text{gs}} \) which affects SiC MOSFET driving process. Figure 6 shows the forward converter topology that is used for the construction of the proposed gate driver, along with the parasitic elements of the \( LC \) filter. \( R_s \) and \( ESR \) are the equivalent series resistances of the inductor and the capacitor, respectively, and \( R_p \) represents the parallel resistance, which is correlated with the parallel leakage path, associated with the inductor. Based on (13), output inductor current ripple \( \Delta I_{\text{L,x}} \) can be reduced by increasing switching frequency, reducing the needness for a larger \( LC \) filter. However, (12) states that increasing \( f_{\text{sw}} \), results in \( V_{\text{var,step}} \) increase. In addition, (13) states that inductor (\( L \)) selection influences \( \Delta I_{\text{L,x}} \), and (14) supports the idea that capacitor (\( C \)) magnitude affects output voltage ripple \( \Delta V_{\text{out}} \). Therefore, \( \Delta V_{\text{out}} \) can also be reduced by the proper selection of \( LC \) values. For selecting \( LC \) magnitude, it should be considered, that the larger the inductor magnitude is, the larger its parasitic resistors are, resulting in a voltage drop in the converter output voltage. Another essential factor that affects unbalance mitigation is the transient response time which significantly depends on capacitor magnitude. Therefore, converter transient response time can be reduced by using a smaller capacitor, making the forward converter respond faster to duty cycle \( D \) variations and vary output voltage \( V_{\text{out}} \) in less time. In conclusion, the proper forward converter design is a trade-off between switching frequency and \( LC \) filter selection with the purpose of producing an output voltage with the least ripple, combining the ability to vary the output voltage in
quite short period of time (μseconds). In addition, resistance \( R \) should be as great as possible for reducing output current and power consumption, considering that \( R \) selection also affects the transient response time of the converter.

\[
\Delta I_{LX} = \frac{V_{out} (1 - D)}{L f_{sw}}
\]

(13)

\[
\Delta V_{out} = \Delta I_{LX} \left( \frac{1}{8 C f_{sw}} + ESR \right)
\]

(14)

**Figure 6.** Forward converter circuit.

### 3.2. Current Sensing System

Each \( I_o \) is measured by a current sensing resistor \( R_{shunt} \), connected in series with the drain of each parallel-connected SiC MOSFET. The current that flows through \( R_{shunt} \) develops a voltage across it which is proportional to the current passing through it. The magnitude of the shunt resistor should be quite small, on the order of milliohms (mΩ), without resulting in significant power loss and reducing the efficiency of the system. In addition, the current level should be affected as little as possible. As a result, the voltage developed across each shunt resistor is also quite small and requires amplification before being converted by the ADC. For this reason, a differential amplifier circuit using an operational amplifier (OPA) is implemented that converts the small differential voltage developed across the shunt resistor to a larger output voltage. The current sensing circuit which includes the \( R_{shunt} \) and the differential amplifier along with the current sensing system is shown in Figure 7b. Assuming that \( R_1 = R_2 \) and \( R_1 = R_2 \), the amplified voltage \( V_{amp} \) of sensed voltage \( V_{shunt} = V_2 - V_1 \) across \( R_{shunt} \) is given by:

\[
V_{amp} = \frac{R_f}{R_1} (V_2 - V_1)
\]

(15)

The reliability of the proposed current balancing method depends, to a large extent, on measurement accuracy and response time of current sensing system, especially for capturing the transient behavior of the power switch current with high fidelity. According to [34], \( R_{shunt} \) can offer great accuracy when its measurement bandwidth is quite high on the order of hundreds of megahertz, and its parasitic inductance is quite low on the order of nanohenry or even fractions of nanohenry (nH). In addition, the tolerance of \( R_{shunt} \) should be quite small keeping measurement accuracy as steady as possible. Moreover, \( R_{shunt} \) magnitude can be affected by temperature variations, even transient ones, resulting in measurement uncertainty. To overcome this problem, the temperature coefficient of \( R_{shunt} \) should be low, mitigating temperature influence upon \( R_{shunt} \) value. Another factor that affects measurement accuracy is the settling time of the operational amplifier which is the time it takes the output to respond to a step change of the input and it is the principal factor that determines the maximum data transfer rate for a given accuracy. In addition, settling time includes a very brief propagation delay, plus the time required for the output to be slew to the vicinity of the final value [35]. For these reasons, settling time should be ranged within several nanoseconds to synchronize with \( V_{shunt} \) step changes. Measurement accuracy is also related to the sampling rate of ADC which should be large enough for the digital controller to sense the rapid changes in the current and with the least error due to
ADC resolution. Therefore, the response time of both $R_{\text{shunt}}$ and amplifier should be within the sampling time of ADC to maintain the desired accuracy of the current measuring system.

![Figure 7. Schematic of: (a) current sensing system; and (b) shunt resistor and differential amplifier.](image)

To investigate the performance of the current sensing system and especially at capturing the switching variations of currents, a simulation is performed, measuring the currents of the two parallel-connected SiC MOSFETs. The purpose of this test is to compare the measurement accuracy between the Simulink probes, the amplified $V_{\text{amp}}$ signals, and the output voltages of the ADCs during turn-on and turn-off intervals. Based on [34], it is possible to tackle the parasitic inductance, overcoming the measurement problems caused by the presence of parasitic inductance resistor. Therefore, it is assumed that the parasitic inductance of $R_{\text{shunt}}$ is too low and can be neglected. The magnitude of $R_{\text{shunt}}$ is 5 mΩ, its tolerance is 0.1% and its temperature coefficient is assumed to be 15 PPM/°C, satisfying the above requirements about the proper selection of $R_{\text{shunt}}$. For the construction of the differential amplifier, $R_1 = R_2 = 2$ kΩ and $R_f = R_g = 400$ kΩ which means that the differential amplifier gain is two hundred. Its settling time is assumed to be a few nanoseconds, whereas each ADC samples the current at 200 Msps. ADC can sample only positive values of the SiC MOSFET current.

In addition, two different time delays are included. One is the propagation delay of each OPA, which is equal to 1 ns, as indicated by the LT1818 high-speed operational amplifier datasheet [36]. The other one is the sampling delay of each ADC, which is set to 2.6 ns, as also indicated by the ADC08200 Analog-to-Digital Converter datasheet [37]. According to Figure 8, there is a time difference ($\Delta t$) between the current signal of each Simulink probe (light blue and purple) and its amplified $V_{\text{amp}}$ signal (orange and blue). This time difference is attributed to the propagation delay of each operational amplifier. However, the currents measured by the Simulink probes and the amplified $V_{\text{amp}}$ signals are at the same level during the time duration. Therefore, the sensing process with the usage of current sensing resistors is accurate. The only measurement error derives from the sampling capacity of each ADC and its resolution (brown and green).
3.3. Digital Controller Functions

The digital controller of the proposed active current balancing process includes several basic functions, as shown in Figure 9. Initially, the controller receives the currents of the parallel SiC MOSFETs through the external ADCs, inserted between each sensor and the controller with the purpose of converting the analog sensor signals to digital form. In each cycle, the controller directly samples the currents during steady-state as well as turn-on and turn-off transients, separately. In the process, it estimates the magnitude and polarities of the three unbalances during the three stages. In addition, it examines whether static or/and dynamic unbalance exists and automatically identifies which of the parallel SiC MOSFETs carries the largest and least current during the three stages. Once the operating process has been entered in steady-state, the controller starts to apply the appropriate corrections to the control parameters of the correct SiC MOSFET, until the overall unbalance is minimized. Finally, in case the overall unbalance is reduced under a specific level, the controller can store the modifications applied to the control parameters, avoiding repeating the entire balancing process in every ignition of the power application. In the next subsections, the basic functions of the digital controller are described in detail.

3.3.1. Current Sampling System

The digital controller samples the parallel currents at the proper time point/areas of the period during the three current states. For the estimation of the static current unbalance, the current sampling system samples the parallel currents during steady-state at a specific time point \( (i_{\text{static}}) \), as shown in Figure 10. As for the dynamic current unbalance measurement, the sampling system can detect the peaks of parallel currents during turn-
on and turn-off transients ($i_{\text{on-peak}}$ and $i_{\text{off-peak}}$, respectively), around the proper time areas of the period, as shown in Figure 11.

![Figure 10. Current sampling points during steady-state.](image)

**Figure 10.** Current sampling points during steady-state.

![Figure 11. Current sampling points during: (a) turn-on state; and (b) turn-off state.](image)

**Figure 11.** Current sampling points during: (a) turn-on state; and (b) turn-off state.

In addition, during the turn-on transient, the sampling system samples the parallel currents when PWM becomes “high” and until both currents exceed a certain limit, as shown in Figure 12a. Contrariwise, during turn-off transient, the sampling system samples the parallel currents when PWM becomes “low” and until both currents become smaller than a specific limit, as shown in Figure 12b. In this way, the digital controller can measure the turn-on ($t_{\text{on}}$) and turn-off ($t_{\text{off}}$) time delays of each SiC MOSFET and calculate their differences ($\Delta t_{\text{on}}$ and $\Delta t_{\text{off}}$, respectively). Moreover, the sampling system samples the parallel currents during the turn-off state to discover the greatest difference between parallel currents during this interval ($\Delta i_{\text{off-max}}$), as shown in Figure 13. The digital controller is synchronized with the driving signals of the power switches and is capable of automatically changing the sampling time point/areas according to the duty cycle and the operating switching frequency. The AD conversion of current signals is required for the implementation of the proposed method by feeding the signal to the digital controller. The sampling rate for AD conversion is crucial to minimize the peak current sampling error as well as to capture the rapidly varying feedback signal. In this case, the sampling frequency of the ADC is adopted to capture the dynamic characteristic of MOSFET currents significantly considering the fundamental clock. This is because the sampling rate of the ADC is provided by the digital controller. The higher the fundamental frequency clock of the controller, the higher the sampling rate of the ADC can be.
3.3.2. Current Unbalance Suppression System of the Digital Controller

Once the current sampling process is complete, the digital controller estimates the magnitudes and the polarities of the three unbalances, checking if static or/and dynamic unbalance exists. The controller does not initiate the current balancing process from the first cycle but when the operating process has been entered in steady-state. In this way, the current unbalance estimation is more precise.

In the next stage, the controller begins to apply the necessary corrections to the control parameters of the appropriate SiC MOSFET, suppressing the three types of unbalances in a specific order, and not simultaneously, as shown in Figure 14. If the static current unbalance is greater than a specific limit (e.g., 0.1 A), the controller only starts to increase the $V_{CC}$ of the power switch that carries the least current during steady-state, suppressing static current unbalance and affecting dynamic current sharing. If $V_{CC}$ increases to a certain point and static current unbalance still exists, the controller ceases to increase $V_{CC}$ and starts to decrease the $V_{CC}$ of the power switch that carries the greatest current during steady-state.

As soon as the static unbalance becomes less than a certain value, if dynamic unbalance still exists, the controller performs the following described actions to suppress it. To minimize dynamic unbalance, peak currents during turn-on and turn-off transitions should be as equal as possible. If the turn-on dynamic unbalance is greater than a predefined limit ($\gamma_{\text{dynamic}}$) and $\Delta t_{\text{on}}$ is greater than zero, the controller begins to increase only the firing angle of the pulse which controls the SiC MOSFET, carrying the largest current during turn-on transient, suppressing the turn-on unbalance. Whether this unbalance decreases under $\gamma_{\text{dynamic}}$ or $\Delta t_{\text{on}}$ becomes zero, the controller does not modify the firing angle any further but reduces the charging gate current of the SiC MOSFET, carrying the largest current, by increasing the $R_{DS\text{-on}}$ of the appropriate auxiliary MOSFET to the point of min-
imizing the difference between peak currents during turn-on. In case the controller realizes that turn-off dynamic unbalance exists, if this unbalance is greater than \( \gamma_{\text{dynamic}} \) and \( \Delta I_{\text{td,off}} \) is greater than zero, the controller begins to reduce only the duty cycle of the pulse controlling the SiC MOSFET carrying the highest current during turn-off. When this unbalance decreases below \( \gamma_{\text{dynamic}} \) or \( \Delta I_{\text{td,off}} \) is zero, the controller ceases to modify the duty cycle. In the process, the controller begins to increase the charging gate current of the SiC MOSFET carrying the largest current during turn-off transient by reducing the \( R_{DS(on)} \) of the appropriate auxiliary MOSFET to the point of minimizing the difference between peak currents as well as the maximum current difference during turn-off. The mitigation of both dynamic unbalances is carried out simultaneously.

Figure 14. Flow of the suppressing order of the three current unbalance types.

If for some reason static unbalance becomes greater than a specific value, then the suppression of the dynamic unbalance is suspended until static unbalance is reduced once again below the predetermined limit. The fact that the balancing process follows this pattern is particularly important. When static unbalance exists, the two dynamic unbalances include both their own and the static one as well. Therefore, these unbalances are far greater compared with the case when the static current balance has been achieved. If this precaution is not taken, the digital controller may impose unnecessary modifications to the control parameters in order to suppress transient unbalances.

The current balancing procedure of each unbalance is shown in Figure 15. Before the ignition of each operating cycle, the controller identifies which of the control parameters between the two SiC MOSFETs has previously received modifications to their control parameters (e.g., \( V_{GS1} \) and \( V_{GS2} \)). In Figure 15, \( \text{Mod,1} \) and \( \text{Mod,2} \) represent the modifications upon control parameters of the two power switches. If neither of the two control parameters has been previously modified, the controller follows the current balancing pattern which is described above. Otherwise, the controller checks the correctness of the imposed modifications considering the current unbalance polarity (\( \text{Pol} \)). If the polarity is consistent with the correctness of the modifications, the controller maintains the modification method. If not, the controller applies the modification method in the opposite way. For instance, if \( i_{D1} > i_{D2} \) during steady-state, the controller normally will attempt to increase \( V_{GS2} \). As long as \( \Delta I_{\text{d,static}} \) exists and \( i_{D1} \) remains greater than \( i_{D2} \), the controller will continue to increase \( V_{GS2} \) in each cycle. In case \( i_{D1} \) becomes less than \( i_{D2} \) and \( \Delta I_{\text{d,static}} > 0.1 \) A, the controller starts to decrease \( V_{GS2} \) until \( \Delta I_{\text{d,static}} \) is minimized. As mentioned above, current unbalance elimination is strongly related to the minimum modification step. However, modifying control parameters by using only the minimum variation step requires a significant number of balancing cycles until the balancing process is complete, especially when unbalance is too great. Therefore, it is essential to utilize greater modification steps to suppress the unbalances as quickly as possible, reducing the required balancing cycles. For this reason, the digital controller examines the effect of
every minimum variation step on each current unbalance and appropriately increases it, eliminating a portion of the current unbalance in each cycle. As shown in Figure 15, the controller calculates the size of the modification step ($\Delta_{\text{step}}$) which was imposed during the previous cycle. If $\Delta_{\text{step}}$ is zero, the controller uses the least modification step ($LS$) for the upcoming cycle. Otherwise, the controller calculates the increase, the modification step should receive, by executing the following procedure. As shown in Figure 15, it calculates the current unbalance which was suppressed through the imposition of the modification step which was imposed in the previous cycle ($\Delta_{\text{icycle}}$) dividing it with $\Delta_{\text{step}}$. In this way, the controller discovers the magnitude of the current unbalance that can be suppressed by imposing one modification step ($A$). In the process, the controller calculates the increase in the modification step ($CS$) with the goal of reducing the current unbalance by a specific magnitude ($\Delta_{\text{istep}}$) by dividing $\Delta_{\text{istep}}$ with $A$. Finally, the total step will be the sum of $CS$ and $LS$ which is imposed during the ignition of the next cycle. In this way, the current balancing process can be executed in a safe manner without requiring a significant number of operating cycles until it is completed. The calculation of $CS$ applies only for the mitigation of the unbalance with the aid of the forward converts. As for the variation of the firing angle and duty cycle, the controller always uses their minimum variation steps to mitigate dynamic unbalance.

![Figure 15. Flow of current balancing process.](image)

3.3.3. Modification Storage System

Besides the advantages of the active balancing methods mentioned above [5,15,16], a characteristic disadvantage of them is the necessity for a significant number of operating cycles until the current unbalance is eliminated, depending on its magnitude [38]. Therefore, these techniques are incapable of offering a well-balanced current distribution from the first cycle. Such a requirement may be a difficult task, but it is possible to reduce the number of balancing cycles. For this reason, if the overall unbalance is reduced under a certain limit, the digital controller can store a combination of applied modifications upon control parameters. Additionally, the digital controller imposes a stored combination in each next activation of the application, avoiding repeating the whole current balancing process from the beginning. Therefore, in the next starting of the application, the number of the required operating cycles will be decreased, allowing the balancing process to require only a few balancing cycles until the current balance is achieved.

All the aforementioned capabilities can be executed with an algorithm that can be implemented into a field programmable gate array (FPGA). Refs. [39,40] have successfully applied active current balancing methods for parallel-connected IGBTs using a current
balancing algorithm, implemented into an FPGA. Additionally, Refs. [41,42] have successfully implemented a balancing current algorithm into a complex programmable logic device (CPLD) and a digital signal controller (DSC) in balancing currents between parallel-connected SiC MOSFET modules and SiC JFETs, respectively. Additionally, these methods manage to achieve an adequate time resolution to handle the current unbalance issue since SiC devices normally switch much faster than IGBTs.

4. Test Platform and Simulation Results

To evaluate the efficiency of the proposed method, a buck converter with two parallel-connected SiC MOSFETs was built as the test platform inside Matlab/Simulink.

4.1. Test Platform

As shown in Figure 16, the test platform includes the buck converter with the two parallel-connected SiC MOSFETs (M1 and M2), model C2M0080120D, and a SiC Schottky C4D40120D as the free-wheeling diode. For the implementation of the proposed technique, two current sensors, the digital controller, and two gate drivers are used. For the realization of the digital controller, an FPGA board has been developed within the Simulink environment, capable of performing all the functions which were described in the previous section. The FPGA board includes the FPGA block which contains the digital controller execution algorithm, written in the VHDL programming language with the aid of Xilinx Vivado, representing FPGA Artix-7 with a fundamental clock speed of 450 MHz. In addition, it contains a block that represents the Flash Memory in which the required modifications of all control parameters can be stored and loaded. It also includes a block that contains the FPGA outputs (FPGA Output Ports). The “FPGA Control Unit” block is responsible for the control of the duty cycle of the power buck converter as well as the switching frequency of the power switches. This block has two functions through which the inserted data of duty cycle and frequency are converted into the appropriate information needed by the FPGA algorithm to produce the driving pulses of the SiC MOSFETs. In addition, this block includes a pulse generator that produces the FPGA control pulses as well as a mechanism that resets the counters of the algorithm before their ignition. Each current sensor block includes a shunt resistor of 5 mΩ and a differential amplifier which amplifies $V_{\text{shunt}}$ by twenty. In this way, 3.3 V as an input voltage for each ADC is proportional to 33 A. All requirements about the proper selection of $R_{\text{shunt}}$ and operational amplifier have been considered.

![Figure 16. Test platform implemented in Matlab/Simulink.](image-url)

The digitalization of the analog signals deriving from the current sensors, are conducted with the aid of two external Analog to Digital Converters, capable of sampling...
at 200 Msps, connected to the FPGA board inputs. The current sensors send their information to the inputs of ADCs through the six blocks marked as “Id1” and “Id2”. Finally, for each parallel SiC MOSFET through the six blocks marked as “Id1” and “Id2”. Finally, for each parallel SiC MOSFET, the parasitic inductance attributed to PCB layout of power circuit are included ($L_d$ and $L_s$). In the test platform, “Gate Driver” blocks include the proposed gate driver. The initial values of the control voltages for the activation and deactivation of the SiC MOSFETs are set to 20–5 V, respectively. Both fixed gate resistors ($R_{g-on}$ and $R_{g-off}$) are 10 Ω whereas the initial values of the control voltages for both auxiliary MOSFETs ($M_{on}$ and $M_{off}$) are equal to 5 V.

The test conditions of the buck converter have been selected as follows: $V_{dc} = 600$ V, Duty Cycle = 70%, $R_{load} = 22$ Ω and frequency = 25 kHz. The layout is assumed symmetric to exclude the unbalance caused by layout ($L_d = L_s = L_d = L_s = 20$ nH). The proposed technique requires a drive circuit for each parallel SiC MOSFET. This requirement causes an additional dynamic current unbalance due to the propagation delay difference between gate drivers. For this reason, the propagation delay of the gate driver which controls M2 is 5 ns greater than the gate driver of M1. Finally, junction temperatures of SiC MOSFETs are the same and equal to 70 °C.

### 4.2. Simulation Results under Mismatched Parameters

In this subsection, the reliability of the proposed technique is examined by performing four simulations assuming that the two parallel devices have different technical characteristics, as shown in Table 1. Besides the effect of the mismatches of $R_{DS-on}$, $V_{th}$, and $g_m$ upon current sharing, [43] supports that $C_{iss}$ mismatch ($\Delta C_{iss}$) may also affect the current distribution and its effect should not be taken lightly. For this reason, the fourth simulation test is conducted using power devices with different $C_{iss}$. The results of the four simulations are shown in Figures 17–28, illustrating the drain current and switching power loss distribution between parallel devices, as well as the gate currents of SiC MOSFETs during turn-on and turn-off transients. Tables 2–5 show the modifications imposed on the control parameters by the proposed technique.

### Table 1. Device parameter mismatches of the four simulation trials.

| Simulation | $R_{DS-on,M1}$ (mΩ) | $R_{DS-on,M2}$ (mΩ) | $V_{th,M1}$ (V) | $V_{th,M2}$ (V) | $g_m,M1$ (S) | $g_m,M2$ (S) | $C_{iss,M1}$ (pF) | $C_{iss,M2}$ (pF) |
|------------|----------------------|----------------------|-----------------|-----------------|---------------|---------------|-----------------|-----------------|
| 1st        | 98                   | 80                   | 2.6             | 2.6             | 8.1           | 8.1           | 950             | 950             |
| 2nd        | 80                   | 80                   | 2               | 4               | 8.1           | 8.1           | 950             | 950             |
| 3rd        | 80                   | 80                   | 2.91            | 2.74            | 8.42          | 9.88          | 950             | 950             |
| 4th        | 80                   | 80                   | 2.6             | 2.6             | 8.1           | 8.1           | 1107.6          | 907.6           |

![Figure 17](image1.png)

(a)

![Figure 17](image2.png)

(b)

**Figure 17.** Simulation results, when $\Delta R_{DS-on} = 18$ mΩ: (a) without; and (b) with the proposed method.
Figure 18. Turn-on waveforms, power loss and gate currents, when $\Delta R_{D\cdotS\cdoton} = 18 \text{ m}\Omega$: (a) without; and (b) with the proposed method.

Figure 19. Turn-off waveforms, power loss and gate currents, when $\Delta R_{D\cdotS\cdoton} = 18 \text{ m}\Omega$: (a) without; and (b) with the proposed method.

Table 2. Control parameters (a) without solution; and (b) with modifications of the first simulation.

|   | $V_{G\cdotS\cdot1}$ (V) | $V_{G\cdotS\cdot2}$ (V) | $t_{dl\cdoton\cdot1}$ (ns) | $t_{dl\cdoton\cdot2}$ (ns) | $t_{dl\cdotoff\cdot1}$ (ns) | $t_{dl\cdotoff\cdot2}$ (ns) | $V_{ctl\cdotM\cdoton\cdot1}$ (V) | $V_{ctl\cdotM\cdoton\cdot2}$ (V) | $V_{ctl\cdotM\cdotoff\cdot1}$ (V) | $V_{ctl\cdotM\cdotoff\cdot2}$ (V) |
|---|----------------------|----------------------|--------------------------|--------------------------|---------------------------|---------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| (a) | 20                   | 20                   | 0                        | 0                        | 0                         | 0                         | 5                           | 5                           | 5                           | 5                           |
| (b) | 23                   | 19                   | 5                        | 0                        | 7.5                       | 0                         | 5                           | 4.97                        | 5.02                        | 5                           |
Figure 20. Simulation results, when $\Delta V_{th} = 2$ V: (a) without solution; and (b) with the proposed method.

Figure 21. Turn-on waveforms, power loss and gate currents, when $\Delta V_{th} = 2$ V: (a) without; and (b) with the proposed method.
Figure 22. Turn-off waveforms, power loss and gate currents, when $\Delta V_{th} = 2$ V: (a) without; and (b) with the proposed method.

Table 3. Control parameters (a) without solution; and (b) with modifications of the second simulation.

| a/a | $V_{GS,1}$ (V) | $V_{GS,2}$ (V) | $t_{dl,on,1}$ (ns) | $t_{dl,on,2}$ (ns) | $t_{dl,off,1}$ (ns) | $t_{dl,off,2}$ (ns) | $V_{ctl-M_{on,1}}$ (V) | $V_{ctl-M_{on,2}}$ (V) | $V_{ctl-M_{off,1}}$ (V) | $V_{ctl-M_{off,2}}$ (V) |
|-----|----------------|----------------|------------------|------------------|------------------|------------------|----------------|----------------|----------------|----------------|
| (a) | 20             | 20             | 0                | 0                | 0                | 0                | 5              | 5              | 5              | 5              |
| (b) | 20             | 20             | 12.5             | 0                | 0                | 0                | 5              | 4.98           | 5.07           | 5              |

Figure 23. Simulation results, when $\Delta V_b = 0.17$ V and $\Delta g_m = 1.46$ S: (a) without; and (b) with the proposed method.
Figure 24. Turn-on waveforms, power loss and gate currents, when $\Delta V_{th} = 0.17$ V and $\Delta g_m = 1.46$ S: (a) without; and (b) with the method.

Figure 25. Turn-off waveforms, power loss and gate currents, when $\Delta V_{th} = 0.17$ V and $\Delta g_m = 1.46$ S: (a) without; and (b) with the method.

Table 4. Control parameters (a) without solution; and (b) with modifications of the third simulation.

| a/a | $V_{GS,1}$ (V) | $V_{GS,2}$ (V) | $t_{dl,on,1}$ (ns) | $t_{dl,on,2}$ (ns) | $t_{dl,off,1}$ (ns) | $t_{dl,off,2}$ (ns) | $V_{ctl-M,on,1}$ (V) | $V_{ctl-M,on,2}$ (V) | $V_{ctl-M,off,1}$ (V) | $V_{ctl-M,off,2}$ (V) |
|-----|----------------|----------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|
| (a) | 20             | 20             | 0                 | 0                 | 0                 | 0                 | 5                | 5                | 5                | 5                |
| (b) | 23             | 19.81          | 5                 | 0                 | 0                 | 0                 | 5                | 5                | 4.97             | 5.02             | 5                |
Figure 26. Simulation results, when ΔCiss = 200 pF: (a) without; and (b) with the proposed method.

Figure 27. Turn-on waveforms, power loss and gate currents, when ΔCiss = 200 pF: (a) without; and (b) with the proposed method.
Figure 28. Turn-off waveforms, power loss and gate currents, when $\Delta C_{iss} = 200 \text{ pF}$: (a) without; and (b) with the proposed method.

Table 5. Control parameters (a) without solution; and (b) with modifications of the fourth simulation.

| a/a | $V_{GS,1}$ (V) | $V_{GS,2}$ (V) | $t_{dl,on,1}$ (ns) | $t_{dl,off,1}$ (ns) | $t_{dl,off,2}$ (ns) | $V_{ctl-M,on,1}$ (V) | $V_{ctl-M,on,2}$ (V) | $V_{ctl-M,off,1}$ (V) | $V_{ctl-M,off,2}$ (V) |
|-----|----------------|----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| (a) | 20             | 20             | 0                 | 0                 | 0                 | 5                 | 5                 | 5                 | 5                 |
| (b) | 20             | 20             | 0                 | 2.5               | 5                 | 0                 | 4.91              | 4.99              | 5                 |

Based on the above simulation results, before the activation of the proposed method, a large unbalance in the drain currents during steady-state and turn-on and turn-off transitions can be seen. On the other hand, once the operating process has been entered in steady-state, the proposed technique is enabled to begin to suppress the entire current unbalance. In all cases, the proposed method applies the proper adjustments to the appropriate control parameters, offering a well-balanced current sharing between power devices, verifying its performance against multiple impact factors. In addition, the switching power loss unbalance at both transitions is greatly reduced. As a result, a more evenly power loss distribution is achieved, improving the reliability of the system and making thermal management easier.

4.3. Efficiency of the Modification Storage System

As mentioned above, the digital controller can store a combination of modifications in case the three unbalances are kept at a low level. In addition, the controller applies the stored modifications during the beginning of the application. Once the operating process has been entered in steady-state, the current balancing process is initiated. In order to examine the efficiency of the storing ability, another two simulations are performed, when the technical parameters of the power switches are selected as follows: $R_{DS-on,M1} = 80 \text{ m}\Omega$, $V_{th,M1} = 2 \text{ V}$, $R_{DS-on,M2} = 98 \text{ m}\Omega$ and $V_{th,M2} = 4 \text{ V}$. In this simulation test, a comparison between the initial starting and a next one is conducted with the purpose of illustrating the magnitude of the current unbalance without and with the application of a stored combination of modifications during the beginning of the operating process. Figure 29a illustrates the current sharing between parallel SiC MOSFETs in case the controller does
not apply any stored combination at the beginning of the operating process. As shown in Figure 29b, the controller applies a stored combination of modifications from the beginning of the simulation. In Figure 29b, it is observed that the implementation of the stored modifications at the ignition of the application leads to a well-balanced current distribution even from the first operating cycles, illustrating the effectiveness of the controller storing capability. Additionally, the level of the overall unbalance is very low, resulting in low variation of conduction and switching losses even from the first operating cycles.

![Figure 29. Simulation results: (a) without; and (b) with a stored combination of modifications.](image)

As mentioned above, operating and temperature conditions change during the operating process. Therefore, it is unlikely that the same conditions will prevail at every initiation of the operating process. To further investigate the efficiency of the controller storing ability, another two simulations are performed. At the first simulation, the duty cycle is set to 40% instead of 70%, reducing the drain current level of each SiC MOSFET. At the second simulation, junction temperatures of SiC MOSFETs are equal to 40 °C. As illustrated in Figure 30, in both cases, a well-balanced current sharing between parallel devices is achieved, even if the operating and temperature conditions have changed. Nevertheless, the level of the whole current unbalance is quite low even from the first operating cycles.

![Figure 30. Simulation results using a stored combination of modifications: (a) with duty cycle of 40%; and (b) junction temperature of 40 °C.](image)

5. Extension of Proposed Current Balancing Method

The feasibility and effectiveness of the proposed current balancing technique have been examined only for two parallel-connected SiC MOSFETs. Nevertheless, medium- and high-power applications require increased current capacity. Therefore, the number of
parallel-connected devices cannot be limited to two parallel SiC MOSFETs, and the scalability of the proposed technique is very important. When more SiC devices are connected in parallel, the algorithm of the proposed method must be modified, because it is necessary to receive information about the currents from all current sensors. Additionally, the algorithm should be able to take decisions about the application of the correct modifications upon the control parameters of more than two power devices. In addition, one current sensor and one gate driver circuit are mandatory for each parallel-connected SiC MOSFET.

Based on [41], in the case of implementing an active closed-loop current balancing technique for more than two parallel-connected SiC MOSFETs, the most efficient control method for modifying control parameters of power devices is the master–slave topology. According to the master–slave control topology, one of the drain currents is defined as the master whereas the rest currents are defined as the slaves. In this way, the digital controller must apply the proper modifications to the correct control parameters, forcing the slave currents to reach the master one. To incorporate the master–slave topology into the proposed method, the master current should be pre-defined only between the currents of transient intervals. For this reason, the digital controller can autonomously decide which drain current should be defined as the master one during steady-state, to function properly and apply the proper adjustments to the correct parameters. In this way, the static current balancing process can be executed in a safer manner. On the contrary, the master current for the suppression of dynamic unbalance is set manually.

Before the ignition of the static current unbalance suppression, the digital controller samples the parallel currents during steady-state at a specific time point, as shown in Figure 31. In this way, it identifies which of the parallel currents during steady-state is the highest and defines it as the master current. In the process, it starts to apply the proper corrections to the control voltages of all SiC MOSFET currents which are not balanced with the master current, until currents during steady-state becomes balanced. However, the digital controller can modify the control voltage of the master SiC MOSFET, in case the control voltage adjustment of a slave SiC MOSFET is greater than 3 V, and static unbalance still exists between the slave SiC MOSFET and the master one.

**Figure 31.** Current sampling points during steady-state for three parallel-connected SiC MOSFETs.

Once static current unbalance is lower than 0.1 A, the digital controller begins to suppress dynamic current processes for both turn-on and turn off transients as described in the Section 3.3.2. Additionally, the transient suppression control parameters of the master SiC MOSFET, concerning the dynamic intervals, do not receive any modification.
6. Conclusions

This paper presents an active auto-suppression current unbalance technique for a number of parallel-connected SiC MOSFETs. The proposed method can sample the parallel currents during steady and transient states, individually, and estimate the magnitude of the three current unbalances, separately. It is also able to automatically identify the power device which carries the greatest current during these current states, based on the polarity of each unbalance. The proposed method does not require any knowledge about either the mismatch of the technical characteristics of the devices or the operating conditions. Additionally, it can modify the control voltage of the proper device(s) and actively suppress static current unbalance between parallel SiC MOSFETs. Moreover, it can tune the gate delays of the power switches by modifying the firing angle and duty cycle of the driving pulses, suppressing most portion of the dynamic unbalance. Additionally, it can vary the gate currents, matching the peak currents during turn-on and turn-off transitions and eliminating the rest of the dynamic unbalance. In addition, the proposed method can store a combination of modifications, with the purpose of using it in every next starting of the application, offering a well-balanced current sharing from the first operating cycles.

In conclusion, the proposed method is a negative feedback loop system that actively inspects the current sharing state and adjusts the modifications of the control parameters as operating conditions change. The forced current-sharing capability of the proposed active method is validated by several simulations, confirming its effectiveness and robustness against the impact factors which compromise the reliable operation of the power switches. All these merits increase the probabilities of the proposed method to be more realistic and deal with the requirements of the industrial applications.

In the near future, the proposed method will be realized and investigated through various experimental tests. In this way, its efficiency and effectiveness will be tested under real operating conditions, validating its feasibility and reliability against the problems created by the parallelization of SiC MOSFETs. Until now, many post-synthesis timing simulations with the aid of Vivado have been performed to examine the feasibility of the algorithm. This kind of simulation allows to ensure that the implemented design meets functional and timing requirements and has the expected behavior in the FPGA. In this way, it is most probable that the FPGA can execute the algorithm fast enough to estimate all current unbalances and apply the correct modifications to the control parameters of each SiC MOSFET.

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