Formalizing Timing Diagram Requirements in Discrete Duration Calculus

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Abstract. Several temporal logics have been proposed to formalise timing diagram requirements over hardware and embedded controllers. These include LTL [CF05], discrete time MTL [AH93] and the recent industry standard PSL [EP16]. However, succinctness and visual structure of a timing diagram are not adequately captured by their formulae [CF05]. Interval temporal logic QDDC is a highly succinct and visual notation for specifying patterns of behaviours [Pan00].

In this paper, we propose a practically useful notation called SeCeNL which enhances negation free fragment of QDDC with features of nominals and limited liveness. We show that timing diagrams can be naturally (compositionally) and succinctly formalised in SeCeNL as compared with PSL-Sugar and MTL. We give a linear time translation from timing diagrams to SeCeNL. As our second main result, we propose a linear time translation of SeCeNL into QDDC. This allows QDDC tools such as DCVALID [Pan00,Pan01] and DCSynth to be used for checking consistency of timing diagram requirements as well as for automatic synthesis of property monitors and controllers. We give examples of a minepump controller and a bus arbiter to illustrate our tools. Giving a theoretical analysis, we show that for the proposed SeCeNL, the satisfiability and model checking have elementary complexity as compared to the non-elementary complexity for the full logic QDDC.

1 Introduction

A timing diagram is a collection of binary signals and a set of timing constraints on them. It is a widely used visual formalism in the realm of digital hardware design, communication protocol specification and embedded controller specification. The advantages of timing diagrams in hardware design are twofold, one, since designers can visualize waveforms of signals they are easy to comprehend and two, they are very convenient for specifying ordering and timing constraints between events (see figures Fig. 1 and Fig. 2 below).

There have been numerous attempts at formalizing timing diagram constraints in the framework of temporal logics such as the timing diagram logic [Fis99], with LTL formulas [CF05], and as synchronous regular timing diagrams.
Moreover, there are industry standard property specification languages such as PSL/Sugar and OVA for associating temporal assertions to hardware designs [EF16]. The main motivation for these attempts was to exploit automatic verification techniques that these formalisms support for validation and automatic circuit synthesis. However, commenting on their success, Fisler et. al. state that the less than satisfactory adoption of formal methods in timing diagram domain can be partly attributed to the gulf that exists between graphical timing diagrams and textual temporal logic – expressing various timing dependencies that can exist among signals that can be illustrated so naturally in timing diagrams is rather tedious in temporal logics [CF05]. As a result, hardware designers use timing diagrams informally without any well defined semantics which make them unamenable to automatic design verification techniques.

In this paper, we take a fresh look at formalizing timing diagram requirements with emphasis on the following three features of the formalism that we propose here.

Firstly, we propose the use of an interval temporal logic QDDC to specify patterns of behaviours. QDDC is a highly succinct and visual notation for specifying regular patterns of behaviours [Pan00,Pan01,KP05]. We identify a quantifier and negation-free subset SeCe of QDDC which is sufficient for formalizing timing diagram patterns. It includes generalized regular expression like syntax with counting constructs. Constraints imposed by timing diagrams are straightforwardly and compactly stated in this logic. For example, the timing diagram in Fig. 1 stating that $P$ transits from 0 to 1 somewhere in interval $u$ to $u + 3$ cycles is captured by the SeCe formula $\neg P \leq u \land \neg P \leq [P] \land [P]$. The main advantage of SeCe is that it has elementary satisfiability as compared to the non-elementary satisfiability of general QDDC.

Secondly, it is very typical for timing diagrams to have partial ordering and synchronization constraints between distinct events. Emphasizing this aspect, formalisms such as two dimensional regular expressions [Fis07] have been proposed for timing diagrams. We find that synchronization in timing diagram may even extend across different patterns of limited liveness properties. In order to handle such synchronization, we extend our logic SeCe with nominals from hybrid temporal logics [FdRS03]. Nominals are temporal variables which “freeze” the positions of occurrences of events. They naturally allow synchronization across formulae.
Thirdly, we enhance the timing diagram specifications (as well as logic SeCe) with limited liveness operators. While timing diagrams visually specify patterns of occurrence of signals, they do not make precise the modalities of occurrences of such patterns. We explicitly introduce modalities such as a) initially, a specified pattern must occur, or that b) every occurrence of pattern1 is necessarily and immediately followed by an occurrence of pattern2, or that c) occurrence of a specified pattern is forbidden anywhere within a behaviour. In this, we are inspired by Allen’s Interval Algebra relations [All83] as well as the LSC operators of Harel for message sequence charts [DH01]. We confine ourselves to limited liveness properties where good things are achieved within specified bounds. For example, in specifying a modulo 6 counter, we can say that the counter will stabilize before completion of first 15 cycles. Astute readers will notice that, technically, our limited liveness operators only give rise to “safety” properties (in the sense of Alpern and Schneider [ASS7]). However, from a designer’s perspective they do achieve the practical goal of forcing good things to happen.

Putting all these together, we define a logic SeCeNL which includes negation-free QDDC together with limited liveness operators as well as nominals. The formal syntax and semantics of SeCeNL formulas is given in [2,3]. We claim that SeCeNL provides a natural and convenient formalism for encoding timing diagram requirements. Substantiating this, we formulate a translation of timing diagrams into SeCeNL formulae in [3]. The translation is succinct, in fact, linear time computable in the size of the timing diagram. (A textual syntax is used for timing diagrams. The textual syntax of timing diagrams used is inspired by the tool WaveDrom [CP16], which is also used for graphical rendering of our timing diagram specifications.) Moreover, the translation is compositional, i.e. it translates each element of the timing diagram as one small formula and overall specification is just the conjunction of such constraints. Hence, the translation preserves the structure of the diagram.

With several examples of timing diagrams, we compare its SeCeNL formula with the formula in logics such as PSL-Sugar and MTL. Logic PSL-Sugar is amongst the most expressive notations for requirements. Logic PSL-Sugar is syntactically a superset of MTL and LTL. It extends LTL with SERE (regular expressions with intersection) which are similar to our SeCe. In spite of this, we show natural examples where SeCeNL formula is at least one exponent more succinct as compared to PSL-Sugar.

As the second main contribution of this paper, we consider formal verification and controller synthesis from SeCeNL specifications. In [3,4] we formulate a reduction from a SeCeNL formula to an equivalent QDDC formula. This allows QDDC tools to be used for SeCeNL. It may be noted that, though expressively no more powerful than QDDC, logic SeCeNL considerably more efficient for satisfiability and model checking. We show that these problems have elementary complexity as compared with full QDDC which exhibits non-elementary complexity. Also, the presence of limited liveness and nominals makes it more convenient as compared to QDDC for practical use.
By implementing the above reductions, we have constructed a Python based translator which converts a requirement consisting of a boolean combination of timing diagram specifications (augmented with limited liveness) and SeCeNL formulae into an equivalent QDDC formula. We can analyze the resulting formula using the QDDC tools DCVALID \cite{Pan00,Pan01} as well as DCSynthG for model checking and controller synthesis, respectively (see Fig. \ref{fig:toolchain} for the tool chain). We illustrate the use of our tools by the case studies of a synchronous bus arbiter and a minepump controller in \cite{Zhu2010}. Readers may note that we specify rather rich quantitative requirements not commonly considered, and our tools are able to automatically synthesize monitors and controllers for such specifications.

2 Logic QDDC

Let $\Sigma$ be a finite non empty set of propositional variables. A word $\sigma$ over $\Sigma$ is a finite sequence of the form $P_0 \cdots P_n$ where $P_i \subseteq \Sigma$ for each $i \in \{0, \ldots, n\}$. Let $\text{len}(\sigma) = n + 1$, $\text{dom}(\sigma) = \{0, \ldots, n\}$ and $\forall i \in \text{dom}(\sigma) : \sigma(i) = P_i$.

The syntax of a propositional formula over $\Sigma$ is given by:

$$\varphi ::= \, 0 \mid 1 \mid p \in \Sigma \mid \varphi \land \varphi \mid \varphi \lor \varphi \mid \neg \varphi,$$

and operators such as $\Rightarrow$ and $\Leftrightarrow$ are defined as usual. Let $\Omega_\Sigma$ be the set of all propositional formulas over $\Sigma$.

Let $\sigma = P_0 \cdots P_n$ be a word and $\varphi \in \Omega_\Sigma$. Then, for an $i \in \text{dom}(\sigma)$ the satisfaction relation $\sigma \models \varphi$ is defined inductively as expected: $\sigma \models p$ iff $p \in \sigma(i)$; $\sigma \models \neg p$ iff $\sigma \not\models p$, and the satisfaction relation for the rest of the boolean combinations defined in a natural way.

The syntax of a QDDC formula over $\Sigma$ is given by:

$$D ::= \langle \varphi \rangle \mid [\varphi] \mid [\{\varphi\}] \mid [\{\{\varphi\}\}] \mid D \cdots D \mid \neg D \mid D \lor D \mid D \land D \mid D^* \mid \exists \varphi . \, D \mid \forall \varphi . \, D \mid \text{slen} \circ \varphi . \, \text{d} \mid \text{scount} \circ \varphi . \, \text{d} \mid \text{sdur} \circ \varphi . \, \text{d},$$

where $\varphi \in \Omega_\Sigma$, $p \in \Sigma$, $c \in \mathbb{N}$ and $\circ \in \{<,\leq,\forall,\exists,\geq,\}$. An interval over a word $\sigma$ is of the form $[b,e]$ where $b,e \in \text{dom}(\sigma)$ and $b \leq e$. An interval $[b_1,e_1]$ is a sub interval of $[b,e]$ if $b \leq b_1$ and $e_1 \leq e$. Let $\text{Intv}(\sigma)$ be the set of all intervals over $\sigma$.

Let $\sigma$ be a word over $\Sigma$ and let $[b,e] \in \text{Intv}(\sigma)$ be an interval. Then the satisfaction relation of a QDDC formula $D$ over $\Sigma$, written $\sigma, [b,e] \models D$, is defined inductively as follows:

$$\begin{align*}
\sigma, [b,e] &\models \langle \varphi \rangle \quad \text{iff} \quad \sigma, b \models \varphi, \\
\sigma, [b,e] &\models [\varphi] \quad \text{iff} \quad \forall b \leq i < e : \sigma, i \models \varphi, \\
\sigma, [b,e] &\models [\{\varphi\}] \quad \text{iff} \quad \forall b \leq i \leq e : \sigma, i \models \varphi, \\
\sigma, [b,e] &\models [\{\{\varphi\}\}] \quad \text{iff} \quad e = b+1 \text{ and } \sigma, b \models \varphi, \\
\sigma, [b,e] &\models \neg D \quad \text{iff} \quad \sigma, [b,e] \not\models D, \\
\sigma, [b,e] &\models D_1 \lor D_2 \quad \text{iff} \quad \sigma, [b,e] \models D_1 \text{ or } \sigma, [b,e] \models D_2, \\
\sigma, [b,e] &\models D_1 \land D_2 \quad \text{iff} \quad \sigma, [b,e] \models D_1 \text{ and } \sigma, [b,e] \models D_2, \\
\sigma, [b,e] &\models D_1 \ast D_2 \quad \text{iff} \quad \exists b \leq i \leq e : \sigma, [b,i] \models D_1 \text{ and } \sigma, [i,e] \models D_2.
\end{align*}$$
We call word $\sigma'$ a $p$-variant, $p \in \Sigma$, of a word $\sigma$ if $\forall i \in \text{dom}(\sigma), \forall q \neq p : \sigma'(i)(q) = \sigma(i)(q)$. Then $\sigma, [b, e] |= \exists p. D \iff \sigma', [b, e] |= D$ for some $p$-variant $\sigma'$ of $\sigma$ and, $\sigma, [b, e] |= \forall p. D \iff \sigma, [b, e] \neq \exists p. \neg D$. We define $\sigma |= D$ iff $\sigma, [0, \text{len}(\sigma)] |= D$.

**Example 1.** Let $\Sigma = \{p, q\}$ and let $\sigma = P_0 \cdots P_7$ be such that $\forall 0 \leq i < 7 : P_i = \{p\}$ and $P_7 = \{q\}$. Then $\sigma, [0, 7] |= [p]$ but not $\sigma, [0, 7] |= [\neg p]$ as $p \notin P_7$.

**Example 2.** Let $\Sigma = \{p, q, r\}$ and let $\sigma = P_0 \cdots P_{10}$ be such that $\forall 0 \leq i < 4 : P_i = \{p\}, \forall 4 \leq i < 8 : P_i = \{p, q, r\}$ and $\forall 8 \leq i < 10 : P_i = \{q, r\}$. Then $\sigma, [0, 10] |= [p][\neg p \land r]$ because for $i \in \{8, 9, 10\}$ the condition $\exists 0 \leq i < 10 : \sigma, [0, i] |= [p]$ and $\sigma, [i, 10] |= [\neg p \land r]$ is met. But $\sigma, [0, 7] \neq [p][\neg p \land r]$ as $\neg\exists 0 \leq i \leq 7 : \sigma, [0, i] |= [p]$. But $\sigma, [i, 7] |= [\neg p \land r]$.

Entities $\text{slen}$, $\text{scount}$, and $\text{sdur}$ are called terms in QDCC. The term $\text{slen}$ gives the length of the interval in which it is measured, $\text{scount}$ $\varphi$ where $\varphi \in \Omega_{\Sigma}$, counts the number of positions including the last point in the interval under consideration where $\varphi$ holds, and $\text{sdur}$ $\varphi$ gives the number of positions excluding the last point in the interval where $\varphi$ holds. Formally, for $\varphi \in \Omega_{\Sigma}$ we have $\text{slen}(\sigma, [b, e]) = e - b, \text{scount}(\sigma, \varphi, [b, e]) = \sum_{i=b}^{e-1} 1, \text{if } \sigma, i |= \varphi, \} \text{and } 0, \text{otherwise.} \}$ and $\text{sdur}(\sigma, \varphi, [b, e]) = \sum_{i=b}^{e-1} \begin{cases} 1, \text{if } \sigma, i |= \varphi, \} \\ 0, \text{otherwise.} \}$

In addition we also use the following derived constructs: $\sigma, [b, e] |= pt$ if $b = c; \sigma, [b, e] |= \text{ext}$ if $b < c$; $\sigma, [b, e] |= \Diamond D$ if $\text{true} \land \Diamond D$ true and $\sigma, [b, e] |= \Box D$ if $\sigma, [b, e] \neq \Diamond D$.

A formula automaton for a QDCC formula $D$ is a deterministic finite state automaton which accepts precisely language $L = \{\sigma \mid \sigma |= D\}$.

**Theorem 1.** [Pan01] For every QDCC formula $D$ over $\Sigma$ we can construct a DFA $A(D)$ for $D$ such $L(D) = L(A(D))$. The size of $A(D)$ is non elementary in the size of $D$ in the worst case.

### 2.1 Chop expressions: Ce and SeCe

**Definition 1.** The logic Semi extended Chop expressions (SeCe) is a syntactic subset of QDCC in which the operators $\exists p$, $\forall p, D$ and negation are not allowed. The logic Chop expressions (Ce) is a sublogic of SeCe in which conjunction is not allowed.

**Lemma 1.** For any chop expression $D$ of size $n$ we can effectively construct a language equivalent DFA $A$ of size $\Omega(2^n)$. 

**Proof.** We observe that for any chop expression $D$ we can construct a language equivalent NFA which is at most exponential in size of $D$ including the constants appearing in it (for a detailed proof see [BP12] wherein a similar result has been proved). But this implies there exists a DFA of size $2^{2^n}$ which accepts exactly the set of words $\sigma$ such that $\sigma \models D$. 

Corollary 1. For any SeCe $D$ of size $n$ we can effectively construct a language equivalent DFA $A$ of size $\Omega(2^{2^{2^n}})$.

Proof. Proof follows from the definition of SeCe, lemma [1] and from the fact that the size of the product of DFA’s can be atmost exponential in the size of individual DFA’s.

2.2 DCVALID and DCSynthG

The reduction from a QDDC formula to its formula automaton has been implemented into the tool DCVALID [Pan00, Pan01]. The formula automaton it generates is total, deterministic and minimal automaton for the formula. DCVALID can also translate the formula automaton into Lustre/SCADE, Esterel, SMV and Verilog observer module. By connecting this observer module to run synchronously with a system we can reduce model checking of QDDC property to reachability checking in observer augmented system. See [Pan00, Pan01] for details. A further use of formula automata can be seen in the tool called DCSynthG which synthesizes synchronous dataflow controller in SCADE/NuSMV/Verilog from QDDC specification.

2.3 Logic SeCeNL: Syntax and Semantics

We can now introduce our logic SeCeNL which builds upon SeCe by augmenting it with nominals and limited liveness operators.

Syntax : The syntax of SeCeNL atomic formula is as follows. Let $D$, $D_1$, $D_2$ and $D_3$ range over SeCe formulae and let $\Theta$, $\Theta_1$, $\Theta_2$ and $\Theta_3$ range over subset of propositional variables occurring in SeCe formula. The notation $D : \Theta$, called a nominated formula, denotes that $\Theta$ is the set of variables used as nominals in the formula $D$.

\[
\begin{align*}
\text{init}(D_1 : \Theta_1 / D_2 : \Theta_2) & \mid \text{anti}(D : \Theta) \mid \text{pref}(D : \Theta) \\
\text{implies}(D_1 : \Theta_1 \rightsquigarrow D_2 : \Theta_2) & \mid \text{follows}(D_1 : \Theta_1 \rightsquigarrow D_2 : \Theta_2 / D_3 : \Theta_3) \\
\text{triggers}(D_1 : \Theta_1 \rightsquigarrow D_2 : \Theta_2 / D_3 : \Theta_3)
\end{align*}
\]

An SeCeNL formula is a boolean combination of atomic SeCeNL formulae of the form above. As a convention, $D : \emptyset$ is abbreviated as $D$ when the set of nominals $\Theta$ is empty.

Limited Liveness Operators : Given an word $\sigma$ and a position $i \in \text{dom}(\sigma)$, we state that $\sigma, i \models D$ iff $\sigma[0 : i] \models D$. Thus, the interpretation is that the past of the position $i$ in execution satisfies $D$.

For a SeCe formula $D$ we let $\Xi(D) = D \land \neg (D^*\text{ext})$, which says that if $\sigma, [b, e] \models \Xi(D)$ then $\sigma, [b, e] \models D$ and there exists no proper prefix interval $[b, e_1]$, (i. e. $[b, e_1] \in \text{Intv}(\sigma)$ and $b \leq e_1 < e$) such that $\sigma, [b, e_1] \models D$. We say $\sigma' \preceq_{\text{prefix}} \sigma$ if $\sigma'$ is a prefix of $\sigma$, and $\sigma' \prec_{\text{prefix}} \sigma$ if $\sigma'$ is a proper prefix of $\sigma$. 
We first explain the semantics of limited liveness operators assuming no nominals are used in the specification, i.e. $\Theta, \Theta_1, \Theta_2$ and $\Theta_3$ are all empty. A set $S \subseteq \Sigma^*$ is prefix closed if $\sigma \in S$ then $\forall \sigma' : \sigma' \preceq_{\text{prefix}} \sigma \Rightarrow \sigma' \in S$. We observe that each atomic liveness formula denotes a prefix closed subset of $(2^\Sigma)^+$.

- $L(\text{pref}(D)) = \{ \sigma \mid \forall \sigma' \preceq_{\text{prefix}} \sigma : \sigma' \models D \}$. Operator $\text{pref}(D)$ denotes that $D$ holds invariantly throughout the execution.
- $L(\text{init}(D_1/D_2)) = \{ \sigma \mid \forall j : [0,j] \models D_2 \Rightarrow \exists k \leq j : [0,k] \models D_1 \}$. Operator $\text{init}(D_1/D_2)$ basically states that if $j$ is the first position which satisfies $D_2$ in the execution then there exists an $i \leq j$ such that $i$ satisfies $D_1$. Thus, initially $D_1$ holds before $D_2$ unless the execution (is too short and hence) does not satisfy $D_2$ anywhere.
- $L(\text{anti}(D)) = \{ \sigma \mid \exists i, j : [i,j] \not\models D \}$. Operator $\text{anti}(D)$ states that there is no observation sub interval of the execution which satisfies $D$.
- $L(\text{implies}(D_1 \Rightarrow D_2)) = \{ \sigma \mid \forall i, j : ([i,j] \models D_1 \Rightarrow [i,j] \models D_2) \}$. Operator $\text{implies}(D_1 \Rightarrow D_2)$ states all observation intervals which satisfy $D_1$ will also satisfy $D_2$.
- $L(\text{follows}(D_1 \Rightarrow D_2/D_3)) = \{ \sigma \mid \forall i, j : ([i,j] \models D_1 \Rightarrow \forall k : [i,j,k] \models D_3 \Rightarrow \exists l \leq k : [i,j,l] \models D_2) \}$. Operator $\text{follows}(D_1 \Rightarrow D_2/D_3)$ states that if any observation interval $[i,j]$ satisfies $D_1$ and there is a following shortest interval $[j,k]$ which satisfies $D_3$ then there exists a prefix interval of $[j,k]$ which satisfies $D_2$.
- $L(\text{triggers}(D_1 \Rightarrow D_2/D_3)) = \{ \sigma \mid \forall i, j : ([i,j] \models D_1 \Rightarrow \forall k : [i,j,k] \models D_3 \Rightarrow \exists l \leq k : [i,j,l] \models D_2) \}$. Operator $\text{triggers}(D_1 \Rightarrow D_2/D_3)$ states that if any observation interval $[i,j]$ satisfies $D_1$ and if $[i,k]$ is the shortest interval which satisfies $D_3$ then $D_2$ holds for a prefix interval of $[i,k]$.

Based on this semantics, we can translate an atomic SeCeNL formula $\zeta$ without nominals into equivalent SeCe formula $\mathfrak{R}(\zeta)$ as follows.

1. $\mathfrak{R}(\text{pref}(D)) \overset{\text{def}}{=} \neg((\neg D)^* \text{true })$.
2. $\mathfrak{R}(\text{init}(D_1/D_2)) \overset{\text{def}}{=} \text{pref}(\Xi(D_2) \Rightarrow D_1^* \text{true })$.
3. $\mathfrak{R}(\text{anti}(D)) \overset{\text{def}}{=} \neg(\text{true }^* D^{*} \text{true })$.
4. $\mathfrak{R}(\text{implies}(D_1 \Rightarrow D_2)) \overset{\text{def}}{=} \Box(D_1 \Rightarrow D_2)$.
5. $\mathfrak{R}(\text{follows}(D_1 \Rightarrow D_2/D_3)) \overset{\text{def}}{=} \Box((\Box(D_1 \Rightarrow \Xi(D_3) \Rightarrow \Xi(D_2^* \text{true })) \land \Box(D_1 \Rightarrow \Xi(D_3) \Rightarrow D_2^* \text{true }))$.
6. $\mathfrak{R}(\text{triggers}(D_1 \Rightarrow D_2/D_3)) \overset{\text{def}}{=} \Box((\Box(D_1 \Rightarrow \Xi(D_3) \Rightarrow \Xi(D_2^* \text{true })) \land \Box(D_1 \Rightarrow \Xi(D_3) \Rightarrow D_2^* \text{true }))$.

**Lemma 2.** For any $\zeta \in \text{SeCeNL}$, if $\zeta$ does not use nominals then $\sigma \in L(\zeta)$ iff $\sigma \in L(\mathfrak{R}(\zeta))$.

The proof follows from examination of the semantics of $\zeta$ and the definition of $\mathfrak{R}(\zeta)$. We omit the details.
**Nominals**: Consider a nominated formula \(D : \Theta\) where \(D\) is a SeCe formula over propositional variables \(\Sigma \cup \Theta\). As we shall see later, the propositional variables in \(\Theta\) are treated as “place holders” - variables which are meant to be true exactly at one point - and we call them nominals following [FGRS03].

Given an interval \([b, e] \in Intv(\mathbb{N})\) we define a nominal valuation over \([b, e]\) to be a map \(\nu : \Theta \to \{i \mid b \leq i \leq e\}\). It assigns a unique position within \([b, e]\) to each nominal variable. We can then straightforwardly define \(\sigma, [b, e] \models \nu D\) by constructing a word \(\sigma_\nu\) over \(\Sigma \cup \Theta\) such that \(\forall p \in \Sigma : p \in \sigma_\nu(i) \iff p \in \sigma(i)\) and \(\forall u \in \Theta : u \in \sigma_\nu(i) \iff \nu(u) = i\). Then \(\sigma_\nu, [b, e] \models D \iff \sigma_\nu, [b, e] \models \nu D\). We state that \(\nu_1 \models \Theta_1\) and \(\nu_2 \models \Theta_2\) are consistent if \(\nu_1(u) = \nu_2(u)\) for all \(u \in \Theta_1 \cap \Theta_2\). We denote this by \(\nu_1 \parallel \nu_2\).

**Semantics of SeCeNL**: Now we consider the semantics of SeCeNL where nominals are used and shared between different parts \(D_1, D_2\) and \(D_3\) of an atomic formula such as \(\text{implies}(D_1 : \Theta_1 \leadsto D_2 : \Theta_2)\).

**Example 3**: Let \(D_1 : \{u, v\}\) be the formula \((\text{<u> " [P]\} \land (\text{<slen=n} \land \text{<v> " true})\) which holds for an interval where \(P\) is \(\text{true}\) throughout the interval and \(e\) marks the \(n + 1\) position from \(u\) denoting the start of the interval. Let \(D_2 : \{v\}\) be the formula \(\text{true} \land \text{<v> " [Q]}.\) Then, \(\text{implies}(D_1 : \{u, v\} \leadsto D_2 : \{v\}\) states that for all observation intervals \([i, j]\) and all nominal valuations \(\nu\) over \([i, j]\) if \(\sigma, [i, j] \models \nu D_1\) then \(\sigma, [i, j] \models \nu D_2\). This formula is given by live timing diagram in Fig. 2 below.

![Fig. 2. Live timing diagram.](image)

We now give the semantics of SeCeNL.

- \(L(\text{pref}(D : \Theta)) = \{\sigma \mid \forall \sigma' \preceq_{\text{prefix}} \sigma : \exists \nu. \; \sigma' \models \nu D\}\).
- \(L(\text{init}(D_1 : \Theta_1 / D_2 : \Theta_2)) = \{\sigma \mid \forall i \forall \nu : \sigma, [0, j] \models \nu D_2 \Rightarrow \exists k \leq j \exists \nu_2 : \nu_1 \parallel \nu_2 \land \sigma, [0, k] \models \nu_2 D_1\}\).
- \(L(\text{anti}(D : \Theta)) = \{\sigma \mid \exists i, j \exists \nu : \sigma, [i, j] \not\models \nu D\}\).
- \(L(\text{implies}(D_1 : \Theta_1 \leadsto D_2 : \Theta_2)) = \{\sigma \mid \forall i \exists j \exists \nu_1 : (\sigma, [i, j] \models \nu_1 D_1 \Rightarrow \exists \nu_2 : \nu_1 \parallel \nu_2 \land \sigma, [i, j] \models \nu_2 D_2\}\}\).

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3 Here we wish to point out that the illustration was made with the timing diagram editor WaveDrom and due to its limitation on naming nominals we were forced to rename the nominal \(v\) appearing in \(D_2\) as \(a\).
Proof. The formula $\zeta$ can be written in terms of a negation and two existential quantifiers. Note that each application of existential quantifier will result in an NFA and each time we determinize we get a DFA which is at most exponential in the size of NFA. Since that both $A(D_1)$ and $A(D_2)$ are DFA’s to start with, this implies we can construct a DFA $A(\zeta)$ of size at most $2^{2^m \cdot n^2}$ for $\zeta$.

In a similar way we can show that the size of formula automata for other SeCeNL atomic formulae are also elementary.

**Lemma 4.** For any $\zeta \in \text{SeCeNL}$ the size of the automaton $A(\zeta)$ for $\zeta$ is elementary.
3 Formalizing timing diagrams

In this section we give a formal semantics to timing diagrams and formula translation from timing diagrams to SeCeNL. We begin by giving a textual syntax for timing diagrams which is derived from the timing diagram format of WaveDrom [CP16,Wav16].

The symbols in a waveform come from $\Lambda = \{0, 1, 2, x, 0|, 1|, 2|, x|\}$ and $\Theta$, an atomic set of nominals. Let $\Gamma = \Theta \cup \Lambda$. The syntax of a waveform over $\Gamma$ is given by the grammar:

$$\pi := 0 \parallel 1 \parallel 2 \parallel x \parallel 0| \parallel 1| \parallel 2| \parallel x| \parallel u : \pi \parallel \pi_1 \pi_2,$$

where $u \in \Theta$ and $\pi \in \Lambda$. We call the elements in $\Theta$ the nominals. As we shall see later, when we convert a waveform to a SeCeNL formula the nominals that appear in the formula are exactly the nominals in the waveform and hence the name. Let $Wf$ be the set of all waveforms over $\Gamma$.

An example of a waveform is $0 \parallel 1 \parallel x \parallel 0| \parallel 1| \parallel 2| \parallel x| \parallel u : \pi \parallel \pi_1 \pi_2$ with $\Theta = \{a, b, c\}$. Intuitively, in a waveform 0 denotes low, 1 high, 2 and x don’t cares (there is a subtle difference between 2 and x though) and “|” the stuttering operator.

Let $\Sigma$ be a set of propositional variables. A timing diagram over $\Sigma$ is a tuple $\langle W, \Sigma, C, \Theta \rangle$ where $W = \{W_p \in Wf \mid p \in \Sigma\}$ and $C \subset \Theta \times \Theta \times Intv(N)$ a set of timing constraints.

Fig. 3 shows an example timing diagram $T = \langle \{W_p, W_q\}, \{(a, b, [10 : 10]), (a, d, [1 : 8]), (c, d, [20 : 30])\}, \{a, b, c, d, e, f\}\rangle$ along with its rendering in WaveDrom. The shared nominals have to be renamed in WaveDrom as commented in §2.3 in this case $a$ and $c$ in $W_q$ have been renamed $q$ and $h$ respectively. As in the case with SeCeNL formulas, nominals act as place holders in timing diagrams which can be shared among multiple waveforms. For example, in the figure $W_p$ and $W_q$ share the nominals $a$ and $c$. As a result a timing constraint in one timing diagram can implicitly induce a timing constraint in the other. For instance, even though there is no direct timing constraint between $a$ and $c$ in $W_p$ the constraints between $a$ and $d$, and $d$ and $c$ together impose one on them.

| waveform $W_p$ | 01a : 2x011xb : x2|220c : 00 |
|----------------|--------------------------|
| waveform $W_q$ | 00a : 0|d : 11|e : xxx|f : 01c : 11 |
| timing constraints: | d-a\in[1:8], c-d\in[20:30], b-a\in[10:10] |

Fig. 3. Timing diagram $T$ and its WaveDrom rendering.
Let $T = (W, \Sigma, C, \Theta), W = \{W_p \in \text{Wf} \mid p \in \Sigma\}$, be a timing diagram. Let $\nu : \Theta \to [b, e]$ be a nominal valuation. Let $\sigma : [0, n] \to 2^\Sigma$ be a word over $\Sigma$ and for all $p \in \Sigma$ let $\sigma_p : [0, n] \to \{0, 1\}$ given by $\sigma_p(i) = 1$ iff $p \in \sigma(i)$. Then the satisfaction relation $\sigma_p$ over a waveform $W$ under the valuation $\nu$ is defined as follows.

$\sigma_p, [b, e] \models_\nu 0$ iff $e = b + 1$ and $\sigma_p(b) = 0$,

$\sigma_p, [b, e] \models_\nu 1$ iff $e = b + 1$ and $\sigma_p(b) = 1$,

$\sigma_p, [b, e] \models_\nu \lambda$ iff $e = b + 1$ and $\lambda \in \{2, x\}$,

$\sigma_p, [b, e] \models_\nu 0$ iff $\forall b \leq i < e : \sigma_p(i) = 0$,

$\sigma_p, [b, e] \models_\nu 1$ iff $\exists b \leq i < e : \sigma_p(i) = 1$,

$\sigma_p, [b, e] \models_\nu x$ iff $\forall b \leq i < e : \sigma_p(i) = 1$ or $\exists b \leq i < e : \sigma_p(i) = 0$,

$\sigma_p, [b, e] \models_\nu V W$ iff $\exists b \leq i < e : \sigma_p, [b, i] \models_\nu V$ and $\sigma_p, [i, e] \models_\nu W$, and $\nu_1, \nu_2 |\nu$.

We say $\nu \models C$ iff $\forall (a, b, (l, r)) \in C : \nu(b) - \nu(a) \in \langle l, r \rangle$. We define $\sigma, [b, e] \models_\nu \langle W, \Sigma, C, \Theta \rangle$ iff $\forall p \in \Sigma : \sigma_p, [b, e] \models_\nu W_p$ and $\nu \models C$.

3.1 Waveform to SeCeNL translation

We translate a waveform $W_p$ to SeCeNL as follows: every 0 occurring in $P$ is translated to $\{\{\neg P\}\}$, 1 to $\{\{P\}\}$, 2 and $x$ to $\text{slen}=1$, 0 to $\text{ptv}[-P], 1$ to $\text{ptv}[P], 2$ to $\text{true}$, and $x$ to $\text{ptv}[P]\neg[-P]$. A nominal $u$ that is appearing in $W_p$ is translated to $\langle u \rangle$. For instance, the waveform $W_p=01a:2x011xb:x220c:00$ in $T$ of Fig. 3 will be translated to SeCeNL formula as below.

$\langle \{\neg P\}\rangle \langle \{P\}\rangle \langle \text{slen}=1 \rangle \langle \text{slen}=1 \rangle \langle \{\neg P\}\rangle \langle \{P\}\rangle \langle \text{slen}=1 \rangle \langle \text{true} \rangle \langle \text{slen}=1 \rangle \langle \text{slen}=1 \rangle \langle \{\neg P\}\rangle \langle \{P\}\rangle \langle \{\neg P\}\rangle$.

We denote the translated SeCeNL formula by $\xi(T, W_p)$. Similarly we can translate $W_q$ to get the formula $\xi(T, W_q)$. The timing constraints in $C$ is roughly translated to the SeCeNL formula $\xi(T, C)$ as follows.

$((\text{true} \langle a \rangle \langle \text{slen}=1 \rangle \langle \text{slen}=8 \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle \langle \text{true} \rangle)$. 

We define $\xi(T) = \xi(T, W_p) \wedge \xi(T, W_q) \wedge \xi(T, C)$. For a timing diagram $T = \langle W, \Sigma, C, \Theta \rangle, W = \{W_p \mid p \in \Sigma\}$ we define $\xi(T) = \bigwedge_{p \in \Sigma} \xi(T, W_p) \wedge \xi(T, C)$.

Theorem 3. Let $T$ be a timing diagram. Then, for all $\sigma \in \Sigma^*$, for all $[b, e] \in \text{Intv}(\sigma)$ and for all nominal valuation $\nu$ over $[b, e], \sigma, [b, e] \models_\nu T$ iff $\sigma, [b, e] \models_\nu \xi(T) : \Theta$. Also, the translation $\xi(T) : \Theta$ is linear in the size of $T$. 
Proof. Proof is not difficult and is by induction on the length of the waveform.

Due above theorem we can now use timing diagrams in place of nominated formulas with liveness operators. We call such timing diagrams live timing diagrams. For an example of a live timing diagram see Fig. 2.

3.2 Comparison with other temporal logics

In previous section, Lemma 3 showed that timing diagrams can be translated to equivalent SeCeNL formulas with only linear blowup in size. In this section we compare our logic SeCeNL with other relevant logics in the literature viz, LTL, discrete time MTL, and PSL-Sugar. Of these, PSL-Sugar is the most expressive and discrete time MTL and LTL are its syntactic subset. We show by examples that SeCeNL formulae are more succinct (smaller in size) than PSL-Sugar and we believe that they capture the diagrams more directly. Appendix A gives several more examples which could not be included due to lack of space.

Example (Ordered Stack) Let us now consider the timing diagram in Fig. 4 adapted from [CF05]. Rise and fall of successive signals follow a stack discipline. The language described by it is given by the SeCeNL formula:

\[
\begin{align*}
&\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e \\
&\land (\neg a \land \neg b \land \neg c \land \neg d \land \neg e.
\end{align*}
\]

Note that first five conjuncts exactly correspond to the five waveforms. The last constraint enforces the ordering constraints between waveforms. In general, if \( n \) signals are stacked, its SeCeNL specification has size \( O(n) \).
An equivalent MTL (or LTL) formula is given by:

\[(-a \land -b \land -c \land -d \land -e) \up U U [a \land -b \land -c \land -d \land -e] \up U U [a \land b \land c \land d \land -e] \up U U [a \land b \land c \land -d \land -e] \up U U [a \land b \land -c \land -d \land -e] \up U U [a \land -b \land -c \land -d \land -e] \up U U \]

where \( a \) \( \up U U \) \( b \) is the derived modality \( a \land X(aUb) \). For a stack of \( n \) signals, the size of the MTL formula is \( O(n^2) \).

Above formula is also a PSL-Sugar formula. We attempt to specify the pattern as a PSL-Sugar regular expression as follows:

\[
((-a \land -b \land -c \land -d \land -e);[+] ; (a \land -b \land -c \land -d \land -e);[+]; (a \land b \land c \land -d \land -e);[+]; (a \land b \land c \land -d \land -e);[+]; (a \land b \land -c \land -d \land -e);[+]; (a \land -b \land -c \land -d \land -e);[+]; (-a \land -b \land -c \land -d \land -e);[+])
\]

For a stack of \( n \) signals, the size of the PSL-Sugar SERE expression is \( O(n^2) \).

We believe that there is no formula of size \( O(n) \) in PSL-Sugar which can express the above property. Compare this with size \( O(n) \) formula of SeCeNL.

**Example (Unordered Stack)** In ordered stack signal \( a \) turns on first and turns off last followed by signals \( b, c, d, e \) in that order. We consider a variation of the ordered stack example above where signals turn on and off in first-on-last-off order but there is no restriction on which signal becomes highest first. This can be compactly specified in SeCeNL as follows.

\[
((-a \land <ua> \land [-a]) \land ((-b \land <ub> \land [b] \land <vb> \land [-b]) \land
(-c \land <uc> \land [c] \land <vd> \land [-c]) \land
(-d \land <ud> \land [d] \land <vd> \land [-d]) \land
(-e \land <ue> \land [e] \land <uc> \land [-e]) \land (ext \land <u1> \land ext \land <u2> \land ext ) \land
(ext \land <u3> \land ext ) \land (ext \land <u4> \land ext \land <u5> \land ext ) \land
(ext \land <v1> \land ext ) \land (ext \land <v3> \land ext ) \land (ext \land <v2> \land ext ) \land
Bijectiona, ub, uc, ud, ae, va, vb, vc, vd, ve, u1, u2, u3, u4, u5, v1, v2, v3, v4, v5)
\]

where formula Bijection below states that there is one to one correspondence between positions marked by \( ua, ub, uc, ud, ae, va, vb, vc, vd, ve \) and positions marked by \( u1, u2, u3, u4, u5, v1, v2, v3, v4, v5 \). Moreover, it states that if \( u_a \) maps to \( v_3 \) than \( u_a \) must map to \( v_3 \) and so on.

\[
[(u1 \lor u2 \lor u3 \lor u4 \lor u5) \leftrightarrow (ua \lor ub \lor uc \lor ud \lor ae)] \land [(\Lambda_{1 \leq i, j < 5, i \neq j} \neg(u_i \land u_j))] \land
[(v1 \lor v2 \lor v3 \lor v4 \lor v5) \leftrightarrow (va \lor vb \lor vc \lor vd \lor ve)] \land [(\Lambda_{1 \leq i, j < 5, i \neq j} \neg(v_i \land v_j))] \land
\Lambda_{1 \leq i, j < 5, a, b, c, de} (true \land <u_i \land u_j> \land true) \leftrightarrow (true \land <v_i \land v_j> \land true)
\]

Note that, in general, if \( n \) signals are stacked, then the above SeCeNL specification has size \( O(n^2) \).
Now we discuss encoding of unordered stack in PSL-Sugar. In absence of nominals, it is difficult to state the above behaviour succinctly in logics PSL-Sugar even using its SERE regular expressions. Each order of occurrence of signals has to be enumerated as a disjunction where each disjunct is as in the example ordered stack (where the order was $a, b, c, d, e$). As there are $n!$ orders possible between $n$ signals, the size of the PSL-Sugar formula is also $O(n!)$. We believe that there is no polynomially sized formula in PSL-Sugar encoding this property. This shows that SeCeNL is exponentially more succinct as compared to PSL-Sugar.

In general, presence of nominals distinguishes SeCeNL from logics like PSL-Sugar. In formalizing behaviour of hardware circuits it has been proposed that regular expressions are not enough and operators such as pipelining have been introduced [CF05]. These are a form of synchronization and they can be easily expressed using nominals too.

4 Case study: Minepump Specification

We first specify some useful generic timing diagram properties which would used for requirement specification in this (and many other) case studies.

- **lags**($P, Q, n$): it is defined by Fig. 5. It specifies that in any observation interval if $P$ holds continuously for $n + 1$ cycles and persists then $Q$ holds from $(n + 1)^{th}$ cycle onwards and persists till $P$ persists.

- **tracks**($P, Q, n$): defined Fig. 6. In any observation interval if $P$ becomes true then $Q$ sustains as long as $P$ sustains or upto $n$ cycles whichever is shorter.

- **sep**($P, n$): Fig. 7 defines this property. Any interval which begins with a falling edge of $P$ and ends with a rising edge of $P$ then the length of the interval should be at least $n$ cycles.

- **ubound**($P, n$): Fig. 8 defines the property. In any observation interval $P$ can be continuously true for at most $n$ cycles.

Note that we have presented these formulae diagrammatically. The textual version of these live timing diagrams can be found in Appendix C.

We now state the minepump problem. Imagine a minepump which keeps the water level in a mine under control for the safety of miners. The pump is driven by a controller which can switch it on and off. Mines are prone to methane leakage trapped underground which is highly flammable. So as a safety measure if a methane leakage is detected the controller is not allowed to switch on the pump under no circumstances.

The controller has two input sensors - HH2O which becomes 1 when water level is high, and HCH4 which is 1 when there is a methane leakage; and can generate two output signals - ALARM which is set to 1 to sound/persist the alarm, and PUMPON which is set to 1 to switch on the pump. The objective of the controller is to safely operate the pump and the alarm in such a way that the water level is never dangerous, indicated by the indicator variable DH2O, whenever certain assumptions hold. We have the following assumptions on the mine and the pump.
- Sensor reliability assumption: \( \text{pref}([\text{DH}2\text{O} \Rightarrow \text{HH}2\text{O}]) \). If HH2O is false then so is DH2O.
- Water seepage assumptions: \( \text{tracks}(\text{HH}2\text{O}, \text{DH}2\text{O}, \kappa_1) \). The minimum no. of cycles for water level to become dangerous once it becomes high is \( \kappa_1 \).
- Pump capacity assumption: \( \text{lags}(\text{PUMPON}, \neg \text{HH}2\text{O}, \kappa_2) \). If pump is switched on for at least \( \kappa_2 + 1 \) cycles then water level will not be high after \( \kappa_2 \) cycles.
- Methane release assumptions: \( \text{sep}(\text{HCH}4, \kappa_3) \) and \( \text{ubound}(\text{HCH}4, \kappa_4) \). The minimum separation between the two leaks of methane is \( \kappa_3 \) cycles and the methane leak cannot persist for more than \( \kappa_4 \) cycles.
- Initial condition assumption: \( \text{init}(\langle \neg \text{HH}2\text{O} \rangle \land \langle \neg \text{HCH}4 \rangle, \text{slen} = 0) \). Initially neither the water level is high nor there is a methane leakage.

Let the conjunction of these SeCeNL formulas be denoted as \( \text{MINEASSUME} \).

The commitments are:

- Alarm control: \( \text{lags}(\text{HH}2\text{O}, \text{ALARM}, \kappa_5) \) and \( \text{lags}(\text{HCH}4, \text{ALARM}, \kappa_6) \) and \( \text{lags}(\neg \text{HH}2\text{O} \land \neg \text{HCH}4, \neg \text{ALARM}, \kappa_7) \). If the water level is dangerous then alarm will be high after \( \kappa_5 \) cycles and if there is a methane leakage then alarm will be high after \( \kappa_6 \) cycles. If neither the water level is dangerous nor there is a methane leakage then alarm should be off after \( \kappa_7 \) cycle.
- Safety condition: \( \text{pref}([\neg \text{DH}2\text{O} \Rightarrow (\text{HCH}4 \Rightarrow \neg \text{PUMPON})]) \). The water level should never become dangerous and whenever there is a methane leakage pump should be off.

Let the conjunction of these commitments be denoted as \( \text{MINECOMMIT} \).

Then the requirement over the minepump controller is given by the formula \( \text{MINEASSUME} \Rightarrow \text{MINECOMMIT} \). A textual version of this full minepump specification, which can be input to our tools is given in Appendix C. Note that the requirement consists of a mixture of timing diagram constraints (such as pump capacity assumption above) as well as SeCeNL formulas (such as Safety condition above).

We can automatically synthesize a controller for the values say \( \kappa_1 = 10, \kappa_2 = 2, \kappa_3 = 14, \kappa_4 = 2, \) and \( \kappa_5 = \kappa_6 = \kappa_7 = 1 \). The tool outputs a SCADE/SMV
controller meeting the specification. A snapshot of SCADE code for the controller synthesized by DCSynthG for minepump can be found in Appendix D. If the specification is not realizable we output an explanation.

A second case study of synchronous bus arbiter specification can be found in Appendix E. We can automatically synthesize a property monitor for such requirement and use it to model check a given arbiter design; or we can directly synthesize a controller meeting the requirement. The appendix gives results of both these experiments.

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A Examples of Comparison with other logics

Example 1 (Ordering with timing) Consider the timing diagram in Fig. 9 which says that $a$ holds invariantly in the interval $[0, i]$ where $i \geq 1$, $b$ holds invariantly in the interval $[i, j]$, $j \geq i + 1$, and $c$ holds at $j$ and $j \leq n$.

The language described by the above timing diagram is given by the SeCeNL formula $([a \land \neg b] \land [b \land \neg a \land \neg c] \land <c>) \land (slen \leq n)$ which is of size $O(\log(n))$. It is assumed that all timing constants such as $n$ are encoded in binary and hence they contribute size $\log(n)$.

An equivalent MTL formula is $\bigvee_{i=1}^{n-1} (a \land \neg b[0 \leq i \leq n]) \land (b \land \neg a[1, n - i] \land c))$ whose size is $O(n \log(n))$.

Equivalent LTL formula is $\bigvee_{i=1}^{n-1} \bigvee_{j=1}^{i} (a \land b \land X^n)$ where $X^k = X \cdot \ldots \cdot X$, whose size is $O(n^2)$.

Equivalent PSL-Sugar formula is $(a \land \neg b[+]; b \land \neg a \land \neg c[+]; c) \land ((a | b)[< n]; c)$ with size $O(\log(n))$.

We also give examples of complex dependancy constraints. Consider the timing diagram in Fig. 10. In this diagram, $a$ occurs before $b$ and $c$, and $c$ occurs before $d$ and $e$. The point $e$ occurs after $d$ and $e$, and $d$ occurs after $b$ and $v$.

Fig. 9. Example 1.

Fig. 10. Example 3.
The behaviour is described straightforwardly by the SeCeNL formula:

\[
(\neg a \cdot <ua> \cdot [a] \cdot <ua> \cdot [\neg a]) \land (\neg b \cdot <ub> \cdot [b] \cdot <vb> \cdot [\neg b]) \land \\
(\neg c \cdot <uc> \cdot [c] \cdot <vc> \cdot [\neg c]) \land (\neg d \cdot <ud> \cdot [d] \cdot <vd> \cdot [\neg d]) \land \\
(\neg e \cdot <ue> \cdot [e] \cdot <ve> \cdot [\neg e]) \land (\text{ext} \cdot <ua> \cdot \text{ext} \cdot <ub> \cdot \text{true}) \land \\
(\text{ext} \cdot <uc> \cdot \text{ext} \cdot <uc> \cdot \text{true}) \land (\text{ext} \cdot <uc> \cdot \text{ext} \cdot <ud> \cdot \text{true}) \land \\
(\text{ext} \cdot <uc> \cdot \text{ext} \cdot <ve> \cdot \text{true}) \land (\text{ext} \cdot <ve> \cdot \text{ext} \cdot <vc> \cdot \text{true}) \land \\
(\text{ext} \cdot <vd> \cdot \text{ext} \cdot <vd> \cdot \text{true}).
\]

This formula is linear in the size of the timing diagram. Unfortunately, specifying these dependencies in PSL-Sugar is complex and formula size blows up at least quadratically.

B Implementation

We propose a textual framework with a well defined syntax and semantics for requirement specification (of the form assumptions ⇒ commitments). Our framework is heterogeneous in the sense that it supports both SeCeNL formulas and timing diagrams with nominals for system specification. It can also handle all of our limited liveness operators. (see Appendix. C for the code for minepump in our framework).

We have also developed a Python based translator which takes requirements in our textual format as input and produces property monitors as well as controllers as output. Fig. 11 gives a broad picture of the current status of our tool chain.

![Our tool chain.](image_url)

C Minepump Code

The example code for minepump is written using textual syntax for QDDC which can be found in [Pan00, Pan01].

```bash
#lhrs "minepump"
interface
{
```
input HH2O, HCH4;
output ALARM monitor x, PUMPON monitor x;
constant delta = 1, w = 10, epsilon=2, zeta=14, kappa=2;
auxvar DH2O;
softreq (!YHCH4) || (!PUMPON);
}
#implies lag(P, Q, n)
{
    td lagspeclet1(P, n)
    {
        P: <u>1|<v>1;
        @sync: (u, v, n);
    }
    td lagspeclet2(Q)
    {
        Q: 2|<v>1;
    }
}
#implies tracks(P, Q, n)
{
    td tracksspeclet1(P, n)
    {
        P: 0<u>1|<v>1;
        @sync: (u,v,[n]);
    }
    td tracksspeclet2(Q)
    {
        Q: 2<u>1|<v>0;
    }
}
#implies tracks2(P, Q, n)
{
    td tracks2speclet1(P, n)
    {
        P: 0<u>1|<v>0;
        @sync: (u,v,[n]);
    }
    td tracks2speclet2(Q)
    {
        Q: 2<u>0|<v>2;
    }
}
#implies sep(P, n)
{
    td sepspeclet1(P)
    P: 1<u>0|<v>1;
    td sepspeclet2(n)
    {
        @null: 2<u>2|<v>2;
@sync: (u, v, (n,])
}

#implies ubound(P, n)
{
    td boundspeclet1(P)
P: <c>1<d>1;
    td boundspeclet2(n)
    {
        @null: <c>2<d>2;
        @sync: (c, d, [n]);
    }
}
dc safe(DH2O) {
    pt || [!DH2O && ((HCH4 || !HH2O) => !PUMPON)];
}
main()
{
    assume (<!HH2O> ` true);
    assume (pt || [DH2O => HH2O]);
    assume tracks(HH2O, !DH2O, w);
    assume tracks2 (HH2O, DH2O, w);
    assume lag(PUMPON, !HH2O, epsilon);
    assume sep(HCH4, zeta);
    assume ubound(HCH4, kappa);
    req (<!ALARM> ` true);
    req lag(HH2O, ALARM, delta);
    req lag(HCH4, ALARM, delta);
    req lag(!HCH4 && !HH2O, !ALARM, delta);
    req safe(DH2O);
}
D Synthesized controller for minepump

A snapshot of a controller synthesized from the minepump requirement in §4.
The controller had approximately 140 states and it took less than a second for synthesis.

```plaintext
node minepump ( HH2O, HCH4:bool) returns ( ALARM, PUMPON:bool)
var cstate: int;
let
  ALARM, PUMPON, cstate = 
    ( if true and not HH2O and not HCH4 then ( false, false, 2)
    else if true and not HH2O and HCH4 then ( false, false, 4)
    else if true and HH2O and not HCH4 then ( false, false, 4)
    else if true and HH2O and HCH4 then ( false, false, 4)
    else ( dontCare, dontCare, 1)) ⇒
    if pre cstate = 1 and not HH2O and not HCH4 then ( false, false, 2)
    else if pre cstate = 1 and not HH2O and HCH4 then ( false, false, 4)
    else if pre cstate = 1 and HH2O and not HCH4 then ( false, false, 4)
    else if pre cstate = 1 and HH2O and HCH4 then ( false, false, 4)
    else if pre cstate = 2 and not HH2O and not HCH4 then ( false, false, 2)
    else if pre cstate = 2 and not HH2O and HCH4 then ( false, false, 7)
    else if pre cstate = 2 and HH2O and not HCH4 then ( false, false, 9)
    else if pre cstate = 2 and HH2O and HCH4 then ( false, false, 11)
    else if pre cstate = 4 and not HH2O and not HCH4 then ( false, false, 4)
    else if pre cstate = 4 and not HH2O and HCH4 then ( false, false, 4)
    else ( dontCare, dontCare, pre cstate) ;
```

E Case study: 3-cell arbiter

In this section we illustrate another application of our specification format and associated tools. For this we use the standard McMillan arbiter circuit given in NuSMV examples and do the model checking against the specification below.

A synchronous 3-cell bus arbiter has 3 request lines req1, req2 and req3, and corresponding acknowledgement lines ack1, ack2 and ack3. At any time instance a subset of request lines can be high and arbiter decides which request should be
granted permission to access the bus by making corresponding acknowledgement line high. The requirements for such a bus arbiter are as formulated below.

- Exclusion: \( \text{pref}([[(\bigwedge_{i \neq j} \neg (ack_i \land ack_j))]]) \). At most 1 acknowledgement can be given at a time.
- No spurious acknowledgement: \( \text{pref}([[(\bigwedge_i (ack_i \Rightarrow req_i))]]) \). A request should be granted access to the bus only if it has requested it.
- Response time: \( \text{implies}(([req]) \land slen = n,\ true \ \sim <ack>\sim true \ ) \). One of the most important property of an arbiter is that it any request should be granted within \( n \) cycles, i.e. if a request is continuously true for sometime then it should be heard.
- Deadtime: to specify this property we first specify lost cycle as follows: \( Lost \equiv (\bigvee_i req_i) \land (\neg (\bigvee_i ack_i)) \). Then \( \text{Deadtime} \equiv \text{anti}([[[Lost]] \land slen > n] \). This specifies the maximum number of consecutive cycles that can be lost by the arbiter is \( n \).

The requirement \( ARBREQ \) is a conjunction of above formulas.

We ran the requirement through our tool chain to generate NuSMV module for the requirement monitor. This module was then instantiated synchronously with McMillan arbiter implementation in NuSMV and NuSMV model checker was called in to check the property \( G(\text{assumptions} \Rightarrow \text{commitments}) \).

**Model checking** : Experimental results show that the deadtime for 3-cell McMillan arbiter is 3. If we specify the deadtime as 2 cycles then a counter example is generated by NuSMV as depicted in Fig. 12. This counter examples show that even though there is an request line high in 4th, 5th and 6th cycle, but no acknowledgment is given by arbiter. Similarly, the response time for 1st request is 3 cycles whereas for 2nd and 3rd cell it is 6 cycles. If we specify the response time of 2 and 5 cycles for 1st and 2nd then NuSMV generates counter examples in Fig. 13 and Fig. 14 respectively. Fig. 14 shows that the request line for cell 2 (i.e. \( req_2 \)) is high continuously for 5 cycles starting from 3rd without an acknowledgement from the arbiter.

![Counter Example]

Fig. 12. Counter Example showing deadtime exceeding 2 cycles
Fig. 13. Counter Example showing response time of 1st cell exceeding 2 cycles
Fig. 14. Counter Example showing response time of 2nd cell exceeding 5 cycles
Controller synthesis: We have also synthesized a controller for the arbiter specification using our tool DCSynthG. We have tightened the requirements by specifying the response time as 3 cycles uniformly for all three cells and deadtime as 0 cycles, i.e. there is no lost cycle. The tool could synthesize a controller in 0.03 seconds with 17 states.