Review—Management of Copper Damascene Plating

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An overview of process and quality control issues faced in controlling copper damascene plating is provided. The challenges for effective management of a copper damascene plating process have evolved due to early limitations and problems which were discovered, and then as more demands resulted from Chemical Mechanical Planarization issues, yield and reliability concerns, reduction in critical feature size and the shift to 300 mm wafers as well as the adoption of dielectric films with low dielectric constants. The demands have been addressed by adherence to quality control methodology, improvements in plater design and operation, advancements in plating electrolytes, and by new metrology tools and methodology. The key measurement areas outlined here are bath concentration measurement and control, film properties metrology, contamination issues, and defects. Particular attention is given to the use of electrochemical and optical methods with enhanced capabilities. This includes the use of chemometrics for electroanalytical bath concentration control and optical methods for film thickness, surface roughness, and film stress/wafer curvature measurements.

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The focus of this paper is on processing and quality control issues which are faced in the copper damascene electroplating processing. The paper draws heavily from the authors’ work in this field. No attempt is being made here to provide a comprehensive review of the wealth of studies published on Cu damascene electroplating. Many groups and individuals in industry and academics have made contributions; however, the pioneering work at IBM begun in the 1990s where the Cu damascene process was conceived,3–4 followed by the continuous work at National Bureau of Standards,5–15 plater and process development work at Novellus (now Lam Research),16,17 and Semitool (now Applied Materials),18,19 as well as the university studies of Professors Alan C. West of Columbia University20–24 and Uziel Landau of Case Western Reserve University25–28 and their research students deserve high recognition. A list of representative publications from these groups is provided in the bibliography. Most of the progress in the processing and quality areas occurred initially after Cu damascene processing was adopted in the semiconductor industry at approximately the 250 nm node and during the subsequent decade. Perhaps, the greatest advancements were made at the 130 nm and 90 nm nodes. However, during about the last ten years Through-Silicon-Via (TSV) plating has been the subject of much development work with reduced relative efforts being spent on Cu damascene plating at the 45–60 nm, 32 nm, and 22 nm nodes. At the 22 nm node, direct barrier plating is being pursued where special treatment of the barrier to remove any surface oxide is assuming a role. Each reduction in feature size has meant a reduction plating thickness and more concern about constraints of grain growth within the smaller features and resulting resistivity issues. It should be noted that many manufacturers do not use the most advanced plating technology. Work is progressing now on Cu electroplating for sub-10 nm features in the event the apparent limitations confronted with Cu resistivity characteristics cannot be overcome. For these smaller features, the ratio between the Cu to the higher resistance barrier layer increases, making the overall resistance unacceptable. It may be possible to replace Cu by Co and not employ a barrier layer.

It should also be noted that this paper is not a metrology paper. It does list those techniques which were available to the authors and which were found to be useful in process control of the Cu electroplating process. The application of some of these techniques such as AC voltammetry combined with chemometric data analysis (by RTA approach), scatterometry, the surface acoustic waves technique, and the coherent gradient technique for stress curvature and stress measurements were applied by the authors in ways that warrant providing details here. Professor Alain Diebold, now at College of Nanoscale Science Albany, NY, has a long track record of advancing metrology tools for interconnect applications, including for the Cu damascene process.29

Process control of Cu damascene electroplating has received little emphasis in the literature, so it is the focus of this paper. Process control helps to minimize process drift, shift, and other variability. In the course of conducting a process control program, metrology operations must be employed to characterize and monitor the process. The total variation is not only the process variation but also the metrology variation, so this variation must also be characterized and taken into account. Temporal and spatial variation must be considered at different scales; namely, within wafer, wafer-to-wafer and lot-to-lot. A quality control program must have provisions for initial tool and process qualification and subsequent process or tool changes which include repairs or upgrades. For any semiconductor process, the main issues which must be addressed for controlling process equipment, according to Emami-Naeini and Roover,30 can be summed up by the following five questions: What are the processes involved (physics)?, What are the actuators (inputs)?, What sensors are available (outputs)?, What are the performance metrics?, and What are the disturbances and uncertainties? These five aspects will be considered here.

Background

Copper electroplating became in the late 1990s and today remains the choice for multilevel metalization due to its ability to fill the trenches and vias without seams and voids in a damascene architecture. In addition, Cu has lower resistance and higher electromigration resistance than Al, provided that the grain structure is optimized and impurity concentrations are minimized. Moreover, electrodeposition is faster and has other advantages over other Cu metal deposition processes such as Physical Vapor (PVD) and Chemical Vapor Deposition (CVD). Cu electroplating is unlike other additive processes used previously in the semiconductor industry since is conducted at atmospheric pressure, near room temperature, and in aqueous electrolytes. When the shift from aluminum based metalization to copper metallization began in the late 1990s, there was a general lack of experience for conducting copper based processes. An incomplete understanding of how to achieve requirements was greatest for the copper
plating and copper Chemical Mechanical Planarization (CMP). Managing plating baths of large volume with multiple components whose composition changes at variable rates has been one of the major challenges for copper plating. Copper has unusual properties. It is known to be susceptible to oxidation under ambient conditions. Electroplated copper has unstable grains, so it had to be properly thermally stabilized or it will spontaneously undergo room temperature annealing. The instability of the electroplated copper film increases the complications of the metrology. Other challenges in metrology arise from the large and unrepeatable changes in thickness near the edge contacts, near structure, and over regions which may have defects or oxidation. Another major concern is how to prevent general copper contamination throughout the fab, especially when there is a need to use common process and metrology tools for Cu containing and non-Cu processes. All factors being considered, controlling a copper electroplating process has created ongoing process control challenges.

The requirements for copper damascene plating are product dependent and have a major impact on yield and reliability. The requirements can be divided into the categories of feature filling, thickness and thickness uniformity, film properties, defects, impurities, and issues related to copper contamination. Quality methodology must be applied to insure that the variations in the critical parameters are met at each stage of the plater life-cycle. The quality metrics must be quantified into specifications. An array of analytical instruments and methodology must be selected and qualified for use in measuring the parameters associated with the specifications.

Realization and modifications of the plating requirements will be a function of the incoming substrate to be plated which in almost all cases has a sputter deposited barrier overlaid with a thin Cu seed film, the plating chemistry, plater and plating process, the annealing process, the issues being faced at the Cu CMP process following the plating process, and the product test results such as electrical tests and reliability tests. Attention here will only be given to each of the first four categories. In addition, protocols have to be adopted and followed closely during each step of the damascene process to prevent unwanted copper contamination in the fab. This is especially important for those metrology and processing tools which must be shared for copper and non-copper processes.

In general, the incoming wafer characteristics of importance to plating include wafer size, design layout, feature sizes, aspect ratios, PVD copper feature coverage and thickness and thickness uniformity, defects from this process and those remaining from previous operations, and age of PVD seed before plating. The wafer size has increased from 200 mm to 300 mm. The critical feature size have decreased from 250 nm to < 22 nm. There are multiple barrier/seed requirements. In-situ deposition of the Cu seed layer on the barrier layer is critical to obtaining a strong (111) texture in the seed layer, and this texture of the Cu seed layer favors the development of highly textured, large grains in the electroplated Cu in the damascene structures which extends reliability.34 Seed age prior to plating is an issue since sputtered Cu films will undergo self-annealing and spontaneous surface copper oxide growth which affect seed wetting by the plating electrolyte. It is important to minimize seed loss due to etching by the plating solution when the wafer is first immersed into the plating bath. An edge exclusion is required to aid in contamination control as more layers are stacked, and it will be applied after plating. In addition, there has been significant progress made in the replacement of silicon dioxide dielectric films with low dielectric constant films which have created integration challenges. Thinner Cu seed will result in higher over-potentials for plating and a resulting greater S incorporation from the accelerator and a smaller grain structure.35 Many studies have been performed on different barrier materials and even direct plating on barrier films without a seed layer. The barrier material has a major effect on the overall resistivity of the metal interconnects and affects the grain structure of the plated copper film. Many of these issues will be considered in more detail later in this paper.

Most plating reactors are of the fountain type with a vertical design in which the wafer is immersed upside down in the plating cell and rotated during the plating operation. A schematic of advanced commercial plater is not available in the literature. Figure 133 provides a schematic of a prototype 200 mm plater which utilizes a unique hardware design to study the effects of variation of the current distribution upon thickness uniformity and compare the experimental results numerical analysis.38 Only general features of commercial plating tools cannot be listed, due the proprietary concerns. Introducing the wafer into the bath requires special provisions to insure wetting of the seeded surface without the trapping of air bubbles which were found to leave a swirl pattern in the plated film if current was applied when the wafer is immersed. Multiple plating cells (often 3) are connected to a large volume plating bath (approximately 150 to 200 liters) whose temperature is closely controlled in the vicinity of room temperature. Either a membrane or ceramic separator is present between the copper anode and the cathode compartment. Shields and diffusers are employed to maximize the uniformity of the current distribution. The plating bath solution is recirculated through filters at a higher flow rate while wafers are being processed. Plating electrolyte at a defined flow is directed in at the wafer surface. Electrical contact is made to the wafer by metal contacts uniformly positioned around the outer circumference. The contacts in some platers are maintained in a dry state and have no exposure to the electrolyte. In other platers, the contacts become immersed in the electrolyte. In this latter case, the copper which is plated onto the contacts must be removed by de-plating or by chemical etching. The current density is larger at the edges of the wafer, where electrical contact is made than at the center of the wafer which is far from the point of electrical contact. This phenomenon is known as the terminal effect, and it results in non-uniform copper thickness distribution across the substrate surface. A planar phosphorous doped Cu anode faces the wafer being plated. Non-consumable anodes are generally not employed due to the possibility of gas bubble generation which could result in plating defects. The wafer is usually plated galvanostatically with a multi-step DC current waveform with the first, lowest current step optimized for filling the smallest features, the second, higher current step aimed at filling larger trenches, and the third step at the highest current intended to complete the plating process as quickly as possible to maximize wafer throughput. Pulse plating waveforms with bipolar power supplies have also been utilized at times in platers. After plating, the wafer must be rinsed and dried before it can be removed from the plater. Provisions in newer plater models have been included for creating an edge exclusion area. Other improvements include electrolyte bleed-and-feed, automatic concentration replenishment algorithms based on predictive modeling, anode chamber isolation, improved diffusers and clamshells, independent control of split, concentric anodes for thickness profile shaping, etc.

Plating chemistry has undergone major changes from the earliest plating chemistry which was adopted from the Printed Circuit Board (PCB) industry. The objective for the plating bath formulation is bottom-up filling with inhibited growth at the edges and tops of the trenches or vias. The main driving forces for improvements in plating chemistry have been increased thickness uniformity requirements and the gap-free filling of reduced feature sizes. The plating chemistry also has an important role in determining the electroplated grain structure. The electroplated grain structure is unstable, so recrystallization is required for stabilization of film properties. This will occur by self-annealing if the plated wafers are left undisturbed. To expedite the damascene process flow and to insure reproducibility for the Cu CMP it is necessary to anneal the electroplated copper film and thereby stabilize the microstructure to insure that the CMP removal rate is reproducible.

Cu CMP has required major development for damascene processing. Complete clearing of the copper overburden and barrier layer as well as the minimization of dishing and erosion are highly dependent upon the thickness and the local and global non-uniformity of the electroplated copper. Achieving global and local non-uniformity to meet the needs of CMP has been an ongoing struggle for the copper plating process. An early incentive for uniformity improvements was a consequence of the momentum plating that occurred in dense array structures for plating chemistry that employed only an accelerator and
suppressor. The initial two component plating chemistry consisting of a suppressor and an accelerator displayed an overshoot in the gap filling process which resulted in protrusions or bumps over densely patterned features. The momentum problem is a result of the accelerator species dominating the surface absorption sites and controlling the kinetics of the deposition process. As the smallest features fill, the evolving and accelerator enriched regions at the feature openings will continue to deposit copper at a faster rate than the surrounding surface. This problem is illustrated in Figure 2. These overplated copper mounds created difficulties for the CMP process. Consideration must be given to the different feature size range within the die. In this regard, the plated areas over the larger features such as bond pads are depressions rather than protrusions. The amount of overall Cu overplating across the wafer must be adequate to insure that the bottom of these depressions are still above the plane of the surface, so that the final post-polished surface will be conformal with the surface plane. In order to reduce the CMP time, it is desirable to attain good Cu plating planarity between the dense, high aspect ratio features as well as the larger features which are more isolated which will permit the overplating thickness to be minimized. The Cu filling process starts with the small features and progresses to the larger features. The plating time to fill the smallest features has been reduced from approximately 35 s at the 180 nm node to approximately 5 s at the 45 nm node. The overplating thickness has also been significantly reduced at each node, requiring improved plating uniformity. Pulse plating was evaluated as a possible solution to momentum plating, but in general it was not found to be totally effective in preventing this problem and in some cases the defect density increased. Leveler, a third organic additive, was found to be more effective in preventing hillock formation. The leveler does so by minimizing the absorption at the feature openings of the accelerator. The use of levelers enabled a return to multi-step DC plating. When a shift was made from 200 mm to 300 mm plating, the terminal effect was partially overcome by the adoption of high copper/low acid plating chemistry from low copper/high acid plating chemistry which had been the choice initially for 200 mm plating. The low acid chemistry was, however, beset with a higher propensity for crystal formation, which requires frequent cell rinses. Progress by a number of investigators using modelling and an array of characterization techniques has been and continues to be made in gaining more insight about the mechanism responsible for superfilling which has resulted in needed additive enhancements.

**Quality Control Implementation**

Quality control of a process semiconductor requires the application of statistical methods from the very outset of tool qualification, at process optimization, during gauge and capability studies for the metrology tools, and for statistical process control of the key parameters which are used to monitor the performance of the process tool. Quality control of a plater operation requires monitoring and fine-tuning of the plating process to achieve desired performance characteristics. This includes monitoring of plating chemistry, current distribution, and plating uniformity. The implementation of a quality control program ensures that the plating process is under control and meets the required specifications.

Figure 1. Prototype 200 mm Plater which enables the current distribution to be varied.33

Figure 2. SEM cross section showing severe overplating.
controlling the wafers to be plated, the plating chemistry, the plating tool operation itself, and the plated wafers before and after annealing to insure that the requirements placed upon the plating process by CMP, those for yield and reliability, and those required for contamination control are satisfied.

Operational specifications need to be written, followed by training and qualification of involved processing personnel. Provisions for tool maintenance and repair need to be established for not only the process tool but also the metrology tools. Provisions must also be made for quality checks on the required chemicals and consumables. Each lot of chemicals should be accompanied by a lot certification and/or incoming quality tests should be performed before the chemical is used for processing.

The use of blanket wafers for the majority of quality control studies is favored; however, pattern wafers must still be included to properly assess gap filling. The effective area and seed resistivity for pattern wafers are greater than observed on blanket wafers with the same seed deposition process, so some differences can be expected in plating performance. Wafer flows need to be established for both blanket and pattern monitor wafers. The pattern wafers preferably should be prepared in a short loop flow to minimize costs. A large number of Cu seeded monitor and conditioning wafers are required for plater operation. The monitor and conditioning wafers could be from separate lots. Alternatively, the monitors can be separate for convenience in measurement activities and even reserved for later use in CMP tool qualifications. The PVD copper seed thickness and deposition recipe should be the same as that used for product wafers. It will be desirable to pre-measure the thickness and profile of the seed and track this as an SPC parameter. In some cases the Cu seed age prior to plating can affect the in-film defectivity of the plated Cu films, so this will have to be established. Each plating cell must be properly conditioned after idle periods and after maintenance operations such as contact changes or cell rinses and prior to each qualification preceding production runs. The number of wafers required for conditioning must be determined, as well as the plating thickness. The conditioning wafers can be used more than once. Both the conditioning and monitor wafers can be recycled by stripping the copper using nitric acid or a sulfuric acid/hydrogen peroxide mixture. The barrier will remain intact, so the wafers can be re-seeded for repeat usage. Alternatively, prior to rework, it may be convenient to send the used monitors on to the CMP process for use as conditioning and qualification wafers for the copper CMP process.

For the metrology tools, the questions that need to be resolved include the size of the measurement variation, the sources of measurement variation, stability of the instrument over time and over the measurement range of interest, calibration frequency and technique, and whether an SPC procedure for the metrology tool itself needs to be established. To evaluate a metrology instrument a Gauge Repeatability and Reproducibility (GRR) study must be performed. The gauge study will help to establish whether the metrology tool has the capability to measure the parameter of interest. These gauge studies are particularly important for copper film parameter measurements. Repeatability measurements on blanket plated wafers are performed in a metrology gauge study using a diameter scan and/or contour map. Pattern wafer Cu repeatability gauge studies should be performed on multiple features, multiple sites in a die and multiple die. In conducting a gauge study, multiple operators measure several wafers repeatedly over a number of days. An analysis of the data reveals the operator capability to repeat their own results as well as how reproducible the measurements are from one operator to another. The precision of the measurement is the total measurement variation which includes the combined effect of repeatability and reproducibility. Besides the actual measurement, some variation can be attributed to the wafer handling mechanism of the tool and there may also be environmental influences that may be related to the time-of-day and the day-to-day variation. It is of note that the total variation measured for the process is equal to the square root of the sum of the square of the process variation and the square of the metrology system reproducibility.

For acceptance, the plater must conform to the performance and reliability specifications which were agreed upon both by the tool customer and the supplier. The plating chemistry chosen as well as the process details selected for the qualification are usually a process of record (POR) recommended by the supplier.

After acceptance of the tool, optimization of the process for the product or products of interest should be conducted. The optimization process has as its goal the development of plating recipes for the specific products for which the plater is to be utilized. These recipes are most conveniently adapted from the POR recipes provided by the supplier. This optimization process should include input and involvement from other damascene process owners. It probably will be necessary to optimize the parameters used for the PVD barrier and seed process that will be employed for the blanket and patterned wafers to be plated. The PVD optimization will seek to provide the most favorable plating results. An annealing process for the plated films must be developed to stabilize the films. It will be necessary to coordinate with the CMP process tool owner to insure that the plating recipes yield the best CMP results. Due to the large number of parameters which can impact the process, process optimization is accomplished by the use of experimental design. Once the desired production process (POR) is selected, another marathon is generally in order. It is usually possible from the results of this marathon to arrive at limits for the statistical control parameters. These parameters are often called the critical parameters and are the minimum number of key control parameters that will be used for monitoring the process.

In general, a Statistical Process Control (SPC) Program needs to be implemented to monitor and control process variability. SPC is a two-step process with the goal of distinguishing between systematic or normal variations from special or unusual variations. The initial step in SPC is to calculate a Process Capability Index (Cpk) by measuring normal variations in the key parameters from the data collected at the various stages of processing. A capable process is one where the critical parameters fall within the specification limits. The second step, which is performed after processing product wafers after the tool has been idled, for example, involves plating and monitoring the Cu seeded qualification wafers. The qualification step usually is followed by the use of suitable sampling plans for monitoring plated product wafers. Control charts are employed for the key parameters measured from the plated qualification and product wafers monitored to reveal whether there is a violation of SPC rules. In case of violations, alarms are generated that give early warnings of process issues. SPC by its very nature is a passive process, and it provides no clue as to what went wrong. An out-of-control action plan needs to be formulated and applied whenever process drift which violate the SPC rules is encountered. One of the actions taken could be suspension of processing until the SPC parameter or parameters are brought back within the control limits by suitable corrective measures.

SPC charts need to be set up for each critical parameter being monitored. This will include the measured value of the parameter and in most cases the non-uniformity of that parameter for a multi-point diameter or contour map. An example is shown in Figure 3. The bath component concentrations should also have separate control charts. Concentration monitoring and control is really a special case, since it should even be performed periodically, even when the tool is idled, it to keep the concentrations from drifting out of control. All the SPC charts should be available on an online tracking system and Cpk calculations performed periodically. Adjustments in control limits should be made if indicated by the data. Thickness profile measurements and in-film defectivity on blanket plated wafers should be a bare minimum. For reasons, discussed in this paper, surface roughness also is very diagnostic of multiple plating parameters, as will be shown in this paper, and is a valuable parameter to monitor. There will be some parameters such as fine feature filling of vias and trenches on patterned wafers which can be measured periodically but not before each qualification. Short loop fine patterned wafers can be dedicated to this purpose which will facilitate comparisons between tests. The width of the edge exclusion created during the plating process and its concentricity need to be measured on a periodic basis. Copper contamination
levels on the edge bead and wafer back side should be measured periodically. Secondary Ion Mass Spectrometry (SIMS) measurement of incorporated impurities originating from additive breakdown is desirable. Defect and wafer curvature measurements on pattern product wafers after plating can provide valuable information not only on the plating process but also in some cases the results can be related to the consistency of earlier steps. Copper thickness measurements can also be performed on lot samples of product wafers at different features at different sites on the wafers by the nondestructive optical technique described later. The sampling plan should measure the performance of each of the plating cells involved in the plating operation.

Any change to the process such as a change in hardware, software, or plating chemistry will need to be qualified before committing product wafers. A qualification process can range from a full marathon to a more abbreviated version, such as the normal qualification, depending upon the nature of the process change. A marathon can also provide key metrics not only on process performance but also on tool performance, including reliability information. It is important to recognize that many such parameter changes cannot usually be made independently, due to synergetic effects. For example, a change in the plating chemistry will require not only a replacement of all consumables to prevent contamination, but possibly changes to the actual plating recipes, and certainly new analytical methods for composition control. Performing an experimental design to optimize the process may be required as well as a complete marathon in some cases. A change to the barrier/seed process, for example, will have major effects on the plating results, so considerable process optimization will be required, and this will include the use of some pattern wafers.

In the case of tool failures, Failure Mode Effect Analysis (FMEA), a quality methodology, is often employed to drive actions to eliminate or reduce the likelihood of actual tool failures.36

### Plater Bath Composition Control

Bottom-up plating of trenches and vias which makes Cu damascene processing possible relies upon organic additives. These additives are classified as “brighteners or accelerators”, “suppressors or carriers” which are wetting agents, and “levelers”. These additives are competitively adsorbed on the cathode during the plating process and thereby affect the thickness distribution and properties of the electroplated Cu. The suppressors are primarily polyether or polyoxyether polymers with optimized molecular weight. Polyethylene glycol (PEG) is a widely used suppressor. The suppressor is uniformly adsorbed on surface, causing interfacing polarization and reducing the plating rate. The suppressor forms a complex with the chloride ions in the electrolyte. It is necessary to optimize the chloride concentration for this synergy. Moreover, the molecular weight of the suppressor is an important factor in its performance. The suppressor is characterized by slow diffusion. The accelerator most often is a thiol, disulfide, or mercaptan which contains a pendant sulfur atoms. A common accelerator is bis-(sodium-sulfopropyl)-disulfide, usually abbreviated SPS. This functional group on the accelerator enables it to competitively replace the suppressor and reduce the polarization relative to that of an electrolyte containing only the suppressor. Based on many of the superfilling models, the accelerator is able to replace the suppressor more rapidly at the bottom of features than elsewhere on the Cu seeded wafer, creating a differential plating rate which favors the bottom-up fill process. The accelerator participates directly in actual electroplating process and can be partially transformed by the process. Fractions of the accelerator can be incorporated in the film, adding to the impurity level of the electrodeposited polycrystal which influence the grain structure and other properties of the Cu. Incorporation of nonmetallic impurities (C, O, S, N, and Cl) are often found in electroplated Cu films. Some products of the accelerator that are not consumed can retain electrochemical activity and build up in the plating bath, leading to altered plating performance over time, such as 3-mercaptopropylsulfonic acid, abbreviated MPS, which is the reaction product of SPS. The accelerator is a relatively small molecule which can diffuse rapidly. The leveler has suppressing properties, but it is nitrogen containing and acquires a positive charge in acidic solutions, since it is protonated. An example is polyvinylpyrrolidone. The leveler molecules become strongly adsorbed at the seeded edges and surface irregularities during plating, causing the greatest polarization and plating inhibition at these locations. It is probably able to displace the accelerator on the wafer surface. Redox processes involving the organic additives or additive by-products at both electrodes are possible as well as oxidation processes with the dissolved oxygen in solution. The accelerator can be consumed even during idle periods. Some advanced platers have separated anode chambers to minimize the effects of organic decomposition products.

One of the key requirements for controlling a copper damascene electroplating is monitoring and control of the concentration of each of the plating cells involved in the plating operation. Proper concentration control is vital to insure
void-free and complete via and trenched filling as well as to obtain the optimum deposition rate, mechanical properties, and grain structure of the plated copper film. The three organic additives (accelerator, leveler, and suppressor) as well as the inorganic components (sulfuric acid, chloride ion and copper (II) ion) concentrations must be all measured and controlled since they can be consumed, there can be some drop-out, and errors can occur in the automatic control algorithms, if present. Another important issue is the buildup of additive breakdown products which can be electrochemically active. Optimally, real time monitoring should be conducted and automatic adjustments made to the components which are out of spec. It should first be verified that the component concentrations are within the specification limits before proceeding with any additional qualification steps and before product wafers are plated. If plating is performed without the concentrations being within the specification range, deleterious effects may occur to the product which also may not be evident until a later stage.

Multiple complications must be overcome to perform concentration control. Among these is the requirement to quantify six components with different concentrations and different chemical and electrochemical properties. For example, a common suppressor such as polyethylene glycol (PEG) is slow diffusing and fast absorbing, while a common accelerator such as SPS is fast diffusing and slow absorbing. The 3 organic additives and the chloride concentration are in the ppm range, while the sulfuric acid and cupric ion concentrations are most commonly in the range of 10 to 175 g/L in the former case and 17 to 50 g/L in the latter case. However, some plating chemistries can fall out of these ranges. Lower inorganic concentrations are now being considered for future production nodes. Even though the organic additives are in the ppm range, the organic concentrates, whose identities are proprietary, are provided to the end user at a concentration of 1000 mL/liter. That is, no standard concentration units are employed. Thus, specifications for the additives are in terms of milliliters per liter of plating bath solution.

Bath concentration control is complicated by composition changes that occur at different rates for each of the components during idle and as the plating process proceeds. Drop-out is one issue in which some plating solution is carried out of the bath as the plated wafers are removed. During plating, the compositional changes depend upon the number of wafers being plated and the parameters which are employed in plating recipes. By-products from the organic additives can build up in the bath over time, whose presence may adversely impact the plating performance. In the early phase of copper damascene plating, bath measurement and control was highly dependent upon the skill of the manufacturing operators and relied upon removing aliquots from the bath for external laboratory analysis which were costly and time consuming. Moreover, progressive depletion of additive concentrations occurs in samples sent to an external laboratory, especially if such samples are exposed to extreme conditions such as exposure to elevated temperature during shipment. Errors in concentration adjustments can prove to be very problematical since the plating bath generally is of very large volume (typically 150 to 200 liters) and corrections can be both expensive and time consuming. Improvements have been made in the analytical methodology and instrumentation making possible automated analysis to be conducted on sample aliquots taken directly from the bath by the analytical tool which is in close proximity to the plater. In some cases, the results of the analyses are entered into special software which makes the concentration adjustments automatically and thereby removing the human factor.

Automatic bleed-and-feed implementation has helped prevent the buildup of additive breakdown products. Automatic concentration replenishment algorithms based on predictive modeling that includes the number of wafers plated, the charge passed, and other plating parameters have also helped in concentration control. These algorithms are not perfect, so actual component analysis is still required for continuous verification and adjustment of the algorithm.

There are currently two major options for copper plating bath additive and inorganic component concentration control in wide usage. Both options have been shown under normal conditions to be comparable. One technique is based upon cyclic stripping voltammetry (CVS). The organic additives are quantitatively measured by the CVS response of both the plating electrolyte, which contains all the inorganic components, without organic additives, known as the Virgin Makeup Solution (VMS) solution, and different procedure-specific solutions of the plating bath after additions of a known amount of the standard additive. It was transitioned from the PCB industry into damascene processing at the very outset. This technique now has enhanced capabilities and automated systems are available. The second technique based upon AC voltammetry and chemometrics and has now won widespread acceptance. There are other electrochemical, chromatographic, and mass spectroscopic techniques which have been developed for organic additive analysis, but these techniques will not be reviewed here.

As noted above, the CVS technique for the organic additives is based on the cyclic process of plating and stripping of metal from an electrode. Adsorption of additive on the surface of a rotating working electrode inhibits the rate of copper deposition. This decrease is quantified by measuring the anodic charge in the anodic stripping peak. The decrease in deposited charge is related to the change in concentration of the additives. Figure 47 provides an overlay of cyclic voltammograms for the High Acid (HA) (containing about 180 g/L of sulfuric acid) electrolyte with and without the 3 organic additives at the proper operational concentration for 200 mm plating with the Low Acid (LA) (containing about 10 g/L H2SO4) electrolyte with and without the same 3 organic additives but with different optimum concentrations for 300 mm Cu plating. These cyclic voltammograms utilized the same potentiostatic parameters and a rotating disc Pt electrode. It is clear from the size of the stripping peaks, that the plating rates of Cu differ for each solution. The LA without additives has the highest plating rate. The ratio between the oxidation peaks for the HA electrolyte with additives to that electrolyte without additives is 0.077, while the corresponding ratio for the LA electrolyte with additives to the LA electrolyte without additives is 0.242. Clearly, there is more suppression in the case of the HA chemistry. As expected, the plating rate is highest for the LA electrolyte which has the higher copper concentration.

The three additives and some of the additive breakdown products all compete for adsorption on the surface of the cathodic electrode and affect the measurement, so separate titration procedures which employ CVS are required to establish the concentration of each additive in the plating bath solution. Additional techniques are employed for the acid, chloride, and copper ion concentrations. Manual implementation of the different required procedures are not only time consuming but also create the need for staff on multiple shifts with analytical skills. Automated instrumentation is now, however, available. This technique has been discussed in previous publications which can be consulted for additional details.

Specifics of the second technique based upon AC voltammetry and chemometrics are less widely known, so will be briefly outlined here. This technique relies upon the functionality of the components in the plating process, so there is no need to know the identity or the exact molar concentration. Ludwig in 198647 revealed a method based on AC voltammetry in which the AC current is measured in relation to a varying DC potential. The AC voltammograms obtained contain fine structure and enable in-situ monitoring of minor plating bath constituents without any sample preparation or routine, repetitive utilization of standard solutions. Figures 54 and 64 provide examples of the AC voltammograms. Employment of this approach, establishing optimum conditions for acquiring voltammograms for each of the bath components, and the adoption of multivariate chemometric data analysis techniques, which continue to be refined and expanded upon, have resulted in a several successful generations of Real Time Analyzers (RTA).

The Real Time Analyzer (RTA), available today utilizes numerous DC- and AC-voltammetric techniques and serves as an in-situ, online monitoring system that provides a complete chemical analysis of plating solutions.44-46 Even the Cu reference electrode is created and utilized during the analytical sequence. The RTA’s unique feature is
its capability of analyzing non-invasively the solution sample without any pretreatment, returning the unaltered sample solution back to the plating tank. The fully-computerized instrumentation requires no specialized chemical operators. The analysis can be performed automatically in a 15 to 30 minute time frame. Actually, a series of separate scans are utilized not only to predict concentrations but also for monitoring the bath health based upon the shape/deformation of these extra scans. The system has highly reliability, since the only moving part is a small sampling pump. The analytical results are readily accessible and, thanks to the integration and customization of the open-architecture software system, they can also be ported to the bleed-and-feed system for concentration adjustments and tracking. Master calibration is in fact performed at the factory, so the need for a chemical analytical laboratory in or near the fab is eliminated. It is of note that such an electroanalysis is extremely challenging due to synergistic functions of bath additives, their various chemical structures, different concentration ranges and the presence of accumulating degradation products. Since the electroanalysis mimics to a certain degree the actual plating process on a microscale, the issues affecting the plating process will also quite likely manifest their presence on the voltammetric signals, thereby enabling early fault detection which minimizes production losses.

By utilizing extensively chemometrics for analysis of AC voltammetric data recorded with a single voltammetric sensor, the RTA...
addresses both major objectives of bath analysis; namely, I) prediction of concentration of bath constituents, and II) early fault detection and diagnosis and classification of detected disturbance. The first objective is reached by employing for the calibration calculation methods that rely on two-way data chemometric decomposition techniques, including hierarchical techniques, along with multi-way methods. An emphasis is put on aspects of variable selection, as well as transference of the master calibration analytical model calculated for the primary instrument to secondary instruments. Also, methods for mitigation of adverse temperature effect on voltammograms are elaborated upon extensively. Achieving the other objective, various applied-by-RTA methods of early fault detection and diagnosis are described in, with a real-life application in a case study presented in. Soft Independent Modeling of Class Analogy (SIMCA) was implemented for supervised classification of various disturbances likely to occur in the plating solutions.

By way of comparison, the CVS technique typically focuses on separating the effect of a single component at a time while suppressing matrix effects by a sample pretreatment. It provides an accurate prediction of the concentration of the deliberately added constituents, but insufficient information about total accelerating or suppressing effect. RTA by analyzing the sample “as is” provides a measure of the apparent, consolidated effect of deliberately added bath constituents and degradation products still having accelerating or suppressing activity.

### Thickness and Thickness Uniformity Measurements

The plating thickness profile is a major parameter which must be closely monitored and controlled. It is important to achieve plating cell and plater-to-plater matching. Variations to the ohmic contacts made to the wafer along the outside periphery is one of the common problems which can arise and which can adversely affect the plating profile. It is also necessary to insure the reproducibility of the edge bead process.

As was noted earlier, the Cu plating profile is partly dependent upon the copper seed thickness and profile. The plating profile is usually edge thick due to the resistivity of the thin copper seed and the conductivity of the plating bath. A change was required from high sulfuric acid electrolyte to a low acid and high copper ion concentration electrolyte to move from 200 mm to 300 mm plating. The High Acid electrolyte, HA, has a conductivity of 510 mS/cm, while the Low Acid electrolyte conductivity is approximately 65 mS/cm at 25°C. That is, the Low Acid electrolyte, LA, has a higher resistivity. As feature sizes are decreased, the barrier and seed layer thickness must be reduced to prevent necking. The reduction in Cu seed thickness and the resulting high substrate resistance, cause the plating current distribution to be more non-uniform. Moreover, the corrosion of the Cu seed by the dissolved oxygen in the plating bath becomes a greater concern as the seed thickness is decreased. Figure 7 reveals that the LA electrolyte has a higher etch rate for the Cu seed than the HA electrolyte.

In many cases, the CMP process will be optimized to accommodate the plating profile. In some cases, it may be found desirable to instead adjust the Cu plating profile for the CMP process. It is important to eliminate any pattern dependency in the plating and minimize the plating overburden to increase the plater throughput and to decrease CMP polish time, to improve the polishing uniformity, and to help reduce dishing and erosion of features.

An analytical procedure for process monitoring and control must provide accuracy, reproducibility, and robustness. Thickness metrology must possess the same attributes to insure that the thickness and uniformity specifications are being met. It should be easily adaptable for different plating chemistries. One complications of Cu plating thickness metrology is that the electrodeposited (ECD) copper is plated on a Cu seed film having a barrier under-layer; thus the actual plated thickness must derived by subtracting the Cu seed thickness from the total metal stack thickness. Another complication is that the materials parameters change as the ECD copper undergoes annealing. It is imperative for quality control applications to make rapid, multiple point measurements on the wafer to obtain a true picture of the plating profile. It is desirable to have good spatial resolution to enable the edge exclusion area to be mapped and to also to compare the copper filling of large features on patterned wafers. It is beneficial to have a measurement technique which is nondestructive.

The most common metrology tools for copper thickness measurements are not absolute measurement techniques so they must be calibrated. It has been found necessary to perform a separate calibration for as-deposited ECD films and another for annealed ECD Cu films. Thus, different recipes must be used to measure pre- and post-annealed copper thickness by the electrical or optical thickness measurement techniques which are discussed here. It may be necessary to recalibrate after a change in plating chemistry which can also impact the film properties. Calibration is required for the PVD barrier/Cu

![Figure 6. AC voltammograms of copper damascene solution showing a multiplicity of features, each of potential analytical application for soft modeling.](image)
There are multiple choices for obtaining the absolute Cu thickness for the calibration. The cross-sectional Scanning Electron Microscopy (SEM) analysis and anodic chronopotentiometry were used for our work. Using an ECI Technology Surface Scan QC-100 (East Rutherford, NJ) for the anodic chronopotentiometry, the Cu thickness of a circular area of 0.02 cm$^2$ of the plated film can be determined. Figure 8 is a schematic of QC-100. An anodic chronopotentiogram obtained using an aqueous ammonium nitrate electrolyte in which the current is held at a constant value and the potential is monitored is shown in Figure 9. The end point is clear from the rapid increase in voltage when the copper has been completely removed by oxidation. Using Faraday’s Principle which is given below, the seed layer thickness, $T$, from this measurement was found to be 1020 Å while that of the electroplated film was evaluated to be 16020 Å. The calibration standardization measurements are required at multiple sites due to the relative non-uniformity of ECD films. It is, of course, necessary to match metrology tools.

$$T = \frac{M \times I \times t \times 10^8}{n \times F \times S \times D}$$ \[1\]

- $M$ = molecular weight (g/mol)
- $I$ = current (A)
- $t$ = time (s)
- $n$ = number of electrons
- $F$ = Faraday’s constant (96,498 C/mol)
- $D$ = density (g/cm$^3$)

The 4 pt probe technique has been extensively employed for Cu film thickness measurements. The 4 pt probe technique can be used to monitor the sheet resistivity which is an important materials parameter of the Cu film. One of the disadvantages is that the measurement is sensitive to the microstructure, so neither the film thickness nor the electrical resistivity can be measured independently. There is a calibration requirement to arrive at a factor to convert sheet resistance to thickness. Moreover, the factor does change as the plated film undergoes self-annealing or after an annealing process which is part of the damascene flow. This means that one recipe is required to measure the thickness of as-deposited Cu films, and a second recipe for annealed films. This technique has limited spatial resolution which is not adequate for the measuring the width of the edge bead. It also leaves probe marks on the plated copper surface which limit the usefulness of the plated films for other tests. It is also not acceptable technique for patterned wafers. It is still is of value to monitor the sheet resistivity since it is a materials parameter of the copper film.

A very valuable optically based tool overcomes almost all the limitations of the 4 pt probe technique. This laser based technique, known as the Surface Acoustic Waves (SAWs) technique was developed by Philips Analytical. This technique is also known as Impulsive Figure 7. Cu seed thickness etch curve for high acid electrolyte, solid line, and low acid electrolyte, dashed line.
Stimulated Thermal Scattering (ISTS) or Transient Gradient Optoacoustics. The SAWs measurement is a technique for surface acoustic wavelength measurement in a small spot configuration allowing user-selectable acoustic wavelength. Two sub-nanosecond excitation laser pulses are crossed at the sample surface to form a spatially periodic intensity pattern with a period in the range of approximately 2 to 11 micrometer, controlled by the measurement recipe. Absorption of optical radiation results in a temperature rise and subsequent impulsive thermal expansion that launches two counter-propagating surface acoustic waves with a period equal to the intensity pattern, as well as thermal grating associated with the temperature profile. This technique will be made more clear by Figures 10 and 11. The time dependent surface displacement caused by the SAWs and the thermal grating is monitored via diffraction of a probe laser beam. The signal waveforms are averaged over approximately 1000 excitation pulses, which takes approximately 1 s. The measurement apparatus is described in more detail elsewhere.\textsuperscript{60,61}

It was found that the ISTS technique can be applied for the following in copper damascene copper plating management: PVD monitoring of the barrier/Cu seed process, ECD thickness and uniformity monitoring, edge control, and Cu fill control. The merits of this technique for these applications include thickness sensitivity, good precision, small spot size capability for wafer edge (see Figure 12) as well as small feature characterization, good throughput, capability to determine other materials parameters for the Cu films, including sheet resistivity, capability to measure the thickness of the underlying barrier metal, and nondestructive nature which allows the wafer to be used for subsequent processing and/or measurements. Figures 13 and 14 are contour maps obtained with this tool on 200 mm plated blanket wafers which clearly show thickness nonuniformities at the...
wafer edge. It can be employed for on-product measurements, and the capability is especially valuable after CMP processes. It should be noted that calibration is still required. For the most accurate results, different recipes should be used to measure pre- and post-annealed copper thickness. In one study a 3.7% increase in the copper acoustic velocities was found after annealing, revealing that the copper gets stiffer and its acoustic properties change during annealing.

The simultaneous monitoring of thickness, resistivity, and grain structure with the ISTS technique have been demonstrated. Some additional signal processing and calibration is required to derive the resistivity and grain structure. Figure 15 demonstrates that both thickness and resistivity can be simultaneously measured by the ISTS technique. Excellent agreement between thickness measurements performed on the same 300 mm blanket electrodeposited Cu and annealed film by four point probe, FPP, sheet resistivity measurements and by the ISTS technique are shown in Figure 16. For copper, the thermal and electrical conductivity are dominated by electron transport and have been shown to well correlate with each other. The Surface Wave signal is fitted with an exponential function to extract the decay time. The decay time is proportional to the ratio of the thermal bulk resistivity to the per-volume heat capacity, based upon some reasonable assumptions (i.e. that conductivity of the dielectric is much worse than that of the copper).

Surface Roughness Measurement

An optical technique which is based upon Total Integrated Scattering (TIS) has proven to be extremely valuable for plated film surface roughness characterization. Surface roughness is a measure of the micro-topography of the plated film. Micro-roughness of a surface has proven in many products to have a determining role on the geometrical, mechanical, physicochemical, electronic and optical properties. Besides being related to grain structure, roughness within the features being plated is thought to have a negative effect on the gap filling process. Moreover, roughness must be minimized so that defects can be more easily detected. Monitoring the surface roughness provides a sensitive, rapid, nondestructive measure of the plating process reproducibility. Studies reviewed below indicate that the surface roughness displays dependence to many of the plating variables, such as the mass transport processes. TIS measurements are easily and nondestructively performed on a blanket plated qualification wafer before or after a thickness profile check by optical means.

The particular instrument which was used in this work, a Veeco TMS-3000 W, is capable of providing rapid, reproducible, nondestructive, full wafer surface measurements on both 200 mm and 300 mm wafers. The instrument features a Root Mean Square (RMS) surface roughness measurement range of 0.1 Å to 5000 Å with a resolution of ±0.1 Å or 1%, and a speed of 50 test points per second. In addition, the rotary stage has an accuracy of ±0.05° and a linear stage accuracy of ±0.05%.
of $\pm$ 0.03 mm. A combination of these stages provides means for any part of the wafer surface to be positioned at the measurement location under the optical assembly. Figure 17 provides a schematic of the optical assembly of instrument. This tool directs 670 nm laser radiation at the wafer surface of interest at near normal incidence (5 degrees). The specular reflected light as well as the diffusely scattered light is collected by an integrating sphere and directed to several detectors as the wafer scanned using an operator defined sequence. (Specular reflectance which is at an angle matching the angle of incidence constitutes the majority of reflected light. The diffuse scattering, on the other hand, is weaker in intensity and since it occurs at a wide range of angles it is best collected with an integrating sphere. The specular reflected light is coherent, while the diffusely scattered light is incoherent.) The ratio of the diffuse scattering to the reflected specular scattering energy is used to compute the surface roughness using the following equation:

$$TIS = \frac{P_s}{P_r} = \left[\frac{4\pi N \cos \theta_1}{\lambda}\right]^2$$

where $TIS$ is the total integrated scatter, $P_s$ is the diffused scattered light energy measurement, and $P_r$ is the reflected specular beam energy measurement.
N = rms roughness
θ = angle of incidence
λ = wavelength of incident radiation

TIS measurements for surface roughness have been shown to correlate closely with AFM measurements over wide range. The correlation on electroplated Cu films which was measured between this tool and AFM for surface roughness is shown in Figure 18. The wafers used for this correlation were 200 mm blanket wafers that were plated to at different thicknesses with a 1 Amp plating current (3.4 mA/cm² current density). It was found that the surface roughness under the plating conditions used increased significantly with thickness. It is of interest that the change in electroplated Cu surface roughness as a function of thickness was also found to be greater for films plated at 1 Amp plating current when compared to Cu films plated 15 Amp plating current (50 mA/cm² current density) when the films were subjected to an anneal.

Since surface roughness of the deposition surface is one of the parameters related to film texture, the surface roughness is of great process relevance. The deposition surface of the dielectric was demonstrated to play an important role on the crystallographic texture of PVD copper seed layers which in turn plays a role on the texture of the ECD copper. It has been shown that the additional Cu seed roughness that was added by self-annealing reduces the wettability relative to as-received seed. A major dependence of ECD surface roughness upon plating chemistry has been shown by TIS studies. Figure 19 clearly shows that the surface roughness for a 1 μm Cu electroplated films changes significantly by the use of different organic additives or different concentrations of the same additives which is the case for Viaform High Acid (HA) and Low Acid (LA) optimized plating chemistries. Historically, this indicates that the newer organic additive packages have reduced the surface roughness progressively. Figure 20 illustrates the dependence of surface roughness on individual plating organic additives and their combinations for a specific advanced plating chemistry.

In a full factorial experiment of two component chemistry (this study did not include a leveler). In this full factorial study, the suppressor was varied from 10 to 25 mL/liter, the accelerator over the range of 1 to 3 mL/liter, and the chloride concentration over the range of 25 to 75 ppm. The plating current was 25 mA/cm², and the plating thickness was 1 μm. It was shown that there was no effect upon the RMS surface roughness response by the suppressor but a linear dependence upon accelerator and chloride concentration. The chloride had the largest effect. There is a major effect of current density which is larger as the film increases in thickness for two component chemistry i.e. accelerator and suppressor, only. Figure 21 provides more quantitative information on the experiment.
Roughness was found to be a function of plating thickness and plating current density for both 2 and 3 organic additive chemistry. Roughness of plated copper films was also shown to be dependent upon the barrier metal, the PVD seed process, and plating waveform, and the rotational speed of the wafer as well as the electrolyte flow during plating. Figures 22 and 23 can be used to compare the Cu seed contour profile with a plated Cu film profile. Notice that the average RMS surface roughness for the Cu seeded wafer is 1.86 Å while that for 200 mm 10kÅ electroplated Cu film is 157.51 Å. The contour map shows considerable nonuniformity for the plated film. This can probably be attributed to nonuniformity in the current distribution during plating. The nonuniformity and process dependence upon electrolyte flow and wafer spin speed during plating is also evident from the diameter scans in Figure 24.

One of the early problems in copper damascene plating was clearly revealed by a swirl pattern in the surface roughness contour map illustrated in Figure 25. Trace impurity differences which were measured by SIMS were found in the swirl pattern areas that displayed differences in measured surface roughness. The swirl problem was related to surface wetting of the seed when hot entry was employed. It was observed in Figure 26 that the swirl does not occur when cold entry is employed. The problem was corrected by the efforts of the plater supplier by modification of the procedure for introduction of the wafer into the plating bath.

Optical Defect Measurement and Control

Monitoring copper plating defects such as crystals, particles, or pits in both patterned and blanket plated films is an essential part of process control. Two types of inspection tools are both of value for defect detection - one for pattern wafers and the other for blanket metal films. Full-wafer optical defect detection tools are usually the backbone of an in-line defect detection strategy. The most common defect tools which are used principally for blanket wafers do not classify the nature of the defects, so the defects detected are just referred to as light point defects. Examples of full wafer blanket wafer defect maps are shown in Figure 27. This figure highlights the value of such defects maps in process development and process monitoring. Defect measurement tools are used for almost every process in the fabrication line, so sharing of these tools among processes and integration activities is often necessary. Thus, caution must be exercised to insure that the instrument used for defect measurement is properly decontaminated after running copper containing wafers.

All optical inspection systems depend on photon scattering from the inspected surface area. Defect systems which rely upon electron scattering are also available. Bright-field systems, which are basically a high-speed microscope, collect both the scattered and reflected light through the same objective aperture to obtain an image. The automated microscope that captures bright-field images of patterned wafers looks for defects by comparing die images (die-to-die comparison).
Figure 20. Comparison of organic additive additions (suppressor, accelerator, and leveler) upon surface roughness of Cu plated films.\textsuperscript{66,70}

Darkfield systems, on the other hand, only collect the scattered light; no part of the reflected light falls within the collection angle. They can have a wide variety of configurations, depending on the angle and type of illumination, collection angles, and detector type. The detected scattered photons or electrons as a function of position contains the information required to determine whether a defect is present. An image processing system decides if there is a defect. Thus, defect detection is comprised of three main steps: first, obtaining the image, second, processing the image, and third, applying criteria to this processed image to detect defects. The inspection rate is an important operational parameter. Figure 28 illustrates common defects observed in plated films. Figure 29 illustrates a pitting defect in a copper line which is present even after the CMP process.

It usually is essential to run conditioning wafers if the plater has been idled for a period of time to reduce surface defects. During idle periods, the electrolyte circulation flow is reduced, while the flow is...
increased for plating operations. The number of wafers which need to be run in the conditioning step needs to be established, and then the efficiency of the conditioning step needs to be periodically checked. Frequent plater cell rinses may be required when using plating chemistry, such as low acid, high copper ion electrolyte, having a tendency for crystal formation which can contribute defects. Seed wetting can also be a defect related concern, and it is discussed later in this document. Some of the copper plating surface defects are not yield-killing defects, including those which are removed during CMP. In the case of damascene patterned wafers, many of the defects actually originate from process steps that are up-stream to the Cu plating step, such as the plasma etch/cleaning process. Such defects often do not show up

Figure 22. TIS RMS surface roughness contour map for PVD seed on 200 mm wafer.

Figure 23. TIS surface roughness contour map of 200 mm electroplated film which was 1 micron thick.
Figure 24. Radial surface roughness uniformity dependence upon flow rate and wafer spin speed for 200 mm electroplated films.67

under wafer inspection with a defect review tool until after copper plating which enhances the appearance of the defects. This explains why defect review, classification, and analysis are best considered from an integration perspective to aid in identifying and correcting yield problems.

**Defectivity: Swirl Defect Deposit Composition**

![Defectivity Chart](image)

**Film Stress and Wafer Curvature Measurements**

In general, the thermal mechanical integrity of semiconductor structures needs to be maintained and stabilized during fabrication. This becomes a key concern when new materials are being evaluated, which has been ongoing for metallization process development. Metallization film stress and wafer curvature are valuable parameters to monitor in metal processing. For example, stress metal induced voids in aluminum metallization at one stage of feature shrinkage caused tremendous reliability problems. The wafer curvature has been shown to impact metal and oxide CMP processes.73 Evidence has been advanced that the stress relaxation from compressive to tensile electroplated Cu which even occur at room temperature is the driving force for the recrystallization and associated grain growth and decreased in concentration of defects such as vacancies and dislocations. The stress induced relaxation process is reflected in a decrease in resistivity and an increase in film hardness.74

From an integration perspective, the overall thermal budget must be considered. The margins of the post plating annealing process must be carefully considered. This process impacts copper grain growth, as has been noted. Moreover, when low K dielectric films are employed, it has been found that too high annealing temperature can result in film delamination during the CMP process.75 Stress-temperature hysteresis measurements have been performed on blanket Cu plated films as a function of temperature in a controlled atmosphere in order to understand how best to stabilize the stress and minimize void formation during the annealing process. An example of a heating and cooling curve of an as-deposited Cu film is shown in Figure30. A FSM 900TC from Frontier Semiconductor, Inc.(Milpitas, CA), which is a

Figure 25. Surface roughness map manifestation of the swirl problem due to wetting issues during wafer introduction into the plating bath. SIMS impurity profiles reveal spatial nonuniformities in incorporated impurities.70

Entry line: initial current density
specialized tool for measuring the stress as a function of temperature in a controlled atmosphere, was used for these studies.\textsuperscript{76}

In the course of our work, a new optical technique for curvature and stress measurements which is based upon coherent gradient sensing was utilized.\textsuperscript{77–79} A schematics of the optics of this instrument is provided in Figure 31.\textsuperscript{80} The coherent gradient sensing interferometry has much better spatial resolution than the other options for wafer curvature and stress measurements. It was shown that the largest changes in wafer curvature during copper damascene processing occur as a consequence of the metallization processing steps, i.e., PVD, Cu plating, Cu anneal, and Cu CMP. This is clearly shown in Figure 32.\textsuperscript{80} The barrier film, even though very thin in comparison to the Cu plating thickness, causes convex shape changes due to tensile stress. Copper plating results in compressive stresses which cause the pattern wafer to assume a concave shape that increases upon annealing. The shape change is largely relieved by the subsequent CMP process.\textsuperscript{80} The wafer curvature continues to progressively increase as more levels of metallization are added. Refer to Figure 33.\textsuperscript{80} Thus, not only can copper plating and the annealing processes be nondestructively monitored but also pre- and post-processes in the damascene flow. Any deviations from the normal curvature changes for a product will serve as an alert. These findings support previous measurements made using capacitance probe methodology.\textsuperscript{84}

Contamination and Nonmetallic Film Impurity Measurement

Copper contamination monitoring is required for the plating process as well as for other tools which are involved with copper plated wafers. The cleaning process on the back side of the plated wafers as well as the edge bead etch must be monitored. TXRF is the metrology tool of choice for the back side. Total Reflection X-Ray Fluorescence (TXRF) is a fast and versatile surface analytical technique with multi elemental capability and low detection limits for medium-Z and high-Z elements ($1 \times 10^9$ to $1 \times 10^{10}$ atoms/cm$^2$). There is no need for sample preparation or a vacuum, and this technique has been used extensively to characterize semiconductor cleaning processes.\textsuperscript{82} Trace metallic contamination at the edge, bevel, and edge exclusion area was difficult historically since scattering effects of the incident radiation limits TXRF to an edge exclusion area of greater than 10 mm. However, a new procedure was developed which allow the analysis of the edge, bevel, and edge exclusion to be performed. This procedure involves chemical extraction of these areas with dilute hydrogen peroxide and hydrofluoric acid solution using a special mechanical jig (Universal Engineering, Lowell, MA) that allows rotation of the wafer, followed by inductively coupled plasma mass spectroscopy of the solution used for the extraction.\textsuperscript{83}

The incorporated impurities in the plated Cu film are most commonly measured by SIMS profiling which was illustrated earlier in Figure 25.\textsuperscript{70} These impurities generally originate from the plating additives, so C, S, Cl, N, and O are typically measured during profiling. The impurities can vary across the surface of the wafer, depending upon uniformity of the plating process.\textsuperscript{37} As the copper lines are shrunk below 50 nm, more concern is being paid to the role that nonmetallic incorporation plays in inhibiting grain growth in these narrow features which is necessary for the creation of “bamboo-like” grains that are essential for the attainment of low Cu resistivity and improved electromigration resistance.\textsuperscript{84}

Contact Angle Measurements

Wetting of the copper seed by the plating electrolyte can prove to be an insightful measurement. It has been shown that the defectivity of the electroplated film is related to the wetting characteristics of the Cu seeded wafer when immersed into the plating electrolyte. Wetting is partially dependent upon the structure of the seed layer such as roughness as well as composition of the plating electrolyte. The wetting even shows a dependence upon the concentration of additive decomposition products.\textsuperscript{69} Our results in Figure 34 confirm that the dependence of the Cu plated film contact angle of the plating solution upon usage which can be attributed to the buildup of decomposition products. Wetting of the seeded Cu wafer has a dependence on the seed layer surface oxidation, how the wafer is immersed in the bath (Figure 25\textsuperscript{70}), and how the plating is initiated (Figure 26\textsuperscript{70}).
The spontaneous growth of oxide on the copper seed surface of wafers prior to plating affects the wetting properties. Copper oxide growth is dependent upon multiple factors including time. The copper oxide thickness can be measured by cathodic chronopotentiometry at small areas on the surface. Figures 35 and 36 are examples of such a cathodic chronopotentiogram for 200 and 300 mm PVD Cu seeded wafers; the latter was immediately after the PVD process and the former after aging. In this technique, also known as Sequential Electrochemical Reduction Analysis, the metal oxides on the plated surface are reduced. Plateaus occur on the curve which are characteristic of the species being reduced. The duration of each reduction plateau can be related to the amount of reducible species present on the surface. The oxide thickness and type can be evaluated from the reduction charge using Equation 1. The stripping time shows that the 300 mm process has a much thinner copper oxide film than the 200 mm PVD seed. The oxide thickness at several sites on the 200 mm PVD seeded wafer is approximately 20 Å. A deaerated borate buffer solution (pH = 8.4) was used as the electrolyte for this measurement. It has been shown that the wetting can be improved by rinsing prior to plating.

Contact angle measurements permit liquid-solid interactions to be characterized. Contact angles can readily be measured optically at multiple points on the full wafer surface by static drop sessile contact measurements. The silhouette of the back-lighted drop is optically imaged and the angle subtended by the drop at the point of solid-liquid contact (on left and right sides) estimated by computerized image analysis. See Figure 37. Wettability (tensiometry) can be characterized by performing dynamic contact angle measurements using the same instrument. For these measurements, the advancing and receding...
contact angles are measured by capturing the liquid droplet on the wafer surface with the fine needle connected to the measurement syringe, and then the advancing contact angle or receding contact angle can be read by adding or withdrawing water from the drop, respectively. This is shown in Figure 38. Contact angles are measured from images captured by a CCD camera when observable motion had ceased. In Figure 39, the ascending contact angle remains constant as a function of drop volume, while the receding contact angle shows a linear increase with drop volume. The difference between the advancing and receding contact angle is called hysteresis. It is due to the interplay of the liquid motion with the surface and it is a measure of the liquid’s inability to simply flow over the surface. Hysteresis is in part due to surface roughness. It was shown by Thomas et al. that there is a good correlation between corrosion rates and the receding contact angles which are obtained on previously wetted surfaces.

In the Figures 40 and 41 the advancing contact angle over time is shown for the VMS LA electrolyte and VMS HA. These measurements differ from the preceding dynamic measurements. In this case, a 2.0 μL sessile drop was monitored optically over time as it spread on the Cu seed surface. The preceding measurements were conducted by means of a motorized syringe which dispenses or withdraws the test drop on the Cu surface, which was DI water in this case, and the

Figure 31. Optical schematic of the reflection-mode Oraxion Coherent Gradient Sensing (CGS) Interferometer used for full wafer curvature and stress measurements. The reflected beam undergoes diffraction, interference, and spatial filtering to obtain image containing interference fringes that can be related to curvature.

Figure 32. Stress Change for 300 nm full wafer damascene film stack measured at each step of the metal steps at the metal 2 level for different anneal conditions measured by coherent gradient sensing interferometry.

Figure 33. Interferometric total film stack stress for patterned 300 mm two level metallization sequence showing stress changes at each step and progressive increase with each metal level. Add straight line showing trend.

Figure 34. Sessile Contact Angle for Cu plating bath vs bath age.
Figure 35. Cathodic chronopotentiograms at $-30 \mu A/cm^2$ for surface oxide (principally cuprous oxide) measurement on 200 mm Cu PVD seed.\textsuperscript{58}

Figure 36. Cathodic chronopotentiograms at $-30 \mu A/cm^2$ for surface oxide (principally cuprous oxide) measurement on 300 mm Cu PVD seed.\textsuperscript{58}

Figure 37. Optical image of sessile drop on Cu surface, showing how left contact angle is measured.\textsuperscript{70}

Figure 38. Dynamic contact angle schematic with syringe needle withdrawing liquid from drop for receding angle measurements and adding liquid to drop for ascending angle measurements.

Figure 39. Dynamic Contact Angle Measurements of water on plated Cu film; red symbols receding angle measurements; blue symbols, ascending measurements.\textsuperscript{58}

image of the drop is captured as the drop advances or recedes across the surface. A comparison is also made in Figures 40 and 41 for both the LA and HA electrolytes containing the appropriate Enthone Vi-aForm additives. The contact angles are lower for both electrolytes containing the additives when compared to those without additives. The acid preclean which removes the surface copper oxides clearly reduced the contact angles and improved wettability. This indicates that the copper surface which is free of copper oxides is more hydrophilic

Figure 40. Ascending contact angle measurements for HA and LA electrolytes on Cu PVD surface with and without acid pre-clean process.\textsuperscript{37}
than the copper oxide coated surface. The suppressor is a wetting agent, so the comparative results between the VMS electrolytes and the corresponding VMS with additives is an expected finding. In addition, the HA electrolyte with additives contains four times more suppressor than the LA electrolyte with additives, so it is expected to wet the surface better.

Scanning Electron Microscopic Characterization

It was stated earlier that SEM analysis can be useful for thickness calibration. Seed coverage and Cu filling studies can also be characterized by SEM. Feature filling is best studied by cross-sectional SEM studies. Shown in Figures 42 and 43 are cross sections of plated features. Figure 42 shows partial and complete filling and has no voiding, while Figure 43 shows the effect of the accelerator, A, and suppressor, S, concentration upon voiding. In general, voiding may be related to the plating bath composition issues such as the additives being at the wrong concentration or it could be due to seed layer nonuniformities such as inadequate or no coverage at the bottom of the features, discontinuities, or corrosion by the plating bath. Another common application is defect review of in-film plating defects which was shown previously. The grain size can also be visualized by using cross sectional SEM micrographs of different size trenches after focused ion beam (FIB) sectioning as illustrated in Figure 44 which shows the effects of anneal.

The Cu film microstructure must receive attention, since the microstructure controls the stress and stress voiding, resistivity, and mechanical properties of the electroplated Cu which ultimately impact reliability. Characterization of the microstructure of the plated Cu film is, thus, vital during the process development phase to optimize all the process parameters. It is also important to monitor the microstructure regularly for process control. The microstructural parameters include copper grain size distribution, grain boundary character distribution, and crystallographic texture (preferred orientation of the grains). In addition to the plating process itself, changes in microstructure which occur as a function of linewidth and the evolution of this microstructure evolution upon annealing must be optimized. In fact, the microstructure of the Cu in the trenches may be different than the blanket films due to the geometrical confinement of the plated Cu which impact in the grain growth kinetics and the final grain structure.

When the SEM has automated BackScattering Diffraction (EBSD) capability, the following measurements can be performed: grain

Figure 41. Ascending contact angle measurements of LA and HA electrolytes containing Viaform Additives at optimal concentrations on Cu PVD seed surface with and without acid pre-clean.

Figure 42. Cross sectional analysis of partially and completely Cu filled trenches with no voiding.

Figure 43. Cross sections of Cu filled trenches showing comparisons of different accelerator (A) and suppressor concentrations (S) upon voiding.

Figure 44. SEM/ FIB cross sectional comparisons of Cu film plated at 3.4 mA/cm² and at 50 mA/cm² as-plated (top) and after anneal (bottom) at 150°C for 30 min. No leveler was utilized.
orientation mapping of polycrystalline Cu films both sputtered and plated before and after annealing, local texture, point-to-point orientation correlations, and phase identification and distributions. EBSD results for a blanket copper film are given in Figure 45 which shows a small area map of the film. The inverse pole figure, showing the Miller Indices for the crystal orientations, which is derived from the data is shown in Figure 45. Oxford Instruments website can be consulted on the inverse pole figures. The grain size derived from the measurements is shown in Figure 46. The grain size of plated copper in trenches has been measured with this technique and was shown to be a function of the plating chemistry. XRD also enables crystallographic texture and grain information to be measured. Due to the higher photon energy employed for the X-ray probing beam has a higher photon energy than the electron beam used in EBSD, the beam penetration into the metal film is deeper.
in XRD than in EBSD. A 4-circle goniometer is required for pole figure measurements rather than the traditional 2-circle X-ray powder diffractometer. With such an advanced instrument, it is possible to measure multiple pole figures on multiple layers of different materials, with such an advanced instrument, it is possible to perform these measurements.70

### Conclusions

An outline of the process and quality control issues faced in controlling copper damascene plating is provided in this paper. In addition, a brief outline of the initial and evolving challenges faced in Cu damascene processing has been provided. These demands have been addressed by adherence to quality control methodology, improvements in plater design and operation, advancements in plating electrolytes, and by new metrology tools and methodology. Due to their importance, an emphasis has been placed on bath concentration measurement and control, film properties metrology, contamination issues, and defects. Examples from the authors’ work are provided on performing some of the metrology measurements such as thickness measurements, bath concentration control, and microstructural characterization are mentioned.

The Cu damascene processing has remained as the mainstream interconnect process for the last two decades since it first was adopted for feature sizes ≤0.25 μm and after multiple reductions in feature size. Even though many process improvements have been made which are partly discussed in this paper, not all manufacturers find it necessary to use the most advanced processes and 300 mm wafers for their products. Instead some manufacturers still rely upon 200 mm processing. Going forward, limitations of plated Cu now be experienced at sub-10 nm feature size must be solved which is being attempted by other chemistries and concentrations of components, and the plater capabilities and proper operation. Ascertainment that the performance metrics which must be met before committing wafers for processing requires strict adherence to a comprehensive quality control program such as the one outlined here. Not all of the tests described here, however, can be done due to time constraints or do they need to be performed for each qualification of the plater, but some tests such as fill performance can be performed on a periodic basis if a problem is suspected. Streamlining and automation of the multiple quality and process control functions is highly desirable from a number of perspectives. Bath concentration control has reached the stage now where automation is possible and is being achieved in some fabs. Advancements in non-destructive techniques such as optical techniques make the metrology functions cheaper and more convenient to implement. The current gaps in metrology exist in nondestructive detection of voids in copper plated lines and in measuring the barrier/seed sidewall coverage.

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