High Performance Field-Effect Transistor Based on Multilayer Tungsten Disulfide

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ABSTRACT:

Semiconducting two-dimensional transition metal chalcogenide crystals have been regarded as the promising candidate for the future generation of transistor in modern electronics. However, how to fabricate those crystals into practical devices with acceptable performance still remains as a challenge. Employing tungsten disulfide multilayer thin crystals, we demonstrate that using gold as the only contact metal and choosing appropriate thickness of the crystal, high performance transistor with on/off ratio of $10^8$ and mobility up to $234 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature can be realized in a simple device structure. Further low temperature study revealed that the high performance of our device is caused by the minimized Schottky barrier at the contact and the existence of a shallow impurity level around 80meV right below the conduction band edge. From the analysis on temperature dependence of field-effect mobility, we conclude that strongly suppressed phonon scattering and relatively low charge impurity density are the key factors leading to the high mobility of our tungsten disulfide devices.

KEYWORDS: transition metal chalcogenide • two-dimensional • field-effect transistor • tungsten disulfide • WS$_2$

Semiconducting transition-metal dichalcogenide (TMD) MX$_2$ with the thickness of atomic level, where M represents transition metal (Mo, W) and X represents chalcogen (Se, S), has attracted a lot of attention recently due to the new emerging electrical and optical properties and its great potential in practical applications. Its atomically thin structure can be easily obtained via techniques such as the micromechanical cleavage$^{1,2}$ and liquid-phase exfoliation$^{3-5}$ because of the weak van der Waals bonding between neighboring chalcogen/metal/chalcogen layers. Not only bulk semiconducting TMD has the ideal size of band gap (1.1-2eV) for the making of transistor,$^6$ but also the band gap transforms from indirect to direct when the thickness of crystal approaches single atomic layer.$^7$-11 Consequently, significant enhancement of photoluminescence$^8,^9$ has been observed in monolayer MoS$_2$. $^7$ Ultrasensitive photodetectors$^{12}$ based on MoS$_2$ has also been demonstrated. Moreover, the intrinsically broken valley degeneracy in monolayers makes TMD the perfect model system for studying “valleytronics”.$^{13-15}$ Besides the exciting optical properties, the semiconducting TMDs show excellent electrical switching properties and, therefore, is expected to hold promise in modern nano-electronics applications. The electron mobility based on single atomic layer MoS$_2$ field-effect transistors (FET) ranges from $\sim1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ to $\sim200\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. $^{16}$ MoS$_2$ FET with $10^8$ on/off ratio has been achieved by using high-\(\kappa\) oxide
as the top gate dielectric grown by using atomic layer deposition (ALD). However, the challenges of obtaining monolayer, complicated device fabrication process and chemically modified interface make it difficult to study the intrinsic properties. Besides MoS$_2$, researchers are also interested in other members of this semiconducting TMD group such as WSe$_2$ and MoSe$_2$, which exhibit good switching behavior as well. Compared with MoS$_2$, WSe$_2$ and MoSe$_2$, tungsten disulfide (WS$_2$) has a larger band gap in both bulk crystal (~1.3eV) and monolayer (~2.1eV). Although WS$_2$ is expected to have the best transistor performance (the highest on-state current density and mobility) among all semiconducting TMDs according to earlier theoretical calculation, only a few FET studies on WS$_2$ atomic crystal have been reported with the reached on/off ratio of $10^5$ and electron mobility of $20\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and yet, a device with performance comparable to that of MoS$_2$ has not been realized. In this paper, we report our studies on multilayer WS$_2$ field-effect transistor with simple back-gate device structure. Our devices exhibit exceptionally high on/off ratio reaching $10^8$ and mobility up to $234\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. We have further performed low temperature measurements and revealed that minimized Schottky barrier at the contacts and appropriate impurity level plays critical roles in our WS$_2$ device.

RESULTS AND DISCUSSIONS

The example of as fabricated device is shown in Figure 1a and b. In this report, devices with various WS$_2$ crystal thicknesses ranging from 3nm to 100nm were studied. To characterize the electrical properties of the device, we use conventional three-terminal configuration setup with heavily doped silicon as the back-gate electrode, as illustrated by the schematic drawing in Figure 1c. Based on our test on more than one hundred devices, we find that WS$_2$ crystals with thickness around 6-10nm exhibit the best switching behavior (see supporting information for more details). Similar thickness dependence in MoS$_2$ has also been reported by Li et.al. A typical measurement of source-drain current $I_{ds}$ vs. back gate voltage $V_{bg}$ at room temperature is shown in Figure 2a. The device appears to be $n$-type FET with the neutrality point of -45V. As shown in the log scale plot of $I_{ds}$ vs. $V_{bg}$, the device can be tuned into an off-state with the minimum current $I_{ds}$ less than $10^{-14}$ A when $V_{bg}$ is set in the range of -30V to -50V. Also, the device have a weak ambipolar FET behavior with the sign of p-type carriers appearing at negative gate voltage ($V_{bg}$<-50V). The current $I_{ds}$ at on-state can reach 20µA at $V_{bg}$ ~ 60V with source-drain bias $V_{ds}$=1V. The on/off ratio at room temperature for this device reaches $10^8$, which is extremely high compared with the earlier results from other semiconducting members of the MX$_2$. This is a surprising result given that we only use the device structure of back gating with 300nm SiO$_2$ as the dielectric layer. According to the gate sweep, we can extract the gate voltage induced carrier density $n_{2D}$ using the parallel-plate capacitor model $n_{2D} = C_{ox}(V_{bg} - V_{bg,th})/\epsilon$, where $C_{ox}$ is the dielectric capacitance per unit area and $V_{bg,th}$ is the threshold voltage and $\epsilon$ is the unit charge. $C_{ox}$ can be further calculated from $C_{ox} = \epsilon_0\epsilon_r/d_{ox}$, where $\epsilon_0$ is the dielectric constant of vacuum, and $\epsilon_r$ represents the relative dielectric constant of 3.9 for SiO$_2$. The carrier density is estimated to be $2.6 \times 10^{12}$ cm$^{-2}$ when $V_{bg}$=60V and $V_{ds}$=1V. Figure 2b shows the trace and retrace sweeps of $I_{ds}$ vs. $V_{bg}$ with $V_{ds}$ fixed at 0.1V. The maximum voltage difference between trace and retrace sweeps is less than 1V indicating a small hysteresis in our device. This observation is in contrast to the relatively large hysteresis reported in other multilayer transition metal chalcogenides devices. Multiple factors, such as water or oxygen molecules absorbed on the surface or charge injection at the oxide dielectric interface, should be considered as the possible causes. Figure 2c shows the $I_{ds}$ vs. $V_{ds}$ characteristics at room temperature for different $V_{bg}$. At low source-drain bias from -0.1V to 0.1V, the $I_{ds}$ vs. $V_{ds}$ presents near-linear and symmetric behavior indicating good contacts formed between gold contact metal and WS$_2$ crystal. However, when source-drain bias is swept up to 5V, as shown in Figure 2d, the $I_{ds}$
starts to display an upturn at $V_{ds}=1V$, and no signs of current saturation appears even when $V_{ds}$ is increased to 5V. To extract the room temperature field-effect mobility $\mu$ of our device, we utilize the field-effect transistor model $\mu = \left[ \frac{dl_{ds}}{dV_{bg}} \right] \times \left[ L/(WC_{ox}V_{ds}) \right]$, where $L$ and $W$ are the channel length and width respectively. At room temperature, the extracted mobility of this particular devices corresponding to Figure 2 reaches $234cm^{2}V^{-1}s^{-1}$ at $V_{bg}-V_{th}=25V$ (here $V_{th}$ is the threshold voltage), which is significantly higher than the mobility (typical value of 10 to $180cm^{2}V^{-1}s^{-1}$) of MoS$_2$ devices with SiO$_2$ as the gate dielectrics.\textsuperscript{2,16,17,26,31}

In order to reveal the origin of the high performance of our device, we have conducted low temperature transport measurement and studied the detailed transport mechanism on multiple devices. A device with channel dimensions of 8nm in thickness, 6um in length and 3um in width is selected for the following discussion. As shown in Figure 3a, the $I_{ds}$-$V_{ds}$ sweeps are recorded with back gate voltage fixed at $V_{bg}=60V$ at different temperatures. It is apparent that the nonlinearity of $I_{ds}$-$V_{ds}$ is enhanced when the device has been cooled from 300K to 5K. In particular, unlike the relatively linear behavior of $I_{ds}$-$V_{ds}$ sweep at room temperature, the low temperature $I_{ds}$-$V_{ds}$ sweeps ($T=200K$ to 5K) exhibit a distinct new feature: the device shows a relatively insulating state in the low source-drain bias regime ($-0.6V<V_{ds}<0.6V$) and a conducting state at large bias regime ($V_{ds}>0.6V$ or $V_{ds}<-0.6V$). The crossover source-drain voltage between the two regimes is around 0.6V. Above the crossover, $I_{ds}$ increases rapidly with $V_{ds}$ as can be seen more clearly in the insert of Figure 3a. We conjecture that the different temperature dependence behavior at small and large source-drain bias regimes may be caused by the existence of Schottky barrier, a typical situation for contacts between metal and semiconducting TMDs,\textsuperscript{32} yet rarely explored in WS$_2$ device. Therefore, to highlight the possible Schottky barrier effect, we focus on the temperature dependence of source drain current at large $V_{bg}$ (60V to 35V) with small $V_{ds}$ (0.02V), as shown in Figure 3b. With large $V_{bg}$, the WS$_2$ crystal is tuned into the conducting on-state as illustrated by the band diagram of Figure 4a. Thus, the total conductance of the device will be limited only by the Schottky contacts. In Figure 3b, the $I_{ds}$ shows a near-exponential temperature dependence from room temperature to 90K, indicating a thermally activated charge transport mechanism. To accurately extract the Schottky barrier height of our device, we used the two dimensional (2D) thermionic emission transport equation $I_{ds} = A^{*}wT^{3}\exp\left(\frac{-q\phi_{B}}{k_{B}T}\right)\left\{ \exp\left(\frac{qV_{ds}}{k_{B}T}\right) - 1 \right\}$ to fit our data, where $A^{*}$ is the 2D Richardson constant, $w$ is the physical width of FET, $q$ is the unit charge, $\phi_{B}$ is the effective Schottky barrier height and $k_{B}$ is the Boltzmann constant.\textsuperscript{33} By using the flat band voltage condition of $V_{bg}=V_{FB}$,\textsuperscript{32} the actual Schottky barrier height $\phi_{SB}$ can be extracted to be 27.2meV for this particular device as shown in the insert in Figure 3b (see more extraction examples in Supporting Information). This barrier height is comparable to the thermal energy ($k_{B}T\sim26meV$) at room temperature. Therefore, the electrons at the Fermi level can be easily excited thermally to overcome Schottky barrier formed in our WS$_2$ device, which explains the near-linear $I_{ds}$-$V_{ds}$ curve at room temperature.

Intrinsic WS$_2$ crystal has an indirect band gap of 1.35eV,\textsuperscript{11,35} which in general leads to a poor gatability using thick dielectric layer of 300nm SiO$_2$. However, the high on-off ratio in our multilayer WS$_2$ crystal indicates the opposite. This unusual behavior may suggest that our multilayer WS$_2$ crystal is fundamentally different to intrinsic WS$_2$. For conventional semiconductor, doping is the most common method to enhance the gatability of device\textsuperscript{36,37} by modulating the Fermi level within the band gap. Hence, we suspect our multilayer WS$_2$ crystal may also contains impurity. In order to set this impurity effect
apart from the Schottky barrier effect, we measured the temperature dependence of conductance at a large source drain bias \( V_{ds} = 2V \) with back gate voltage varied from -15V to 0V as shown in Figure 3c. The purpose of applying large source drain voltage up to 2V is to supply enough forward bias to lower the height of Schottky barrier at the drain side (illustrated by the band diagram in Figure 4b). Consequently, this favors the electron’s transport toward drain electrode and minimizes the contact resistance caused by Schottky barrier. However, it is noteworthy that, because the WS\(_2\) crystal is also tuned into the off-state by setting gate in the range of -15V to 0V, the charge carriers, i.e. electrons in this case, are mostly created through thermal excitations and we assume this is the major effective mechanism led to the conductance of our device in this configuration. Of course, if both gate voltage and source drain voltage are set to the configuration that WS\(_2\) crystal is in on-state and Schottky barriers are minimized at the contacts, the device will be turned into a highly conductive state. This situation can be easily seen in the band diagram of Figure 4c. Now, we focus on the configuration that enables us to study the thermal activation behavior, i.e. large source drain bias and \( V_g = -15V \) to 0V. Figure 3c shows the temperature dependence of conductance, which indeed changes exponentially from 300K to 100K. We can fit the conductance data \( G \) with the thermal activation equation of \( G = G_0 e^{-E_a/kbT} \) that describes the temperature dependence of conductance for thermally activated charge carriers. Here \( G_0 \) is the conductance limit at high temperature and \( E_a \) is the thermal activation energy. As shown in the insert of Figure 3c, the extracted thermal activation energy \( E_a \) ranges from 80meV to 35meV, which is consistent with the value also been reported in MoS\(_2\).\(^{16}\) The obtained activation energy implies that the energy level generated by impurities is near the bottom of conduction band for our multilayer WS\(_2\) crystal. Yet, the origin of impurity level is still under investigation and is one of the focuses in future work.

To further understand how the transport of charge carriers affected by the impurities or other possible scattering sources, we studied the temperature dependence of field effect mobility \( \mu \). Figure 5a shows the on-state mobility at \( V_g = V_{th} = 25V \) plotted as a function of temperature at different source-drain bias \( (V_{ds} = 0.1V \sim 2V) \). At small source-drain bias below 0.6V, mobility is underestimated due to the apparent Schottky barrier. At large source-drain bias \( (V_{ds} \rightarrow 2V) \), contact resistance becomes negligible, which leads to more accurate extraction of mobility. On cooling from room temperature, the mobility follows a power law \( (\mu \sim T^\gamma) \), and then remains at a saturated value below 100 K. The extracted power law constant \( \gamma \) converges towards 1.15 at \( V_{ds} = 2V \) as shown in the insert of Figure 5a.

Now we focus on the detailed charge scattering mechanism of our device, which plays critical role in the FET performance of our devices. Similar to other TMD systems like MoS\(_2\),\(^{38}\) it is reasonable to consider that charge carriers in multilayer WS\(_2\) crystal are usually scattered by acoustic phonon, optical phonon and charged impurities. For optical phonon scattering,\(^{16,39}\) the temperature dependence can be described with the equation \( \mu_{op} = \frac{4\pi\varepsilon_0\varepsilon_r\hbar^2}{\varepsilon_\omega \omega_{\omega}^{\omega} Z_0} \left[ \frac{\hbar\omega}{e\varepsilon_\omega \omega_{\omega}^{\omega}} - 1 \right] \), where \( \frac{1}{\varepsilon_p} = \frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_S} \) with \( \varepsilon_\infty \) and \( \varepsilon_S \) are the high frequency and static dielectric constant respectively. \( m^* \) is the effective mass of electron, \( \hbar\omega \) is the optical phonon energy and \( Z_0 \) is the crystal thickness. For acoustic phonon scattering, under the deformation potential approximation, the mobility limited by acoustic phonons can be described by \( \mu_{ac} = \frac{e\hbar^2\rho v}{(m^*)^2\Xi_2 k_b T} \), where \( \rho \) is the crystal density, \( \Xi_2 \) is the deformation potential and \( v \) is the acoustic phonon velocity.\(^{38,40}\) We shall include the background charge impurity scattering, which contributes to the mobility in the form\(^{41}\)
\[
\mu_{\text{imp}} = \frac{8\pi\hbar^2 e^2 k_F^2 \int_0^{\pi} \frac{\sin^2 \theta}{(\sin \theta + \beta)^2} d\theta}{\varepsilon m^* N_{\text{imp}}}. \]

Here \( \beta = \frac{S_0}{2k_F} \) and \( k_F \) is the wavevector on the Fermi surface, \( N_{\text{imp}} \) is the impurity density and \( S_0 \) is the screening constant which takes the form of \( S_0 = \frac{e^2 m^*}{2\pi\hbar^2} \). Then the total mobility of a device was calculated using Mathiessen’s rule \( \mu^{-1} = \mu_{\text{op}}^{-1} + \mu_{\text{ac}}^{-1} + \mu_{\text{imp}}^{-1} \) by combine contributions from all three scattering sources. Using this model, we can fit the measured mobility (circles in Figure 5b) by changing variables of optical phonon energy \( \hbar \omega \), deformation potential \( \Xi_\Delta \) and charge impurity density \( N_{\text{imp}} \) (other parameters were directly adopted from literatures of bulk WS\(_2\)). Figure 5b shows the fitted result (black curve), which agrees well with the data from our measurement. We extracted the optical phonon energy about \( \omega \sim 240 \text{ cm}^{-1} \), which is close to the theoretical value\(^{33} \) of 300 cm\(^{-1}\). The extracted deformation potential \( \Xi_\Delta \) is around 2.0 eV which is also close to the value of MoS\(_2\).\(^{38} \) The extracted charged impurity density of our WS\(_2\) crystal is around 2 \( \times 10^9 \) cm\(^{-2}\), which is relatively small compared with other 2D crystals (MoS\(_2\) with \( 1.8 \times 10^{10} \text{ cm}^{-2} \) and grapheme with \( \sim 10^{11} \text{ cm}^{-2} \)).\(^{38} \) From the fitted plot we conclude: 1. Charge impurity dominates the mobility at low temperature below 100K. 2. The acoustic phonon contribution to the mobility (blue curve) is marginal at all temperatures. 3. Optical phonon limits the mobility at temperatures above 100K. In particular, from 300K to 100K a power law temperature dependence of \( \mu \sim T^{-\gamma} \) can be fitted with \( \gamma \) approaching 1.15 at \( V_{\text{ds}} = 2 \text{ V} \) as mentioned earlier. Comparing to the results from previously reported MoS\(_2\) devices,\(^{16} \) where \( \gamma = 1.4 \) for back-gated device and 0.55 for dual-gated (both top-gate and back-gate are used) device, \( \gamma = 1.15 \) from our WS\(_2\) device indicates that optical phonon mode quenching may occur. It has been shown by earlier studies that top gate using high-\( k \) dielectrics\(^{2, 17, 46-48} \) is the reason to cause the suppression of optical phonons and screening of charged impurities and to improve the device mobility on MoS\(_2\). However, in our WS\(_2\) device the mobility is surprisingly high (up to 234 cm\(^2\)V\(^{-1}\)s\(^{-1}\)) without such top gate/-\( k \) dielectric structure. This may imply that simple structure like a few layer WS\(_2\) crystals on SiO\(_2\) surface can also have optical phonon suppressed by other reasons. The overall charge scattering behavior of our WS\(_2\) device appears similarly to that of two dimensional electron gas (2DEG) system containing low density and high mobility of electrons, such as AlGaN/GaN field-effect transistor.\(^{49} \)

**CONCLUSIONS**

In conclusion, we have successfully fabricated back gated field-effect transistors based on multilayer WS\(_2\) crystals with thermal SiO\(_2\) as the dielectric layer and pure gold as the contact metal. These devices exhibit on/off ratios up to \( 10^5 \) and mobilities reaching 234 cm\(^2\)V\(^{-1}\)s\(^{-1}\) at room temperature. We found that the device performance strongly depends on the thickness of WS\(_2\) channel crystal and the best performance appears in the thickness between 6 to 10nm. By studying low temperature transport behavior, we have identified that the high performance of our device is a combined result of low contact Schottky barrier and shallow impurity level inside WS\(_2\) crystal. We also revealed that the scattering of charge carriers is mainly caused by optical phonons and charge impurities. Our work demonstrates that, comparing to other semiconducting TMDs, multilayer WS\(_2\) crystal is indeed an excellent channel material for the making of high performance FET required for both energy saving and high power electronics applications.

**METHODS**

The high quality WS\(_2\) bulk single crystals were synthesized using chemical vapor transport\(^{50} \) with iodine acting as transport agent. The standard micromechanical exfoliation technique\(^2 \) was adopted to obtain
WS₂ thin flakes on the substrate of silicon with 300nm thermal oxide. The flakes with desired thicknesses were screened by using an optical microscope via color contrast. Then 35nm gold metal contacts connecting the WS₂ flakes were patterned and deposited by using standard electron beam lithography and thermal evaporation. Then, the devices were annealed in forming gas at 200°C for 2 hours in order to remove organic residues introduced during the fabrication process. The accurate thickness of WS₂ flakes were further determined by using Atomic Force Microscope (AFM).

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Supporting Information Available: Mobility histogram; Schottky barrier height extraction. This material is available free of charge via the Internet at http://pubs.acs.org.
Figure 1. Device fabrication of WS$_2$ FET. (a) Optical image of a multilayer WS$_2$ device with gold as the contact metal and Si/SiO$_2$ as the substrate. (b) Atomic force microscope image of the device shown in (a). The insert shows the line trace of 7.5 nm thick WS$_2$ crystal obtained at the location of white line. (c) Schematic drawing of the measurement setup for electrical transport characterization.
Figure 2. Electrical property characterization of WS$_2$ device (shown in Figure 1) at room temperature. The lateral dimension is 4.8um in length and 1.8um in width. (a) $I_{ds}$-$V_{bg}$ sweeps under different source drain voltages $V_{ds}$=0.04V, 0.1V, 0.4V, 1V plotted in log scale (left vertical axis) and linear scale (right vertical axis). Note: for this particular device, the maximum $I_{ds}$ on/off ratio reaches $10^8$ at $V_{ds}$=1V and the mobility extracted reaches $234 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature. (b) Trace and retrace $I_{ds}$-$V_{bg}$ sweep at $V_{ds}$=0.1V showing small hysteresis at room temperature. (c) $I_{ds}$-$V_{ds}$ sweeps in small source-drain bias regime (-0.1 to 0.1V) at room temperature, showing near-linear behavior. (d) $I_{ds}$-$V_{ds}$ sweeps in large source-drain bias regime (0 to 5V), exhibiting clear nonlinearity.
Figure 3. Low temperature characterization. (a) $I_{ds}$-$V_{ds}$ sweeps in the range of $V_{ds} = \pm 1\,\text{V}$ at on-state ($V_{bg}=60\,\text{V}$) under different temperatures from 300K to 5K. Insert: zoomed out $I_{ds}$-$V_{ds}$ sweeps in the range of $V_{ds} = \pm 6\,\text{V}$. (b) Source drain current $I_{ds}$ (in log scale) vs. temperature $T$ (in reciprocal scale) for the same device in (a) with $V_{ds}=0.02\,\text{V}$ and $V_{bg}=45\,\text{V}$~60V. Insert: the extracted effective Schottky barrier height $\phi_B$ and the arrow indicates the actual Schottky barrier height $\phi_{sb}$. (c) Conductance $G$ (in log scale) vs. temperature $T$ (in reciprocal scale) for the same device in (a) with $V_{ds}=2\,\text{V}$ and $V_{bg}=-15$~5V. Insert: the extracted thermal activation energy $E_a$. 
Figure 4. (a) Band diagram of a WS$_2$ device operating at low temperature and low source-drain bias, when the WS$_2$ crystal is set to on-state with appropriate gate voltage. This diagram illustrates that at low temperature, Schottky barrier becomes the major factor to limit the source-drain current. (b) Band diagram of a WS$_2$ device operating at low temperature and large source-drain bias, when the WS$_2$ crystal is set to off-state with appropriate gate voltage. This diagram illustrates that at low temperature thermal excitation between impurity band and conduction band are the main mechanism generating charge carriers. (c) Band diagram of a WS$_2$ device operating at room temperature with large source-drain bias, while the WS$_2$ is set to on-state with appropriate gate voltage. (Note: all the band diagrams are only for the purpose of illustrations and not drawn to scale.)
Figure 5. (a) Temperature dependence of field-effect mobility for a WS$_2$ device at different source-drain bias (0.1V to 2V) with fixed effective gate voltage ($V_{bg}-V_{th}=25$V). Insert: the power law constant $\gamma$ vs. source-drain bias (extracted from (a)). Dimension of the device: thickness 7.5nm, channel length 6µm and channel width 3µm. (b) Temperature dependence of measured electron mobility (hollow circular dots) at $V_{ds}=2$V and the fitted electron mobility (black line). The fitted data includes the scattering contribution from acoustic phonons (blue line), optical phonons (red line) and charge impurities (magenta line).
REFERENCES AND NOTES

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A., Electric Field Effect in Atomically Thin Carbon Films. *Science* 2004, 306, 666-669.
2. Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K., Two-Dimensional Atomic Crystals. *Proceedings of the National Academy of Sciences of the United States of America* 2005, 102, 10451-10453.
3. Coleman, J. N.; Lotya, M.; O’Neill, A.; Bergin, S. D.; King, P. J.; Khan, U.; Young, K.; Gaucher, A.; De, S.; Smith, R. J., et al., Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* 2011, 331, 568-571.
4. Lee, K.; Kim, H.-Y.; Lotya, M.; Coleman, J. N.; Kim, G.-T.; Duesberg, G. S., Electrical Characteristics of Molybdenum Disulfide Flakes Produced by Liquid Exfoliation. *Advanced Materials* 2011, 23, 4178-4182.
5. Smith, R. J.; King, P. J.; Lotya, M.; Wirtz, C.; Khan, U.; De, S.; O’Neill, A.; Duesberg, G. S.; Grunlan, J. C.; Moriarty, G., et al., Large-Scale Exfoliation of Inorganic Layered Compounds in Aqueous Surfactant Solutions. *Advanced Materials* 2011, 23, 3944.
6. Wilson, J. A.; Yoffe, A. D., The Transition Metal Dichalcogenides Discussion and Interpretation of the Observed Optical, Electrical and Structural Properties. *Advances in Physics* 1969, 18, 193-335.
7. Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F., Atomically Thin MoS2: A New Direct-Gap Semiconductor. *Phys Rev Lett* 2010, 105, 136805.
8. Splendiani, A.; Sun, L.; Zhang, Y. B.; Li, T. S.; Kim, J.; Chim, C. Y.; Galli, G.; Wang, F., Emerging Photoluminescence in Monolayer MoS2. *Nano Lett* 2010, 10, 1271-1275.
9. Eda, G.; Yamaguchi, H.; Voiry, D.; Fujita, T.; Chen, M. W.; Chhowalla, M., Photoluminescence from Chemically Exfoliated MoS2. *Nano Lett* 2011, 11, 5111-5116.
10. Lebègue, S.; Eriksson, O., Electronic Structure of Two-Dimensional Crystals from ab Initio Theory. *Physical Review B* 2009, 79, 115409.
11. Kuc, A.; Zibouche, N.; Heine, T., Influence of Quantum Confinement on the Electronic Structure of the Transition Metal Sulfide TS2. *Physical Review B* 2011, 83, 245213.
12. Lopez-Sanchez, O.; Lembke, D.; Kayci, M.; Radenovic, A.; Kis, A., Ultrasensitive Photodetectors Based on Monolayer MoS2. *Nature Nanotechnology* 2013, 8, 497-501.
13. Mak, K. F.; He, K. L.; Shan, J.; Heinz, T. F., Control of Valley Polarization in Monolayer MoS2 by Optical Helicity. *Nature Nanotechnology* 2012, 7, 494-498.
14. Zeng, H. L.; Dai, J. F.; Yao, W.; Xiao, D.; Cui, X. D., Valley Polarization in MoS2 Monolayers by Optical Pumping. *Nature Nanotechnology* 2012, 7, 490-493.
15. Wu, S.; Ross, J. S.; Liu, G.-B.; Aivazian, G.; Jones, A.; Fei, Z.; Zhu, W.; Xiao, D.; Yao, W.; Cobden, D., et al., Electrical Tuning of Valley Magnetic Moment Through Symmetry Control in Bilayer MoS2. *Nature Physics* 2013, 9, 149-153.
16. Radisavljevic, B.; Kis, A., Mobility Engineering and a Metal-Insulator Transition in Monolayer MoS2. *Nat Mater* 2013, 12, 815-820.
17. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A., Single-Layer MoS2 Transistors. *Nature Nanotechnology* 2011, 6, 147-150.
18. Li, H.-M.; Lee, D.-Y.; Choi, M. S.; Qu, D.; Liu, X.; Ra, C.-H.; Yoo, W. J., Metal-Semiconductor Barrier Modulation for High Photoresponse in Transition Metal Dichalcogenide Field Effect Transistors. *Scientific Reports* 2014, 4, 404.
19. Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A., High-Performance Single Layered WSe2 p-FETs with Chemically Doped Contacts. *Nano Lett* 2012, 12, 3788-3792.
20. Liu, W.; Kang, J.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K., Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe2 Field Effect Transistors. *Nano Lett* 2013, 13, 1983-1990.

21. Larentis, S.; Fallahazad, B.; Tutuc, E., Field-Effect Transistors and Intrinsic Mobility in Ultra-Thin MoSe2 Layers. *Appl Phys Lett* 2012, 101, 223104.

22. Chamglagain, B.; Li, Q.; Ghimire, N. J.; Chuang, H.-J.; Perera, M. M.; Tu, H.; Xu, Y.; Pan, M.; Xia, D.; Yan, J., et al., Mobility Improvement and Temperature Dependence in MoSe2 Field-Effect Transistors on Parylene-C Substrate. *ACS Nano* 2014, 8, 5079.

23. Liu, L. T.; Kumar, S. B.; Ouyang, Y.; Guo, J., Performance Limits of Monolayer Transition Metal Dichalcogenide Transistors. *IEEE Trans Electron Dev* 2011, 58, 3042-3047.

24. Hwang, W. S.; Remskar, M.; Yan, R. S.; Protasenko, V.; Tahy, K.; Chae, S. D.; Zhao, P.; Konar, A.; Xing, H. L.; Seabaugh, A., et al., Transistors with Chemically Synthesized Layered Semiconductor WS2 Exhibiting 10^5 Room Temperature Modulation and Ambipolar Behavior. *Appl Phys Lett* 2012, 101, 013107.

25. Braga, D.; Lezama, I. G.; Berger, H.; Morpurgo, A. F., Quantitative Determination of the Band Gap of WS2 with Ambipolar Ionic Liquid-Gated Transistors. *Nano Lett* 2012, 12, 5218-5223.

26. Li, S.-L.; Wakabayashi, K.; Xu, Y.; Nakahara, S.; Komatsu, K.; Li, W.-W.; Lin, Y.-F.; Aparecido-Ferreira, A.; Tsukagoshi, K., Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors. *Nano Lett* 2013, 13, 3546-3552.

27. Late, D. J.; Liu, B.; Matte, H. S. S. R.; Dravid, V. P.; Rao, C. N. R., Hysteresis in Single-Layer MoS2 Field Effect Transistors. *ACS Nano* 2012, 6, 5635-5641.

28. Li, T.; Du, G.; Zhang, B.; Zeng, Z., Scaling behavior of hysteresis in multilayer MoS2 field effect transistors. *Appl Phys Lett* 2014, 105, 093107.

29. Qiu, H.; Pan, L.; Yao, Z.; Li, J.; Shi, Y.; Wang, X., Electrical Characterization of Back-Gated Bi-Layer MoS2 Field-Effect Transistors and the Effect of Ambient on Their Performances. *Appl Phys Lett* 2012, 100, 123104.

30. Cho, A.-J.; Yang, S.; Park, K.; Namgung, S. D.; Kim, H.; Kwon, J.-Y., Multi-Layer MoS2 FET with Small Hysteresis by Using Atomic Layer Deposition Al2O3 as Gate Insulator. *ECS Solid State Letters* 2014, 3, Q67-Q69.

31. Jariwala, D.; Sangwan, V. K.; Late, D. J.; Johns, J. E.; Dravid, V. P.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C., Band-Like Transport in High Mobility Unencapsulated Single-Layer MoS2 Transistors. *Appl Phys Lett* 2013, 102, 173107.

32. Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J., High Performance Multilayer MoS2 Transistors with Scandium Contacts. *Nano Lett* 2013, 13, 100-105.

33. Calvet, L. E. Electrical Transport in Schottky Barrier MOSFETs. Thesis, Yale University, 2001.

34. Appenzeller, J.; Radosavljević, M.; Knoch, J.; Avouris, P., Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors. *Phys Rev Lett* 2004, 92, 048301.

35. Kam, K. K.; Parkinson, B. A., Detailed Photocurrent Spectroscopy of the Semiconducting Group VIB Transition Metal Dichalcogenides. *The Journal of Physical Chemistry* 1982, 86, 463-467.

36. Le Comber, P. G.; Spear, W. E., Electronic Transport in Amorphous Silicon Films. *Phys Rev Lett* 1970, 25, 509-511.

37. Sze, S. M., *Semiconductor Devices: Pioneering Papers*. World Scientific Publishing Company, Incorporated: 1991.

38. Kim, S.; Konar, A.; Hwang, W.-S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.-B.; Choi, J.-Y., et al., High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS2 Crystals. *Nature Communications* 2012, 3, 1011.

39. Gelmont, B. L.; Shur, M.; Stroscio, M., Polar Optical-Phonon Scattering in 3-Dimensional and 2-Dimensional Electron Gases. *J Appl Phys* 1995, 77, 657-660.
40. Lisesivdin, S. B.; Acar, S.; Kasap, M.; Ozcelik, S.; Gokden, S.; Ozbay, E., Scattering Analysis of 2DEG Carrier Extracted by QMSA in Undoped Al0.25Ga0.75N/GaN Heterostructures. *Semicond Sci Tech* 2007, 22, 543-548.

41. Hess, K., Impurity and Phonon-Scattering in Layered Structures. *Appl Phys Lett* 1979, 35, 484-486.

42. Lee, K.; Shur, M. S.; Drummond, T. J.; Morkoc, H., Low Field Mobility of 2-D Electron-Gas in Modulation Doped AlxGa1-Xas/Gaas Layers. *J Appl Phys* 1983, 54, 6432-6438.

43. Molina-Sanchez, A.; Wirtz, L., Phonons in Single-Layer and Few-layer MoS2 and WS2. *Physical Review B* 2011, 84, 155413.

44. Shi, H.; Pan, H.; Zhang, Y.-W.; Yakobson, B. I., Quasiparticle Band Structures and Optical Properties of Strained Monolayer MoS2 and WS2. *Physical Review B* 2013, 87, 155304.

45. Burson, K. M.; Cullen, W. G.; Adam, S.; Dean, C. R.; Watanabe, K.; Taniguchi, T.; Kim, P.; Fuhrer, M. S., Direct Imaging of Charged Impurity Density in Common Graphene Substrates. *Nano Lett* 2013, 13, 3576-3580.

46. Kaasbjerg, K.; Thygesen, K. S.; Jacobsen, K. W., Phonon-Limited Mobility in n-type Single-Layer MoS2 From First Principles. *Physical Review B* 2012, 85, 115317.

47. Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S., Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat Nanotechnol* 2012, 7, 699-712.

48. Ayari, A.; Cobas, E.; Ogundadegbe, O.; Fuhrer, M. S., Realization and Electrical Characterization of Ultrathin Crystals of Layered Transition-Metal Dichalcogenides. *J Appl Phys* 2007, 101, 014507.

49. Henriksen, E. A.; Syed, S.; Ahmadian, Y.; Manfra, M. J.; Baldwin, K. W.; Sergent, A. M.; Molnar, R. J.; Stormer, H. L., Acoustic Phonon Scattering in a Low Density, High Mobility AlGaN / GaN Field-Effect Transistor. *Appl Phys Lett* 2005, 86, 252108.

50. Lieth, R. M. A., *Preparation and Crystal Growth of Materials with Layered Structures*. Springer: 1977.