Research on Weak Current Detection System Based on Embedded System

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Abstract. In today's society, the rapid development of science and technology requires the detection of weak current signals in many fields of scientific research. The research of its detection technology plays a very important role in promoting the development of science and technology. Considering that the weak current signal has strong background noise, it is easy to be submerged, the detection is difficult, and the professional requirement is strong. This research proposes a weak current detection system based on an embedded system that can detect nanoampere-level weak currents. The detection system is mainly composed of signal conversion amplifier filter circuit module, signal acquisition circuit, STM32, FPGA, upper computer and so on. Through experimental inspection, the researched detection system has the advantages of high accuracy and good stability.

1. Introduction
The measurement of weak current signals is a technique that uses modern electronic information technology to obtain useful signals from noise. This technique is usually used in aerospace, medical, biology, physics and other fields. With the rapid development of science and technology, high-precision measurement of weak current signals is becoming more and more important. In scientific research, many small temperature differences, small displacements, etc., which are difficult or impossible to detect directly, are usually collected by sensors, and the signals are converted into current signals and then measured, and the current signals output by the sensors are usually at Naan level or even smaller, and the signal is very weak. When detecting a weak current signal, the signal is extremely susceptible to interference from factors such as environment and noise, and it is difficult to measure. Therefore, it is very necessary to study a high-precision weak current detection system[1-6].

Current signal detection usually uses a multimeter. Ordinary multimeters are cheap but do not have the weak current detection function, and usually do not have the corresponding detection range. There are special weak current detection meters on the market, but the price is very expensive and the accuracy is not high enough. This paper aims at some problems existing in weak current signal detection. This design studies a high-precision weak current detection system based on STM32+FPGA, which has the advantages of simple circuit structure, high precision, low cost, easy maintenance, development, and expansion, and can measure nA current.

2. The overall structure of the system
The main function of the weak current signal detection system is to convert, process and effectively display the collected weak current signal. The main guiding ideology of the high-precision weak current detection system design based on STM32+FPGA is high integration, high precision and low cost.
According to the requirements of the detection system, the overall structure of the measurement system is shown in Figure 1. The system is mainly composed of I/V conversion module, signal amplification module, noise removal filter module, A/D conversion acquisition module, control circuit module, and host computer.

The main working process of the system is: the weak current signal is first transformed into the corresponding voltage signal by the I/V conversion circuit, and then the voltage signal is standardized by the program-controlled amplifier circuit, and then the filter circuit eliminates the useless background noise to obtain the useful signal, and the useful signal passes through The A/D conversion module collects and obtains the corresponding digital signal, and then uses the MCU processor to process the signal and then transmits it to the computer via the bus for analysis, processing, calculation and display. This article focuses on the design of several core module circuits in the detection system.

3. Schematic design of the core module

3.1. Current/voltage conversion

The main function of the current/voltage conversion circuit is to convert the input micro-current signal that needs to be detected into a corresponding voltage signal. Detecting micro-current signals usually can use capacitance integration method, sampling resistance method, and op amp construction method. After comprehensive consideration, the detection system of this design uses the op amp construction method, as shown in Figure 2. This circuit design has the characteristics of simple structure, small output impedance, and large input impedance, which is suitable for the detection of weak current signals. Assuming that the op-amp is in an ideal state, the input bias current is 0, according to the "virtual break and virtual short" characteristics of the op-amp in the ideal state, it can be obtained that the relationship between the output voltage of the operational amplifier and the measured input microcurrent and the feedback resistance is satisfied \( V_o = I_i \times R_f \). Here, \( V_i \) and \( V_o \) are linearly proportional. The actual operational amplifier has a bias current, which is not ideal. The shunt of the bias current will reduce \( I_i \) and affect the measurement of \( I_i \). The relationship between the actual output voltage \( V_o \) and the input current \( I_i \) satisfies \( V_o = -I_i \times R_f + (V_{os} - V_o/A_j) + I_b \times R_f \). Among them, \( V_{os} \) is the offset voltage of the op amp, \( A_j \) is the open-loop magnification, and \( I_b \) is the input bias current. Error of circuit output voltage \( \Delta V_o = V_{os} + I_b \times R_f - V_o/A_j \). Therefore, if the current signal to be measured is more accurate, \( I_b \) needs to
be much smaller than $I_i$, and $A_d$ needs to be large enough. Therefore, when choosing the type of amplifier, you should choose low noise, low drift, high input impedance, low input offset voltage and current, and low input bias current to reduce the influence of bias current on actual weak current signal measurement. Based on the above considerations, the op amp of this design is TCL277CP, which has the advantages of low offset voltage (less than or equal to 0.5mV) and low input bias current (less than or equal to 0.6pA). At the same time, in order to reduce the influence of the thermal noise caused by the feedback large resistance $R_f$ on the measurement accuracy, the T-type resistor network will be improved, so that the voltage amplification that meets the requirements can be obtained, and the resistance value is reduced, thereby reducing the thermal noise.

![Figure 2. Current/Voltage Conversion Circuit Scheme](image)

3.2. Signal conditioning and data acquisition circuit
The signal conditioning circuit is mainly composed of a program-controlled amplifier circuit and an active low-pass filter circuit. The voltage signal obtained by the weak current signal after the current/voltage conversion output is still small, so it needs to be amplified. The main function of the program-controlled amplifier circuit is to appropriately amplify the input weak signal to facilitate signal measurement, and the amplified gain can be changed by programming. The whole circuit is mainly composed of amplifier module and peripheral variable resistance feedback network module. The variable resistance feedback network module is mainly composed of some peripheral filter circuits. The amplifier chip selects TI product PGA2XX, which has the characteristics of high precision and programmable. The useful signal output by the program-controlled amplifier circuit may be mixed with high-frequency noise, which will affect the measurement accuracy of the detection system. Therefore, a filter circuit is required to eliminate the noise. Considering the requirements of the filter circuit of this system, the Butterworth filter is adopted.

3.3. A/D conversion
The main function of the A/D data conversion circuit is to convert the analog voltage signal output by the conditioning circuit into a digital signal for processing and analysis by a computer. Commonly used A/D conversion mainly includes double integral, V/F conversion, and successive approximation. According to the performance requirements of the detection system of this design, the SNR (signal-to-noise ratio) of the A/D conversion is at least 98.09dB. There are many types of A/D conversion chips that meet the above requirements. This design uses the Σ-Δ type A/D converter that has emerged in recent years. This type of sampler has the advantages of high sampling rate and high resolution. Considering comprehensively, choose the AD7768-4 chip, which is a 24-bit ADC of ADI, with a signal-to-noise ratio of up to 111dB, which meets the requirements of the detection system of this design. In actual detection, the sampling clock will affect the accuracy of the detection. Therefore, the provision
of a stable sampling clock is very important. In this design, STM32 outputs a clock signal, which is
processed by FPGA as an external clock (MCLK) for A/D conversion.

3.4. Control circuit
The normal and orderly data acquisition of A/D conversion requires the control circuit to provide a clock
for control, and the program-controlled amplifying circuit can appropriately amplify the signal as
required and also needs the control circuit to control it. Generally, there are many solutions for designing
control circuits, some are controlled by a single MCU or controlled by multiple MCUs. As shown in
Figure 3, this design adopts the STM32+FPGA control scheme, in which the main controller is
STM32F103ZE. By writing a control program, a variety of internal resources are reasonably called to
realize the control of the program-controlled amplification and other functional sub-modules. FPGA is
used as an auxiliary controller to share and control the A/D conversion data collection work, which
effectively reduces the burden of STM32, improves the real-time performance of data processing, and
makes programming logic simpler.

Figure 3. Block diagram of control circuit

4. Software scheme design
The software design of this design mainly includes two parts: the upper computer program design and
the lower computer program design. The host computer uses the Visual Studio 2019 Community Edition
development environment for development, which is flexible, efficient and easy to use. The lower
computer is mainly STM32 and FPGA. The STM32 uses STM32F103ZE. This chip has the advantages
of fast processing speed and low power consumption. The operating frequency fOSC can reach up to 72
MHz, the CPU is 32 bits, and the core is based on ARM CortexTM- M3 has considerable internal
resources. What FPGA chooses is the Spartan series chip of Xilinx Company, the available resources
inside this series chip are very abundant. The functions that the program designed by the lower computer
need to realize are mainly to control A/D conversion data acquisition and reading and processing, gear
switching and calibration, and system self-check; the functions that the program designed by the upper
computer need to realize are mainly data display and Processing, data saving and other functions.

5. System test results
In order to test whether the measurement of the micro current detection system is accurate, the United
States Keithley 6220 DC precision current source is used to provide a micro current signal to conduct
an experimental test on the detection system. There are 3 gears for measurement. Each gear has 5 sets
of data, and each set is tested at an interval of 3 minutes. The test data results are shown in Table 1. The
relative errors of the 5 sets of data under the 3-speed test are 9.333%, 5.467%, 4.434%, 3.913%, and
3.597% respectively. When the measured current value is between 10-10A and 10-9A, the relative error
is less than 10%; When the measured current value is between 10-9A and 10-8A, the relative error is
less than 5%, and the performance indicators meet the design requirements.
Table 1. Formatting sections, subsections and subsubsections.

| Input Current (n A) | 0.100 | 0.500 | 1.000 | 5.000 | 10.000 |
|---------------------|-------|-------|-------|-------|--------|
| Measured current level 1 (n A) | 0.109 | 0.529 | 1.052 | 5.240 | 10.351 |
| Measured current 2 gears (n A) | 0.111 | 0.522 | 1.038 | 5.112 | 10.327 |
| Measured current 3 gears (n A) | 0.092 | 0.531 | 1.043 | 5.235 | 10.401 |
| Average relative error (%) | 9.333 | 5.467 | 4.434 | 3.913 | 3.597 |

6. Conclusions

Weak current detection is very susceptible to the detection system itself and the environment. The STM32+FPGA-based detection system proposed in this study has experimental results that meet the performance requirements of the design, with better stability and higher accuracy. The detection system originally designed has a certain universality and has certain application reference value for the measurement of other weak signals.

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