An on-chip antenna integrated with a transceiver in 0.18-µm CMOS technology

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Abstract: This paper presents an on-chip antenna integrated with a Ku-band transceiver using a standard 0.18-µm CMOS process. An off-chip guard ring is used to improve the gain of the antenna. As the guard ring is implemented on the test carrier board, this gain improvement technology does not require additional process, and it is easy to implement. It is shown that, a gain improvement of 5.8 dBi can be obtained by using the guard ring with the radiation efficiency improved from 18% to 32%. Additionally, the influence of the CMOS process metal rules and the existence of the transceiver on the antenna performance are studied in this paper. The proposed antenna is fabricated with and without the transceiver, respectively. It is shown that the single-chip antenna (without transceiver) has a gain of 2.4 dBi at 17 GHz, with a 3-dB bandwidth from 14.2 GHz to 21.5 GHz. Meanwhile, the transceiver (with integrated antenna) has a 3-dB bandwidth from 15.8 GHz to 18.0 GHz, with a peak gain of 13.5 dB in the transmitter link and a peak gain of 15.3 dB in the receiver link.

Keywords: on-chip antenna, CMOS process, guard ring

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

On-chip antenna has received great attention in the last decade for its attractive advantages. For example, it can remove the lossy interconnection between the RF front-end IC and the off-chip antenna. Furthermore, with the on-chip antenna, single-chip transceiver is available for many applications, such as wireless communications and phased array systems. To the best of our knowledge, most of the on-chip antenna is implemented using the silicon process from the point of view of cost reduction [1, 2, 3, 4, 5]. However, the silicon-based on-chip antenna suffers from low radiation gain and low efficiency due to the high permittivity and low resistivity substrate used in the process. As a result, most of the energy is consumed rather than radiated by the antenna in the form of surface-wave and heat [6]. This is the bottleneck for the design of an on-chip antenna.

Up to now, so many methods have been proposed to solve this problem, such as the micro-machining technology [7], the dielectric-lens-based concept [6] and the dielectric-resonance-based technology [8]. These techniques, however, need additional processes for the antenna fabrications. This, accordingly, extends the complexity of the implementation of the on-chip antenna.

In this work, a single-chip Ku-band (15.8–18 GHz) transceiver integrated with an on-chip antenna is presented using the standard 0.18-µm CMOS process. To improve the gain of the on-chip antenna, an off-chip guard ring and an off-chip reflector are introduced. The ring and the reflector are implemented on a printed
circuit board (PCB), which is also used as the carrier board of the transceiver for test. Obviously, this gain improvement technology does not require additional process, and is easy to realize. Moreover, to satisfy the strict metal design rules of the CMOS technology, a large number of holes are etched in the antenna and plenty of metal dummy blocks are placed under this antenna. The influence of these holes and dummy blocks on the performance of the antenna has been investigated in this paper. In addition, this paper studies the coupling between the antenna and the on-chip inductor to reveal the unwanted coupling level between the antenna and the transceiver circuit. The single-chip antenna and the whole transceiver (with antenna) are on-wafer measured, respectively. It shows that, the single on-chip antenna has a gain of 2.4 dBi at 17 GHz. Meanwhile, the peak gain of the transmitter link and the receiver link of the transceiver is 13.5 dB (at 17.5 GHz) and 15.3 dB (at 17.0 GHz), respectively.

2 Transceiver architecture

Fig. 1 illustrates the block diagram of the proposed Ku-band transceiver fabricated in 0.18-µm CMOS process. To achieve a simple layout and low power consumption, the all-RF architecture is utilized to implement this transceiver [9]. As is seen that, the transmit link consists a power amplifier, a 4-bit attenuator and a 5-bit phase shifter, while the receiver link consists three stages of low noise amplifier, two stages of phase shifters and an attenuator. The transceiver operates in time division duplex (TDD) model and two switches are used to achieve the channel selection. Additionally, an on-chip antenna is integrated with these two channels. As a result, the proposed transceiver has much more integration density and less transmission loss when compared with the traditional one.

3 On-chip antenna design

In this work, a folded monopole antenna is adopted, for it is suitable for this bar-type layout of the transceiver. The die photograph and the 3-D simulation model of the antenna are presented in Fig. 2. As is shown that, this antenna is implemented on the top metal layer of the chip, and a microstrip line is used to feed this antenna. A ground-signal-ground (GSG) pad with the pitch of 100 µm is added at the antenna input port for the single antenna test in the later section. To improve the antenna gain, an off-chip reflector is adopted, as is presented in our previous literature [5]. This reflector is implemented using the bottom metal of a print circuit board (PCB) and this PCB is also used as the test carrier board for the antenna. The optimized thickness of the PCB is around 2.5 mm, which is about \(1/4 \lambda_g\) (\(\lambda_g\) is the
guided wavelength in the PCB substrate). In addition, a guard ring is designed to suppress the surface wave that propagating along the surface of PCB. With this ring, the antenna gain has an obviously enhancement of 5.8 dB according to the following simulations. The final dimensions of the antenna are shown in Fig. 2(c). With the test pad, the proposed on-chip antenna occupies a die area of only $1.3 \times 2.5 \, \text{mm}^2$.

### 3.1 Guard ring design

As mentioned above, the on-chip antenna is mounted on a thick PCB reflector to improve the gain of the antenna. However, the antenna on the electrically thick substrate can suffer strongly from the loss of the surface wave modes [10]. Therefore, in this work, a guard ring is introduced to suppress the surface wave and improve the antenna gain. The guard ring consists of a metal ring on the top layer of PCB and a shorting wall with grounded vias as shown in Fig. 3. The thickness of the dielectric layer is designed to 2.5 mm (around $1/4 \lambda_g$), which leads the equivalent surface impedance of the guard ring $Z_{\text{ring}} \to \infty$. In order to explain this in detail, the propagation constant $k_z$ of the propagation wave in the dielectric layer is also presented in Fig. 3. Then it will get
Where \( k \) is the propagation constant in the free space, \( k = \frac{2\pi}{\lambda}, \quad k = \sqrt{\varepsilon_r} \cdot k \), while \( k_x \) and \( k_y \) are the components of the \( k_c \) in the horizontal and vertical directions, respectively. Note that the component \( k_y \) will transform the metal ring to an equivalent surface impedance \( Z_{\text{ring}} \) at the dielectric surface as

\[
Z_{\text{ring}} = j \tan(k_yd)Z_0\sqrt{(\varepsilon_r - 1)/\varepsilon_r}
\]

where \( Z_0 \) is wave impedance in the free space and \( d \) is the thickness of the dielectric layer \([11]\). It is easily seen that when

\[
k_yd = \pi/2, \quad i.e. \quad d = \lambda/(4\sqrt{\varepsilon_r - 1})
\]

the \( Z_{\text{ring}} = \infty \). As a result, with this guard ring the surface wave can be suppressed and the antenna gain can be improved.

Then, with the fixed thickness of PCB, the size of the guard ring is optimized. Fig. 4 shows the comparisons of the simulated reflection coefficient and the gain pattern (at 17 GHz) with different ring size (\( l \times l \) mm\(^2\)). It is seen that the \(-10\) dB bandwidth of the antenna is slightly affected by the ring size. But the ring size has a significant influence on the antenna gain. Increasing the ring size in a certain range can increase the gain of the antenna and a peak gain of 2.8 dBi is observed when the \( l = 10 \) mm. However, further increasing the ring size (\( l = 12 \) mm for example) will result in an increase in the side lobe level of the antenna. The width of the ring has little influence on the antenna performance. Therefore it is not shown in this paper. The reflection coefficient, the radiation efficiency and the gain pattern of the antenna without the guard ring are also presented in Fig. 4 for comparison. It is
shown that with the proposed guard ring, the resonant frequency of the antenna is shifted down by around 1.9 GHz. Meanwhile, applying this guard ring the antenna gain has a maximum improvement of 5.8 dB and the antenna efficiency has an improvement from 18% to 32%. Fig. 4(c) shows the electric field distributions on the surface of the PCB for the on-chip antenna with and without the guard ring. It is obviously seen that the electric field is indeed contained inside the guard ring, and the surface wave is significantly deduced. As a result, the gain and the directivity of the antenna can be improved.

3.2 Investigate of the CMOS process metal rules influence on the antenna performance

![Fig. 5. (a) Reflection coefficient of antenna with and without dummy blocks and holes. (b) 3-D pattern of antenna without dummy blocks and holes (at 17 GHz). (c) 3-D pattern of antenna with dummy blocks and holes (at 17 GHz).](image)

To satisfy the metal rules of the 0.18-µm CMOS process, a large number of dummy blocks are buried under the antenna and plenty of holes are etched in the antenna as Fig. 2(c) presented. The size of the blocks and the holes are 25 µm x 25 µm and 5 µm x 5 µm, respectively. Fig. 5 illustrates the comparisons of the S11 and the 3-D pattern of the antenna with and without the dummy blocks and holes (l is fixed to 10 mm). It is shown that with the buried dummy fills and etched holes, the resonant frequency of the antenna is shifted down by around 300 MHz, which is 1.5% with respect to the center frequency. Additionally, according to the 3-D pattern, the peak gain is reduced by 0.12 dBi with these metal blocks and holes. However, these deviations are too small, and we choose to ignore these minor deviations to improve the efficiency of the simulation. Therefore, the influence of the process metal rules is not taken into account in the optimal design of the antenna in this work.

3.3 Investigate of the transceiver influence on the antenna performance

For the antenna is integrated with the transceiver in a single chip, the influence of the substrate under the transceiver and the crosstalk between the antenna and the transceiver circuit are studied in this section. Additionally, as the on-chip inductor has the largest size in the transceiver circuit, by investigating the crosstalk between the antenna and the inductor can reveal the coupling level between the on-chip
antenna and the transceiver circuit [12]. The simulation model beside with the simulated results is shown in Fig. 6. It is seen that the additional substrate and inductor have few influences on the antenna resonant frequency. But a notable change in the E-plane pattern with a 0.9 dB decrease of the antenna gain can be observed. This is due to the increase of the lossy substrate area. Meanwhile, it is shown that the existence of the simplified transceiver reduces the cross-polarization level of the antenna by 3.9 dB in the H-plane. Furthermore, according to Fig. 6(b), the simulated crosstalk level is less than $\approx 63$ dB in the operating bandwidth, which shows a good performance in the unwanted coupling.

4 Measurement results

The proposed antenna is fabricated and tested with and without the transceiver respectively. The measured setup is shown in Fig. 7(a), which contains a vector network analyzer (VNA), a spectrum analyzer, a DC power, a GSG probe, and a standard horn antenna, as reported in our previous work [5]. For the first step, the single-chip antenna without the transceiver is mounted on a PCB and measured. The comparison between the measured and simulated antenna input reflection coefficient and gain pattern (at 17 GHz) are presented in Fig. 7(b) and Fig. 7(c). It is seen that the proposed antenna has a 3-dB bandwidth of 7.3 GHz, from 14.2 GHz to 21.5 GHz and a measured peak gain of 2.4 dBi is obtained at $\theta = 20^\circ$ @ 17 GHz. A good agreement between the simulated and the measured results can be observed. The shift of the resonance frequency and the deviation of the pattern may due to the process deviation, the existence of the metal probe and the influence of the dummy fills. Additionally, the cross-polarization levels are less than $-15$ dB in both of the E- and H-plane.
For the second step, the transceiver integrated with the on-chip antenna is tested. As Fig. 7(d) presented, the peak gain of the receiver link (with antenna) is 15.3 dB at 17.0 GHz, with a 3-dB bandwidth from 15.7 GHz to 18.1 GHz. Meanwhile, the transmitter link (with antenna) has a peak gain of 13.5 dB at 17.5 GHz, with a 3-dB bandwidth from 15.8 GHz to 18.0 GHz. In addition, the effect of the transceiver on the antenna pattern has been validated. Fig. 7(e) shows the normalized pattern of the antenna integrated with transceiver at 17 GHz. The peak gain is obtained at $\theta = 0^\circ$ and the cross-polarization levels are less than $-15$ dB in E-plane and less than $-12$ dB in H-plane, which are agree with the predicted results presented in Fig. 6(c).

### 5 Conclusion

A Ku-band on-chip antenna is fabricated with and without an integrated transceiver in this work respectively. An off-chip guard ring is proposed to raise the antenna gain by 5.8 dB and the radiation efficiency is improved from 18% to 32%. Moreover, in the design of antenna, dummy fills and metal slots are introduced.
to satisfy the metal design rules of the CMOS technology. It shows that these fills and slots have a little influence on the antenna performance (1.5% shift of frequency and 0.12 dB decrease of gain). The proposed antenna has a size of 1.3 × 2.5 mm² with a gain of 2.4 dBi at 17 GHz.

Acknowledgments

This work is supported by National Natural Science Foundation of China (Grant No. 61331006, 61422104), National Science and Technology Major Project of the Ministry of Science and Technology of China (Grand No. 2016ZX03001015-004) and Fundamental Research Funds for the Central Universities (Grant No. ZYGX2015J016).