A Non-Closed-Form Mathematical Model for Uniform and Non-Uniform Distributed Amplifiers

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Abstract—A non-closed-form general mathematical model for CMOS distributed amplifier (DA) for broadband applications is presented. Contrary to the artificial transmission line (TL) assumption made in the conventional analytical models, the proposed model treats the DA as a discrete set of cells connected together, and hence considers propagation and mismatch between inter-cells. This approach provides designers with a much more accurate first sizing of the DA compared to conventional ways and, as a result, leads to a reduced design time and complexity. The model enables both quantitative and qualitative analysis of a DA, for the purpose of aiding the designers in predicting the relations between DA performance and its multi-design parameters, especially in the context of non-uniform designs. In addition, it is well suited to Computer-Automated Design (CAutoD), to help in achieving designs having a given set of performance goals. The validation of the model is demonstrated on two designs, by a comparison with ADS simulation charts were provided in [5] through a fine description of the equivalent model of the distributed amplifier stage, including TL tapering. However, this approach does not accurately represent inter-cells mismatches which give rise to gain ripple, since they are founded on the basis of artificial TL assumption besides neglecting the propagation effect of inter-TL segments. Furthermore, the design approach in [5] highly relies on experience and on intensive simulation-based tuning.

In this context, a theoretical analysis of a DA structure is presented in this paper, considering a fine modeling of uniformly, or non-uniformly, distributed Gm-cells, in addition with their inter-cells mismatches. Also, a non-closed-form mathematical model is proposed to describe the DA behavior. This model, combined with a numerical software, enables the proper examination of each building element and its effects on the overall response in order to support designers. For that reason, emphasis was made on keeping the model (as well as its representation) as simple as possible. Also, the number of active Gm-cells, \( N \), will be considered as a variable, and not an input parameter contrarily to what is proposed in [7], to give more flexibility in the design.

In Section II, the background principle of a DA is presented, and a detailed explanation of the derived mathematical tools is reported. In Section III, the proposed model is subjected to a validation test with ADS simulation using CMOS part of BiCMOS 55-nm DK technology, while in Section IV we discuss the attained results.

II. DISTRIBUTED AMPLIFIER ANALYSIS

As shown in Fig. 1, a DA consists of several transconductances embedded between two TLs. The combination of one active element (Gm-cell) and a pair of TL segments on both its ends is commonly referred to as a unit-cell. Since every Gm-cell is loading both physical input and output TLs by their own specific input and output complex
impedances, respectively, each nth cell is considered attached
to a defined periodic structure of loaded TLs. RF signal feeds
the DA input line, denoted with subscript ‘g’ for gate line, and
reaches the DA output line, denoted with subscript ‘d’ for
drain line, as an amplified version established by the number
of unit cells used (N).

When it comes to the uniform DA designs, as proposed in
[7], identical output-side TL segments of similar characteristics
\((Z_{d,y,d})\) and same lengths \(l_d/2\) are used. The
same applies for the input-side TLs. In the model presented
in this paper, each unit-cell can differ from its neighbors in terms
of Gm-cell, and in terms of left and right TL segments. The
CMOS Gm-cell model is detailed hereafter in section A while
the output (drain) and input (gate) sides analysis are presented
in sections B and C, before their correlation is considered in
D.

A. Gm-Cell Model

In this paper, a MOSFET based cascode topology is used
in the Gm-cell, as represented in Fig. 2(a), which helps to
reduce the Miller effect and to improve reverse-isolation. This
Gm-cell is modeled by a simplified equivalent circuit depicted
in Fig. 2(b), where the device will be considered unilateral as
a first approach, i.e. \(C_{gd}\) will be neglected.

\[ I_{twn} = -I_{Dn} f_{Rn} + I_{outn-1} f_{Sn} T_{dLn} \]  

(1)

where \(f_{Rn}\) represents how much current generated by the nth
current source, \(I_{Dn}\), is incident on the right TL, and is
calculated from (2);

\[ f_{Sn} = \frac{R_{dsn}}{(1 + jw R_{dsn} C_{dsn})Z_{inRn} + (Z_{inLn} + Z_{inRn})R_{dsn}} \]  

(2)

and \(f_{Sn}\) represents the splitting current factor between the
right part of the nth Gm-cell, just before the right TL
\((Z_{dRn}, Y_{dRn})\), and the dissipated part in the transistor drain
impedance. \(f_{Sn}\) is given by (3).

\[ f_{Sn} = \frac{R_{dsn}}{(1 + jw R_{dsn} C_{dsn})Z_{inRn} + R_{dsn}} \]  

(3)

Finally, \(T_{dLn}\), is the nth left drain TL \((Z_{dLn}, Y_{dLn})\)
transmission coefficient which takes into account the multiple
reflections that occur at its boundaries. \(T_{dLn}\) can be calculated
using (4) on the basis of Fig. 3:

\[ T_{dLn} = \frac{(1 + jI_{indLn})(1 + jI_{outdLn})e^{-Z_{dLn}l_d}}{1 + I_{indLn} I_{outdLn} e^{-Z_{dLn}l_d}} \]  

(4a)

\[ I_{indLn} = \frac{Z_{Ln} - Z_{dLn}}{Z_{Ln} + Z_{dLn}}, \quad I_{outdLn} = \frac{Z_{dLn} - Z_{Rn}}{Z_{dLn} + Z_{Rn}} \]  

(4b)

\(Z_{Ln}\) is the TL input impedance seen at the left side of the
left TL loaded by \(Z_{inRn}\) in parallel with \((R_{dsn}, C_{dsn})\). \(Z_{Rn}\) is
the TL input impedance seen at the right side of the left TL
loaded by \(Z_{eqLn}\). Previous impedances are plotted on Fig. 3.

In order to determine the amount of current that a given
nth unit-cell transmits to subsequent cells, represented as an
equivalent load impedance, \(Z_{eqLn}\), in Fig. 3, the transmission
coefficient of the right-side TL is introduced to the input
current expressed in (1), and hence the total output current
comes to:

\[ I_{outn} = T_{dLn} I_{twn} \]  

\[ = -I_{Dn} f_{Rn} T_{dLn} + I_{outn-1} f_{Sn} T_{dLn} T_{dRn} \]  

(5)
where the transmission coefficient $T_{d,n}$ stands for the nth right drain TL and is calculated using (6):

$$
T_{d,n} = \frac{(1 + l_{ind}^R_n)(1 + l_{outd}^R_n)e^{-v_{ds,n}^d}}{1 + l_{ind}^R_n l_{outd}^R_n e^{-v_{ds,n}^d}}
$$

where $l_{ind}^R_n = \frac{Z_{c_{gs,n}} - Z_{s,n}}{Z_{s,n} + Z_{g,n}}$, and $l_{outd}^R_n = \frac{Z_{d,n} - Z_{g,n}}{Z_{s,n} + Z_{g,n}}$.

$Z_{s,n}$ is the TL input impedance seen at the left side of the right TL loaded by $Z_{equ}^g$, and $Z_{g,n}$ is the TL input impedance seen at the right side of the right TL loaded by $Z_{ind}^g$ in parallel with $(R_{d,n}, C_{d,n})$. Previous impedances are represented on Fig. 3.

2) N-Distributed Unit-cells Study: Fig. 4 illustrates the case where $N$ unit-cells, shown in Fig. 3, are distributed.

![Drain loaded line representation.](image)

By developing (5), the total output current generated from the drain line of a DA is expressed in (7):

$$
I_{out}^d = \sum_{n=1}^{N} -I_{in}^d \left[ \prod_{i=1}^{n} (T_{di} l_{fi})^{k_{di}} \left( f_{ni} T_{di} T_{ri} \right)^{1-s_{di,0}} \right]
$$

where $\delta_{i,n}$ represents the “Kronecker” Delta.

C. Gate Line Analysis

For the gate line analysis, a similar approach to that of the drain line analysis was applied. Based on Fig. 2(a), the gate side of the Gm-cell is depicted as an equivalent impedance of series resistor and capacitor, denoted $R_g$ and $C_{gs}$, respectively. By referring to the definition of a DA, the gate line is thus described as a transmission line periodically loaded by $N$ equivalent $R_g$ in series with $C_{gs}$ impedances.

![Gate loaded line representation.](image)

Based on this configuration, the approach was focused on determining the voltage $V_{c,n}$ at each gate-source capacitor $C_{gs,n}$ for the nth unit-cell when a given voltage source $V_c$ is applied and it resulted in the capacitor voltage expression (8):

$$
V_{c,n} = \frac{Z_{in} \left( \frac{1}{Z_{in} + R_g} \right) \prod_{i=1}^{n} T_{gi}^{-1-s_{gi,0}}}{C_{gs,n} j \omega R_g C_{gs,n}}
$$

where $Z_{in}$ is the input impedance of the whole DA and $R_g$ is the internal resistance of the signal source. $T_{gi,n}(T_{gi,n})$ is the nth transmission coefficient of the left (right) side gate TL which is determined by using the same equations as (4a) ((6a) respectively). The only difference lies in the expression of the boundary reflection coefficients.

$$
\Gamma_{in,gi,n} = \frac{Z_{in} - Z_{g,n}}{Z_{in} + Z_{g,n}}; \Gamma_{out,gi,n} = \frac{Z_{g,n} - Z_{in,n}}{Z_{g,n} + Z_{in,n}}
$$

D. Relationship Between DA Gate and Drain Lines

The parameter linking the drain line, modeled by (7), and the gate line, modeled by (8), is the transconductance, $g_m$, of the Gm-cell which relates its output current, $I_{out}^g$, to its input voltage, $V_{c,n}$, as given below.

$$
I_{out}^g = g_m V_{c,n}
$$

E. Summary

Throughout Section II, the quantitative analysis of a non-uniform DA was presented and resulted in two non-closed form mathematical models (7) and (8) for both the drain and gate lines, respectively, linked with a key equation (10). Those equations, when implemented in a numerical software, can give to the DA designer a better comprehension of the relation between the parameters listed in Table I below and the DA behavior.

| Parameters | Definition |
|------------|------------|
| $R_g$      | Series gate resistance |
| $C_{gs}$   | Gate-to-source capacitance |
| $R_{d,n}$  | Drain-to-source resistance |
| $C_{d,n}$  | Drain-to-source capacitance |
| $g_m$      | Transconductance |
| $Z_{d,n}$  | Drain and gate, right or left, TL characteristic impedance |
| $Y_{d,n}$  | Drain and gate, right or left, TL propagation constant |
| $l_{d,n}$  | Drain and gate, right or left, TL physical length |

III. Validation Examples

A. Non-Uniform Distributed Amplifier

In order to examine the degree of accuracy of the proposed mathematical model, initially a non-uniform tapered DA was considered and implemented in Matlab© software. The same DA was designed in Keysight’s ADS software, used as a reference for comparison. For each Gm-cell configuration depicted in Fig. 2(a), the common-gate transistor, M2, is chosen with a channel width double to that of the common-source transistor, M1, to balance input and output capacitances of the cascode cell. Intrinsic elements extraction of Table I, for both NMOS and TLs, is performed on the basis of simulation conducted with the design kit of the B55 technology from STMicroelectronics. We adopted a 4 unit-cell DA with identical TL segments lengths. For the first, leftmost, unit-cell the transistors widths were chosen equal to 20 and 40 $\mu$m respectively. The two drain side TL segments were chosen equal to 1.0 $\mu$m. Inspired from [5], a tapering coefficient is then applied to the remaining cells where each Gm-cell is widen by a factor $k_n$, in which $n$ represents the
In a second step, the uniform DA is tuned in a CAD software. For a gate biasing of 0.7 V and a drain biasing of 1.2 V, with a reference impedance of 50 Ω, the resulting power gain and input return loss obtained from our model is compared against ADS simulations in Fig. 6, validating the accuracy of the proposed model. Simulation results show a very good agreement up to 200 GHz, with small discrepancy appearing attributed to the Gm-cell unilateral assumption.

As a proof of concept, the design analysis is used for a non-uniform 4 unit-cells DA, at 50 Ω reference impedance, with tapered drain line and cascode cells. Solid line: Model – Dotted line: ADS

**B. CAutoD Uniform Distributed Amplifier**

Fig. 6 validated the proposed model that can be considered now for another DA design. We propose in this case a uniform one. Traditionally, DA design is performed in two steps. First, based on conventional analytical equations [7], an optimum number of cells is determined, corresponding to an optimum gain, available only at the considered frequency of calculation. In a second step, the uniform DA is tuned in a CAD software. Hence, with this methodology, maximizing the performance consists in tuning each cell independently, that is to say a high number of variables as stated on Table I. Modifying the number of cells assume to redo all the CAD optimization procedure. On the contrary, the proposed model includes this number of cells as any variable parameter.

As a proof of concept, the design analysis is used throughout a CAutoD, implemented on Matlab©, and enabling to optimize both the design parameters listed in Table I and the number of unit-cells, \( N \). The DA is based on the cascode topology and includes inductive peaking to compensate losses, as described in [8]. Results show very good agreement between analytical model convergence and the CAD implementation in ADS as shown on Fig. 7. By only using NMOS transistors available through the B55 DK, a 1-dB bandwidth of 100 GHz was coded as the design goal, which resulted in a DA having a power gain of 8 dB with a maximum of -10 dB matching inside passband, by using only 5 unit-cells.

![Fig. 6. Comparison between small-signal power gain and input return loss for a non-uniform 4 unit-cells DA, at 50 Ω reference impedance, with tapered drain line and cascode cells. Solid line: Model – Dotted line: ADS](image)

![Fig. 7. Comparison between the proposed DA model including inductive peaking and the same DA in ADS for \( N=5 \) and \( W=31 \) μm (M1) -62 μm (M2), in terms of power gain and input return loss. Solid line: Model – Dotted line: ADS. For a gate biasing of 0.7 V and a drain biasing of 1.2 V, with a reference impedance of 50 Ω.](image)

**IV. Conclusion**

In this paper, a non-closed-form mathematical model for DA was proposed and tested. The model takes into account propagation and mismatches between adjacent cells and hence showed excellent agreement with ADS simulation results in both uniform and non-uniform cases, even with unilateral assumption. This model was also applied to a CAutoD of a DA targeting 100-GHz bandwidth with successful outcome. The device is under fabrication process at that time. This model will be applied in further DA studies such as parametric analysis in addition to optimization algorithms with the purpose of exploring all the potentialities of non-uniform designs. It can allow amplifier designers to gain a better comprehension of the relation between the main parameters of the DA structure and its performance characteristics, and will hopefully help in coming up with new design techniques targeting specifications not achievable by the conventional design approaches, such as high flat gain, low power consumption and compact form distributed amplifiers.

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