Design of Dual Priority Persistent CSMA Protocol Based on FPGA

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Abstract. In order to study the MAC layer protocol in the wireless sensor network under the actual channel condition, the field programmable gate array (FPGA) hardware circuit is used to provide a dual-priority implementation scheme for the persistence carrier sense multiple access (CSMA) protocol. According to the characteristics of each node in the network, analyzes the system throughput and energy consumption, and the FPGA is used to overcome the shortcomings of the existing implementation scheme and the article combines the actual application, changes the single channel mode, and realizes the dual channel data transmission. Finally, the simulation tests the correctness of the design.

1. Introduction
CSMA(Carrier Sense Multiple Access) is an important random multiple access protocol, which effectively enhances the efficiency of data transmission, and CSMA is widely used in wireless sensor networks and wireless networks. In the communication system accessed by the protocol, each information station adjusts its own information transmission rhythm according to the channel state that is heard, thereby improving node transmission efficiency and system performance.

For the research of CSMA protocol, Literature [1, 2, 3] drawing plot of the theoretical formula by using Matlab, we can verify the theoretical results by the research method only, and does not reflect the principle of protocol control and real-time data transmission in the experimental process. The development of embedded technology provides a good technical support for the implementation of MAC protocol. In the literature [4-6], an implementation scheme based on FPGA to implement CSMA protocol is proposed. Although it can show the information packet transmission process, it only relying on the circuit design, Poisson source is not generated, and the circuit structure is complex, the experimental parameters should not be changed, so the statistical value of the simulation result is quite different from the theoretical value. Based on this, the paper uses Matlab and Quartus software to successfully introduce Poisson data stream into the circuit. The hardware description language Verilog HDL and schematic diagram are combined to build a simple and clear circuit. Design a dual priority data transmission system. The simulation results verify the correctness of the circuit design from the aspects of throughput and node energy consumption, and provide useful reference for the theoretical research and implementation of communication protocol.
2. Overview of dual priority persistent CSMA protocol

2.1. Model of Protocol
Persistence CSMA protocol principle: The network node needs to monitor the channel before transmitting the data, and monitors the channel to have data transmission and continuously monitors; otherwise, it detects that the channel has no data to send and immediately sends the data.

![Figure 1. Protocol model of persistence CSMA.](image)

The above figure 1 is analyzed: “U, B and I” respectively indicate different states of successful transmission of data in the channel, collision of transmitted data, and no data transmission in the channel. “TP” indicates the transmission time of an information packet, and “BU” indicates a joint event in which the information packet is successfully transmitted and a collision occurs; “Tn” indicates a cycle period in which the busy time period and the idle time period occur.

![Figure 2. System model of load balancing.](image)

Figure 2 shows system model of the dual-priority persistence load balancing. There are two channels in the system and there are two priorities. Priority 1 to Priority 2 are priorities from low to high, among these priorities, each priority node can have multiple access users. The channels occupied by different priority nodes are different. If the priority of the node is 2, the node occupies channel 1 and channel 2. The priority is “y” node's arrival rate on channel “x”:

\[ \lambda_y \leq x_y \]

The channel utilization rate is

\[ G = \frac{1}{N + x + 1} \]

Considering the load balancing of the system, the utilization of each channel The same is:

\[ G_1 = G_2 = G \]

2.2. Analysis of system throughput
Before analyzing the random multiple access protocol dual priority persistence CSMA, make the following rules for the system:

The mode of channel access is dual-priority stick-type CSMA, and the information packet arrival process on channel “x” satisfies the Poisson distribution (\( x \geq 2 \)) with independent parameter \( \lambda_x \). The protocol is analyzed by using the time slot method. The length corresponding to the idle state is “a”, and the length corresponding to the data transmission is “1+a” (the value is an integer multiple of a). The information packet that is collided or abandoned will be retransmitted at a later time, and the retransmitted packet has no effect on the arrival process of the channel.

According to the law of Poisson distribution, the average length “\( E(U_2) \)” of the successfully transmitted event “\( u_2 \)” in channel 2 is first solved:

For channel 2 of the dual-priority stick-type CSMA control protocol, only the information packets of priority 2 are transmitted, and the successful packet transmission is divided into the following two cases:

One information packet arrives in the last time slot of the idle period, and is sent immediately in the next time slot. The average number of time slots of the event is:

\[ E(N_{u_2}) = \frac{\alpha \lambda e^{-\alpha \lambda_1}}{1 - e^{-\alpha \lambda_1}} \] (1)

The busy cycle arrives and decides to send in the next time slot. The average number of time slots for this event is:
So: \[ E(U_1) = \frac{a\lambda_1 e^{-\alpha_1}}{1 - e^{-\alpha_1}} + (1 + a)\lambda_2 \] (3)

Secondly, the average length \( E(BU_2) \) of the period of data transmission of channel 2 with \( BU_2 \) is:

\[ E(BU_2) = \frac{1 + a}{e^{(1 + a)\lambda_2}} \] (4)

In addition, the average length of the period \( I_2 \) of channel 2 without data transmission is:

\[ E(I_2) = \frac{a}{1 - e^{-\alpha_2}} \] (5)

In summary, the throughput expression on channel 2 is:

\[
S_2 = \frac{a\lambda_2 e^{-\alpha_2} + (1 + a)\lambda_2}{1 - e^{-\alpha_2} + \frac{a}{1 - e^{-\alpha_2}}}.
\] (6)

Since there are information packets of priority 1 and priority 2 on channel 1, and the arrival rate of priority 2 on channel 1 is \( \frac{1}{2}\lambda_2 \), the utilization is \( \frac{G_1}{2} \), so the throughput expression on channel 1 is:

\[
S_1 = \frac{a\lambda_1 e^{-\alpha_1} + (1 + a)\lambda_1}{1 - e^{-\alpha_1} + \frac{a}{1 - e^{-\alpha_1}}} - \frac{a\lambda_2 e^{-\alpha_2} + (1 + a)\lambda_2}{2 - e^{-\alpha_2} + \frac{a}{1 - e^{-\alpha_2}}}.
\] (7)

In summary, the system total throughput expression of the dual-priority stick-type CSMA is:

\[ S = S_1 + S_2. \]

2.3. Analysis of node power

Before analyzing the node power, first make the following assumptions about the power of the nodes in the wireless sensor network under different states: The power required by the node to transmit data is \( P_T \); the power required when the node is in the channel detection state is: \( P_D \); when the node receives data, the required consumption is \( P_R \).

Specific analysis of dual-priority adherence CSMA:

First, assume that the total number of nodes in the system is \( M \). Only one of the \( M \) nodes has only one packet arriving in the idle time slot and decides to transmit. The system power can be calculated as:

\[ P = P_T + (M - 1)P_D. \] (8)

Therefore, the power required for the channel to be in the transmit state during each averaging period is:

\[ P_T = \frac{E(U)}{E(T)} [P_T + (M - 1)P_D] \] (9)

When no node in the system decides to send a packet in the idle time slot a, when all nodes are in the channel detection state, the power of the system is: \( P_{DP} \), so the power required for the channel to be idle in each averaging period is:

\[ P_D = \frac{E(I)}{E(T)} \cdot MP \] (10)

Combined with the previous analysis, the power of the system when the packet sent by the node collides in each averaging period is:

\[ P_B = \left[ E(B)P_T + \left( M - \frac{1}{E(B)} \right)P_D \right] \frac{1}{E(T)} \] (11)

Among them: \( E(B) = E(BU') - E(U)'(1 + a) \)

Therefore, in each averaging period, the power of the overall system is:

\[ P = P_T + P_B + P_D \] (12)
3. Design of system modular
According to the design characteristics of FPGA top-down [7-8], the implementation of dual-priority stick-type CSMA protocol requires modular design.

3.1. Data storage module
According to the previous analysis of the dual-priority CSMA model, it is known that the information packet arrival on the channel satisfies the Poisson distribution with independent parameter $\lambda$. [9], but it can not generate a Poisson distribution of data streams with IP core or module in the Quartus II. The Poisson data stream is generated here using Matlab software.

3.2. Source processing module
The idle event slot length is $a$ in the dual-priority stick-type CSMA protocol analysis, and the slot length when the information packet is sent is “$1+a$”, which is an integer multiple of “a”. But the idle event has the same slot length as the busy event in the data stream of the initial source, and there is no multiple relationship, so the initial source data needs to be processed.
the output information will retain the last read value. According to this characteristic, when the feedback counter detects that the initial station information stream data is busy data, it immediately gives a low level signal to the read enable, and the pause time of the read enable is controlled by changing the counter value, which is the time slot length of the busy event. Finally we realize the controllable function of the length of the different state slots.

Figure 6. Source processing module simulation timing diagram

Figure 6 is a timing simulation diagram of a time slot length control module, and “do1” represents a real-time data transmission situation of a certain station, where the time slot length of the idle data “0” has an integer multiple relationship with the non-idle data “6”, “7”, which is designed with the original intention matched.

3.3. Channel multiplexing control module

The data streams are processed by the source processing module becomes two priorities. Priority 2 is divided into two parts (priority 2_1 and priority 2_2), where priority 2_2 is transmitted separately on channel 2, and priority 2_1 competes with priority 1 for one channel, so it is necessary to solve the channel multiplexing problem. In order to implement the competition mechanism of the persistent CSMA, the real-time situation of the priority 2_1 and the priority 1 is classified and controlled, and (0, 6, 7) and (1, 8, 9) respectively represent the priority 1 and the priority 2_1. (I, U, B) three states. When there is no data in both priorities, channel 1 is idle; when one of the two priorities is single data and the other is no data, channel 1 is in the successful transmission state. Channel 1 is conflict on the remaining real-time conditions, which reflects the control strategy of the persistent CSMA protocol on the multiplexed channel.

3.4. Selecting the reading module

Priority 2_2 is transmitted separately on channel 2, and there are two states in the channel: the channel is idle, the channel is busy (the joint event of success and collision); therefore, in order to achieve information packet competition in circuit design, information sites are divided into free sites and busy sites. The data of the two sites are from two Poisson data streams in Matlab, and the arrival rates are $\lambda_1$, $\lambda_2$, and $\lambda_1 + \lambda_2 = \lambda_0$. Such a Poisson data site with arrival rate $\lambda_0$ is generated. The information packet processing module selectively reads the information data of the idle or busy station according to the real-time data (I, U, B) on the channel bus, so that the system completes the function of the listening channel and realizes the mechanism of protocol control on the single-channel persistent CSMA.

3.5. Throughput detection module

The throughput detection module implements the function of correctly reading the information of the corresponding station. 

![Throughput detection module](image)

Figure 7. Throughput detection module

Figure 7 shows the throughput detection module. Since the channel utilization cannot be 100%, the module needs to filter the idle data. The function of the filter is that it compare whether the data on the channel is the same as the free data type. If it is different, the data enters the FIFO. If it is the same, it
is automatically filtered. When there is data in the FIFO and it is not read, the counter counts the number of time slots that the data is successfully transmitted on the channel.

\[ S = \frac{N_U \cdot T_{BU}}{t_t} \cdot \frac{1}{1+a} \]  

Equation (13) is the throughput statistics method. Where \(t_t\) is the total duration of the simulation, \(N_U\) is the number of successful time slots for data transmission in the circuit simulation, and \(T_{BU}\) is the length of the time slot in the busy state of the channel. This time slot length is the length of an information packet transmission in the algorithm protocol (“TP”), the theoretical value is “1+a”, and the success time slot length is “1”, so the length of the calculation success state should be multiplied by \(\frac{1}{1+a}\).

4. System evaluation

4.1. Simulation test

The simulation experiment is mainly for testing throughput and node power in dual-priority stick-type CSMA. The value calculated from the theoretical expression of the research protocol derived in Section 2 is the test criterion. The arrival rate \(\lambda\) value of the source can be adjusted by the Poisson function in Matlab. The numerical relationship of different time slots can be adjusted in the counter program of the source processing module. The experimental simulation parameter settings are shown in table 1.

| Parameter Description          | value     |
|-------------------------------|-----------|
| System minimum operating clock cycle | 10ns      |
| System simulation time \(T\)  | 500us     |
| Free time slot \(a\)           | 0.1       |
| Idle information slot length \(T_i\) | 80ns      |
| Busy information slot length \(T_{BU}\) | 800ns     |
| Priority 1 arrival rate \(\lambda_1\) | 1         |
| Priority 2-1 arrival rate \(\lambda_{2,1}\) | 0.5       |
| Priority 2-2 arrival rate \(\lambda_{2,2}\) | 1         |
| Node sends state power \(P_s\) | 70mw      |
| Node listening state power \(P_l\) | 16mw      |
| Node accepts state power \(P_r\) | 40mw      |

![Figure 8. Circuit simulation statistics](image)

As shown in figure 8, “do1” and “do2” are real-time transmission data on channel 1 and channel 2, besides, “C1” and “C2” are the number of time slots in the successful transmission state of data on channel 1 and channel 2, respectively. The hardware circuit is simulated under the condition of the simulation parameters of table 2. After calculation, the simulation values of the throughput of the channel 1 and the channel 2 are 0.624 and 0.472, respectively, which are consistent with the theoretical values of 0.664 and 0.471. According to the system throughput simulation value, the
relative error of the node average power value of 42.16mw and the theoretical value of 42.31mw is calculated to be relatively small, which indicates that the system design is reasonable.

4.2. Statistical analysis

Under the same working conditions, by taking multiple statistics of different simulation durations, according to the number of information slots, which are successfully sent, calculate the throughput statistics \( \bar{S} \) on system channel 1 using equation (13), then calculate the statistical value \( \bar{P} \) of the average power of the system node according to the power analysis. In table 2, the statistical value and the theoretical value are very close, as the working statistical duration increases, the statistical value gradually converges to the theoretical value, which is consistent with the theoretical reality.

Table 2. Comparison of statistical and theoretical values.

| \( T/\mu s \) | \( S \) | \( \bar{S} \) | \( P/mw \) | \( \bar{P}/mW \) |
|------------|--------|------|--------|--------|
| 100us      | 0.664  | 0.609| 42.31  | 41.94  |
| 200us      | 0.664  | 0.617| 42.31  | 42.08  |
| 300us      | 0.664  | 0.621| 42.31  | 42.12  |
| 500us      | 0.664  | 0.624| 42.31  | 42.16  |

5. Conclusion

According to the working characteristics of the nodes in the wireless sensor network, this paper uses FPGA to design the circuit of the dual-priority stick-type CSMA protocol. This circuit not only combines Matlab and Quartus software, but also introduces Poisson data stream into the circuit. At the same time, according to the characteristics of communication protocol algorithm, its working principle is mapped into the circuit system, which shows the double priority data transmission process. After experimental simulation test, under the set simulation conditions, the simulation values of the system's throughput rate and node average power are consistent with the theoretical values, which confirms the accuracy and rationality of the design. FPGA is a kind of hardware performance, FPGA realizes the communication protocol algorithm and can realize the real node transmission process on the hardware parallel circuit. It is a process from theory to practice. It is helpful for us to improve understanding of the theory of communication protocol algorithm.

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