RF Reflectometry for Readout of Charge Transition in a Physically Defined p-channel MOS Silicon Quantum Dot

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We have embedded a physically defined p-channel MOS (PMOS) silicon quantum dot (QD) device into an impedance transformer RC circuit. To decrease the parasitic capacitance of the device which emerges in MOS devices that have a top gate, we fabricate a new device to reduce the device’s top gate area from 400 $\mu$m\textsuperscript{2} to 0.09 $\mu$m\textsuperscript{2}. Having a smaller top gate eliminates parasitic capacitance problem preventing the RF signal from reaching QD. We show that we have fabricated a single QD properly, which is essential for RF single-electron transistor technique. We also analyze and improve the impedance matching condition and show that it is possible to perform readout of charge transition at 4.2 K by RF reflectometry. This will enable fast readout of charge and spin states.

1. Introduction

Qubit based on silicon quantum dots (QDs)\textsuperscript{1,2}) is an appropriate platform for quantum computers thanks to its long coherence time,\textsuperscript{3}) scalability, and compatibility with CMOS technology.\textsuperscript{4,5}) Particularly p-channel MOS (PMOS) silicon QDs are promising for the development of a spin-based qubit system since hole spins have smaller hyperfine interactions than electron spins and can be controlled only with an electric field as they have strong spin-orbit coupling (SOC).\textsuperscript{6–8}) Charge sensing technique, where a capacitively coupled additional single QD (SQD) is required, has been used extensively to map out the charge states in QDs. While this technique is relatively easy to demonstrate since it only requires the devices to be properly fabricated, the integration time ($t_{\text{min}}$), which is the minimum time to discern and characterize the states, should also be considered.\textsuperscript{9}) For a readout to be effective, the measurement needs to be faster than the relaxation time of the system. In quantum computing, in order to perform single
shot readout for quantum error correction, the measurement time should be faster than the coherence time ($T_2^*$). For silicon qubits, $T_2^*$ has been reported to be several tens of $\mu$s\(^{10}\).

Charge sensing is performed at a cryogenic temperature that requires long wiring to connect the sample to the room temperature equipment. Considering the capacitance ($C$) in the cable’s length, which has a typical value of 70 pF/m\(^{11}\) and the resistance of the sample $R \approx 100 \, \text{k}\Omega$, the bandwidth ($BW$) of the measurement is restricted by RC time constant and limited to a few kilohertz or less. Instead of performing a voltage and current tests, namely DC measurement, a so-called RF single-electron transistor (RF-SET) overcomes the low-frequency restriction. LC resonant tank circuit is used to measure RF waves reflected from the SET\(^{39}\). This technique has been used to increase the BW of SET, quantum point contact,\(^{12-16}\) and superconductor-insulator-normal thermometers.\(^{17}\) It is also used to warrant rapid readout of charge sensor,\(^{18}\) complex impedance measurement of circuits,\(^{19-25}\) large gate two-dimensional systems,\(^{26}\) and nanomechanical resonators.\(^{27}\)

In this study, we use SQD part of the PMOS silicon QD device to readout charge transition via RF reflectometry. The device we fabricated is a physically defined QD, therefore, it does not need gates to form confinement potential\(^{28-30}\) and it has less complexity. Since it is a p-channel device and has strong SOC, it does not require additional structure for spin manipulation.\(^{31,32}\) However, MOS devices with a large global top gate have large capacitance and this precludes RF signal from reaching QD area. To tackle this disadvantage, we use a device with a small top gate, as we explain in Section 3.1.

In the extended abstract for SSDM2020\(^{33}\) we presented readout of charge transition via RF reflectometry. In this paper, we analyze and discuss impedance matching condition in detail.

### 2. Device fabrication

A scanning electron microscope (SEM) image and schematic of physically defined PMOS double QD (DQD) and SQD on undoped silicon-on-insulator (SOI) substrate are shown in Fig. 1(a), and 1(b), respectively. The dark and bright regions in Fig. 1(a) indicate the BOX layer of the structure, and the SOI layer, respectively. The device has three side gates ($G_1, G_m, G_r$) capacitively coupled to DQD and one side gate ($G_{SQD}$) capacitively coupled to SQD for controlling electrochemical potential. The device is fabricated on
(100) SOI substrate. The confinement in MOS structure devices lifts the degeneracy between heavy hole state and light hole state so that the lowest sub-band corresponds to heavy holes. Therefore, heavy holes give the largest contribution to carrier properties. The in-plane effective mass of heavy hole is larger than that of electron in (100) SOI substrate, requiring stronger confinement. Hence, relatively small, ~50-nm in diameter of QDs are required. The fabrication process is as follows. A 40-nm thick SOI substrate is etched to form SQD, DQD, and side gates by reactive ion etching technique after electron beam lithography. Next, the thermal oxidation to form a 3-nm-thick SiO$_2$ layer and the plasma chemical vapor deposition (P-CVD) to form a 65-nm-thick TEOS-SiO$_2$ layer were performed. Then, a 100-nm-thick n$^+$-poly-Si layer was deposited by low-pressure CVD as the top gate (TG) material. In order to shrink the conventional TG area of 400 µm$^2$ to 0.09 µm$^2$, we used electron beam lithography in the TG pattern formation. After the TG formation, the BF$_2^+$ ion implantation (I/I) was performed with a dose of $1.5 \times 10^{15}$ cm$^{-2}$ and a tilting angle of 7° at a fixed energy of 10 keV to form source-drain (SD) regions. To activate the implanted impurities, the rapid thermal annealing (RTA) was carried out at 860 °C for 2 s. Finally, contact holes and aluminum electrodes were formed, and the wafers were sintered in forming gas ambient at 450 °C for 30 min. In this measurement, we use only an SQD for studying the effect of reducing TG area of the device on RF reflectometry. In the future experiments, we measure spin states in the DQD by using the SQD as RF-SET.

3. Method and discussion

3.1 Experimental method

In this study, we use the RF reflectometry technique to readout charge transition in a physically defined PMOS silicon QD device. MOS devices with TG can have large gate capacitance $C_g$, which also causes a large parasitic capacitance. Large gate capacitance prevents probing signal from reaching the QD. To suppress large gate capacitance, the TG area is reduced down from 400 µm$^2$ to 0.09 µm$^2$ as shown in Fig. 2.

We perform a DC measurement to check device characteristics where we can see single hole transition by sweeping TG voltage and drain to source voltage of SQD at a temperature of 4.2 K. We obtain multiple Coulomb diamonds that are not in the same size as shown in Fig. 3. Our measurement proves that the device we fabricated has a QD characteristic although some unintended localized states exist both in series and in parallel.\textsuperscript{35,36} In an ideal SQD with no unintended localized states, Coulomb diamonds
Fig. 1. Physically defined p-channel silicon MOS device. (a) Scanning electron microscope image of the device taken after reactive ion etching of SOI. Top gate (TG) position is schematically shown by dashed blue lines. Two QDs in DQD part and one QD in SQD part are circled in yellow. (b) Cross-sectional schematic of the device structure along yellow dashed line in (a).

Fig. 2. Schematic of the region around QD with a square TG that has a side of 20 μm (left) and 300 nm (right). Blue and green regions denote TG and SOI, respectively. To surpass large gate capacitance problem TG area is reduced from 400 μm² to 0.09 μm².

touch at a single point at $V_{ds} = 0$. When there are localized states that charge up or get discharged, some diamonds can be shifted and overlapped. Although there exists some unintended localized states near SQD, the necessary condition of having SQD is satisfied, which is essential for studying RF-SET technique. In the RF measurement, by
Fig. 3. Charge stability diagram. TG voltage, $V_{tg}$, and drain to source voltage, $V_{ds}$, are swept to obtain Coulomb diamonds. Current can flow out of the diamonds whereas it is blocked in the diamond where the first derivative of the current, $dI/dV_{tg}$, is minimum.

using the setup shown in Fig. 4(a), we first find the resonant frequency of the device. Here, the device is mounted on an FR4 printed circuit board (PCB), and the bonding wire is connected to the drain lead of the SQD. Before the signal reaches the sample, it is attenuated with a -40-dB attenuator to protect the device against electrostatic discharges. Electron transition through the SQD causes a change in amplitude of the reflected signal. The directional coupler sends the carrier signal down one line, and the reflected signal up another line. The reflected signal is transmitted through the directional coupler back up the carrier line. Afterwards, the signal is amplified with room temperature amplifiers, which have a gain of 60-dB in total. A 2.2 $\mu$H commercial inductor is used in a series LC resonant tank circuit shown in Fig. 4(a). Fig. 4(b) shows the amplitude change in reflected signal ($S_{21}$) as a function of applied frequency. We find a resonant dip at 210.875 MHz. From the resonant frequency $f_r$ of 210.875 MHz, we derive the parasitic capacitance $C_p$ to be 0.258 pF.

The obtained value of 0.258 pF, is lower than that obtained for the device with 400 $\mu$m$^2$ TG area, which was 0.6 pF,$^{37}$ since the presented one has a smaller TG area. It is worth noting that the parasitic capacitance is affected by material used in the PCB and the thickness of PCB. Besides, the distance between device and the PCB path and the number of bonding wires used to connect the device to the PCB also change the conditions. Furthermore, in actual MOSFET devices, capacitance components are
Fig. 4. (a) Measurement setup. Attenuated RF signal is sent through series LC resonant tank circuit to drain of single quantum dot (SQD) and reflected signal that is separated by directional coupler is amplified at room temperature before it reaches the second port of vectoral network analyzer. (b) $S_{21}$ as a function of frequency. Resonant frequency, $f_r = 210.875$ MHz, of the sample is shown when TG voltage is not applied.

distributed other than top gate capacitance. As a result, there may always not be a direct ratio between reducing top gate area and the obtained parasitic capacitance.

3.2 Analysis of impedance matching

To find out how good impedance matching we analyze the matching conditions. We first subtract the background noise and then fit a Lorentzian shape (see Fig. 5(a)). The loaded quality factor ($Q_L$) is found to be 101 by using $Q_L = f_r/BW$, where 3-dB $BW$ is 2.071 MHz. We then analyze the matching on the polar plot. In Fig. 5(b), the blue line shows the whole trace of the reflected signal. The reflection coefficient is given by $|\Gamma| = |(Z_L - Z_0)/(Z_L + Z_0)|$, where $Z_0$ is the characteristic impedance of the transmission line and has a typical value of 50 Ω and $Z_L$ is loaded impedance. $|\Gamma|$ is found to be 0.048. Perfect matching occurs where $\Gamma$ crosses the origin of the polar axis ($\Gamma = 0$). At the perfect matching point, $Z_L$ is equal to $Z_0$.\textsuperscript{38)}

Having a $|\Gamma|$ of 0.048, our impedance matching is close to the perfect matching point. It is worth mentioning that one could have a better impedance matching by doing
Fig. 5. Analysis of impedance matching. (a) Background noise is subtracted (red line) from $S_{21}$ vs frequency data shown in Fig. 4(b) and then fitted (green line) with a Lorentzian shape. The center frequency is 210.875 MHz and $BW$ of 3-dB regime (yellow line) is 2.0718 MHz. Loaded quality factor, $Q_L$, is found to be 101. (b) Trace of reflected signal (blue line) is shown on a polar plot. Reflection coefficient, |$\Gamma$|, is found to be 0.048. The perfect matching occurs where $\Gamma$ crosses the origin of the polar plot ($\Gamma = 0$).

some more circuit engineering but the present matching condition is enough to perform RF-SET.

3.3 RF readout measurement

Amplitude change in reflected signal ($S_{21}$) caused by charge transition between QD and the leads is mapped out by sweeping the TG voltage as shown in the upper panel of Fig. 6(a). In RF reflectometry, the frequency of probing signal should be adjusted so that it exceeds background noise. Here, we fix the RF frequency at 210.875 MHz. At the same time, we perform standard (DC) I-V measurement, as shown in the lower panel of Fig. 6(a). We also perform a similar measurement by sweeping the voltage $V_{sg}$ applied to G_{SQD} while applying a constant negative voltage to the TG to form a channel between source and drain, as shown in Fig. 6(b). Coulomb peak characteristics are similar in both DC and RF measurements, meaning that we succeeded in the readout of charge transition via RF-SET technique.
Fig. 6. Simultaneous measurements of RF (shown by blue line) and DC (shown by black line) by sweeping $V_{tg}$ (a) and $V_{sg}$ with constant $V_{tg}$ of -2.5 V (b), respectively. RF and DC measurements are alike, implying that electron transition can be readout by RF reflectometry.

4. Conclusions
We have fabricated physically-defined PMOS QDs with smaller TG area and performed RF-SET measurements. Reducing TG area from 400 $\mu$m$^2$ to 0.09 $\mu$m$^2$ resulted in surpassing the large gate capacitance problem and permitting the RF signal to reach QD area. We observed Coulomb peaks via RF, and this result is in good agreement with DC measurement. This result shows us a route to fast readout in our future work.

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