Brief Announcement: On the Limits of Parallelizing Convolutional Neural Networks on GPUs

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ABSTRACT

GPUs are currently the platform of choice for training neural networks. However, training a deep neural network (DNN) is a time-consuming process even on GPUs because of the massive number of parameters that have to be learned. As a result, accelerating DNN training has been an area of significant research in the last couple of years.

While earlier networks such as AlexNet had a linear dependency between layers and operations, state-of-the-art networks such as ResNet, PathNet, and GoogleNet have a non-linear structure that exhibits a higher level of inter-operation parallelism. However, popular deep learning (DL) frameworks such as TensorFlow and PyTorch launch the majority of neural network operations, especially convolutions, serially on GPUs and do not exploit this inter-op parallelism. In this brief announcement, we make a case for the need and potential benefit of exploiting this rich parallelism in state-of-the-art non-linear networks for reducing the training time. We identify the challenges and limitations in enabling concurrent layer execution on GPU backends (such as cuDNN) of DL frameworks and propose potential solutions.

CCS CONCEPTS
• Computing methodologies → Parallel computing methodologies; Machine learning;

KEYWORDS
Convolutional Neural Networks (CNNs), GPU, non-linear networks, parallelization, resource utilization

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1 INTRODUCTION

Convolutional Neural Networks (CNNs) are a popular class of DNNs with several applications such as computer vision [12, 17], voice recognition [2], recommender systems [23], physics simulations [15], and natural language processing [6, 9]. Earlier CNNs were composed of a linear sequence of dependent layers like VGG and AlexNet. However, modern networks such as ResNet, GoogleNet, DenseNet, and PathNet have a more complex architecture. These non-linear networks contain multiple fork/joins resulting in independent paths of chained operations. Figure 1 illustrates the difference in structure between linear (AlexNet) and non-linear (GoogleNet) networks.

Figure 1: Examples of linear (AlexNet on the left) and non-linear (GoogleNet on the right) networks.

GPUs are the platform of choice for training CNNs. Training large-scale CNNs is extremely time-consuming due to the ever-growing number of parameters that have to be learned and the numerous iterations for the model to converge. Two approaches to reducing training time are to increase throughput and reduce the per-iteration execution time. For the former, it is common to parallelize training on multiple GPUs or GPU clusters using different strategies [4, 8]. For the latter, however, there are several solutions in literature [19]. They can be broadly classified into either optimizing the operations in each layer or exploiting the concurrency between CPUs and GPUs by pipelining pre-processing operations (such as resizing, normalization) on the CPU with the rest of the operations on the GPU [18, 20]. As one can infer from Figure 1, unlike linear networks, non-linear networks have multiple independent operations across layers. However, none of the above state-of-the-art approaches exploit this parallelism across multiple paths by...
running independent operations across layers concurrently on a single GPU. In this paper, we investigate why and how to utilize this rich inter-op parallelism in non-linear CNNs to reduce training time.

2 PARALLEL CONVOLUTIONS ON A GPU
A majority of DL frameworks have a GPU backend that compiles the model and generates a computation graph at the granularity of basic operations such as convolution, batch normalization, and pooling. The operations are executed on the device by calling the corresponding APIs in highly optimized third-party libraries such as Nvidia cuDNN [5] and cuBLAS [1]. The kernels implemented in these libraries hold device resources to perform the CNN operations.

The core operation in CNNs is convolution which constitutes the majority of the training time, approximately 60% of the compute time for ImageNet Large Scale Visual Recognition Challenge (ILSVRC) winners [20]. It also typically consumes more memory than other network layers [18, 20]. cuDNN supports multiple algorithms for each type of convolution. For example, for forward convolution, it supports GEMM, IMPLICIT_GEMM, IMPLICIT_PRECOMP_GEMM, WINOGRAD, WINOGRAD_NONFUSED, DIRECT, FFT, and FFT_TILING. Depending on the convolution parameters (input, filter, data layout, etc.), each of the above algorithms has a different execution time, resource utilization, and workspace memory.

To launch multiple convolutions concurrently on a GPU, each convolution has to be assigned to a separate executor (stream in the CUDA programming model). Besides, to accommodate two or more convolutions on a GPU, DL frameworks need to ensure there is enough device memory available at launch time 1. Convolutions in cuDNN use device global memory for storing input, output, filter, and intermediate results (or workspace). The input, output, and filter sizes for convolutions are fixed during model construction, so DL frameworks can only adjust workspace memory.

2.1 Results and Analysis
Our experiments on numerous convolutions (from popular networks such as GoogleNet and ResNet) reveal that it is not feasible to run two or more cuDNN convolutions concurrently. Using the Nvidia profiler, we observe that cuDNN kernels exhaust one or more resources such as registers and shared memory on the GPU Streaming Multiprocessor (SM) and do not allow the GPU scheduler to execute blocks from another kernel on the same SM. Since a convolution typically has enough blocks to occupy all available SMs, execution of a second convolution is postponed to after the first convolution is completed resulting in a sequential execution of the two operations. Even though the profiler reports high occupancy for convolutions, for combinations of inputs and convolution algorithms, the computational efficiency and DRAM utilization are not high enough (e.g. less than 50%) [10, 11, 13, 14].

In addition, current DL frameworks either stick to certain algorithms for convolutions or pick the fastest algorithm. For example, in the first iteration, TensorFlow (r1.10) tests all algorithms for each convolution and chooses the fastest one for subsequent iterations. Even though this method is optimal to reduce the execution time of linear networks, it is not essentially the best option for the parallel execution of operations since the fastest algorithm could inadequately use SM resources and/or consume a large amount of workspace memory preventing concurrent kernel executions. We observe this exact behavior by profiling the resource utilization and workspace memory of convolutions in popular networks.

SM resources. Table 1 shows profiling data for two independent convolutions in the inception module of GoogleNet on a Tesla K40 GPU with CUDA 10.0 and cuDNN 7.6. According to the table, PRECOMP_GEMM algorithm for the first convolution exhausts SM registers (more than 90%) but poorly uses shared memory (39%) while FFT_TILING algorithms have complementary static resource utilization, i.e. bottlenecked by SM shared memory but consume only 38% of registers. Further, these two algorithms exhibit different warp execution characteristics. For example, FFT_TILING (on the second convolution) has 20% ALU utilization but significantly greater memory stalls compared to the PRECOMP_GEMM algorithm (on the first convolution) with high ALU utilization (70%) and lower memory stalls. This indicates, the former algorithm is relatively bound by memory rather than compute resources as in the latter algorithm.

In the past few years, researchers have proposed inter-SM [3, 16, 24] and intra-SM [7, 16, 21, 22] partitioning to improve resource utilization for concurrent kernel execution. Inter-SM partitioning or spatial multitasking [3, 24] which partitions the SMs among kernels has performance benefits when kernels with complementary characteristics are co-located. In intra-SM partitioning, resource utilization is further improved by letting blocks from different kernels share the same SM. For instance, functional units in an SM (ALUs, SFUs, etc.) that are idle when running a memory-intensive kernel can be utilized by the blocks of a compute-intensive kernel. Intra-SM partitioning can practically be achieved when one or more SM static resources such as registers and shared memory remain under-utilized by kernels [7, 16, 22].

Thereby, for two convolutions in Table 1, if we choose PRECOMP_GEMM for the first convolution and FFT_TILING for the second (TensorFlow would pick PRECOMP_GEMM for both) and employ SM partitioning [7, 22, 24], the memory stalls of the second convolution can potentially be hidden by switching to compute-warps from the first convolution. This parallelization can improve resource utilization and reduce latency compared to serial execution. We discover 27 similar cases in this network and more instances in other popular non-linear CNNs such as ResNet.

Device Memory. Table 2 shows the execution time and workspace memory for a convolution operation in GoogleNet. Comparing the FFT algorithm (TensorFlow selection) with Winograd Nonfused, the former is only 21% faster but requires almost 1.5 GB (or 70%) of extra memory. Changing the convolution algorithm is the only way to configure workspace memory. Therefore, careful and profiling-based algorithm selection has the potential to mitigate concurrent kernel execution’s limitations and improve the parallelism on a single GPU.

3 CONCLUDING REMARKS
We conclude that partitioning GPU computing resources among concurrent convolutions depends on the workload (algorithm) which
impacts both the execution time and workspace memory of kernels. While we observe no strong correlation between the execution time and workspace memory, they are mutually dependent. Moreover, selecting independent operations from the ready queue for concurrent execution is a challenging scheduling problem that highly depends on the network topology and resource utilization of operations. Even though we observe the potential for concurrent execution of convolutions, profile-based algorithm selection has to evaluate multiple metrics for optimal parallelism.

Currently, neither does CUDA provide an API for partitioning compute resources between streams nor does cuDNN API support that configuration. Therefore, we are investigating open-source frameworks such as AMD ROCm and GPU simulators for implementing intra- and inter-SM partitioning along with profiling-based algorithm selection.

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Table 1: Resource utilization of two independent convolutions in the first Inception module of GoogleNet on a Tesla K40 GPU.

| Layer | Algorithm | Kernel name | Registers | Shared Memory | Threads | Blocks | ALUs | Memory stalls |
|-------|-----------|-------------|-----------|---------------|---------|--------|------|--------------|
| Incep. 1 (3 + 3) | PRECOMP_GEMM | implicit_convolve_sgemm | 92% | 39% | 19% | 70% | 0.47% |
|       | FFT_TILING | fft2d_c2r_32x32 | 38% | 75% | 25% | 6% | 30% | 15.2% |

Table 2: Comparison of workspace memory and execution time for the 5 × 5 convolution in the third inception module of GoogleNet on a Tesla K40 GPU using all the algorithms implemented in cuDNN. DIRECT and WINOGRAD algorithms are not supported for this input.

| Convolution Algorithm | Workspace Memory | Runtime |
|-----------------------|-----------------|---------|
| GEMM                  | 0               | 58 ms   |
| IMPLICIT GEMM         | 48 KB           | 59 ms   |
| PRECOMP GEMM          | 4.8 GB          | 126 ms  |
| WINOGRAD NONFUSED      | 691 MB          | 46 ms   |
| FFT                   | 2.2 GB          | 36 ms   |
| FFT TILING            | 1.1 GB          | 48 ms   |