Complementary junction field-effect transistor logic gate operational at 300°C with 1.4 V supply voltage.

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Integrated circuits (ICs) that can operate at high temperature have a wide variety of applications in the fields of automotive, aerospace, space exploration, and deep-well drilling. Conventional silicon-based complementary metal-oxide-semiconductor (CMOS) circuits cannot work at higher than 200°C, leading to the use of wide bandgap semiconductor, especially silicon carbide (SiC). However, high-density defects at an oxide-SiC interface make it impossible to predict electrical characteristics of SiC CMOS logic gates in a wide temperature range and high supply voltage (typically $\geq 15$ V) is required to compensate their large logic threshold voltage shift. Here, we show that SiC complementary logic gates composed of p- and n-channel junction field-effect transistors (JFETs) operate at 300°C with a supply voltage as low as 1.4 V. The logic threshold voltage shift of the complementary JFET (CJFET) inverter is 0.2 V from room temperature to 300°C. Furthermore, temperature dependencies of the static and dynamic characteristics of the CJFET inverter are well explained by a simple analytical model of SiC JFETs. This allows us to perform electronic circuit simulation, leading to superior designability of complex circuits or memories based on SiC CJFET technology, which operate within a wide temperature range.
The electronics operational at high temperature has a wide variety of applications in the fields of automotive, aerospace, and energy industry. However, conventional silicon (Si) complementary metal-oxide-semiconductor (CMOS) ICs are not operational at higher than 200 °C since p-n junctions do not work as device isolation. Then, Si CMOS on silicon-on-insulator (SOI) is developed and push the temperature limitation up to 300 °C. For further high temperature operation, the use of a wide bandgap semiconductor has attracted much attention. The intrinsic carrier density in a wide bandgap semiconductor is many-orders-of-magnitude lower than that in Si, where p-n junction can be used as device isolation at higher temperature. Among wide bandgap semiconductors, silicon carbide (SiC) has several advantages in terms of fabrication of ICs such as mature ion implantation technology and mass production of SiC power devices. As in the case of Si, SiC CMOS circuits have been developed and high temperature operation has been demonstrated. However, SiC CMOS characteristics cannot be predicted within a wide temperature range due to the high-density defects at the silicon dioxide(SiO$_2$)/SiC interface, leading to a high supply voltage ($V_{dd}$, typically 15 V) and large power consumption. Moreover, reliability of SiO$_2$ at high temperature is a serious concern since the high $V_{dd}$ induces the high electric field inside SiO$_2$, resulting in the increase of gate leakage current. Circuits composed of SiC n-channel junction field-effect transistors (n-JFETs) and resistors (JFET-R) were also proposed and long-term reliability has been proved. However, their power dissipation especially in digital logic gates is large because of the use of depletion-mode JFETs and large $V_{dd}$.

A complementary circuit can be assembled with p- and n-channel JFETs and a complementary JFET (CJFET) circuit should exhibit extremely low static power dissipation in the same man-
ner as a CMOS circuit. Operation of CJFET has been reported with gallium arsenide (GaAs)\cite{16,17} and Si\cite{18} for the development of ICs with ultra-low power loss. In CJFET circuits, however, $V_{dd}$ has to be less than a built-in potential of a gate p-n junction to avoid current flowing through the gate p-n junction, indicating less flexibility of device design with Si and GaAs, where a typical value of a built-in potential is around 0.8-1.2 eV. On the other hand, a gate p-n junction of SiC has a large built-in potential of about 3.0 eV at room temperature (RT), resulting in a reasonably higher $V_{dd}$ and large noise margin. Therefore, SiC CJFET technology has a potential to be a suitable choice as low-power-loss and high-reliability ICs operational at high temperature.

For fabrication of CJFET circuits, enhancement-mode JFETs are required and design of threshold voltage in both p- and n-JFETs ($V_{Tp}$ and $V_{Tn}$) is of importance. Conventional SiC JFETs have used an epitaxial layer as a channel, leading to inevitable distribution of $V_{Tn}$ inside a wafer due to the growth rate and doping distribution.\cite{19} To overcome the problem, we have proposed that all the device regions were fabricated by ion implantation and fabrication of enhancement-mode p- and n-JFETs on a same substrate was demonstrated.\cite{20,21} In this article, SiC CJFET logic gates are assembled by the ion-implantation-based p- and n-JFETs. Inverter operation at 300 °C is demonstrated with $V_{dd}$ of 1.4 V and its static and dynamic characteristics are well reproduced by a simple analytical model of SiC JFETs. We have also demonstrated NOR operation at 300 °C.
Fabrication of complementary JFET inverter

Figure 1a shows a CJFET inverter circuit diagram. A CJFET circuit can be assembled by replacing p- and n-MOS field-effect transistors (FETs) in a CMOS circuit by p- and n-JFETs, respectively. The layout design of a CJFET inverter and optical image of the fabricated CJFET inverter are shown in Fig. 1b,c. The CJFET inverter was fabricated by ion implantation into a 4H-SiC high-purity semi-insulating substrate. The semi-insulating region is expected to work as device isolation. Total ion implantation steps are four and details of ion implantation conditions are provided in Supplementary Table 1. As shown in the inset of Fig. 1c, the channel of the JFET is controlled by side gates, which enhances transconductance compared to a standard single gate JFET. The channel width ($W_p$ or $W_n$ in the p- or n-JFET) is defined as the direction orthogonal to the sample surface and $W_p$ and $W_n$ were estimated as 0.6 and 0.45 µm by secondary ion mass spectrometry. The channel thickness ($a_p$ or $a_n$), which determines the $V_{Tp}$ or $V_{Tn}$, and the channel length ($L_p$ or $L_n$) were designed by the mask layout for ion implantation. Owing to the lateral channeling of implanted atoms, the actual values of $a_p$, $a_n$, $L_p$, and $L_n$ differ from the mask design, which will be estimated from the electrical characteristics below.

The transfer characteristics of the fabricated p- and n-JFETs assembling the CJFET inverter (Fig. 1c) and the voltage transfer characteristic (VTC) of the CJFET inverter at RT are shown in Fig. 1d. Although the p- and n-JFETs have the similar channel thickness and width, the n-JFET shows higher drain current since electron mobility is larger than hole mobility in SiC and the ionization ratio of Al in the p-channel is low. For the analysis of the CJFET circuits, a simple
analytic model of a JFET was applied, the details of which are described in Supplementary Note 1. From the transfer characteristics of the p- and n-JFETs, $V_{T_p}$ and $V_{T_n}$ are determined as 0.63 and 0.61 V, leading to the values of $a_p$ and $a_n$ as 460 and 458 nm, respectively. Although the edges of the side gates are rounded due to the lateral straggling, $L_p$, and $L_n$ are not strongly modified and estimated as 4 µm, which are the same values of the mask design. The logic threshold voltage ($V_{th}$) of the CJFET is 0.65 V with $V_{dd}$ of 1.4 V (Fig. 1d). As discussed above, SiC has a wide bandgap, leading to a large built-in potential between a p-n junction. Then, forward current does not flow at the gate p-n junctions in the p- and n-JFETs even with $V_{dd}$ of 1.4 V at RT.

**Static characteristics**

The temperature dependence of the transfer characteristics in the p- and n-JFETs is depicted in Fig. 2a,b. The measurement temperature range is from RT to 573 K. The drain current of the p-JFET is enhanced with elevating the temperature since the hole density in the p-channel increases by enhancement of dopant ionization. The decrease in the drain current of the n-JFET is attributed to electron mobility lowering. These trends are the same as the side gate p- and n-JFETs separately fabricated in our previous study. On the other hand, the leakage current at a gate voltage of 0 V in the fabricated p- and n-JFETs dramatically increases with elevating the temperature. The increasing rate against temperature is much larger than those in our previously reported JFETs (see Supplementary Fig. 1). The leakage current in the JFETs assembling the CJFET inverter mainly consists of the gate-source leakage current whereas the gate leakage current was negligible even at 573 K in the separately fabricated JFETs. In the CJFET inverter, parasitic p-i-p (the source region...
in the p-JFET to the gate region in the n-JFET) or n-i-n (the source region in the n-JFET to the gate region in the p-JFET) structures exist (see Fig. 1b,c). Since the resistivity of semi-insulating region decreases with increasing the temperature, such parasitic p-i-p or n-i-n structure may contribute to the gate leakage current. In this study, we have not fabricated a metal interconnect layer and the gate region had to be large enough to make the side gate structure, leading to an increase in the area of the parasitic p-i-p or n-i-n structure. Such leakage current is likely suppressed by shrinking the area of the parasitic p-i-p or n-i-n structure or fabricating p- or n-well structure like conventional CMOS circuits.

The VTCs in the CJFET inverter within the temperature range between RT and 573 K are presented in Fig. 2c. The $V_{th}$ shift from RT to 573 K is about 0.2V. The output voltage with the low input voltage (0 V) at 573 K is slightly lower than the $V_{dd}$ (1.4 V), which is ascribed to the gate leakage current discussed above. The through current subtracting the gate leakage current from RT to 573 K is shown in Fig. 2d. With elevating the temperature, the absolute values of $V_{Tp}$ and $V_{Tn}$ become smaller, leading to expansion of the voltage range where the through current flows and the higher peak current at higher temperature. Nevertheless, the highest through current is limited as small as about 50 nA. The static current at the input voltage of low (0 V) and high (1.4 V) is negligibly small (< 0.1 nA) at up to the temperature of 473 K, indicating the extremely low static power dissipation. At 573 K, small through current is observed with the input voltage of 0 V even after subtracting the gate leakage current. From the source region of the p-JFET to the source region of the n-JFET, parasitic p-i-n diode exists and the diode was forward biased by applying $V_{dd}$. Then, small current flew through the parasitic p-i-n diode since the built-in potential
of the p-i-n diode was also lowered by elevating the temperature, which can also be prevented by changing the device layout as discussed in the gate leakage current.

The temperature dependencies of low and high noise margins ($NM_L$ and $NM_H$) of the CJFET inverter are shown in Fig. 2c. Definition of $NM_L$ and $NM_H$ is given in Supplementary Note 1. Both of the $NM_L$ and $NM_H$ in the fabricated CJFET become smaller with elevating the temperature since the voltage range in the transition region becomes wider (see Fig. 2c). $NM_L$ at 573 K (0.2 V) still remains much higher than the thermal voltage (0.049 eV), which avoids unintentional transition due to the thermal noise. The dashed and dotted lines denote the $NM_L$ and $NM_H$ extracted from the analytical model (Supplementary Note 1). These curves agree well with the experimental results up to about 423 K and gradually deviate with elevating the temperature. Here, the subthreshold current of JFETs were not considered in the analytical model and non-ideal leakage current also flew as discussed above, resulting in the wider transition region and smaller $V_{OH}$ in the fabricated CJFET inverter (see Supplementary Fig. 2). Nevertheless, $V_{th}$ extracted from the analytical model shows an excellent agreement with the experimental results within the measurement temperature range since the transition region does not affect much on the values of $V_{th}$.

**Dynamic characteristics**

Fig. 3a,b present dynamic characteristics of the CJFET inverter at RT and 573 K, respectively. As demonstrated in the static characteristics (Fig. 2), the output voltage level with $V_{in}$ of 0 V at RT is
equal to the $V_{dd}$ (1.4 V) and slight lowering is observed at 573 K. When focusing on the rise and fall times ($t_r$ and $t_f$) of the output level (defined as a time interval from 0% or 100% to 50% level), the $t_f$ is much shorter than the $t_r$ since the drain current of the n-JFET (directly related to its $t_f$) is larger than that of the p-JFET (its $t_r$). The $t_r$ and $t_f$ clearly depend on the temperature, which are plotted in Fig. 3c. The monotonous decrease in the $t_r$ with elevating the temperature is caused by the increased drain current in the p-JFET, due to the higher ionization ratio of aluminum acceptors and driving voltage enhancement by the $V_{Tp}$ shift. On the other hand, the $t_f$ remains almost constant up to 423 K and gradually increases with temperature, which is attributed to competition between electron mobility lowering and higher driving voltage due to the $V_{Tn}$ shift.

The $t_r$ and $t_f$ were calculated based on the analytical model (Supplementary Note 1). Assuming that each JFET is biased under the saturation region within the time from 0% or 100% to 50% output level, the $t_r$ and $t_f$ are expressed as the following formulae,

\[
\begin{align*}
    t_r &= \frac{CV_{\text{out-high}}}{2I_{dp}}, \\
    t_f &= \frac{CV_{\text{out-high}}}{2I_{dn}},
\end{align*}
\]

where $C$ is the load capacitance and $I_{dp}$ and $I_{dn}$ are the drain current of the p- and n-JFETs, respectively. The $V_{\text{out-high}}$ corresponds to the $V_{\text{out}}$ with $V_{\text{in}}$ of 0 V (100% output level). The $t_r$ and $t_f$ were extracted from the Eqs. (1) and (2), which are depicted as the solid and dashed lines in Fig. 3c, respectively. The $V_{\text{out-high}}$ in Eqs. (1) and (2) is assumed to be $V_{dd}$ in the whole temperature range. We assembled a voltage follower circuit to measure the dynamic characteristics (see Measurement section) and $C$ is regarded as a fitting parameter, resulting in $C = 38 \text{ pF}$. The
curves show a good agreement with the experiments. The slight deviation between the calculation and experiments in $t_r$ may be attributed to inaccuracy of the reported hole mobility in the p-JFET and unintentional voltage drop due to the leakage current discussed above. Note that the long $t_r$ and $t_f$ originate from the small channel width, which can be improved by changing the device design such as a multi-channel structure.

Figures 4a-c depict a CJFET NOR circuit. As in the same as a CJFET inverter, a CJFET NOR circuit can be assembled in a replacement of MOSFETs in a CMOS circuit by JFETs. Two input operations of the CJFET NOR circuit at RT and 573 K with $V_{dd}$ of 1.4 V are demonstrated in Fig. 4d.e. Rail-to-rail (0–1.4 V) operation at RT and slight drop in $V_{out}$ with $V_1$ and $V_2$ of 0 V at 573 K are confirmed, which are the same as can be seen in the CJFET inverter operation.

Here, we compare and discuss the characteristics of the reported high-temperature logic gates, which are listed in Table 1. The SiC bipolar junction transistor (BJT) logic gates can operate with a single power supply and operation at higher than 500 °C has been reported. The SiC JFET-R logic gates also show high-temperature operation at higher than 800 °C. Moreover, year-long stable operation of the JFET-R logic gates at 500 °C has been achieved, which is of importance for the systems that cannot easily be repaired. However, BJTs are current-controlled devices and the JFET-R logic gates use depletion-mode n-JFETs, leading to high static power consumption. On the other hand, the SiC CMOS logic gates show much smaller power consumption owing to complementary operation. However, high-density defects at the SiO$_2$/SiC interface make it difficult to control threshold voltages of p- and n-MOSFETs within a wide temperature range,
requiring high $V_{dd}$ (typically $\geq 15$ V). Moreover, the temperature dependence of drain current in SiC p- and n-MOSFETs strongly depend on each fabrication process and it is rather difficult to develop a universally applicable analytical model for SiC MOSFETs, which is necessary for circuit simulations. Although the Si CMOS on SOI is well developed and already commercialized, its operational temperature is limited by the material properties of Si. The SiC CJFET logic gates fabricated in this study work with a small and single power supply (1.4 V), leading to very small power consumption. Since the SiC JFET-R logic gates demonstrate very high reliability, the SiC CJFET logic gates are also expected to be highly reliable, which should be tested in the future study. Higher-temperature operation of SiC CJFET circuits is expected by improving the CJFET logic gate design. The separately fabricated JFETs in our previous study show stable operation at 400 °C,[21] meaning that the SiC CJFET can also operate at higher than 400 °C.

Gallium nitride (GaN) is another attractive wide bandgap semiconductor and a heterostructure of aluminum gallium nitride (AlGaN) and GaN makes two-dimensional electron gas (2DEG) at the interface, which is used as an n-channel in high electron mobility transistors (HEMTs). Since p-type GaN formation by ion implantation is technologically difficult, logic circuits are basically composed of n-channel HEMTs. $V_{th}$ of AlGaN/GaN HEMTs can be modified by etching of AlGaN or re-growth of p-GaN under the gate region, which allows us to make depletion- and enhancement-mode HEMTs on the same substrate and assemble direct-coupled FET logic (DCFL) circuits. Although 200-300 °C operation of GaN DCFL circuits are reported,[27][29] several issues should be addressed for higher temperature operation, such as leakage current from 2DEG to gate electrode, controllability and uniformity of $V_{th}$, and device modeling including temperature de-
pendencies. Recently, several groups have reported fabrication of GaN p-channel FETs without ion implantation and assemble complementary integrated circuits\textsuperscript{30–32} which dramatically reduces power consumption compared to GaN DCFL circuits, although the same issues of GaN DCFL circuits have to be solved for high-temperature operation.

**Conclusion**

SiC CJFET logic gates were fabricated by ion implantation and inverter and NOR operations were demonstrated in a wide temperature range from RT to 573 K with a single and low supply voltage of 1.4 V. The static characteristics, or $V_{th}$, $NM_L$, and $NM_H$, and dynamic characteristics, or $t_r$ and $t_f$, were well explained by a simple analytical model, which indicates that electronic circuit simulation on SiC CJFETs can predict actual circuit operation. In a similar manner of prosperity in the Si CMOS technology, SiC CJFET technology is widely applicable to digital and analog circuits and memories operating at high temperature with small power consumption.

**Methods**

**Sample preparation.** A 4°-off-axis high-purity semi-insulating 4H-SiC(0001) substrate grown by high-temperature chemical vapor deposition was used as a starting material. All the n-type and p-type regions were formed by ion implantation of phosphorus and aluminum, respectively. A device-isolation process such as mesa etching was not performed in this study. Silicon dioxide ($SiO_2$) with a thickness of 2-3 $\mu$m was deposited as an ion implantation mask. Patterning of the $SiO_2$ mask was performed using photolithography and dry etching. The high-dose regions (n+...
and p⁺) and low-dose regions (n and p) were implanted at 300 °C and room temperature (RT), respectively. The implantation conditions are summarized in Supplementary Table 1. The doping concentration of the gate and channel regions were $5 \times 10^{19}$ and $5 \times 10^{16}$ cm⁻³, respectively, which were confirmed by secondary ion mass spectrometry. After the ion implantation, activation annealing was conducted at 1650 °C for 10 min. Ti/Al and Ni were thermally evaporated as ohmic contacts for p- and n-type regions, respectively. 1-μm-thick Al was finally deposited as metal pads. A detailed device layout is shown in Fig. 1b.

**Measurements.** All the measurements were performed under vacuum condition using a probe station with a temperature controller stage (MJ-10-P6K, APPLOO WAVE). The sample temperature was monitored with a thermocouple sensor located close to the sample. The static characteristics were obtained with a Keithley 4200A semiconductor parameter analyzer. The input signal for the dynamic characteristics was generated by a signal generator (81160A, Agilent Technologies). Due to the high output impedance of the CJFET logic gates in this study, a voltage follower circuit assembled with an op-amp (LT1793, Linear Technology) was connected to the output of the CJFET logic gates. Then, an oscilloscope (DSO9254A, Agilent Technologies) was used to obtain the output signals.

**Data availability.** The data within this paper are available from the corresponding author upon reasonable request.
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**Author contributions**  T.K. supervised the entire project with M.K. M.N. designed the devices with M.K. M.N. fabricated the sample with Q.J. and M.K. M.K. performed the experiments and analyzed the data with M.N. M.K. wrote the manuscript with T.K. All authors discussed the results and contributed to the manuscript.

**Competing Interests**  The authors declare that they have no competing financial interests.

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Figure 1: CJFET inverter. a, A CJFET inverter circuit diagram. b, The layout design of the CJFET inverter. c, An optical image of the fabricated CJFET inverter. The inset shows the magnified image of the n-JFET. d, The transfer characteristics of the p- and n-JFETs and the VTC at room temperature.
Figure 2: Static characteristics of the CJFET inverter. **a,b**, The transfer characteristics of the p- and n-JFETs from RT to 573 K in linear (a) and logarithmic (b) scales. **c,d**, The temperature dependence of the VTC (c) and through current (d). The gate leakage current is subtracted from the through current. **e**, The temperature dependence of the $V_{th}$, $NM_L$, and $NM_H$. The symbols denote the experimental data. Error bars mean the voltage step in the measurements. The solid, dashed, and dotted lines are the $V_{th}$, $NM_L$, and $NM_H$ extracted from the analytical model.
Figure 3: **Dynamic characteristics of the CJFET inverter.** a,b, Input voltage and output of the CJFET inverter at RT (a) and 573 K (b). c, The temperature dependence of $t_r$ and $t_f$. The symbols denote the experimental data. Error bars represent noise height in oscilloscope. The solid and dashed lines are $t_r$ and $t_f$ obtained from the analytical model assuming a load capacitance of 38 pF.
Figure 4: **CJFET NOR operation.** a, A CJFET NOR circuit diagram. b, The layout design of the CJFET NOR logic gate. c, An optical image of the fabricated CJFET NOR logic gate. d,e, Input voltages and output of the CJFET NOR gate at RT (d) and 573 K (e).
Table 1: Comparison of the high-temperature logic gates.

| Gate Type               | $V_{dd}$ | $V_{ss}$ | $V_{th}$ shift | Power consumption | Reliability        | $T$ (demonstrated) |
|--------------------------|----------|----------|----------------|-------------------|---------------------|--------------------|
| SiC BJT                  | $\geq 15$ V | GND | small           | high              | high                | $\geq 500$ °C      |
| SiC JFET-R               | $\geq 25$ V | $\leq -25$ V | small         | high              | very high           | $\geq 800$ °C      |
| SiC CMOS                 | $\geq 15$ V | GND | medium          | low               | SiO₂-limited        | $\geq 400$ °C      |
| Si CMOS on SOI           | $1-5$ V   | GND | small           | very low          | SiO₂-limited        | $\leq 300$ °C      |
| GaN DCFL                 | $\geq 3$ V | GND | medium          | high              | –                   | $\leq 350$ °C      |
| SiC CJFET (this study)   | $\leq 2$ V | GND | small           | very low          | high (expected)     | $300$ °C           |
Supplementary Note 1

An analytical model used in this paper to describe electrical characteristics of SiC p- and n-JFETs is introduced. Drain current of p- and n-JFETs ($I_{dp}$ and $I_{dn}$) with threshold voltages of $V_{Tp}$ and $V_{Tn}$ for uniformly doped p- and n-channel regions is presented as the following formulae under gradual-channel approximation:

$$I_{dp} = \begin{cases} 
0 & (V_{gp} < V_{Tn}) \\
-G_{ip} \left[ |V_{dp}| - \frac{2}{3} \psi_{pp} \left\{ \left( \frac{\psi_{jp}-|V_{gp}-V_{dn}|}{\psi_{pp}} \right)^{1.5} - \left( \frac{\psi_{jn}-|V_{gn}|}{\psi_{pp}} \right)^{1.5} \right\} \right] & (V_{gp} > V_{Tp}, V_{dp} < V_{gp} - V_{Tp}) \\
-G_{ip} \left[ \frac{\psi_{pp}}{3} - (\psi_{jp} - |V_{gp}|) \left( 1 - \frac{2}{3} \sqrt{\frac{\psi_{jp}-|V_{dp}|}{\psi_{pp}}} \right) \right] & (V_{gp} > V_{Tp}, V_{dp} > V_{gp} - V_{Tp})
\end{cases}$$  

(S1)

$$I_{dn} = \begin{cases} 
0 & (V_{gn} < V_{Tn}) \\
G_{in} \left[ V_{dn} - \frac{2}{3} \psi_{pn} \left\{ \left( \frac{\psi_{jn}-V_{gn}+V_{dn}}{\psi_{pn}} \right)^{1.5} - \left( \frac{\psi_{jn}-V_{gn}}{\psi_{pn}} \right)^{1.5} \right\} \right] & (V_{gn} > V_{Tn}, V_{dn} < V_{gn} - V_{Tn}) \\
G_{in} \left[ \frac{\psi_{pn}}{3} - (\psi_{jn} - V_{gn}) \left( 1 - \frac{2}{3} \sqrt{\frac{\psi_{jn}-V_{gn}}{\psi_{pn}}} \right) \right] & (V_{gn} > V_{Tn}, V_{dn} > V_{gn} - V_{Tn})
\end{cases}$$  

(S2)

where $\psi_{jp}$ ($\psi_{jn}$) is the built-in potential of the p-n junction between the gate and channel region in a p-JFET (n-JFET). $\psi_{pp}$ ($\psi_{pn}$) is the pinch-off potential of a p-JFET (n-JFET). $G_{ip}$ and $G_{in}$ are expressed with the following formulae, $G_{ip} = \frac{qW_p\mu_pp_a}{L_p}$ and $G_{in} = \frac{qW_n\mu_n n_a}{L_n}$. $q$ is the elementary charge. $W_p$ ($W_n$), $L_p$ ($L_n$), and $a_p$ ($a_n$) are the channel width, length and thickness of a p-JFET (n-
JFET), respectively. \(\mu_p (\mu_n)\) and \(p_p (n_n)\) are the hole (electron) mobility and density in the channel region.

Voltage transfer characteristics (VTCs) of a SiC CJFET inverter were calculated using Eqs. (S1) and (S2). As indicated in the inverter circuit diagram (Fig. 1), the supply voltage \((V_{dd})\) and input voltage \((V_{in})\) are substituted for \(V_{gp}\) and \(V_{gn}\) as following, \(V_{gp} = V_{in} - V_{dd}\) and \(V_{gn} = V_{in}\). Then, \(V_{out}\) is determined as the \(V_{dp} (= V_{dn})\) where \(I_{dp} = I_{dn}\). For the calculation of Eqs. (S1) and (S2), material properties of 4H-SiC are used, which are obtained from epitaxially grown p- and n-type epilayers.

Next, \(V_{th}, NM_L,\) and \(NM_H\) are calculated. Eqs. (S1) and (S2) are approximated with the following functions when the gate voltage is close to the threshold voltage of JFETs,

\[
I_{dp} = \begin{cases} 
0 & (V_{gp} < V_{Tn}) \\
\frac{G_{ip}}{2\psi_{pp}} (V_{gp} - V_{Tn}) V_{dp} & (V_{gn} > V_{Tn}, V_{dn} < V_{gn} - V_{Tn}) \\
\frac{G_{ip}}{4\psi_{pp}} (V_{gp} - V_{Tn})^2 & (V_{gp} > V_{Tp}, V_{dp} > V_{gp} - V_{Tp})
\end{cases} \tag{S3}
\]

\[
I_{dn} = \begin{cases} 
0 & (V_{gn} < V_{Tn}) \\
\frac{G_{in}}{2\psi_{pn}} (V_{gn} - V_{Tn}) V_{dn} & (V_{gn} > V_{Tn}, V_{dn} < V_{gn} - V_{Tn}) \\
\frac{G_{in}}{4\psi_{pn}} (V_{gn} - V_{Tn})^2 & (V_{gn} > V_{Tn}, V_{dn} > V_{gn} - V_{Tn})
\end{cases} \tag{S4}
\]
When a CJFET inverter reaches $V_{th}$, both of the p- and n-JFETs operate under saturation regions. Therefore, $V_{th}$ corresponds to $V_{in}$ which satisfies the following equation,

\[
\frac{G_{ip}}{4\psi_{pp}} (V_{in} - V_{dd} - V_{Tp})^2 = \frac{G_{in}}{4\psi_{pn}} (V_{in} - V_{Tn})^2,
\]

leading to

\[
V_{th} = \frac{V_{dd} + V_{Tp} + \sqrt{\beta_R}V_{Tn}}{1 + \sqrt{\beta_R}},
\]

where $\beta_R$ is defined as $\beta_R = \frac{G_{in}\psi_{pn}}{G_{ip}\psi_{pp}}$.

When defining $V_{IL}$ and $V_{OH}$ as $V_{in}$ and $V_{out}$ at $dV_{out}/dV_{in} = -1$ within a transition region in a VTC from the high level to $V_{th}$ and $V_{IH}$ and $V_{OL}$ as $V_{in}$ and $V_{out}$ at $dV_{out}/dV_{in} = -1$ within a transition region in a VTC from $V_{th}$ to the low level, $NM_L$ and $NM_H$ are expressed as the following formulae,

\[
NM_L = V_{IL} - V_{OL},
\]

\[
NM_H = V_{OH} - V_{IH}.
\]

When $V_{in} = V_{IL}$, the p- and n-JFETs work under non-saturation and saturation regions, respectively, where the following function holds,

\[
\frac{G_{ip}}{2\psi_{pp}} (V_{in} - V_{dd} - V_{Tp})(V_{out} - V_{dd}) = \frac{G_{in}}{4\psi_{pn}} (V_{in} - V_{Tn})^2.
\]

By differentiating the above equation and substituting $V_{in} = V_{IL}$ and $\frac{dV_{out}}{dV_{in}} = -1$,

\[
V_{out} - V_{IL} + V_{Tp} = \beta_R (V_{IL} - V_{Tn})
\]
is obtained. \( V_{IL} \) is extracted by solving the Eqs. (S9) and (S10). \( V_{OH} \) is obtained from the calculated VTC at \( V_{\text{in}} = V_{IL} \). \( V_{IH} \) and \( V_{OL} \) can be extracted in a similar manner shown above.
Supplementary Figure 1: **Drain and gate leakage current.** a,b, Temperature dependence of drain and gate current without a gate supply voltage (0 V) in p-JFETs (a) and n-JFETs (b). Data obtained from the separately fabricated p- and n-JFET reported in ref. 2 are shown.
Supplementary Figure 2: **VTCs obtained from experiments and the analytical model.** a-d, VTCs obtained from experiments (solid lines) and the analytical model (dashed lines) at RT (a), 373 K (b), 473 K (c), and 573 K (d).
Supplementary Table 1: Ion implantation conditions performed in this study for forming n⁺, p⁺, n, and p regions. The ion implantation was performed with the sample temperature of 300°C for n⁺ and p⁺ regions and RT for n and p regions.

(a) n⁺ region

| Energy [keV] | Dose [cm⁻²] |
|--------------|--------------|
| 10           | 2.50 × 10¹³  |
| 20           | 3.50 × 10¹³  |
| 35           | 8.00 × 10¹³  |
| 55           | 4.50 × 10¹³  |
| 75           | 1.50 × 10¹⁴  |
| 100          | 6.00 × 10¹³  |
| 130          | 2.00 × 10¹⁴  |
| 180          | 1.60 × 10¹⁴  |
| 220          | 1.75 × 10¹⁴  |
| 270          | 2.75 × 10¹⁴  |
| 360          | 3.50 × 10¹⁴  |
| 430          | 2.00 × 10¹⁴  |
| 520          | 4.50 × 10¹⁴  |
| 650          | 3.50 × 10¹⁴  |
| 700          | 5.00 × 10¹⁴  |
| **Total dose** | **3.06 × 10¹⁶** |

(b) p⁺ region

| Energy [keV] | Dose [cm⁻²] |
|--------------|--------------|
| 10           | 2.40 × 10¹³  |
| 15           | 1.00 × 10¹³  |
| 20           | 3.30 × 10¹³  |
| 25           | 3.50 × 10¹³  |
| 40           | 1.00 × 10¹⁴  |
| 50           | 3.00 × 10¹³  |
| 70           | 1.00 × 10¹⁴  |
| 80           | 1.00 × 10¹⁴  |
| 120          | 3.00 × 10¹⁴  |
| 170          | 1.80 × 10¹⁴  |
| 200          | 1.80 × 10¹⁴  |
| 220          | 2.00 × 10¹⁴  |
| 250          | 7.00 × 10¹³  |
| 310          | 5.00 × 10¹⁴  |
| 390          | 2.50 × 10¹⁴  |
| 450          | 5.00 × 10¹³  |
| 470          | 5.00 × 10¹⁴  |
| 600          | 4.00 × 10¹⁴  |
| 650          | 2.50 × 10¹⁴  |
| 700          | 6.00 × 10¹⁴  |
| **Total dose** | **1.80 × 10¹⁵** |

(c) n region

| Energy [keV] | Dose [cm⁻²] |
|--------------|--------------|
| 270          | 3.30 × 10¹¹  |
| 360          | 2.90 × 10¹¹  |
| 390          | 8.50 × 10¹⁰  |
| 450          | 2.90 × 10¹¹  |
| 550          | 4.20 × 10¹¹  |
| 700          | 7.80 × 10¹¹  |
| **Total dose** | **2.20 × 10¹²** |

(d) p region

| Energy [keV] | Dose [cm⁻²] |
|--------------|--------------|
| 200          | 3.00 × 10¹¹  |
| 270          | 4.10 × 10¹¹  |
| 330          | 1.50 × 10¹¹  |
| 360          | 2.50 × 10¹⁰  |
| 390          | 3.40 × 10¹¹  |
| 430          | 6.00 × 10¹²  |
| **Total dose** | **1.83 × 10¹²** |
Supplementary references

1. Sze, S. M. & Ng, K. K. *Physics of Semiconductor Devices.* (Wiley, 2007).

2. Nakajima, M., Kaneko, M. & Kimoto, T. Normally-off 400 °C Operation of n- and p-JFETs With a Side-Gate Structure Fabricated by Ion Implantation Into a High-Purity Semi-Insulating SiC Substrate, *IEEE Electron Device Lett.* **40**, 866 (2019).