Analysis of gate engineered asymmetric junctionless double gate MOSFET for varying operating conditions

Namrata Mendiratta¹, Suman Lata Tripathi² and Bhanu Prakash Kolla³
1,2School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India
3Department of Computer Science and Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P, India.
E-mail: *tri.suman78@gmail.com

Abstract: In this paper an asymmetrical junctionless double-gate MOSFET (AJDG-MOSFET) has been analyzed using different gate oxide material like $\text{SiO}_2$ and $\text{HfO}_2$ and different gate contact material like aluminium, copper and polysilicon. To check the sensitivity of AJDG-MOSFET, a temperature analysis has been performed at a different temperature ranging 250-400K. The performance of AJDG-MOSFET is analyzed with transfer and output characteristics using 2D/3D simulation on Cogenda TCAD. The device performs better using $\text{HfO}_2$ as gate oxide and polysilicon as gate contact. The ideal subthreshold performance (DIBL=65mV/V, SS=68 mV/decade) is observed with a high value of $I_{ON}/I_{OFF}(10^{12})$ for 300K temperature. The analysis for temperature shows a very small variation in OFF current and found suitable for low power applications.

1. INTRODUCTION

One of the biggest challenges in IC technology is a reduction in the size of the MOSFETs. The importance of scaling is to integrate more number of transistors in a single chip. Scaling the size of the MOSFET produces short channel effects (SCEs) degrading the performance of the MOSFET.[1] Further scaling of MOSFET decreases the size of $\text{SiO}_2$ to few nm, further decreasing of size $\text{SiO}_2$ is not feasible causing leakage current. There is the need of replacing the oxide with high K material having more physical thickness[2].

Channel and gate engineering techniques are used to alter the structure for suppressing short channel effects (SCEs). Double gate MOSFET (DG MOSFET) is one of the examples of gate engineering technology for reducing SCEs. The coupling of the gate to channel is doubled, their gate has better control over the channel in DG MOSFET. OFF-state current leakage is reduced and provides good mobility. It has gates on both sides of the channel region controlling the electric field and providing a better subthreshold slope. Hence, the performance of the device increases. Changing the material of the gate contact from metal contacts to polysilicon also improves the performance of the MOSFET. There are many important applications of MOSFET in various fields like biotechnology as a biosensor for detecting molecules and enzymes, memory application like SRAM cell, low power applications in digital circuits for switching[3-14].

In this paper, asymmetrical junctionless double-gate MOSFET is analyzed by using different gate oxide material, different gate contact material and at different temperatures. Temperature analysis is mainly performed to check the sensitivity of the device at harsh temperature conditions. Gate oxide
material used for analysis are SiO$_2$ and HfO$_2$. Different gate contact materials used for analysis are Aluminium, copper and polysilicon. The performance of the MOSFET is observed at different temperatures.

2. ASYMMETRIC JUNCTIONLESS DOUBLE-GATE MOSFET (AJDG-MOSFET)

Figure 1 represents asymmetric junctionless double-gate MOSFET having two gates unsymmetrical to each other. The doping concentration of source, drain and channel is equal. The channel length is determined by the ON and OFF state of the MOSFET. Throughout the ON state of the MOSFET, the channel length is equal to the overlapping region between the two unsymmetrical gates. During its OFF state, the channel length is the total length of the channel excluding the overlapping region between the gates. This device gives better performance than conventional double gate MOSFET[15]. Table 1 shows the dimensions of the AJDG-MOSFET. Gate length ($L_{gate}$) is 20 nm, channel length is 30 nm, overlap region is 10 nm, channel doping is $1 \times 10^{19} \text{cm}^{-3}$ and thickness of silicon ($T_{\text{silicon}}$) is 6 nm.

| Region                             | Dimension      |
|-----------------------------------|----------------|
| Gate length                       | 20 nm          |
| Total Channel length              | 30 nm          |
| Overlap region                    | 10 nm          |
| Drain/source and channel doping    | $1 \times 10^{19} \text{cm}^{-3}$ |
| Thickness of silicon              | 6 nm           |

Figure 1: Structure of asymmetrical junctionless double-gate MOSFET

3. GRAPHICAL ANALYSIS OF MOSFET WITH A DIFFERENT GATE OXIDE AND GATE CONTACT MATERIALS

The design of AJDG-MOSFET has been carried out on 2D/3D Visual TCAD device simulator. The suitable range of gate and drain voltage is of 1-2V for transistor analysis. Figure 2 shows the performance of the MOSFET when the material of gate oxide is used. Two different insulators used are SiO$_2$ and HfO$_2$. It is observed from the graph that when HfO$_2$ is used as the gate oxide, the device performance increases. Using SiO$_2$ as gate oxide forms kink effect in the OFF state region of MOSFET, therefore increasing the OFF-state current and degrading the performance of the device.
Reduction in the size of the MOSFET leads to the scaling down of the gate oxide layer SiO$_2$ that gives rise to polysilicon gate depletion, penetration of gate dopant into the channel and increase in gate leakage current. Using high K oxide like HfO$_2$ leads to an increase in film thickness reducing the gate leakage current as it has more energy bandgap and better thermal stability compared to SiO$_2$ [2].

Figure 2. Graph of drain current with respect to gate voltage for different gate oxide material.

Figure 3. Graph of drain current with respect to gate voltage for different gate contact material.

Figure 3 shows the performance of MOSFET when different gate contacts are used like aluminium, polysilicon and copper. MOSFET shows better performance when polysilicon is used as a gate contact. Metal gates like Aluminium and copper operate at voltages 3V to 5V. The lowering of operating voltages leads to the use of polysilicon gate contact. From the graph we can observe at lower operating voltages polysilicon gate contact gives better performance because the OFF-state current is low. Whereas the OFF-state current of MOSFET with copper and aluminium contact is very high that degrades its performance. The MOSFET shown in this paper is operated at 1V. Other reasons for using polysilicon contact are during the process of fabrication the metal contact like Al and Cu forms misalignment which gives rise to parasitic capacitances and the doping process requires high-temperature annealing process which will melt Al and Cu. The polysilicon does not melt at high temperatures and provides a solution for misalignment by using the self-alignment process [12]. Performance of the asymmetrical junctionless double-gate MOSFET is better than conventional
double-gate MOSFET. Short channel effects like DIBL, subthreshold slope are significantly suppressed. The OFF-state current is reduced and ON-state current is increased, therefore increasing the performance of the asymmetrical junctionless double-gate MOSFET. Table 2 shows the comparison of performance parameter between Asymmetrical double gate junctionless MOSFET and Double gate MOSFET. The value of DIBL, SS and $I_{ON}/I_{OFF}$ ratio is given in table 2. From the table it can be seen that DIBL and SS value i.e. the SCEs of AJDG-MOSFET is lower than DG MOSFET and $I_{ON}/I_{OFF}$ ratio is high for AJDG MOSFET, therefore the performance of AJDG-MOSFET is better than DG MOSFET.

Table 2. Comparison of performance of Asymmetrical double gate junctionless MOSFET and Double gate MOSFET

| Device structure                      | $I_{ON}/I_{OFF}$ | DIBL     | SS       |
|--------------------------------------|------------------|----------|----------|
| Asymmetrical double gate junctionless MOSFET | $1.27 \times 10^{12}$ | 65 mV/V  | 68 mV/dec |
| Double gate MOSFET                   | $4.03 \times 10^{9}$   | 63.34 mV/dec | 79.58 mV/V |

Figure 4. Graph of drain current versus gate voltage at different temperatures

Figure 4 shows the variation of drain current with respect to gate voltage at different temperatures. The temperatures considered are 250K, 300 K, 350K, 400K. With an increase in temperature the OFF-state current increases and ON-state current remains almost the same. $I_{ON}/I_{OFF}$ ratio decreases with increases in temperature, therefore deteriorating the performance of the device. On increasing the temperature, the leakage current increases due to two factors that is current produced due to thermal generation and current produced due to impact ionization(i.e phenomena of a large amount of formation of electron-hole pairs which leak out of depletion region producing current). At high temperatures, the mobility of charge carriers also reduces, therefore, reducing the drain current[15].
Figure 5 shows the graph drain current with respect to drain voltage keeping the gate voltage constant at 0.55V, 0.60V, 0.61V, 0.62V, 0.63V, 0.64V and 0.66V. At the OFF state region of the MOSFET when the threshold voltage is zero, no drain current flows. When the drain voltage increases the drain current starts flowing and becomes constant as represented by horizontal lines[13]. It can be observed from the graph that with a large change in the drain voltage, the variation in drain current is very small, which indicates that the gate has more control over the channel and also has a high output impedance that is suitable for the ideal transistor amplifier circuit.

4. CONCLUSION

AJDG-MOSFET was designed to have shown improved subthreshold performance in low voltage region of operation with $I_{ON}/I_{OFF}$ of $10^{12}$, subthreshold slope of 68 mV/decade and DIBL of 65mV/V. Analysis of the device is performed using different gate oxide material like SiO$_2$ and HfO$_2$ and different gate contact material like aluminum, copper and polysilicon. The device performs better when high K dielectric material such as HfO$_2$ is used. Using polysilicon as gate contact enhances the performance compared to metal contacts like aluminum and copper. The temperature analysis performed showed that the devices work better at 300K. The short channel effects are less in ALDG-MOSFET when compared to DG MOSFET.

REFERENCES

[1]. Srivastava V M, Yadav K S and Singh G 2012 Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch Microelectronics Journal43 873.
[2]. Robertson J 2004 High dielectric constant oxides The European Physical Journal Applied physics28 265.
[3]. Ajay, Narang R, Saxena M, Gupta 2017 Modeling of gate underlap junctionless double gate MOSFET as bio-sensor Materials Science in Semiconductor Processing71 240.
[4]. Ajay, Narang R, Saxena M and Gupta M 2015 Investigation of dielectric modulated (DM) double gate (DG) junctionless MOSFETs for application as a biosensors Superlattices and Microstructures85 557.
[5]. Mishra V K and Chauhan R K 2018 Efficient Layout Design of Junctionless Transistor Based 6-TSRAM Cell Using SOI Technology ECS Journal of Solid State Science and Technology9456.
[6]. Radamson H H 2018 CMOS Past, Present and Future Woodhead Publishing Series in Electronic and Optical Materials 1.
[7]. Buvaneswari B and Balamurugan, N B 2019 2D analytical modeling and simulation of dual material DG MOSFET for biosensing application AEU - International Journal of Electronics and Communications 99 193.

[8]. Colinge J P 2007 Multi-gate SOI MOSFETs Microelectronic Engineering 84 2071.

[9]. Gili E, Kunz V D, Groot C H D, Uchino T, Ashburn P, Donaghy D C, Hall S, Wang Y and Hemment P L F 2004 Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance Solid-State Electronics 48 511.

[10]. Verma J H K, Pratap Y, Haldar S, Gupta R S and Gupta M 2015 Capacitance Modeling of Gate Material Engineered Cylindrical/Surrounded Gate MOSFETs for Sensor Applications Superlattices and Microstructures 88 271.

[11]. Wang Y, Tang Y and Sun L, Cao F 2016 High performance of junctionless MOSFET with asymmetric gate Superlattices and Microstructures 97 8.

[12]. Yeo Y C 2004 Metal gate technology for nanoscale transistors—material selection and process integration issues Thin Solid Films 462 34.

[13]. Kumari V, Saxena M, Gupta R S and Gupta M 2012 Two dimensional analytical Drain current model for Double Gate MOSFET incorporating Dielectric Pocket IEEE Transaction on Electron. Devices 59 2567.

[14]. Mendiratta N and Tripathi S L 2020 A review on performance comparison of advanced MOSFET structures below 45 nm technology node J. Semicond. 41 14.

[15]. Kumari V, Saxena M, Gupta R S, Gupta M 2012 Temperature Dependent Model for Dielectric Pocket Double Gate (DPDG) MOSFET: A Novel Device Architecture International Conference on Emerging Electronics (ICEE) 1 4.