Microsecond non-melt UV laser annealing for future 3D-stacked CMOS

Toshiyuki Tabata1, Fabien Rozé1, Louis Thuries1, Sebastien Halty1, Pierre-Edouard Raynal1, Karim Huet1, Fulvio Mazzamuto1, Abhijet Joshi2, Bülent M. Basol2, Pablo Acosta Alba3, and Sébastien Kerdilès3

1Laser Systems & Solutions of Europe (LASSE), 145 Rue Des Caboëufs, 92230 Génnevilliers, France
2Active Layer Parametrics (ALP), 5500 Butler Lane, Scotts Valley, 95066 California, United States of America
3Université Grenoble Alpes, CEA-Leti, 17 Rue Des Martyrs, 38054 Grenoble, France

E-mail: toshiyuki.tabata@screen-lasse.com

Received April 8, 2022; revised May 3, 2022; accepted May 9, 2022; published online May 18, 2022

Three-dimensional (3D) CMOS technology encourages the use of UV laser annealing (UV-LA) because the shallow absorption of UV light into materials and the process timescale typically from nanoseconds (ns) to microseconds (μs) strongly limit the vertical heat diffusion. In this work, μs UV-LA solid phase epitaxial regrowth demonstrated an active carrier concentration surpassing \(1 \times 10^{21}\) cm\(^{-3}\) in an arsenic ion-implanted silicon-on-insulator substrate. After the subsequent ns UV-LA known for improving CMOS interconnect, only a slight (\(\sim 5\%\)) sheet resistance increase was observed. The results open a possibility to integrate UV-LA at different stages of 3D-stacked CMOS.

© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

Three-dimensional (3D) CMOS technology encourages the use of UV laser annealing (UV-LA) because the shallow absorption of UV light into semiconductor materials and the process timescale typically from nanoseconds (ns) to microseconds (μs) strongly limit the vertical heat diffusion. In this work, μs UV-LA solid phase epitaxial regrowth demonstrated an active carrier concentration surpassing \(1 \times 10^{21}\) cm\(^{-3}\) in an arsenic ion-implanted silicon-on-insulator substrate. After the subsequent ns UV-LA known for improving CMOS interconnect, only a slight (\(\sim 5\%\)) sheet resistance increase was observed. The results open a possibility to integrate UV-LA at different stages of 3D-stacked CMOS.

© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

Three-dimensional (3D) CMOS technology encourages the use of UV laser annealing (UV-LA) because the shallow absorption of UV light into semiconductor materials and the process timescale typically from nanoseconds (ns) to microseconds (μs) strongly limit the vertical heat diffusion. In this work, μs UV-LA solid phase epitaxial regrowth demonstrated an active carrier concentration surpassing \(1 \times 10^{21}\) cm\(^{-3}\) in an arsenic ion-implanted silicon-on-insulator substrate. After the subsequent ns UV-LA known for improving CMOS interconnect, only a slight (\(\sim 5\%\)) sheet resistance increase was observed. The results open a possibility to integrate UV-LA at different stages of 3D-stacked CMOS.

© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

Three-dimensional (3D) CMOS technology encourages the use of UV laser annealing (UV-LA) because the shallow absorption of UV light into semiconductor materials and the process timescale typically from nanoseconds (ns) to microseconds (μs) strongly limit the vertical heat diffusion. In this work, μs UV-LA solid phase epitaxial regrowth demonstrated an active carrier concentration surpassing \(1 \times 10^{21}\) cm\(^{-3}\) in an arsenic ion-implanted silicon-on-insulator substrate. After the subsequent ns UV-LA known for improving CMOS interconnect, only a slight (\(\sim 5\%\)) sheet resistance increase was observed. The results open a possibility to integrate UV-LA at different stages of 3D-stacked CMOS.

© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd
square (RMS) value. A self-consistent time-harmonic solution based on the Maxwell equations allowed to simulate the time profile of the temperature ramping-up and cooling-down induced by UV-LA. The dwell time was defined as the “full width at half maximum” of each profile.

Figure 1 shows the simulated μs UV-LA SPER time-temperature profiles. Both Processes A and B have a maximum temperature ($T_{\text{max}}$) close to 1000 °C without exceeding the melting point of a-Si (1420 K in Ref. 34). The absence of oxygen incorporation (i.e. non-melt) and the monocrystalline regrowth were re-confirmed as in Ref. 26 (data not shown). The dwell time is 8.3 μs and 12.7 μs for Processes A and B, respectively. The measured $R_{\text{sq}}$ values were equivalent (107.9 and 109.3 ohm/sq with an error of ±1.5%). Processes A and B gave a greater RMS value (0.18 and 0.20 nm) than the as-implanted surface (0.10 nm), but these are much reduced compared to the previous μs UV-LA SPER (1.5 nm).26

Figure 2 shows the As SIMS profiles taken before and after μs UV-LA SPER. Both Processes A and B introduced As migration towards the surface. The condensation of impurities at the a/c interface during SPER may explain it.35 This As surface migration may be beneficial for lowering the contact resistivity of transistors.13,36 The As chemical concentration at 20 nm depth is $1.25 \times 10^{21}$ at cm$^{-3}$ for Process A, whereas $9.8 \times 10^{20}$ at cm$^{-3}$ for Process B. Their difference is greater than the measurement error (±10%). The slower ramping-up of Process B (~60 °C μs$^{-1}$) than Process A (~80 °C μs$^{-1}$) might have facilitated the dopants to migrate. By contrast, as expected from the process timescale and the diffusion coefficient of As in c-Si (~10$^{-14}$ cm$^2$ s$^{-1}$ at ~1000 °C from Ref. 37), the as-implanted As profiles were maintained in the non-amorphized SOI after Processes A and B. Figure 2 also shows the DHEM profiles taken after μs UV-LA SPER. The $R_{\text{sq}}$ value measured after Processes A and B by the DHEM equipment was 107.7 ohm/sq and 106.4 ohm/sq with an error of less than ±1.0%, respectively. In both cases, the active level in the initial 30 nm thick layer surpassed the As solid solubility in c-Si at ~1000 °C (~$3 \times 10^{20}$ at cm$^{-3}$ in Ref. 24) and became higher than $1 \times 10^{21}$ at cm$^{-3}$ near the surface. The activation ratio calculated from the SIMS and DHEM profiles (excluding the initial few nanometers because of the presence of a native oxide) was ~76% and ~73% for Processes A and B, respectively. The inactive As could be associated with the formation of deep levels (As$_{\text{n}}$V ($n = 2, 3, \text{and} 4$) clusters, where V stands for vacancies in c-Si).38 In the regrown SOI, V might be generated due to the rapid placement of atoms at the moving a/c interface. In the non-amorphized SOI, V should be related to the I/I damage not fully cured during μs UV-LA. Although As$_{\text{n}}$V grows with time39 and certainly rules the As deactivation, discussing its growth mechanism is beyond the scope of this paper.

The thermal stability of the activated As atoms has been assessed, assuming the typical BEOL anneal conditions (100 °C–420 °C for 10 min to 1 h with furnace anneal,40–43 whereas ~1300 °C for ~10$^{-7}$ to ~10$^{-5}$ s with LA).30,43 In Ref. 24 the As deactivation in Si is discussed, starting from an active level (~$1 \times 10^{21}$ at cm$^{-3}$) similar to our μs UV-LA SPER cases. Then, an Arrhenius plot relevant to a 7% loss of sheet concentration is conceived to extract the activation energy of the As deactivation, which is found to be 2.0 eV and smaller than that of the SPER in intrinsic Si (2.7 eV in Ref. 22). Although the studied temperature range is limited between 350 °C and 410 °C, it would be an interesting attempt to extrapolate this Arrhenius plot towards a higher temperature range and plot the typical BEOL annealing conditions together. Figure 3 shows this benchmarking, indicating that...
most of the presented copper (Cu) BEOL anneals would maintain the high As active level, whereas most of the ruthenium (Ru) ones might lead to non-negligible active As loss.

The deactivation anneal (DA) was performed by ns UV-LA. Figure 4 shows the simulated ns UV-LA time-

temperature profiles, where \( T_{\text{max}} \) is \( \sim 1000 \) °C (Process C) or \( \sim 1300 \) °C (Process D) without exceeding the melting point of c-Si (1690 K in Ref. 44). Figure 5 shows the Rsq evolution as a function of the accumulated DA time. SIMS confirmed no As redistribution during ns UV-LA DA (data not shown). The As deactivation is more pronounced with Process C than Process D. The As solid solubility in c-Si can explain it \( [\sim 3 \times 10^{20}] \) at \( 3 \) cm at \( \sim 1000 \) °C, whereas \( \sim 6 \times 10^{20} \) at \( 3 \) cm at \( \sim 1200 \) °C (possibly a bit higher at \( \sim 1300 \) °C).120 However, Processes C and D reach the same Rsq degradation level as the DA time increases. This must be carefully examined, considering a complex system involving the As diffusion assisted by V or interstitials and the formation energy of various clusters such as \( A_{3}V_{n} \), where \( n \) is \( 3 \).

In summary, the \( \mu \)s UV-LA SPER was investigated to activate the As atoms implanted in the SOI layer. Prior to \( \mu \)s UV-LA, the 37 nm thick amorphization was introduced in the 70 nm thick SOI. Two \( \mu \)s UV-LA SPER conditions (Processes A and B) targeting \( T_{\text{max}} \) close to 1000 °C with different dwell times were applied. Both showed the high active carrier concentration surpassing \( 1 \times 10^{21} \) at \( 3 \) nm near the regrown SOI surface, accompanied by the As surface migration, which is beneficial for lowering the contact resistivity of transistors. The thermal stability of these activated As atoms was assessed by the ns UV-LA DA, where \( T_{\text{max}} \) was set at \( \sim 1000 \) °C (Process C) or \( \sim 1300 \) °C (Process D), considering the typical BEOL LA conditions. The maximum Rsq degradation ratio was \( \sim 5\% \) in the studied DA timescale, encouraging UV-LA integration into different stages of a 3D-stacked transistor fabrication flow to boost chip performance further. Although the level of active carrier concentration achieved in this work meets the current requirement of the state-of-the-art CMOS technologies,45,46 the formation of donor-V complexes (e.g. \( A_{3}V_{n} \)) might restrict its additional enhancement. Then, the use of alternative doping elements, especially the chalcogens such as selenium47 and tellurium,48 may provide a solution. Although these elements are knowns as deep-level impurities, their increasing chemical concentration in Si triggers insulator-to-metal transition and allows non-saturating free-electron generation.

Acknowledgments The work covered by LASSE in this paper was supported by the IT2 project. This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 875999. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Austria, Hungary, United Kingdom, Romania, Israel.

**ORCID iDs** Toshiyuki Tabata © https://orcid.org/0000-0003-4923-5663

1) C. Fenouillet-Beranger et al., “New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI,” 2014 Int. Electron Devices Meeting, p. 642DOI: 10.1109/IEDM.2014.7047121.
2) A. Mallik et al., “The impact of sequential-3D integration on semiconductor scaling roadmap,” 2017 Int. Electron Devices Meeting, p. 717DOI: 10.1109/IEDM.2017.8268483.
3) L. Brunet et al., “Breakthroughs in 3D sequential technology,” 2018 Int. Electron Devices Meeting, p. 153DOI: 10.1109/IEDM.2018.8614553.
4) A. Vandooren et al., “First demonstration of 3D stacked Finfets at a 45 nm fin pitch and 110nm gate pitch technology on 300 mm wafers,” 2018 Int. Electron Devices Meeting, p. 149DOI: 10.1109/IEDM.2018.8614654.
5) P.-Y. Hsieh et al., “Monolithic 3D BEOL FinFET switch arrays using location-controlled granu technique in voltage regulator with better FOM

© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

061002-3
than 2D regulators,” 2019 Int. Electron Devices Meeting, p. 46DOI: 10.1109/IEDM19573.2019.8993441.

6) C. Cavalcante et al., “28 nm FDSOI CMOS technology (FEOL and BEOL) thermal stability for 3D Sequential Integration: yield and reliability analysis,” 2020 Symp. on VLSI Technology, TH3.3DOI: 10.1109/VLSITechnology18217.2020.9265075.

7) C. Fenouillet-Beranger et al., “First demonstration of low temperature ($\leq$500 °C) CMOS devices featuring functional RO and SRAM bitcells toward 3D VLSI integration,” 2020 Symp. on VLSI Technology, TH3.4DOI: 10.1109/VLSITechnology18217.2020.9265092.

8) A. Vandooren et al., “3D sequential low temperature top tier devices using dopant activation with excimer laser anneal and strained silicon as performance boosters,” 2020 Symp. on VLSI Technology, TH3.2DOI: 10.1109/VLSITechnology18217.2020.9265026.

9) P. Batude et al., “3D sequential integration: application-driven technological achievements and guidelines,” 2017 Int. Electron Devices Meeting, p. 52DOI: 10.1109/IEDM.2017.8268316.

10) A. Vandooren et al., “Potential benefits of 2D/3D HBB activation by melt laser annealing in 3D-integrated top-tier FDSOI FETs,” 2021 Int. Conf. on Solid State Devices and Materials, A-6–02, p.45.

11) P. Morin et al., “Impact of the buried oxide thickness in UV laser heated 3D stacks,” 2021 Int. Conf. on Solid State Devices and Materials, A-6–03, p.47.

12) L. C. White et al., “Supersaturated alloys, solute trapping, and zone refining,” Laser Annealing of Semiconductors, ed. J. M. Poutte and J. W. Mayer, (Academic, New York, 1982), p.111, Chap. 5.

13) H. Niimi et al., “Sub-10−9 Ω-cm2 n-type contact resistivity for FinFET technology,” IEEE Electron Device Lett. 37, 1371 (2016).

14) T. Tabata et al., “Segregation and activation of Sb implanted in Si by UV nanosecond-laser-anneal-induced non-equilibrium solidification,” J. Appl. Phys. 127, 135701 (2020).

15) H. Shin et al., “Defect reduction and dopant activation of in situ phosphorus-doped silicon on a (111) silicon substrate using nanosecond laser annealing,” Appl. Phys. Express 14, 012001 (2021).

16) T. Tabata et al., “3D simulation for melt laser anneal integration in FinFET’s contact,” IEEE J. Electron Devices Soc. 8, 1123 (2020).

17) H. Wu et al., “Integrated dual SPE processes with low contact resistivity for future CMOS technologies,” 2017 Int. Electron Devices Meeting, p. 545.

18) A. Gai et al., “A study of the mechanism of cw laser annealing of arsenic implanted silicon,” J. Appl. Phys. 50, 2926 (1979).

19) P. Acosta Alba et al., “Solid phase recrystallization induced by multi-pulse nanosecond laser annealing,” Appl. Surf. Sci. Adv. 3, 100053 (2021).

20) A. Lietoila et al., “Solid solubility of As in Si as determined by ion implantation and cw laser annealing,” Appl. Phys. Lett. 35, 532 (1979).

21) S. C. Tsou et al., “Front and back surface cw CO2-laser annealing of arsenic-ion-implanted silicon,” Appl. Phys. 23, 163 (1980).

22) G. L. Olsen et al., “Kinetics of solid phase crystallization in amorphous silicon,” Mater. Sci. Rep. 3, 1 (1988).

23) B. C. Johnson et al., “Dopant effects on solid phase epitaxy in silicon and germanium,” J. Appl. Phys. 111, 034906 (2012).

24) A. Lietoila et al., “The solid solubility and thermal behavior of metastable concentrations of As in Si,” Appl. Phys. Lett. 36, 765 (1980).

25) P. Bado et al., “High efficiency picosecond pulse generation in the 675-930 NM region from a dye laser synchronously pumped by an argon-ion laser,” Technical Report, AD-A128338: TR-15 United States, 1983.

26) T. Tabata et al., “Solid phase recrystallization in arsenic-ion-implanted silicon-on-insulator by microsecond UV laser annealing,” J. Electron Devices Soc..