Design voltage comparator 14-bit for successive approximation analog-to-digital converter

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Abstract- A comparator plays a significant role in the development of an ADC. This paper presents a comparator design aimed to achieve a small offset value at a high resolution by using double tail latch. In this project, the comparator is designed for the purpose of implementation in a 14-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The SAR architecture is the most ideal counter type ADC for implementation in a high-resolution comparator design. The proposed comparator circuit is designed using Silferra C18G 0.18um process, whereby its schematic design and layout simulation is created by employing Synopsys EDA Tools together with transient and Monte Carlo simulations. A double tail regenerative comparator is studied and investigated during this project. The complete simulation results are generated using a 3.3V power supply. The proposed comparator operates at 5MHz clock frequency with a latch offset voltage of 32mV.

1. Introduction

Successive-approximation-register (SAR) analog to digital converters (ADC) are widely used architectures in medium to high-resolution applications with sampling rates under 5MS/s. SAR ADC implements a binary search algorithm [1]. A binary search algorithm is the closest digital code for an input signal. The ADC sampling rate depends on the number of output samples available over a few successive approximation cycles. The SAR ADC itself consists of a comparator, digital-analog converter, and logic. In the application of an SAR ADC, it provides low power consumption and makes the ADC ideal for particular purposes, such as for data acquisition. Comparator is one of the fundamental parts in analog and mixed-signal circuits which can affect the whole ADC's performance [2-4]. Comparator is used to compare an analog signal with a reference voltage and provides a digital output signal based on the comparison. If the voltage difference between the two-input voltage is higher than the threshold voltage, it returns a HIGH output; otherwise, the output is LOW [5], [6]. This concept is depicted in figure 1.

![Figure 1. Block Diagram of Comparator](image-url)
The expression of the output voltage can be derived as shown in the equation (1). The main requirement in designing a comparator is to have a low offset voltage and the ability to sense an input-referred noise that is less than one ADC Least Significant Bit (LSB) in value. Additionally, to reduce the comparator offset, the offset cancellation technique was proposed which further improved the accuracy of the comparator.

\[ V_{out} = \begin{cases} 1, & \text{if } V^+ > V^- \\ 0, & \text{if } V^+ < V^- \end{cases} \]  

(1)

In this paper, a design architecture of a double tail is present that investigates the offset value latch that affecting high-speed comparators [5]. These high-speed comparators can be realized by increasing the size of the tail transistor, but it induces a large current in the circuit which compromises the die area as well as the power. The conversion speed of the comparator is limited by its internal decision-making process. When designed adequately, the comparator is useful in many applications such as zero-crossing detectors, peak detectors, switching power regulators and data transmission. Therefore, a 14-bit SAR ADC with the implementation of offset cancellation is thoroughly discussed in the following sections which will enable the comparator to achieve its prerequisite design standards.

2. System Level

This section will discuss the resolution of ADC from the previous work that may affect the difference in the input voltage. The work in [2] presents the dynamic latch comparator that able to sense the input different voltage of 3.9mV with an 8-bit resolution SAR ADC. The main purpose of this design is to reset and increase the speed of the comparator due to the low-resolution architecture of this ADC having an inherently fast conversion process. Author [7] implements an 11-bit resolution ADC with a power supply of 1.8V. A preamplifier and latch are included in this work which shows an improved characteristic of the comparator in terms of its speed and resolution. The author in [1] proposes the highest resolution design which introduces a 12-bit SAR architecture with a supply voltage of 3.3V. The design comparator is able to sense an input voltage difference of 610uV and produce the desired output based on the detected difference. Table 1 shows the comparison between the minimum detectable input voltage difference (LSB) of this work and that of previous works with different resolutions and power supply values.

| Author | Technology (µm) | Resolution (bit) | Power Supply (V) | LSB (V) |
|--------|-----------------|-----------------|-----------------|--------|
| [2]    | 0.18            | 8               | 1               | 3.9m   |
| [7]    | 0.18            | 11              | 1.8             | 800µ   |
| [1]    | 0.18            | 12              | 3.3             | 610µ   |
| Proposed | 0.18          | 14              | 3.3             | 181µ   |

3. Comparator Design

This section discusses the comparator design that consists of the pre-amplifier and the regenerative latch. For fully differential topology, the resolution of the comparator must be accurate to half of the Least Significant Bit (LSB). The LSB is calculated depending on the resolution of the ADC. In this present work, the value of LSB is 181uV. The comparator produces the output high when the differential input is greater than 32mV and vice versa.
3.1 Double Tail

Double Tail comparator is shown in figure 2 [8]. This topology provides two tails of transistors which in turn provide current separately to differential amplifier and latch circuit. This structure is consists of two stages such as amplification and latch stage with a less stacked transistor. It can use on low voltage applications. It is also possible to employ low tail current in the amplification stage that can increase the offset of comparator. The operation of the double tail is shown in figure 2. During the reset mode, \( \text{clk} = 0 \), and both \( M1 \) and \( M12 \) are off. Transistor \( M8 \) and \( M9 \) are switched on pre-charged output node to \( V_{DD} \). Transistor \( M4 \) and \( M7 \) are discharges the \( \text{outp} \) and \( \text{outn} \) to the ground. When the clock goes high, \( \text{clk} = 1 \), both \( M1 \) and \( M12 \) are on and \( M8 \) and \( M9 \) are off. During this operation, the charges on the \( fn \) and \( fp \) node begin to decrease with the input voltage different. Thus, the charge value of these nodes depends on the input voltage of \( inn \) and \( inp \). The aspect ratio of the double tail circuit is shown in table 2.

![Double Tail Latch](image)

**Figure 2. Double Tail Latch**

| Transistor | \( W(\mu) \) | \( L(\mu) \) |
|------------|--------------|--------------|
| M1         | 1.8          | 0.34         |
| M2&M3      | 1.8          | 0.34         |
| M4&M7      | 1            | 0.34         |
| M5&M6      | 0.6          | 0.34         |
| M8&M9      | 1.8          | 3.4          |
| M10&M11    | 20           | 0.34         |
| M12        | 0.6          | 0.34         |
3.2 Preamplifier

In the comparator, the basic circuit consists of a preamplifier followed by a latch. Preamplifier is chosen in our design as it exhibits good characteristics in realizing a high resolution and ideal performing comparator [9]. The main purpose of the preamplifier circuit is to amplify the input signal feeds it to the input of latch. Preamplifier amplifies the small difference between the input voltage and reference voltage to a level high enough to be detected by the latch. The offset error caused by the unbalanced charge residues and transistor mismatch is the main drawback of the latched comparator. Figures 4 shows a single-stage fully differential amplifier circuit with PMOS cross-coupled load and current mirror as a bias current. The benefit of cross-coupled load is a fast settling time and a better Common-Mode Rejection Ratio (CMRR). The common-mode input voltage is defined by equation (2) with reference to figure 3 [10]. The current mirror is chosen in this design due to the low gain requirement and circuit simplicity. The aspect ratio of the preamplifier circuit is shown in table 3.

\[
V_{\text{in}} = \frac{Vt + V -}{2}
\]  

(2)

Figure 3. Symbol for ideal op-amp
3.3 Offset cancellation

The offset of the preamplifier is higher than the required comparator offset [1]. Output offset cancellation techniques are applied in this work in order to degrade the preamplifier offset. This output cancellation happens during the sampling phase in the SAR ADC operation. Figure 5 demonstrates the offset cancellation process, whereby three preamplifiers are cascaded together. The gain for each preamplifier is labelled as A1, A2, and A3. The offset of the preamplifier is stored in the capacitor with a value of 20µx20µ A. The capacitors are connected in series and labelled as C1, C2, and C3. Three switches in total are needed to cancel the offset voltage. Figure 6 switch is built using an N-channel MOS (NMOS) transistor with the minimum width and length shown in Table 4.

Switches are used for offset cancellation by utilizing the n-channel MOS. Figure 7 shows the switching timing diagram that happens during the sampling process. Switch phi1 opens (turns off) when switching phi2 and switch phi3 are still closed (turned on). The total value of the offset preamplifier that is produced by the preamplifier A1, A2 and A3 are stored in the capacitors c1, c2 and c3 respectively. These switches act as an output cancellation whereby each of them is connected in series with their respective capacitors. In SAR ADC implementation, voltage input (V_in) is connected to the output DAC and phi1, phi2 and phi3 are connected to the common-mode voltage (V_cm).

Table 3. Aspect Ratio of Preamplifier Circuit

| Transistor | W(µ) | L(µ) | Multiplier |
|------------|------|------|------------|
| M0&M1      | 1    | 0.5  | 2          |
| M2&M3      | 1    | 0.5  | 1          |
| M4&M5      | 5    | 1    | 2          |
| M6         | 1    | 5    | 12         |
| M7         | 1    | 5    | 1          |

Table 4. Aspect Ratio of Switch N-Channel MOS.

| Transistor | W(µ) | L(µ) | Multiplier |
|------------|------|------|------------|
| M0         | 12   | 0.34 | 8          |
Figure 5. Offset Cancellation Process

Figure 6. Switch N-Channel MOS.

Figure 7. Switching Timing Diagram.

4. Simulation Result

Simulation is carried out using 0.18um CMOS technology with an operating voltage of 3.3V. The simulation result is obtained by HSPICE. The latch simulation is carried out using the Monte Carlo simulation. From the simulation, the latch offset obtained about 32mV. Therefore, a preamplifier is needed to amplify a 181μV signal in order to get a higher magnitude. An amplifier requires a minimum gain (Av) is given by equation (3). By referring to this equation and assuming that each preamplifier has a 5.6 gain value.

\[ Av = \frac{32mV}{181\mu V} = 176 \]  

(3)
Figure 8 shows the schematic representation of the complete 14-bit SAR ADC design using the proposed comparator to achieve a higher conversion speed. Figure 9 shows the transient simulation response by the latch. The input of the latch is the differential input voltage. The total simulation time is 760ns, whereby 50ns is consumed for each cycle. The transient signal shows the difference between $INP$ and $INN$. Each phase or level of the simulation uses a small step voltage of 1mV. The output signal indicates a trip in the signal at a certain value of the input difference.

![Comparator Circuit](image)

**Figure 8.** Comparator Circuit

![Transient Response](image)

**Figure 9.** Transient Response of the proposed latch.

Figure 10 shows the simulation results of the Monte Carlo simulation. Monte Carlo simulation is implemented using 500 iterations. In this work, a higher iteration in the simulation process will produce the best output latch result. The input offset voltage of the proposed design is 32mV for one conversion cycle. The positive offset value is 32mV while the negative offset value is 0. The latch output produces a high range of offset value. Based on the analysis of this result, the offset voltage of the latch has an output range of 32mV, which produces the same offset compare to the transient simulation. Since the transient simulation is the same as the Monte Carlo simulation, the proposed design is considered as work successfully.
Figure 10. Result of Monte Carlo

The simulation of comparator SAR ADC are simulated by the input signal are toggled with various variation of step value such as big positive to small negative, big negative to small positive, small positive to small negative and small negative to big positive. This simulation covers the typical case values which could happen during the SAR ADC operation. The preamplifier should higher than 32mV before comparing the signal goes high. The output preamplifier in Figure 11 shows that each input signal is toggled and the output complete before the clock signal goes high.

Figure 11. Result of preamplifier

The output of the comparator is shown in Figure 12. The comparator output goes high value when the input is small and big positive differential input. Therefore, for the small and big negative differential input, the comparator gives low output. This simulation done with the 5Mhz of the 200ns period per cycle.

Figure 12. Comparator Output Signal.

5.0 Conclusion

As a conclusion, a new high-resolution comparator for 14-bit SAR ADC with 5MHz clock frequency was proposed and implemented using 0.18um technology. This paper concludes the lower offset of the
double tail latch and pre-amplifier based comparator design. Therefore, by using the output offset cancellation technique, the comparator offset is degrade to less than 181µV. The design comparator consumes of 171µm x 240µm chip size area.

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