Design and DC fault clearance of modified hybrid MMC with low proportion of full-bridge submodules

Yuzhe Xu  |  Zheren Zhang  |  Zheng Xu

Department of Electrical Engineering, Zhejiang University, Hangzhou, Zhejiang Province, China

Correspondence
Zheng Xu, Zhejiang University, Hangzhou, Zhejiang Province, China
Email: xuzheng007@zju.edu.cn

Abstract
The hybrid modular multilevel converter (MMC) consisting of half bridge submodules (HBSMs) and full bridge submodules (FBSMs) combines the respective advantages of both submodules. In order to further reduce the manufacture cost and power loss, this paper proposed a modified hybrid MMC with lower proportion of FBSMs than the conventional hybrid MMC. First, three main conditions for successful DC fault clearing of the hybrid MMC are analysed, which are: (1) Blocking AC fault current; (2) suppression of DC fault current; (3) capacitor voltage under threshold value. Then the topology and the DC fault clearing strategy of the proposed modified hybrid MMC are introduced. Since the installed AC current blocking switches (ACBSs) block the AC current feed during the fault, the number of FBSMs is only limited by third condition. Furthermore, the maximum capacitor voltage after the DC fault is analysed to obtain the minimum required number of FBSMs. Finally, the DC fault responses of the modified hybrid MMC are compared with the conventional hybrid MMC in a three-terminal MMC-HVDC test system in PSCAD/EMTDC. Simulation results demonstrate the effectiveness and feasibility of the proposed modified hybrid MMC.

1 | INTRODUCTION

In recent years, with the development of power electronic technology, the modular multilevel converter based high-voltage direct current (MMC-HVDC) system has drawn great attention from both the industry and academia [1–3]. Due to the advantages of decoupled control of active and reactive powers, no risk of commutation failure and low harmonics, MMC is expected to be widely used in long distance overhead line transmission as an alternative to the line commutated converter (LCC) [4–6]. In addition, MMC is more suitable for multi-terminal HVDC (MTDC) systems than LCC, since the DC power flow can be reversed by changing current direction instead of voltage polarity. Up till now, there have been several multi-terminal MMC-HVDC projects in China, such as the Kunlilong project and the Zhangbei project [7, 8].

However, DC fault clearance is still a major challenge for MMC-HVDC systems. Theoretically, there are mainly three methods to clear DC fault in MMC-HVDC systems.

1. Tripping AC circuit breakers (CBs). In most of the early MMC-HVDC projects, due to economic and technical constraints, DC line faults are cleared by tripping ACCB. This method will take a long time to resume the active power transmission from DC line faults, and will cause transient AC voltage drop, which may influence the stability of the connected AC systems [9]. Therefore, this method is mainly applied in the projects that use cable as DC transmission line, such as offshore wind power transmission projects.

2. Using HVDC circuit breakers. After the first announcement of the hybrid HVDC CB by ABB in 2012 [10], with the maturity of technology, using DCCB has gradually become one of the mainstream DC fault handling methods for MMC based MTDC systems. It is also applied in the Zhangbei four-terminal MMC-HVDC project [8]. The main disadvantage of the DCCB is the high manufacture cost, which will increase geometrically with the increase of DC grid complexity.
3. Adopting MMCs with DC fault blocking capability. By replacing the half bridge submodules (HBSMs) with the submodules with DC fault blocking capability such as full bridge submodules (FBSMs) and clamp double submodules (CDSMs), the DC fault can be cleared by blocking MMC [11–14]. This method is also applied in the Kunlulong three-terminal MMC-HVDC project. The main disadvantage is that all MMC stations need to be blocked during the DC fault, which makes this method not suitable for the large-scale DC grid [15].

For the MTDC systems with small number of terminals, adopting MMCs with DC fault blocking capability is an economical and effective method to deal with DC fault [15]. Among these SMs with DC fault blocking capability, FBSMs can output negative voltage to enable MMC to work under a wider range of DC voltage. However, FBSMs will also increase the manufacturing cost and operation loss of MMC-HVDC since it uses twice as much power electronic devices as HBSMs. In order to reduce the cost while retaining the advantages of FBSMs, the hybrid MMC with mixed HBSMs and FBSMs has been proposed [16–21]. The modulation and capacitor voltage balancing method of the hybrid MMC are discussed in [16]. In [17, 18], the required number of FBSMs in the hybrid MMC is calculated to ensure successful DC fault blocking and capacitor voltage balancing. Ref. [19] studies the precharging process of the hybrid MMC. The transient DC fault ride-through strategies for hybrid MMC without blocking the converter are studied in [19–21].

However, there are mainly two deficiencies in the existed research. The first is that in most of the above studies, the minimum proportion of FBSMs required for successful DC fault blocking or DC fault ride-through is greater than 50%. And there are few researches on how to reduce the required number of FBSMs. The second is that when designing the minimum proportion of FBSMs, it is not included in the condition that the maximum capacitor voltage during fault cannot exceed the threshold value during the fault.

To overcome the aforementioned deficiencies, a modified hybrid MMC consisting of mixed HBSMs and FBSMs is proposed in this paper. By installing AC current blocking switches (ACBSs) in stat connection on the AC side, the proposed modified hybrid MMC can effectively clear DC faults using fewer FBSMs than the conventional hybrid MMC. The capacitor voltage of FBSMs after fault is also analysed in two stages: before and after blocking. Then a calculation method for required FBSMs proportion is proposed and the relationship between the FBSMs proportion and DC line length is analysed. It is found that when the DC line is short, the required FBSMs proportion is much less than 50%, while when the DC line length exceeds a certain value, the required FBSMs proportion will be more than 50%, but still less than that of the conventional hybrid MMC.

To overcome the aforementioned deficiencies, a modified hybrid MMC consisting of mixed HBSMs and FBSMs is proposed in this paper. By installing AC current blocking switches (ACBSs) in stat connection on the AC side, the proposed modified hybrid MMC can effectively clear DC faults using fewer FBSMs than the conventional hybrid MMC. The capacitor voltage of FBSMs after fault is also analysed in two stages: before and after blocking. Then a calculation method for required FBSMs proportion is proposed and the relationship between the FBSMs proportion and DC line length is analysed. It is found that when the DC line is short, the required FBSMs proportion is much less than 50%, while when the DC line length exceeds a certain value, the required FBSMs proportion will be more than 50%, but still less than that of the conventional hybrid MMC.

The outline of this paper is as follows: Section 2 introduces the operation principle and DC fault clearing conditions of the hybrid MMC. Section 3 introduces the topology and DC fault clearing strategy of the proposed modified hybrid MMC. In Section 4, the maximum capacitor voltage during DC fault is estimated by analyzing the equivalent circuit of the modified hybrid MMC before and after blocking. And the minimum required FBSMs proportion is calculated. In Section 5, the fault clearing capability of the modified hybrid MMC is verified in a three-terminal MMC-HVDC test system in PSCAD/EMTDC. The conclusions are given in Section 6.

## 2 | OPERATION PRINCIPLE AND DC FAULT CLEARING CONDITIONS OF HYBRID MMC

Figure 1(a) shows the basic structure of a three-phase hybrid MMC. The converter consists of six arms, each having a series connection of an arm inductor $L_0$ and $N_{total}$ submodules, including $N_{HB}$ HBSMs and $N_{FB}$ FBSMs as shown in Figure 1(b). $U_d$ denotes the dc-bus voltage and $I_d$ denotes the dc line current. The arm voltage and the arm current are $u_{ij}$ ($i$ = p, n denotes the upper and lower arms; $j$ = a, b, c denotes the three phases a, b, c) and $i_{ij}$ respectively. $u_{ij}$ denotes the ac-side phase to ground voltage of phase $j$, $i_{ij}$ denotes the ac-side current.

The blocked FBSMs can provide reverse electromotive forces (EMF) regardless of the current direction to block the current flow. The equivalent circuit of arm in different current direction after blocking can be obtained as shown in Figure 2.
In order to clear the DC fault, the hybrid MMC needs to meet the following three conditions: (1) The AC current feed can be impeded during the fault; (2) the DC-side fault current can reduce to zero after blocking; (3) the capacitor voltage will not exceed the protection threshold value during the DC fault.

For first condition, the hybrid MMC is required to provide sufficient reverse EMF in the AC current feed path. Figure 3 shows two typical AC current feed paths after blocking. And the reverse EMF in both paths should be greater than the peak line-to-line AC voltage during the DC fault [17]. The conditions for blocking path 1 and path 2 can be expressed as Equations (1) and (2) respectively.

\[
2N_{FB}U_{ac} \geq \sqrt{3}U_{in}
\]  

\[
(2N_{FB} + N_{HB})U_{ac} \geq \sqrt{3}U_{in}
\]  

where, \(U_{ac}\) denotes the rated voltage of SM capacitor and \(U_{in}\) denotes the amplitude of \(u_{f}\). According to Equations (1) and (2), the required number of FBSM can be expressed as:

\[
N_{FB} \geq \frac{\sqrt{3}}{4} mN
\]  

where, \(m\) is the ac-side modulation index and can be expressed as:

\[
m = \frac{U_{in}}{U_{dc}/2}
\]  

For second condition, according to the direction of the fault current and the equivalent circuit of arms in Figure 2, the DC side circuit of the hybrid MMC after blocking can be obtained as shown in Figure 4(a). \(R_{dc}\) and \(L_{dc}\) include the resistance and inductance of smoothing reactor and DC line. \(R_{f}\) represents the equivalent resistance in each arm. The DC side circuit of the blocked hybrid MMC can be further simplified to the equivalent circuit shown in Figure 4(b). Assuming that the DC voltage and fault current is \(U_{dcB}\) and \(I_{dcB}\) respectively at MMC blocking moment, the operational circuit of the blocked hybrid MMC can be obtained as shown in Figure 4(b). Then the DC-side fault current can be obtained by solving the operational circuit in Figure 4(b).

\[
I_{dc}(s) = \frac{j\left(I_{dc} + \frac{2L_0}{3}\right)I_{dcB} - U_{dcB}}{s^2\left(\frac{2}{3}L_0 + L_{dc}\right) + j\left(\frac{2}{3}R_0 + R_{dc}\right) + \frac{2N_{FB}}{3C}}
\]  

The Laplace inverse transform of Equation (5) yields:

\[
I_{dc}(t) = \frac{1}{\sin \theta_{dc}}I_{dcB}e^{-\frac{i}{\omega_{dc}}\sin(\omega_{dc}t - \theta_{dc})} - \frac{U_{dcB}}{R_{dis}}e^{-\frac{i}{\omega_{dc}}\sin \omega_{dc}t}
\]  

where,

\[
\theta_{dc} = \arctan(\tau_{dc}\omega_{dc})
\]  

\[
\tau_{dc} = \frac{4L_0 + 6L_{dc}}{2R_0 + 3R_{dc}}
\]  

\[
\omega_{dc} = \sqrt{\frac{8N_{FB}(2L_0 + 3L_{dc}) - C(2R_0 + 3R_{dc})^2}{4C(2L_0 + 3L_{dc})^2}}
\]  

\[
R_{dis} = \sqrt{\frac{8N_{FB}(2L_0 + 3L_{dc}) - C(2R_0 + 3R_{dc})^2}{36C}}
\]
According to Equation (6), DC-side fault current $i_{dc}(t)$ consists of two components. One is the continuous current of inductor charging the capacitor. Another is the capacitor discharge current in the opposite direction of the fault current. As a result, the DC-side fault current would drop to zero rapidly and remain at zero due to the unidirectional conduction characteristics of the diode. Therefore, the hybrid MMC can always meet the second condition, no matter what the proportion of FBSMs is. Besides, it should be noted from Equation (8) that the time constant will be influenced by the fault circuit inductance $L_{dc}$ and the fault circuit resistance $R_{dc}$, which change with the length of the DC line from the fault point to the converter station.

In addition to the aforementioned two conditions, the hybrid MMC should also ensure that the SM capacitor voltage does not exceed the threshold value set by the protection system after blocking.

3 | MODIFIED HYBRID MMC

According to the analysis in Section II, the proportion of FBSMs in the conventional hybrid MMC is mainly limited by the first condition. According to Equation (3), the proportion of FBSMs should be greater than 43% when $m$ equals 1. However, the proportion required by the second condition is much lower than this value. According to [13], the power loss of the full-bridge MMC in normal operation is 38% more than that of the half-bridge MMC. While the power loss of the hybrid MMC with 40% FBSM is 16% more than that of the half-bridge MMC. Therefore, the power loss of the hybrid MMC is slightly higher than that of the half-bridge MMC and the extra power loss is approximately linear with the proportion of FBSMs. Therefore, in order to reduce the required proportion of FBSMs in hybrid MMC, this paper proposed a modified hybrid MMC, which only need to meet the second condition and third condition for successful DC fault clearance. This section first introduces the structure of the modified hybrid MMC. Then the corresponding DC fault clearance strategy is presented.

3.1 | Topology of modified hybrid MMC

The structure of the modified hybrid MMC is shown in Figure 5. The arm of the modified hybrid MMC is still composed of $N_{total}$ SMs and an arm inductor in series, while the number of FBSMs $N_{FB}$ is reduced. Different from the structure shown in Figure 1, the intersection of upper arm and lower arm in each phase is connected through three AC Current Blocking Switches (ACBSs) in star connection. These ACBSs always remain open in steady state. After the fault occurs, ACBSs are asked to close immediately to block the AC current. In order to guarantee the operation speed of ACBSs, the thyristors which are durable and economical are employed to compose the ACBSs as shown in Figure 5. Then both of the closing time and disconnecting time of the ACBSs can be within 1 ms. In addition, the ultra-fast disconnecter (UFD) is installed on the DC side to isolate the faulty line.

When the DC fault occurs, a three-phase short-circuit can be actively applied at the AC-side of hybrid MMC by close all ACBSs after blocking. Then the AC current feed would be blocked at point M according to the equivalent circuit of the modified hybrid MMC after blocking shown in Figure 6. Therefore, the first condition mentioned in Section II would always hold. And the number of FBSMs $N_{FB}$ no longer needs to satisfy Equation (3). The UFD is mainly used to isolate the faulty line immediately after the fault current drops to zero, then the ACBSs can tripped as soon as possible to remove the three-phase short circuit.
In addition, compared with the conventional hybrid MMC, energy charged into FBSM capacitors after blocking is also reduced because the energy from the AC system is blocked. So the maximum FBSM capacitor voltage of modified hybrid MMC during DC fault is lower than the conventional one with the same number of FBSM. Therefore, the number of FBSMs in the modified hybrid MMC can be reduced without affect the DC fault clearance capability.

3.2 Strategy of DC fault clearance

Take a positive DC line-to-ground fault as an example, the detailed DC fault clearance strategy of the modified hybrid MMC is as follows:

1. Step 1: The DC line-to-fault occurs at $t_0$. With the rapid rise of the fault current, maximum arm currents of six arms exceeds the threshold value (2 times of the rated current of the IGBT) at $t_1$. Then the hybrid MMC is blocked immediately. And ACBSs are closed to apply a three-phase short circuit at AC side after the converter is blocked. Since the time delay of converter blocking is very short, both operations can be considered to be applied at $t_1$. After that, the AC current into the MMC drops to zero and the fault current only includes the DC-side component expressed in Equation (6).

2. Step 2: The fault current drops to zero and the open signal is sent to the UFD at $t_2$ to isolate the faulty line. After a short delay, the UFD fully opens at $t_3$. By now, the physical isolation between the converter and the faulty line is realized and it is no longer necessary to block the AC current feed. Then the tripping signal is send to the ACBSs.

3. Step 3: At $t_4$, all ACBSs in the converter are completely tripped and the state of three-phase short-circuit is removed. The DC-fault clearance is completed and the AC system returns to steady state operation at $t_5$.

In the whole process of fault clearance shown in Figure 7, a three-phase short-circuit fault is actively applied at AC-side in the period from $t_1$ to $t_4$. In order to ensure that the stability of the AC system will not be affected, it is necessary to estimate the existence time of three-phase short circuit $T_{\text{short}}$.

$$T_{\text{short}} = (t_2 - t_1) + (t_3 - t_2) + (t_4 - t_3) = T_{\text{tozero}} + T_{\text{UFDD}} + T_{\text{ACBS}}$$

(11)

According to Equation (11), $T_{\text{short}}$ consists of three components: the time for fault current to drop to zero $T_{\text{tozero}}$, the time delay for UFD to open $T_{\text{UFDD}}$ and the time delay for ACBS to open $T_{\text{ACBS}}$. Among them, $T_{\text{UFDD}}$ is approximately 2 ms according to [22]. $T_{\text{tozero}}$ can be eliminated according to Equation (6). Fault current $i_{\text{dc}}(t)$ consists of a positive component and a negative component. Obviously, the time for the positive component to drop to zero is larger than $T_{\text{tozero}}$. But it can still be used to make a conservative estimate of $T_{\text{tozero}}$ as shown in Equation (12). According to the simulation results in [23] and the estimation results based on the parameters of the practical engineering, $T_{\text{tozero}}$ is smaller than 10 ms in most cases.

$$T_{\text{tozero}} < \frac{\theta_{\text{dc}}}{\omega_{\text{dc}}}$$

(12)

As for $T_{\text{ACBS}}$, it mainly represented the time delay from receiving the tripping signal until the current flowing through ACBSs dropping to zero. Assuming that the AC system frequency is 50 Hz, the maximum value of $T_{\text{ACBS}}$ is 10 ms. According to the above calculations, the existence time of three-phase short circuit $T_{\text{short}}$ would not exceed 22 ms, which is acceptable for most AC systems. Therefore, the proposed DC fault clearance strategy would not affect the stability of the AC system.

In the case of multi-terminal system, it is necessary to use the selective protection to obtain the fault location. Therefore, in addition to the fault clearing strategy introduced above, the following coordination strategies are also needed.

1. The modified hybrid MMCs are blocked when the arm current exceeds the threshold value or receiving the blocking signal from other stations.

2. The UFDs at the end of the faulty line are opened after receiving the tripping signal from the selective protection.

4 ANALYSIS OF CAPACITOR VOLTAGE

Different from the conventional hybrid MMC, the minimum number of FBSMs in the modified hybrid MMC is only limited by the capacitor voltage during fault clearance. In order to minimize the device cost, it is necessary to estimate the maximum capacitor voltage during the fault. The analysis of the capacitor
voltage is applied on the modified hybrid MMC before and after blocking respectively.

4.1 Capacitor voltage before blocking

After the DC fault occurs until the MMC is blocked, the number of inserted SMs in each arm still changes according to the control system. Take the upper arm of phase A as an example, assuming that the capacitor voltage at the moment of fault is \( u_{c0,pa} \), then the capacitor voltage before blocking can be expressed as:

\[
u_{c1,pa} = u_{c0,pa} + \frac{1}{C} \int_{t_0}^{t_1} S_{pa}(t) \dot{u}_{pa}(t) \, dt \tag{13}\]

\( S_{pa}(t) \) denotes the average switching function. Because the time period before blocking is sufficiently short, the expression of \( S_{pa}(t) \) remains the same as in steady state:

\[
S_{pa}(t) = \frac{1 - m \sin(\omega t)}{2} \tag{14}\]

The arm current \( i_{pa}(t) \) consists of AC side current and DC side current and can be expressed as:

\[
i_{pa}(t) = \frac{1}{2} i_{ra}(t) - \frac{1}{3} i_{dc}(t) \tag{15}\]

In the calculation, the change rules of the AC side current \( i_{ra}(t) \) is considered as before the fault. While the expression of the \( i_{dc}(t) \) before blocking can be obtained according to [23]:

\[
i_{ra}(t) = I_{ref} \sin(\omega t + \varphi) \tag{16}\]

\[
i_{dc}(t) = -\frac{1}{\sin \theta_{dc0}} I_{dc0} e^{-\frac{\tau}{\omega_{dc0}}} \sin(\omega_{dc0} t - \theta_{dc0}) + \frac{I_{dc0}}{R_{dc0}} e^{-\frac{\tau}{\omega_{dc0}}} \sin(\omega_{dc0} t) \tag{17}\]

where, \( I_{dc} \) is the DC current before the fault occurs, and

\[
\theta_{dc0} = \arctan(\frac{4L_0 + 6L_{dc}}{2R_0 + 3R_{dc}}) \tag{18}\]

\[
\tau_{dc0} = \frac{4L_0 + 6L_{dc}}{2R_0 + 3R_{dc}} \tag{19}\]

\[
\omega_{dc0} = \sqrt{\frac{2N_{f,dc}(2L_0 + 3L_{dc}) - C(2R_0 + 3R_{dc})^2}{4C(2L_0 + 3L_{dc})^2}} \tag{20}\]

\[
R_{dc0} = \sqrt{\frac{2N_{f,dc}(2L_0 + 3L_{dc}) - C(2R_0 + 3R_{dc})^2}{36C}} \tag{21}\]

According to Equations (13)–(17), the capacitor voltage at the moment of blocking can be expressed as:

\[
u_{c1,pa} = \left[ u_{c0,pa} + \frac{1}{C} \int_{t_0}^{t_1} S_{pa}(t)\left(\frac{1}{2} i_{ra}(t) - \frac{1}{3} I_{dc}(t)\right) \, dt \right] + \frac{1}{C} \int_{t_0}^{t_1} S_{pa}(t)\left(\frac{1}{3} I_{dc} - \frac{1}{3} i_{dc}(t)\right) \, dt \]

\[
= u_{cst,pa} + u_{ctr,pa} \tag{22}\]

where, \( u_{cst,pa} \) denotes the steady state component and \( u_{ctr,pa} \) denotes the transient component of capacitor voltage.

According to Equation (22), \( u_{cst,pa} \) is same as the expression of the capacitor voltage under steady state [24]. In most MMC projects, the maximum capacitor voltage ripple in steady state is limited to 10% of rated capacitor voltage. Therefore, the following inequality can be obtained:

\[
u_{cst,pa} \leq 1.1 U_{in} \tag{23}\]

The maximum value of \( u_{ctr,pa} \) can be estimated as follows:

\[
u_{ctr,pa} = \frac{1}{C} \int_{t_0}^{t_1} \left[ \frac{1 - m \sin(\omega t)}{2} \right] \times \left[ \frac{1}{3} \int_{t_0}^{t_1} \left( I_{idc} - I_{dc}(t) \right) \, dt \right] \]

\[
\leq -\frac{m}{6C} \int_{t_0}^{t_1} \left[ I_{idc} - I_{dc}(t) \right] \, dt \tag{24}\]

Substituting Equation (17) into Equation (24), the expression can be obtained as follows:

\[
u_{ctr,pa} \leq -\frac{1 - m}{6C} [F(t_1 - t_0) - F(0)] \tag{25}\]

where,

\[
F(t) = \frac{I_{dc0}}{\omega_{dc0}} e^{-\frac{\tau}{\omega_{dc0}}} \sin(\omega_{dc0} t) - \frac{\tau^2_{dc0}}{\omega_{dc0}^2} \cos(\omega_{dc0} t) - \frac{1}{\tau_{dc0}} \sin(\omega_{dc0} t) - I_{idc} t \tag{26}\]

Substituting Equations (23) and (25) into Equation (22), the maximum value of \( u_{c1,pa} \) can be estimated as follows:

\[
u_{c1,pa} \leq 1.1 U_{in} - \frac{1 - m}{6C} [F(t_1 - t_0) - F(0)] \tag{27}\]

4.2 Capacitor voltage after blocking

After the modified hybrid MMC is blocked, the DC-side equivalent circuit is shown in Figure 4. Since the AC current feed is blocked due to ACBSs and the energy consumed by the resistor is negligible, the energy in the DC-side circuit is
almost conserved. It can be used to calculate the final value of capacitor voltage after blocking. Assuming that the energy is evenly distributed among the six arms, the final value of capacitor voltage can be calculated as follow:

$$\frac{N_{FB}}{2} C \left( u_{c2,pa}^2 - u_{c1,pa}^2 \right) = \frac{1}{12} \left[ I_{dc} i_{dc}^2(t_1) + L_0 \sum_{r=1}^{N_c} \sum_{j=1}^{N_{pa}} i_j^2(t_1) \right]$$  \hspace{1cm} (28)

where, $u_{c2,pa}$ denotes the final capacitor voltage, and

$$\begin{align*}
  i_j &= \frac{1}{2} i_{rj} - \frac{1}{3} i_{dc} \\
  i_{rj} &= - \frac{1}{2} i_{rj} - \frac{1}{2} i_{dc}
\end{align*}$$  \hspace{1cm} (29)

Substituting Equation (29) into Equation (28), the following relationship can be obtained:

$$\frac{N_{FB}}{2} C \left( u_{c2,pa}^2 - u_{c1,pa}^2 \right) = \left( \frac{I_{dc}}{12} + \frac{I_{vm}}{18} \right) i_{dc}^2(t_1) + \frac{1}{16} L_{dc} i_{dc}^2(t_1)$$  \hspace{1cm} (30)

where, $I_{vm}$ denotes the amplitude value of the AC-side current in steady state.

According to Equation (30), the final rise of capacitor voltage is mainly related to $|i_{dc}(t_1)|$, which is the absolute value of fault current at the moment of blocking. Therefore, it is necessary to calculate the maximum value of fault current before blocking. The arm current can be divided into AC component and DC component, and the expression can be rewrite as:

$$i_{rj} = i_{rj,ac} - \frac{1}{3} i_{dc}$$  \hspace{1cm} (31)

For different arm, the phase angles of AC components differ by 60° in turn:

$$i_{r,j,ac} = \frac{1}{2} I_{rw} \sin \left( \omega t + \varphi_j + \frac{k}{3} \pi \right) \hspace{1cm} (k = 0, 1, 2, 3, 4, 5)$$  \hspace{1cm} (32)

According to the properties of sine function, the minimum value of sine value of six angles which increase by 60 degrees in turn will always be less than $\sin(-\pi/3)$. Therefore, it can be obtained from Equation (32) that:

$$\min(i_{r,j,ac}) \leq \frac{1}{2} I_{rw} \sin \left( -\frac{\pi}{3} \right) = -\frac{\sqrt{3}}{4} I_{rw}$$  \hspace{1cm} (33)

Because the condition of blocking is that one of the six arm currents exceeds the threshold value $|i_{dc}(t_1)|$, the maximum value of $|i_{dc}(t_1)|$ at the moment of blocking can be expressed as:

$$\max(|i_{dc}(t_1)|) = 3 \left( |i_{dc}| - \frac{\sqrt{3}}{4} I_{rw} \right)$$  \hspace{1cm} (34)

Substituting Equation (34) into Equation (30), the maximum value of $u_{c2,pa}$ can be obtained. It is also the maximum value of the capacitor voltage which should be limited under the threshold value (1.4× of $U_{rms}$ in this paper) when setting $N_{FB}$.  

\textbf{FIGURE 8} Relationship between minimum proportion of FBSMs and DC line length

4.3 Calculation of required FBSM proportion

According to the aforementioned analysis, the minimum required proportion of FBSMs $K_{FB,\text{min}}$ in the modified hybrid MMC can be calculated as:

$$K_{FB,\text{min}} = \frac{\left( \frac{L_{dc}}{6} + \frac{I_{vm}}{9} \right) i_{dc}^2(t_1) + \frac{1}{6} L_0 I_{rw}^2}{CN_{total} \left( 1.4 U_{rms} \right)^2 - \xi_{1,pa}}$$  \hspace{1cm} (35)

It can be seen from Equation (35) that in addition to the MMC parameters, the minimum proportion is also related to the fault circuit inductance and resistance. Therefore, the required proportion of FBSMs will change with the DC line length. And the fault resistance is also included in the fault circuit resistance $R_{dc}$. According to Equation (35), $R_{dc}$ can only indirectly influence $K_{FB,\text{min}}$ by affect $\xi_{1,pa}$. And the change of fault resistance has little effect on $\xi_{1,pa}$. Therefore, the effect of fault resistance on $K_{FB,\text{min}}$ is negligible.

The detailed calculation steps of $K_{FB,\text{min}}$ are as follows:

1. Calculate the maximum fault circuit inductance $I_{dc}$ and resistance $R_{dc}$ according to the parameters of the DC line.
2. Calculate the maximum value of $\xi_{1,pa}$ according to Equation (27).
3. Calculate the maximum value of $|i_{dc}(t_1)|$ according to Equation (34).
4. By substituting the calculation results of the steps (1)–(3) into Equation (35), the minimum required proportion of FBSMs can be obtained.

Take the 500 kV/3000 MW MMC station as an example, the 4.5 kV/3kA IGBTs are used in all SMs. The main parameters are listed in Table 1. The rated value and threshold value of capacitor voltage are 2.2 and 3.08 kV respectively. Supposing that the system operates in steady state and DC current $I_{dc}$ is 3 kA before the fault occurs. It is assumed that it takes at least 6 ms from the occurrence of the fault to the blocking of the hybrid converter. Then the relationship between $K_{FB,\text{min}}$ and the DC line length can be obtained according to Equation (35) and is depicted in Figure 8.

As can be seen in Figure 8, for the above system, the required proportion of FBSMs can be reduced to less than 50% when
TABLE 1  Main parameters of MMC station and DC line

| Items                      | Values             |
|----------------------------|--------------------|
| Rated Capacity             | 1500 MVA           |
| Rated DC Voltage           | 500 kV             |
| Transformer MVA            | 1800 MVA           |
| Transformer ratio          | 230 kV /262 kV \(Y_0/\Delta\) |
| Smoothing reactor          | 100 mH             |
| Number of SMs per arm \(N_{\text{total}}\) | 228 |
| Rated Capacitor voltage \(U_{\text{on}}\) | 2.2 kV |
| SM capacitance \(C\)      | 18240 uF           |
| Arm inductor \(L_0\)      | 32 mH              |
| Arm equivalent resistance \(R_0\) | 0.45 \(\Omega\) |
| Rated AC current amplitude \(I_{\text{vm}}\) | 4.67 kA |
| Modulation index \(m\)    | 0.8557             |
| Positive sequence resistance of line \(r\) | 9.735\(\times 10^{-3}\) \(\Omega/km\) |
| Positive sequence inductance of line \(l\) | 8.489\(\times 10^{-3}\) mH/km |
| Positive sequence capacitance of line \(c\) | 1.367\(\times 10^{-2}\) uF/km |

FIGURE 9  Maximum capacitor voltage under different fault time

the length of DC line is short than 243 km. In fact, for the conventional hybrid MMC with the same parameters, the required proportion of FBSMs would also exceed 50% when the DC line is longer than 243 km. This is because the main constraint on the FBSMs proportion of conventional hybrid MMC changes from Equations (1) to (3) introduced in Section 2. Furthermore, the modified hybrid MMC can use less FBSMs than the conventional one to keep the maximum capacitor voltage under threshold value, because the energy charged into FBSM capacitors during the fault is reduced by blocking the energy from the AC system. Therefore, the required proportion of FBSMs of the modified hybrid MMC is always lower than that of the conventional one, and this advantage will be more obvious when the DC line is short.

In order to verify above conclusions, a modified hybrid MMC test system is established in PSCAD/EMTDC. The main circuit parameters of the MMC are same as Table 1. The length of DC line is set as 100 km and the number of FBSMs is correspondingly set to 71 (31% of \(N_{\text{total}}\)) according to Figure 8. It is assumed that the DC fault occurs at the end of the DC line far away from the MMC station. DC fault occurred in different time is simulated in the test system. Figure 9 shows the maximum capacitor voltage when the DC fault occurs at different time in a system cycle.

According to Figure 9, the maximum capacitor voltage would reach 3.004 kV under some specific fault time, which is still lower than the threshold value 3.08 kV. Therefore, the FBSMs proportion calculated by the above method can ensure that the capacitor voltage during the fault under threshold value.

5  CASE STUDY

5.1  Test system

In order to verify the effectiveness and feasibility of the modified hybrid MMC, a three-terminal MMC-HVDC system is established in PSCAD/EMTDC. The system structure is shown in Figure 10. In order to test whether the three-phase short-circuit applied during DC fault will affect the stability of AC system, the four-machine system introduced in [25] is used. MMC-2 station and MMC-3 station are connected to bus 7 and bus 9 of the same four-machine system respectively. The parameters of generators and loads in four-machine system are listed in Table 2. The modified hybrid MMC is used in all MMC stations with the same parameters of Table 1. The number of FBSMs

![FIGURE 10 Structure of test system](image-url)
and HBSMs is 71 and 157 respectively. The length of Line-1 and Line-2 are both 100 km.

The MMC-2 station and MMC-3 station are operated with constant active power control and their reference values are 600 MW and 800 MW respectively. The MMC-1 station adopts constant DC voltage control with the reference value of 500 kV. The capacitor voltage balancing strategy introduced in [17] has been used to achieve the voltage balancing among HBSMs and FBSMs.

5.2 Simulation results

As a comparison, the fault response characteristics of the test system using the conventional hybrid MMC with 50% FBSMs are also simulated. Supposing that the test system is in steady state at the beginning, a permanent DC line-to-ground fault F-1 is applied at the end of Line-2 near the MMC-2 station at $t = 0.2$ s. Fault resistance is 0.001 Ω. The simulation results are depicted in Figure 11.

In the case of using modified hybrid MMC, the arm current of MMC-1 and MMC-2 exceeds the threshold value 6 kA at $t = 0.2044$ s and $t = 0.2050$ s respectively. Both stations are blocked immediately and ACBSs are closed. At $t = 0.2070$ s, MMC-3 station receives and executes the blocking signal. At $t = 0.2136$ s, all DC fault current drops to zero. Then UFD-3 and UFD-4 are opened and the faulty line is isolated. At $t = 0.2230$ s, ACBSs in all stations are completely tripped. At $t = 0.5$ s, MMC-1 and MMC-2 are unblocked and restore to the steady state: MMC-1 station transfers 600 MW active power to MMC-2 station through line-1. As for the test system using conventional hybrid MMCs, the MMC-1 and MMC-2 are blocked at $t = 0.2044$ s and $t = 0.2050$ s respectively. The faulty line is isolated by the UFD at $t = 0.2180$ s. At $t = 0.5$ s, MMC-1 and MMC-2 are unblocked and restore power transmission.

As shown in Figure 11, the test system using modified hybrid MMC has almost the same DC fault response characteristic as the one using conventional hybrid MMC. In addition, the wave form of generator phase angle in four-machine system shows that they have the same effect on AC system when dealing with DC fault. Figure 12 depicts the AC current of the modified hybrid MMC during the DC fault. As can be seen, over current caused by the active three-phase short-circuit lasts for about only 20 ms and maximum value will not exceed the over current.
caused by the three-phase line-to-ground faults on the point of common coupling (PCC). Therefore, it is proved that the three-phase short-circuit applied during DC fault will not affect the stability of the system.

The waveforms of average capacitor voltage in each arm of modified hybrid MMC during the fault are depicted in Figure 13. The capacitor voltage in MMC-1 station increases most during the fault. And the maximum value of capacitor voltage in MMC-1 is 3.03 kV, which is still below the threshold value 3.08 kV. The capacitor voltage in MMC-3 is significantly lower than that of other two stations during the fault. This is because MMC-3 station is blocked due to the blocking signal from other station before its arm current exceeds the threshold value.

In order to ensure that the maximum capacitor voltage will not exceed the threshold value under different faults, the faults at several extreme locations are simulated. These faults are at the ends of the Line-1 and Line-2, which are marked by F-2 to F-4 in Figure 10. The maximum capacitor voltage waveforms of each station under these DC faults are depicted in Figure 14. As can be seen in Figure 14, the maximum capacitor voltage is 3.08 kV appearing in the MMC-1 under the fault F-4, which is still below the threshold value.

Assume that the IGBTs SSNA 3000K452300 with 3 kA current rating and 4.5 kV voltage rating are used in all SMs, and the thyristors STP45Y8500 with 8.5 kV voltage rating is employed in ACBSs. The voltage that a single thyristor bears should be 4.25 kV [22]. Each ACBS needs to withstand the maximum phase-to-ground voltage 214 kV on the AC side. Hence, each ACBS consists of 102 thyristors. The comparison of two strategies is shown in Table 3. It can be seen that the number of IGBTs of the modified hybrid MMC is 516 less than that of the conventional hybrid MMC, while 306 additional thyristors are required. Since the price of the thyristor is much lower than that of the IGBTs, the manufacturing cost of the modified hybrid MMC is significantly reduced compared to the conventional one.

According to the above simulation results, the modified hybrid MMC can effectively deal with the DC fault with less FBSMs than the conventional hybrid MMC, which can signif-
5.3 Case study based on practical engineering

In order to make the above conclusions more representative, a simulation model based on the Kunliulong project in monopole operation state is established in PSCAD/EMTDC. The system structure is shown in Figure 15. In the test system, one LCC with twelve impulse unit connection is adopted as the rectifier station. And another two MMC stations are composed with two modified hybrid MMC units connected in series. The parameters of converter units in each station are listed in Table 4. LCC-1 adopts the constant current control and the reference value of DC current is 5 kA. The MMC-1 station is operated with constant active power control and the reference value is 1500 MW. The MMC-1 station adopts constant DC voltage control with the reference value of 800 kV. The lengths of Line-1 of Line-2 are 932 and 557 km respectively.

Supposing that the test system is in steady state at the beginning, a permanent DC line-to-ground fault is applied at the end of Line-2 near the MMC-1 station at \( t = 0.1 \) s. The simulation results are shown in Figure 16. The arm current of MMC-1 exceeds the threshold value 3.75 kA at \( t = 0.1020 \) s.

Both MMC units of MMC-1 station are blocked immediately and ACBSs are closed. At \( t = 0.1040 \) s, MMC-2 station receives and executes the blocking signal from MMC-1. At \( t = 0.1052 \) s, LCC-1 station receives the blocking signal and forces the firing angle to 145°. At \( t = 0.1190 \) s, all DC fault current drops to zero and UFD-3 and UFD-4 are opened. At \( t = 0.1220 \) s, ACBSs in MMC-1 and MMC-2 are completely tripped. As can be seen in Figure 16, DC fault has been successfully cleared and the maximum average capacitor voltage in each MMC units is 2.32 kV, which is much lower than the threshold value 2.8 kV. Therefore, the feasibility and effectiveness of the modified hybrid MMC have been further verified.

6 CONCLUSION

This paper proposed a modified hybrid MMC with lower proportion of FBSMs than the conventional hybrid MMC, while the DC fault clearance capability is retained. Three DC fault clearing conditions of the hybrid MMC are first introduced.
Figure 16 Simulation results of DC fault in practical engineering based system. (a) DC currents of each station; (b) Active power of each station; (c) Capacitor voltage of MMC-1 upper unit; (d) Capacitor voltage of MMC-1 lower unit; (e) Capacitor voltage of MMC-2 upper unit; (f) Capacitor voltage of MMC-2 lower unit

Project further verifies the effectiveness and feasibility of the proposed modified hybrid MMC.

ORCID
Zheng Xu https://orcid.org/0000-0003-1283-6238

REFERENCES
1. Allebrod, S., Hamerski, R., Marquardt, R.: New transformerless, scalable Modular Multilevel Converters for HVDC-transmission. In: 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece (2008), pp. 174–179
2. Glinka, M., Marquardt, R.: A New AC/AC multilevel converter family. IEEE Trans. Ind. Electron. 52(3), 662–669 (2005)
3. Peralta, J., et al.: Detailed and averaged models for a 401-level MMC-HVDC system. IEEE Trans. Power Deliv. 27(3), 1501–1508 (2012)
4. Xue, Y., Xu, Z.: On the bipolar MMC-HVDC topology suitable for bulk power overhead line transmission: Configuration, control, and DC fault analysis. IEEE Trans. Power Deliv. 29(6), 2420–2429 (2014)
5. Zhang, Z., et al.: Operating area for modular multilevel converter based high-voltage direct current systems. IET Renew. Power Gener. 10(6), 776–787 (2016)
6. Liu, S., et al.: Electromechanical transient modeling of modular multilevel converter based multi-terminal HVDC systems. IEEE Trans. Power Syst. 29(1), 72–83 (2014)
7. Xiao, L., et al.: Electromechanical transient modeling of line commutated converter-multilevel multilevel converter-based hybrid multi-terminal high voltage direct current transmission systems. Energies 11(8), 2102 (2018)
8. Pang, H., Wei, X.: Research on Key Technology and Equipment for Zhangbei 500 kV DC Grid. In: 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE. Asia), Niigata, Japan (2018), pp. 2343–2351
9. Tang, G., Xu, Z., Zhou, Y.: Impacts of three MMC-HVDC configurations on AC system stability under DC line faults. IEEE Trans. Power Syst. 29(6), 3030–3040 (2014)
10. Callavik, M., et al.: The hybrid HVDC breaker—an innovation breakthrough enabling reliable HVDC grids. ABB Grid Syst, (2012)
11. Marquardt, R.: Modular Multilevel Converter topologies with DC-Short circuit current limitation. In: 8th International Conference on Power Electronics - ECCE Asia, Jeju, South Korea (2011), pp. 1425–1431
12. Xue, Y., Xu, Z., Tu, Q.: Modulation and control for a new hybrid cascaded multilevel converter with DC blocking capability. IEEE Trans. Power Deliv. 27(4), 2227–2237 (2012)
13. Qin, J., et al.: Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits. IEEE Trans. Power Deliv. 30(1), 385–394 (2015)
14. Adam, G.P., Williams, B.W.: Half- and full-bridge modular multilevel converter models for simulations of full-scale HVDC links and multiterminal DC grids. IEEE J. Emerg. Sel. Top. Power Electron. 2(4), 1089–1108 (2014)
15. Xu, Z., et al.: Feasibility study of DC circuit breaker-less MTDC systems. Int. Trans. Electr. Energy Syst. 29(1), e2679 (2019)
16. Adam, G.P., Ahmed, K.H., Williams, B.W.: Mixed cells modular multilevel converter. In: 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE), Istanbul, Turkey (2014), pp. 1390–1395
17. Zeng, R., et al.: Precharging and DC fault ride-through of hybrid MMC-based HVDC systems. IEEE Trans. Power Deliv. 30(3), 1394–1403 (2017)
18. Cui, S., Sul, S.-K.: A comprehensive DC short-circuit fault ride through strategy of hybrid Modular Multilevel Converters (MMCs) for overhead line transmission. IEEE Trans. Power Electron. 31(11), 7780–7796 (2016)
19. Liu, G., et al.: Assembly HVDC breaker for HVDC grids with modular multilevel converters. IEEE Trans. Power Electron. 32(2), 931–941 (2017)
20. Xu, Z., et al.: DC fault analysis and clearance solutions of MMC-HVDC systems. Energies 11(6), 941 (2018)
21. Kundur, P.: Power System Stability and Control. McGraw-Hill, New York (1994)

How to cite this article: Xue, Y., Zhang, Z., Xu, Z.: Design and DC fault clearance of modified hybrid MMC with low proportion of full-bridge submodules. IET Gener. Transm. Distrib. 15, 2203–2214 (2021). https://doi.org/10.1049/gtd2.12170