Single-Switch High-Step-Up DC-DC Converter Employing Coupled Inductor and Voltage Multiplier Cell

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ABSTRACT This paper introduces a high-step-up dc-dc converter to provide voltage boosting in low-voltage applications. The circuit contains only a single active switch and is based on the boost-type converter using coupled inductor and voltage multiplier cell. The proposed topology exhibits high efficiency, reduced voltage stress on the semiconductors and requires a low component count. The circuit is intended for applications with rated power in the order of a few hundreds of Watts, which corresponds to the typical level of a single photovoltaic (PV) module. A detailed mathematical description of the circuit operation is carried out, providing the means for the adequate design of the converter. The dynamic analysis is also addressed in the paper, and proper closed-loop operation is demonstrated. A 400 W prototype operating at 90 kHz, with an input voltage range of 24-48 V and output voltage of 400 V was built and tested in laboratory. Experimental results validate the analyses carried out and measurements indicate efficiency levels up to 97.5%, which ratifies the proposed converter as a good solution for typical PV applications.

INDEX TERMS High voltage gain, high step-up, coupled inductor, voltage multiplier cell.

I. INTRODUCTION
Direct current (DC) generation such as photovoltaic power systems has become one of the main sources of electricity supply worldwide. Nevertheless, the energy is produced at relatively low voltage levels, and usually dc-dc converters are required to reach high voltage gain and high efficiency.

It is known that the overall efficiency of a switching converter is strongly affected by switching and conduction losses. Therefore, using circuits with low component count, reduced voltage stress and with the capability of regenerating the leakage energy is key to improving the overall system performance. However, obtaining all these characteristics from a simple dc-dc converter is not an easy task. A good example is the conventional boost converter, which is not appropriate in most applications requiring high voltage conversion ratio because the voltage gain depends solely on the duty cycle [1], [2]. In such case, due to the non-idealities inherent to the elements of the circuit, the efficiency is reduced at high conversion ratio. In this sense, numerous alternative topologies have been proposed to circumvent the conventional step-up converters’ drawbacks, as discussed in the reviews presented in [3] and [4]. As it can be observed in these papers, several voltage boosting techniques are used to achieve high voltage gain, such as coupled inductor, voltage multiplier cell and switched capacitor. Among the numerous solutions proposed in the literature, those based on the single-switch boost converter using coupled inductor and capacitor-diode interaction can be highlighted [5], [6].

Considering typical single-module PV applications, in which voltage and power levels are in the order of some tens of Volts and few hundreds of Watts, respectively, the use of simpler topologies is preferrable. In this sense, converters containing a single active switch, one coupled inductor and reduced number of diodes and capacitors have been widely investigated by researchers worldwide. For instance, using
the conventional boost-flyback topology presented in [7], a larger voltage conversion ratio is achieved by the summing the individual voltage gains of the boost and flyback stages. However, although the voltage stress on the active switch is reduced, an auxiliary snubber circuit is required to limit the voltage spike on the diode contained in the flyback stage. This issue can be addressed by using a voltage doubler with only two windings brings simplicity for the volume reduction. Finally, the use of a single coupled inductor with only two windings brings simplicity for the volume reduction. In addition, the voltages on the circuit are lower than the output voltage, and thus conduction age stresses on all semiconductors contained in the proposed integrated DC-AC conversion in AC PV modules. The volt-

II. PROPOSED SINGLE-SWITCH HIGH STEP-UP DC-DC CONVERTER

The proposed single-switch high step-up dc-dc converter composed of a single coupled-inductor and employing volt-

age multiplier cell is depicted in Fig. 1. The input stage is composed of the primary winding of the coupled inductor and the switch S. The inductances $L_{m}$ and $L_{k}$ represent the magnetizing and leakage inductances of the coupled inductor, respectively. The output stage consists of the secondary winding of the coupled inductor, three diodes ($D_{1}$-$D_{3}$), and three capacitors ($C_{1}$-$C_{3}$). A closer look at the circuit depicted in Fig. 1 unveils some important operational characteristics of the circuit: (a) the output voltage $V_{o}$ corresponds to the sum of the voltages on $C_{2}$ and $C_{3}$; and (b) the pair $D_{1}$-$C_{1}$ provides an alternative path for $i_{Lk}$ towards the output stage after the switch is turned off, thus the energy stored in $L_{k}$ is recycled and the blocking voltage of $S$ becomes naturally clamped. It is also demonstrated in this work that the coupled inductor operates both as a conventional transformer and an inductor, because: (a) energy is processed directly from the primary to the secondary winding during some intervals, as a typical transformer; and (b) energy stored in the magnetizing inductance in one stage is transferred to the output at a later interval, as occurs in the flyback converter.

III. OPERATION PRINCIPLE IN STEADY STATE

A sequence of five distinct stages characterizes the converter operation in steady state, as depicted in Fig. 2. In this work, a detailed analysis is carried out within a switching period $T_{s}$ and the following simplifying assumptions are considered:

1. The magnetizing inductance current $i_{Lm}$ is assumed constant and ripple-free;
2. The voltages on the capacitors $C_{1}$, $C_{2}$ and $C_{3}$ are assumed constant and ripple-free;
3. All the semiconductor elements are assumed as ideal;
4. $L_{k}$ accounts for the total leakage inductance of the primary and secondary windings.

In order to simplify the converter operation within one switching cycle, a general description of the possible five steps is introduced below:

(a) First and third stages, which occur within the respective intervals $\Delta t_{1}$ and $\Delta t_{3}$, start when the switch $S$ is

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FIGURE 2. Operation stages at steady state.

turned-on and turned-off, respectively. During the interval $\Delta t_3$, the energy provided by the leakage inductance $L_k$ is absorbed by $C_1$, thus avoiding the occurrence of a voltage spike on $S$. Under ideal operating conditions both $\Delta t_1$ and $\Delta t_3$ can be neglected, as these intervals are much briefer than those verified for stages 2, 4 and 5. The equivalent circuits of these two operation stages are illustrated in Fig. 2 (a) and Fig. 2 (c).

(b) The second, fourth and fifth operation stages can be considered as the main stages since most of the energy is processed by the converter during the intervals $\Delta t_2$, $\Delta t_4$ and $\Delta t_5$.

During the second stage (c.f., Fig. 2(b)), $S$ is turned on and energy is provided by $V_{in}$ to $L_m$ and also to $C_3$ via direct energy transfer from the primary to the secondary windings of the coupled inductor (transformer-like operation). Regarding the fourth stage (c.f., Fig. 2 (d)), $S$ is turned off, the leakage energy is diverted to $C_1$ and the coupled inductor transfer energy to $C_2$. Finally, during the fifth stage (c.f., Fig. 2 (e)), energy previously stored in $L_m$ is transferred to $C_2$ via the secondary winding of the coupled inductor (flyback-like operation).

Fig. 3 illustrates the main theoretical waveforms for steady-state operation.

The mathematical description of the converter for steady-state operation is carried out from the analysis of the equivalent circuits generated from stages 2, 4 and 5, and also from the waveforms detailed in Fig. 3. In addition, the following
expressions are considered:
\[
\begin{align*}
\Delta t_i &= t_i - t_{i-1}; \quad T_s = \frac{1}{f_s}, \quad n = \frac{N_p}{N_m}; \\
\lambda &= \frac{L_m}{L_k}; \quad k = \frac{1}{\lambda + 1}.
\end{align*}
\] (1)
where: \(i\) is the index that defines the time interval of each stage, which starts at \(t_{i-1}\) and ends at \(t_i\).

The factor \(\lambda\) defined in (1) represents the ratio between the leakage inductance \(L_k\) and the magnetizing inductance \(L_m\). As it is going to be demonstrated in this paper, \(\lambda\) affects the voltage gain of the proposed converter and should be kept as low as possible, which is achieved if the leakage inductance of the coupled inductor is reduced.

**IV. STATIC MODEL**

A complete mathematical description of the converter operation in steady state is derived in this section. The static model is obtained by the analysis of the equivalent circuits of the operating stages depicted in Fig. 2 and the waveforms shown in Fig. 3. Based on the results of this analysis, the static gain and stresses on the components of the circuit can be computed, thus allowing the adequate design of the converter.

Equations (2)–(5), valid for steady-state operation, can be computed, thus allowing the adequate design of the converter.

Equations (2)–(5) are considered
\[
\begin{align*}
I_{k1} &= \left(\frac{V_{in}}{n} + \frac{V_{C2}}{n}\right) \cdot \frac{\Delta t_1}{\lambda L_m}; \\
I_{k2} &= I_{k1} + \left(\frac{V_{in}}{n} - \frac{V_{C3} - V_{C1}}{n}\right) \cdot \frac{\Delta t_2}{\lambda L_m} \\
I_{k3} &= I_{k2} - \left(\frac{V_{in}}{n} - \frac{V_{C3} - V_{C1}}{n}\right) - V_{C1} \cdot \frac{\Delta t_3}{\lambda L_m} \\
I_{k3} &= \left(V_{C1} - \frac{V_{in}}{n} - \frac{V_{C2}}{n}\right) \cdot \frac{\Delta t_4}{\lambda L_m}.
\end{align*}
\] (2–5)
The equilibrium of the energy processed by \(L_m\) can be demonstrated through its Volt-second balance as given in (6). The Volt-second balance in \(L_k\) is not necessary since it is already implicitly considered in (2)–(5).

\[
(V_{C3} - V_{C1}) \cdot (\Delta t_2 + \Delta t_3) = V_{C2} \cdot (\Delta t_4 + \Delta t_5 + \Delta t_1)
\] (6)
The analysis of the proposed high gain dc-dc converter unveils that the average current of \(L_k\), which corresponds to the average value of the current provided by the input voltage source, is given by (7).

\[
I_{k1} DT_s + I_{k2} DT_s = (2V_{in} - I_o) T_s
\] (7)
The average current on \(D_1, D_2\) and \(D_3\), which must be equal to the average value of the output current \(I_o\), can be computed by (8), (9) and (10), respectively. Equating (8) and (9), as well as (8) and (10), results in two expressions, which compose the fundamental equations system of the converter.

\[
n(I_{k2} + I_{k3}) DT_3 + n I_{k3} DT_4 = 2n I_o T_s
\] (8)

\[
2I_m((1 - D)T_s + (\Delta t_1) + (I_{k2} + I_{k3}) DT_3 + I_{k3} DT_4 = 2n I_o T_s
\] (9)

\[
(I_{k2} + I_{k1} - 2I_m) DT_2 + (I_{k2} + I_{k3} - 2I_m) DT_3 = 2n I_o T_s
\] (10)

Equation (11) indicates that the output voltage \(V_o\) must be equal to the sum of \(V_{C2}\) and \(V_{C3}\).

\[
V_{C2} + V_{C3} = V_o
\] (11)
From the analysis of the Fig. 2 (b) it is possible to demonstrate that

\[
V_{C3} - V_{C1} = nk V_{in}.
\] (12)
The modulation strategy adopted for the converter provides the relation between the duty cycle and the intervals of the operating stages, as given by (13) and (14).

\[
\Delta t_1 + \Delta t_2 = D \cdot T_s,
\] (13)
\[
\Delta t_3 + \Delta t_4 + \Delta t_5 = (1 - D) \cdot T_s.
\] (14)
The expressions presented in (2)–(14) define the fundamental equations describing the steady-state operation of the converter. However, this system of equations does not have a trivial analytic solution, thus requiring numerical methods to be solved. However, as already mentioned during the description of the operating stages, both \(\Delta t_1\) and \(\Delta t_3\) can be neglected because their values are usually much smaller than \(\Delta t_2\), \(\Delta t_4\) and \(\Delta t_5\). Considering this simplifying assumption, an approximate mathematical model can be derived, which provides an adequate description of the converter operation in steady state. On the other hand, the influence of the leakage inductance on the system operation is still represented by the decoupling factor \(k\) defined in (1).

Disregarding \(\Delta t_1\) and \(\Delta t_3\), it follows that

\[
\Delta t_2 = D \cdot T_s,
\] (15)
\[
\Delta t_4 + \Delta t_5 = (1 - D) \cdot T_s.
\] (16)
Replacing (12) and (15) into (3) and (15) into (7), the unknowns \(I_{k1}\) and \(I_{k2}\) can be determined by (17) and (18), respectively.

\[
I_{k1} = \frac{I_{in} - I_o}{D} - \frac{(1 - k)D T_s V_{in}}{2 \lambda L_m}
\] (17)
\[
I_{k2} = \frac{I_{in} - I_o}{D} + \frac{(1 - k)D T_s V_{in}}{2 \lambda L_m}
\] (18)
At this point, the current gain of the proposed converter can be derived by substituting (15) into (7) and (10), resulting in (19).

\[
\frac{I_o}{I_{in}} = \frac{1 - D}{1 + kn}.
\] (19)
Considering the power balance between the input and output, it is possible to obtain the static voltage gain \(M\) presented in (20), which demonstrates the dependency of the output voltage on the parameters \(D, k\) and \(n\).

\[
M = \frac{V_o}{V_{in}} = \frac{(1 + kn)}{1 - D}.
\] (20)
The voltage level $V_{C2}$ is determined by substituting (12), (15) and (16) into (6), and then the respective result into (20), yielding (21).

$$V_{C2} = \frac{k n D}{1 - D} \cdot V_{in}$$  \hspace{1cm} (21)

Fig. 4 depicts the voltage gain $M$ as a function of $D$ for different values of $k$. It is demonstrated that the decoupling factor $k$ has a low impact on the ideal static gain.

Isolating $V_o$ in (20) and substituting the result and (21) into (12), it is possible to determine $V_{C3}$ according to (22).

$$V_{C3} = \left(\frac{1}{1 - D} + k n\right) \cdot V_{in}$$  \hspace{1cm} (22)

The voltage on capacitor $C_1$ given in (23) is derived by replacing (22) into (12).

$$V_{C1} = \frac{V_{in}}{1 - D}$$  \hspace{1cm} (23)

In this work, the duty cycle $D$ is chosen to limit the voltage $V_{C1}$ to some desired value. In this way, the designer is able to ensure that the blocking voltage of $S$ is limited, thus guaranteeing that low voltage rating MOSFETs can be employed, which in turn contributes to reducing the conduction losses.

The current level $I_{k3}$ can be computed from (5) and (8), yielding (24).

$$I_{k3} = \sqrt{\frac{2(1 - k)}{1 + n k}} \cdot \frac{V_{in} I_{in} T_s}{\lambda L_m}$$  \hspace{1cm} (24)

Finally, $\Delta t_4$ is determined by substituting (24) into (8), resulting in

$$\Delta t_4 = (1 - D) \sqrt{\frac{2}{(1 + n k)(1 - k)}} \cdot \frac{\lambda L_m I_{in} T_s}{V_{in} D}.$$  \hspace{1cm} (25)

An important step in the steady-state analysis of the proposed converter is determining the values of the passive elements $L_m$, $C_1$, $C_2$ and $C_3$. Initially, the value of $L_m$ is chosen to guarantee that the magnetizing current ripple ($\Delta I_{Lm}$) be limited to some prespecified level. The relation between $L_m$ and $\Delta I_{Lm}$ can be computed from the waveforms shown in Fig. 3, as given by

$$L_m = \frac{k D T_s}{\Delta I_{Lm}} \cdot V_{in}.$$  \hspace{1cm} (26)

From Fig. 2 it is possible to demonstrate that the capacitances $C_1$, $C_2$ and $C_3$ relate with the respective voltage ripples $\Delta V_{C1}$, $\Delta V_{C2}$ and $\Delta V_{C3}$ as follows:

$$C_1 = \frac{T_s}{\Delta V_{C1}} \cdot I_o,$$  \hspace{1cm} (27)

$$C_2 = \frac{D T_s}{\Delta V_{C2}} \cdot I_o,$$  \hspace{1cm} (28)

$$C_3 = \frac{(1 - D) T_s}{\Delta V_{C3}} \cdot I_o.$$  \hspace{1cm} (29)

Finally, the voltage stresses on the semiconductor devices can be computed from the analysis of the topological states depicted in Fig. 2. In the proposed converter, the blocking voltage of both $S$ and $D_1$ are equal to $V_{C1}$ (given in (23)), while $D_2$ and $D_3$ are subjected to $V_o - V_{C1}$ (given in (30)).

$$V_{D2} = V_{D3} = \frac{k n}{1 - D} \cdot V_{in}$$  \hspace{1cm} (30)

A. COMPARATIVE ANALYSIS WITH OTHER SINGLE-SWITCH HIGH-STEP-UP DC-DC CONVERTERS

The comparison of the proposed converter with other high-step-up dc-dc converters is summarized in Table 1. This comparative analysis is restricted to circuits containing one single switch, one coupled inductor with only two windings, and the same number of diodes and capacitors as the proposed converter. The efficiency is estimated based on SPICE simulations using the following devices: MOSFET IRFP4668PBF ($V_{DSS} = 200$ V; $R_{DSon} = 8$ m$\Omega$) and MUR840 diodes ($V_{RRM} = 400$ V; $V_F = 0.75$ V; $R_f = 11$ m$\Omega$). Among all converters, only [7] needs a snubber circuit to prevent the occurrence of voltage spike on the switch. If such snubber is not included, the efficiency of this circuit becomes considerably reduced. Regarding the circuit introduced in [10], which is based on the zeta-type configuration, an isolated gate driver and higher energy on the capacitors are required. In comparison with the topologies presented in [11], [12], [13], and [14], the proposed converter has a lower voltage gain considering the same conditions of $D$ and $n$. Therefore, the number of turns ratio must be increased to ensure the same voltage gain at a particular duty cycle level. However, in [11], the secondary winding inductance directly influences the converter voltage gain, which has a direct impact on the volume and conduction loss of the coupled inductor, and, in such introduced converters, more energy must be processed by the capacitors under similar operating conditions, which would inevitably increase the cost and size of the circuit. Among all solutions considered, only [8] requires a lower energy on the capacitors. Regarding [13] and [14], the blocking voltages on the active switches are higher than proposed converter, thus their estimated efficiencies are lower than the proposed converter under the same operating conditions.
TABLE 1. Comparison with other single-switch single-coupled-inductor high-step-up dc-dc converters.

| Coupled-inductor Based Circuit | Voltage Gain \((\frac{V_{o}}{V_{i}})\) | Voltage stress on the switch | Voltage stress on the diodes | Estimated efficiency \(\eta\) | \(\sum E_{c}\) |
|-------------------------------|----------------|----------------|-----------------|------------|----------|
| Proposed Converter           | \(\frac{1 + nk}{1 - D}\) | \(\frac{V_{in}}{1 - D}\) | \(\frac{k n V_{in}}{1 - D}\) | 97.6       | 160      |
| Converter in [7]             | \(1 + n k D\) | \(\frac{V_{in}}{1 - D}\) | \(\frac{k n V_{in}}{1 - D}\) | 96.7       | 267      |
| Converter in [8]             | \(1 + n k\) | \(\frac{V_{in}}{1 - D}\) | \(\frac{k n V_{in}}{1 - D}\) | 97.3       | 150      |
| Converter in [10]            | \(\frac{1 + n k}{1 - D}\) | \(\frac{V_{in}}{1 - D}\) | \(\frac{k n V_{in}}{1 - D}\) | 97.0       | 343      |
| Converter in [11]            | \(2 + n k\) | \(\frac{V_{in}}{1 - D}\) | \(\frac{k n V_{in}}{1 - D}\) | 97.6       | 290      |
| Converter in [12]            | \(\frac{(2 + n k) + (n k - 1) D}{1 - D}\) | \(\frac{(1 + kn)V_{in}}{1 - D}\) | \(\frac{(1 + k n)V_{in}}{1 - D}\) | 97.3       | 291      |
| Converter in [13]            | \(\frac{(1 + 2 n k + n k D)}{1 - D}\) | \(\frac{(1 + kn)V_{in}}{1 - D}\) | \(\frac{(1 + kn)V_{in}}{1 - D}\) | 96.4       | 280      |
| Converter in [14]            | \(\frac{(1 + nk + 2 nk D)}{1 - D}\) | \(\frac{(1 + kn)V_{in}}{1 - D}\) | \(\frac{(1 + kn)V_{in}}{1 - D}\) | 95         | 325      |

1Voltage on Diode snubber
2Limited by snubber RCD

1The voltage stress on the \(D_{2}\) and \(D_{4}\) is not informed in the published papers.
2Efficiency estimated by the Orcad 17.2 Lite computing software considering: \(f_{s} = 100\ kHz\), \(D = 65\%\) and \(P_{o} = 400\ W\). Similar parasitic resistances were included to estimate conduction and magnetic losses on the coupled inductor.

Based on the results of the comparative analysis, it can be concluded that the proposed circuit shows potential advantages for high-step-up operation, as it exhibits high efficiency and requires a relatively low capacitive energy. An important remark is that, although the proposed circuit does not have the higher voltage gain among all the circuits considered, its estimated performance under operating conditions similar to typical PV modules makes it a good candidate for low power PV applications.

V. DESIGN PROCEDURE

A design procedure is elaborated for the adequate design of the proposed converter using the key results derived in the mathematical analysis carried out in section IV, as detailed in the following steps:

1 – Define the value of the voltage on \(C_{1}\) according to the desired voltage stress on \(S\);
2 – From (23) compute the duty cycle \(D\);
3 – Assuming a realistic value for \(\lambda\) (typically something in the range 1–5\%), compute \(k\) using (1) and determine \(n\) from the static gain expression given in (20);
4 – Calculate \(V_{C2}\) and \(V_{C3}\) through (21) and (12), respectively;
5 – Define the current ripple \(\Delta I_{Lm}\) and calculate \(L_{m}\) using (26);
6 – Define the voltage ripples \(\Delta V_{C1}\), \(\Delta V_{C2}\) and \(\Delta V_{C3}\) and compute \(C_{1}\), \(C_{2}\) and \(C_{3}\) using (27), (28) and (29), respectively.

TABLE 2. Design specifications for the 400 W prototype.

| Description                  | Value  |
|------------------------------|--------|
| \(V_{in}\)                   | 48 V   |
| \(f_{s}\)                    | 90 kHz |
| \(P_{o}\)                    | 400 W  |
| \(V_{C1}\)                   | 400 V  |
| \(C_{1}\)                    | 150 V  |
| \(\Delta I_{Lm}\)            | 40 % of \(I_{m}\) |
| \(\Delta V_{C1}\)            | 5 % of \(V_{C1}\) |
| \(\Delta V_{C2}\)            | 1 % of \(V_{C2}\) |
| \(\Delta V_{C3}\)            | 1 % of \(V_{C3}\) |

TABLE 3. Specified parameters.

| Parameter | Value               |
|-----------|---------------------|
| \(n\)     | 1.72                |
| \(D\)     | 0.68                |
| \(k\)     | 0.98                |
| \(I_{m}\) | 80 \(\mu H (E42/15) \rightarrow n_{r}=14; n_{r}=24\) |
| \(C_{1}\) | 1 \(\mu F\)        |
| \(C_{2}\) | 4.4 \(\mu F\)      |
| \(C_{3}\) | 4.4 \(\mu F\)      |

Following the previous steps and applying the design specifications presented in Table 2, the converter parameters presented in Table 3 can be found.
VI. DYNAMIC MODEL

In practical applications, the proposed converter must operate in closed loop to ensure that some desired control output (e.g., input current or output voltage) be properly regulated. For instance, in typical grid-tied PV systems, the step-up dc-dc converter is responsible for adjusting its input current (or input voltage) to realize the maximum power point tracking (MPPT) algorithm. Therefore, the behavior of the circuit under transient conditions must be well understood, so the designer is able to determine an adequate compensator for proper closed-loop operation. In this work, a small-signal model is derived based on the operating stages depicted in Fig. 2. The technique used in this analysis is based on the Taylor’s series expansion of the non-linear set of equations given in (2)–(14), considering the rated output power condition as the quiescent point. However, since the algebraic solution of the dynamic analysis is very extensive, only the resulting transfer function of the input current versus duty cycle considering the data shown in Tables 2 and 3 is presented, as given in (31).

\[
\hat{i}_{\text{in}}(s) = \frac{6.5 \times 10^6 s^2 + 7.5 \times 10^{11} s + 1.3 \times 10^{15}}{3.56 s^3 + 4 \times 10^{5} s^2 + 9.95 \times 10^8 s + 2.54 \times 10^{12}}
\]

(31)

In this study, the input current is chosen to be controlled, and the control scheme follows the block diagram depicted in Fig. 5. Here, a simple proportional-integral (PI) compensator is enough to ensure stability and proper response of the system in closed-loop operation. Using the transfer function (31) and considering requirements of an overshoot lower than 20% and a zero-crossing frequency of 1.7 kHz, it is possible to determine the proportional and integral gains of 0.005 and 15, respectively. This yields a controller’s transfer function composed of a pole at the origin, a zero at 477.46 Hz and a gain of 15, as given by (32). The controller is implemented using the digital signal processor TMS320F28377S and the current is measured with the Hall effect current transducer LAH 25-NP. Fig. 6 depicts the converter response in closed-loop operation for steps changing the input current reference from 8.4–9.4 A and 9.4–8.4 A.

VII. EXPERIMENTAL RESULTS

A 400 W prototype of the proposed converter using the data presented in Tables 2 and 3 was built to verify the feasibility of the proposed converter. A picture of the experimental setup is shown in Fig. 7.

Fig. 8 presents the waveforms of the input voltage, input current and output voltage. The input current corresponds to the signal measured before the decoupling capacitor $C_{\text{in}}$, and hence some filtering is achieved. The voltages on $C_1$, $C_2$ and $C_3$ are shown in Fig. 9. The measurements indicate that the experimental results are in agreement with the theoretical predictions given in (21)–(23). The waveforms of the voltage and current on $S$ are shown in the Fig. 10. As expected, the blocking voltage corresponds to the value of $V_{C1}$ defined by (23). Fig. 11 presents the...
turn-on/turn-off transient intervals regarding \( S \). Even though ZVS is not achieved, the turn-on loss is low because there is almost no simultaneous current and voltage during this interval. Fig. 12 shows the waveforms of the voltage and current on \( D_1 \), \( D_2 \) and \( D_3 \), respectively. It can be observed that the blocking voltage values are close to those defined by (23) and (30). In addition, zero-current-switching (ZCS) is verified for \( D_1 \) and \( D_3 \) and it is noticeable that the turn-on loss on \( D_2 \) is low, thus contributing to enhancing the overall converter efficiency.

Fig. 13 presents the system efficiency measured with a Yokogawa WT500 precision power analyzer. Fig. 13 (a) illustrates the efficiency curve as function of the variation of the output power. Values of 96.5\% and 97.5\% at 100\% and 20\% of the rated output power, respectively, have been achieved by the proposed high step-up converter.

In applications in which nominal power is maintained while the input voltage is reduced, the proposed converter presents efficiency levels according to Fig. 13 (b).

As expected, efficiency is also reduced as the input voltage decreases due to higher current stresses. However, a more realistic condition is to consider that the output power is also reduced for lower input voltage conditions, which leads to a lower efficiency drop at low voltage levels, as shown in Fig. 13 (c).

It is noteworthy that an unusual behavior on the efficiency curve can be observed in Fig. 13 (a) at 20\% of rated output power, which is a consequence of better switching conditions due to operation in the discontinuous conduction mode. This improved operating condition can be verified by the drain-to-source (\( v_{DS} \)) and gate-to-source (\( v_{GS} \)) voltages on the MOSFET at 20\% of output power, as shown in Fig. 14. As can be seen, at this particular operating point, the switching occurs at zero voltage (ZVS), which can be explained by the fact the converter enters in the discontinuous conduction mode and the turn-on of the MOSFET occurs at the valley of the resonant transition occurring after \( L_m \) is completely discharged.
FIGURE 13. Efficiency measurements: (a) as function of output power; (b) as a function of input voltage with \( P_o = 400 \) W; and (c) as function of input voltage and output power.

FIGURE 14. Drain-to-source (\( V_{DS} \)) and gate-to-source (\( V_{GS} \)) voltage on the MOSFET at 20% of rated output power.

Operation at 10% of rated output power was also investigated and the waveforms of voltage and current on S are provided in Fig. 15 for this condition.

Finally, proper closed-loop operation is demonstrated in Fig. 16, which depicts the response of the input current for 4–8.5 A and 8.5–4 A reference steps with the output voltage fixed at 400 V. For this test, the constant voltage load was implemented using the 4-quadrant ac-load NHR 9430.

VIII. CONCLUSION

This paper introduced a single-switch high-voltage-gain dc-dc converter based on the boost converter employing coupled inductor and voltage multiplier cell. The main advantages of the proposed topology are high efficiency, natural voltage clamping in all semiconductors and reduced component count. Both static and dynamic analyses were detailed in the paper, and a comprehensive design methodology was proposed to ensure proper closed-loop operation. The feasibility of the converter was demonstrated through experimental tests with a 400 W prototype operating with a voltage conversion ratio in the range of 8.33–13.33 and a switching frequency of 90 kHz. Measurements indicated a maximum efficiency of 97.5% at approximately 80 W and an efficiency level of 96.5% at nominal conditions. It is also remarkable that the efficiency is higher than 96% for the entire range of 10–100% of rated output power. Based on the results, the proposed converter shows itself as a good candidate for typical single-module PV applications, in which voltage levels in the order of tens of Volts and power levels up to several hundreds of Watts are usual.
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