Dielectric Engineered Tunnel Field-Effect Transistor

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Abstract—The dielectric engineered tunnel field-effect transistor (DE-TFET) as a high performance steep transistor is proposed. In this device, a combination of high-k and low-k dielectrics results in a high electric field at the tunnel junction. As a result a record ON-current of about 1000 uA/um and a subthreshold swing (SS) below 20mV/dec are predicted for WTe$_2$ DE-TFET. The proposed TFET works based on a homojunction channel and electrically doped contacts both of which are immune to interface states, dopant fluctuations, and dopant states in the band gap which typically deteriorate the OFF-state performance and SS in conventional TFETs.

Index Terms—TFETs, dielectric engineering, electrical doping.

I. INTRODUCTION

Tunnel FETs (TFETs) are strong candidates for future electronics applications due to their promise of low power consumption originating from their subthreshold-swing (SS) being less than the conventional limit of 60 mV/dec [1]. However, TFETs usually suffer from lower ON-currents if compared to ultra-scaled MOSFETs [2], since their currents are the result of the tunneling process. To overcome the low ON-current challenge, two obvious solutions are: 1) Increasing the electric field at the tunnel junction, 2) decreasing the band gap and effective mass of the channel material. However, reducing the band gap increases the OFF-current of the device and limits the maximum allowable supply voltage $V_{DD}$. Accordingly, there is a lower limit on the band gap for any $V_{DD}$ ($E_g \geq qV_{DD}$).

Previous approaches for increasing the electric field at the tunnel junction included using an internal field (i.e. piezoelectric field) in nitride heterostructures [3] or employing 2D channel materials with tight gate control [4], [5]. In this work, a new method for increasing the electric field is proposed. It is shown that using a low-k dielectric next to high-k dielectrics can, in principle, increase the electric field in homo-junction TFETs significantly. The structure of the dielectric engineered TFET (DE-TFET) is shown in Fig. 1a. At the interface between the dielectrics, the displacement vector should be continuous ($\epsilon_1 E_1 = \epsilon_2 E_2$). With $\epsilon_2 \ll \epsilon_1$, the low-k dielectric has a larger electric field $E_2$ as illustrated in Fig. 1b. Since the high electric field region occurs right at the top of the tunnel junction, the ON-current of the device is amplified. Notice that the same idea (combination of high-k and low-k dielectrics) can be used in other device structures; e.g. gate-all-around, double and single gated TFETs.

Fig. 1 compares the potential profile for a conventional electrically doped TFET (ED-TFET) [6] with that of a DE-TFET. In case of the ED-TFETs, the width of the potential spread is proportional to the total thickness of the device $T_{tot}$ (the body thickness plus the oxide thickness shown as $T_{tot}$ in Figs. 1a and 1b). In contrast, most of the potential drop in the DE-TFET occurs over the width of the low-k dielectric region (labeled as $S$ in Fig. 1a). Equation (1) compares the average electric field of a conventional ED-TFET with that of the DE-TFET showing a possible gain in the electric field for the DE-TFET (as long as $S < 4T_{tot}/\pi$).

$$\langle E_{-TFET} \rangle \approx \frac{V_1 - V_2}{S} > \langle E_{-TFET} \rangle \approx \frac{\pi V_1 - V_2}{4T_{tot}} \quad (1)$$

Furthermore, the DE-TFET offers several other advantages:
1) The performance is not very sensitive to the spacing (shown as $S$ in Fig. 1) when $S$ is chosen around the optimum value, in contrast to the conventional ED-TFET in which the ON-current decreases monotonically with increasing $S$ [6] (i.e. lack of optimum $S$: $\frac{dI_{ON}}{dS} \neq 0$). 2) Increasing the oxide thickness does not deteriorate the performance of the device, while the performance of electrically doped devices strongly depends on the thickness [6]. 3) There is no need for chemical doping which means the DE-TFET does not exhibit the drawbacks of chemically doped devices [7] (i.e. dopant states in the bandgap which deteriorate the OFF-state performance and SS in addition to the disorder introduced by fluctuations in dopant locations). Note that despite the oxide thickness having less impact on the performance of the DE-TFETs compared to ED-TFETs, a thinner oxide is still slightly beneficial for an improved ON-state.

In Section III, full-band quantum transport simulations are performed on a monolayer WTe$_2$ homojunction DE-TFET to investigate its performance. The performance sensitivity of the DE-TFETs to the spacing, thickness, and channel material (WSe$_2$ and WTe$_2$) is discussed by both analytic modeling and numerical simulations in Section IV.
II. SIMULATION DETAILS
To represent WSe$_2$ and WTe$_2$ as channel materials of the DE-TFET atomistically, we have utilized a sp$^3$d$^5$ 2nd nearest neighbor tight-binding model with spin-orbit coupling. Atomistic quantum transport simulations employing a self-consistent Poisson-NEGF (Non-equilibirum Green’s Function) method have been utilized. The details of the simulation methods and material properties can be found in [4]. The simulated double gated DE-TFETs assume a structure shown in Fig. 1(a). Each gate has a length of 12nm, with the low-k spacing $S$. Notice that the low-k dielectric fills the space between the gates, right on top of the tunnel junction. A source-drain voltage $V_{DS}$ of 0.8V is used throughout, and the relative dielectric constants of high-k and low-k dielectrics are set to 20 and 1 (i.e. air gap) respectively unless mentioned otherwise. The total thickness of the device equals 4.4nm by default, including the body thickness of the channel ($\approx 0.7nm$). All of the transport simulations have been performed with the simulation tool NEMO5 [8].

Fig. 2: a) Physical structure, transfer characteristics, and b) band diagrams of a monolayer WTe$_2$ double gated DE-TFET with left and right oxide lengths of 12nm. $V_{G2}$ is fixed to 1V. c) The dependence of the ON-current of a WTe$_2$ DE-TFET on the spacing for different $T_{tot}$. d) Comparison of performance sensitivity to $T_{tot}$ of WTe$_2$ DE-TFET with ED-TFET.

III. SIMULATION RESULTS
Fig. 2 shows transfer characteristics of a monolayer WTe$_2$ DE-TFET with an ON-current of about 1000 $\mu$A/um and SS of 16 mV/dec. This is a record $I_{ON}$-value among all reported ON-currents from full band atomistic simulations of planar homojunction steep devices [9]. Having a high ON-current without using a hetero-junction and chemical doping has advantages in terms of OFF-state performance. Chemical doping can introduce dopant states within the band gap [7], and hetero-junctions often suffer from interface states. Both of these effects increase SS of the device. Fig. 2(b) shows the conduction and valence band profiles of the WTe$_2$ DE-TFET. The electric field at the tunnel junction is about 0.9 V/nm. This large value of electric field and ON-current is due to the presence of the low-k dielectric ($\epsilon_2 \ll \epsilon_1$).

The ON-current of a WTe$_2$ DE-TFET as a function of low-k spacing is shown in Fig. 2(c). The optimum spacing $S$ to gain the maximum ON-current depends on the total thickness of the device (shown as $T_{tot}$ in Fig. 2(a)). For example, the optimum $S$ varies from about 1nm to 2nm when $T_{tot}$ changes from 4.4nm to 10.2nm. Fig. 2(d) compares the performance sensitivity of the WTe$_2$ DE-TFET with the conventional ED-TFET. The performance of the DE-TFET is much less sensitive to oxide thickness variations if compared to the conventional ED-TFET.

IV. ANALYTICAL MODELING
It is apparent that the width of the low-k dielectric ($S$) affects the performance of DE-TFETs. When $S$ equals 0, the device converts to a conventional ED-TFET and the electric field at the tunnel junction reduces. On the other hand, when $S$ becomes very large, the electric field reduces to 0. Accordingly, there exists an optimum spacing where the electric field is high. Notice that achieving the highest electric field is not a sufficient condition to ensure best performance. For example, if the electric field is high only over a very small distance such that the potential drop across the low-k dielectric is not large enough (compared to the band gap), then the tunneling window with high field will be small.

Fig. 3 shows the conduction band profile for a WTe$_2$ DE-TFET with different spacing values. The lower the spacing, the higher is the electric field. However, this does not always translate into better performance. For example, a spacing of 0.5nm has a larger electric field compared to the spacing of 1.0nm but the energy window with high electric field of $S$ varies from about 1nm to 2nm when $T_{tot}$ changes from 4.4nm to 10.2nm. Fig. 2(b) compares the performance sensitivity of the WTe$_2$ DE-TFET with the conventional ED-TFET. The performance of the DE-TFET is much less sensitive to oxide thickness variations if compared to the conventional ED-TFET.

To understand the impact of low-k spacing $S$ on the potential profile and performance, an analytic model is developed. For the case of $S = 0$, it was previously proven that the potential can be described by a $\exp(-x/\lambda)$ dependence with $\lambda = T_{tot}/x$ [4]. For the sake of simplicity, the channel thickness is assumed to be 0 first ($t_{ch} = 0$). Later, on, an empirical term is added to include the impact of $t_{ch}$. Simulations reveal that in the case of DE-TFETs, the potential is linear within the low-k dielectric as shown in Fig. 3. Accordingly, the potential profile can be approximated as:

$$V \approx \begin{cases} 
-V_1 & x < x_M - \frac{S}{2} \\
\frac{\Delta V_S}{S} (x - x_M) + \frac{V_1 + V_2}{2} & x_M - \frac{S}{2} < x < x_M + \frac{S}{2} \\
-V_2 & x > x_M + \frac{S}{2}
\end{cases}$$

(2)

Here, $\Delta V_S$ is the potential drop across the low-k dielectric and $x_M$ is the position of the center of the low-k dielectric.
To determine $\Delta V_S$, a capacitor network is used as shown in Fig. 3b.

$$\Delta V_S = \frac{S}{S + 2\epsilon_2 \lambda + \delta_{ch}} (V_1 - V_2) \quad (3)$$

where $\delta_{ch}$ is an empirical term to include the impact of the channel ($\delta_{ch} = 2t_{ch}/\pi$). Fig. 3b compares the analytic potential using (2) and (3) with the numerical solution of the 2D Poisson equation which shows that the analytic solution captures the effect of the low-k spacing $S$ and the ratio of dielectric constants ($\epsilon_1/\epsilon_2$) accurately. The maximum performance as a function of $S$ occurs when $\Delta V_S$ becomes a significant portion of the total band bending ($\Delta V_{BS} / V_1 \approx 0.6 - 0.7$).

$$S_{opt} \approx t_{ch} + \frac{\epsilon_2}{\epsilon_1} T_{tot} \quad (4)$$

Fig. 3c depicts the optimum spacing ($S_{opt}$) for the best performance of WTe$_2$ and WSe$_2$ DE-TFETs. Notice that $S_{opt}$ does not depend on the material significantly.

**Fig. 3:** a) Conduction band profile ($E_c$) of WTe$_2$ DE-TFETs with different $S$ obtained from atomistic simulations. b) Different sections of $E_c$ profile and equivalent capacitance network. c) Comparison between the analytic model (circle symbols) and numerical solution (solid lines) for various $S$ (left side) and $\epsilon_1/\epsilon_2$ values (right side). d) Comparing $S_{opt}$ in WTe$_2$ (dashed lines) and WSe$_2$ (solid lines) DE-TFETs with a $T_{tot}$ of 4.4nm (red curves labeled as thin) and 7.3nm (black curves labeled as thick).

**V. Conclusion**

In summary, a new high performance TFET is proposed with a simulated record ON-current of 1000 $\mu$A/um and SS of 16 mV/dec. The high performance and high electric field in DE-TFETs is a result of the combination of low-k and high-k dielectrics. Moreover, DE-TFETs offer other advantages: e.g., smaller sensitivity to the oxide thickness compared to conventional ED-TFETs. The same idea can be applied to other device structures (e.g. nanowire TFETs) and other channel materials (e.g. III-V materials) to bring the ON-current of TFETs on par with MOSFETs and keep their excellent OFF-state performance intact.

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