Design optimization for capacitive-resistively driven on-chip global interconnect

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Abstract: On-chip global wires are speed and power bottleneck in state-of-the-art chips. AC coupling technique is an efficient way to reduce interconnection delay and power. This paper proposes a new capacitive-resistively driven AC coupling global link. Bandwidth performance of the proposed wire is analyzed and an optimization algorithm for capacitive-resistively driven wire is presented. Simulation results show that our optimization methodology can improve the bandwidth. By applying our optimization algorithm, data rate can be improved from 2 Gb/s to 2.5 Gb/s in the implemented transceiver circuit. The proposed optimization algorithm can be applied in high speed global communication.

Keywords: AC coupling, global interconnect, high speed, on-chip, low power

Classification: Electron devices, circuits, and systems

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1 Introduction

With technology scaling down, local wires shrink with transistors in VLSI chips. Global wires shrink in cross section area, but do not shrink in length when devices get smaller [1]. In 2.5D ICs, global wires need to undertake the long die-to-die communication on a silicon carrier. On-chip global wires have increased speed and power problems. Many techniques have been proposed to reduce delay and energy consumption in global communication. Among these solutions, repeater insertion is simple, but the performance is limited by the area and delay from the inserted cell itself [2]. Modulation [3] and transmission line [4] benefit from the effect of the wire inductance, however, they tend to operate at very high frequency or need larger sized wires. Current mode signaling can achieve high speed, but has problems from power consumption [5]. AC coupled links have been taken as good candidates for high speed chip-to-chip communication [5, 6]. As one type of the AC coupled links, the capacitive pre-emphasis circuit has a bandwidth as the current mode signaling and achieves low swing signaling without a second power supply [7, 8, 9]. AC coupled wire is a promising solution for on-chip communication.

In Fig. 1, different types of wire are presented. In a conventional wire, as shown in Fig. 1(a), the bandwidth is limited by the wire resistance and capacitance. Either a small resistance or a coupling capacitance can increase the bandwidth of a wire, which is described in Fig. 1(b) and (c). To further improve the bandwidth, as in Fig. 1(d), a capacitive-resistive pre-emphasis technology is proposed in [10]. By adding a resistance to ground, the bandwidth of capacitively driven wire can be improved. Since a resistance to ground can improve the bandwidth in Fig. 1(b) and Fig. 1(d), we can combine Fig. 1(b) with Fig. 1(c) to get a new different capacitive-resistively driven wire.

![Fig. 1. Wires for global interconnect: (a) Conventional wire, (b) Current mode wire, (c) Capacitively driven wire, (d) Capacitive-resistively driven wire in [10], (e) Proposed capacitive-resistively driven wire.](image-url)
tive-resistively driven wire as in Fig. 1(e). To explore the difference of the different capacitively driven wires, in this paper, the bandwidth performance will be presented and compared. To further improve the performance, design optimization methodology for capacitive-resistively driven on-chip global interconnect is discussed. The rest of this paper is organized as follows. In Section 2, performance of the proposed wire is analyzed. Simulation environment is setup to verify our analysis. In Section 3, we present an optimized design methodology. The proposed design is simulated and discussed. Finally, the results are analyzed and compared.

2 Bandwidth analysis

2.1 Bandwidth performance analysis

In order to interpret the performance of the different wires, analytical method is applied for bandwidth analysis.

The global wire with a driver pre-emphasis circuit can be modeled as a two-port network as shown in Fig. 2(a), where the $V_{out}$ is the output voltage and $Z_L$ is the load impedance. For capacitively driven wire, as described in Fig. 1(c), the load impedance typically represents the input capacitance of the receiver. For the proposed capacitive-resistively driven wire in Fig. 1(e), the load impedance includes the resistance to ground and the input capacitance of the receiver. In this paper, a distributed model is applied to reduce the accuracy loss in the analysis. In a capacitively driven wire, the pre-emphasis circuit can also be modeled as a two-port network as described in Fig. 2(b). In Fig. 2(b), the transmission matrix of the pre-emphasis circuit in the frequency domain is as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{sC_C} \\ 0 & 1 \end{bmatrix}. \tag{1}$$

For the global wire using distributed $RLC$ model, the closed-form expression of its transmission matrix in the frequency domain is given by [11]

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0\sinh(\gamma l) \\ \frac{1}{Z_0}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \tag{2}$$

where $\gamma$ is the propagation constant, $l$ is the length of the wire and $Z_0$ is the line characteristic impedance. So, in Fig. 2(a), the transmission matrix of the wire with pre-emphasis circuit can be represented by

![Wire model: (a) Wire model with pre-emphasis circuit, (b) Capacitively driven pre-emphasis circuit.](Image)
\[
\begin{bmatrix}
V_{in} \\
I_{in}
\end{bmatrix} = \begin{bmatrix}
A_1 & B_1 \\
C_1 & D_1
\end{bmatrix} \begin{bmatrix}
A_2 & B_2 \\
C_2 & D_2
\end{bmatrix} \begin{bmatrix}
V_{out} \\
I_{out}
\end{bmatrix}.
\]  

(3)

Since the inductive components could not dominate resistive components until tens of GHz, the long and narrow on-chip interconnects are normally represented by a distributed RC model. In this paper, RC models are applied for global interconnect analysis. By applying the RC model, in Eq. (2), the wire characteristic impedance \(Z_0\) is defined as:

\[
Z_0 = \sqrt{\frac{R}{sC}}.
\]

(4)

In RC model, we also have

\[
\gamma l = \sqrt{sRC}.
\]

(5)

We can rewrite Eq. (3) as

\[
\begin{bmatrix}
V_{in} \\
I_{in}
\end{bmatrix} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix} \begin{bmatrix}
V_{out} \\
I_{out}
\end{bmatrix}.
\]

(6)

where \(A = A_1 A_2 + B_1 C_2\), \(B = A_1 B_2 + B_1 D_2\). So, the transform function of the wire is

\[
H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{A + \frac{B}{Z_L}}
\]

(7)

where

\[
A = \cosh(\gamma l) + \frac{1}{sC} \frac{\sinh(\gamma l)}{Z_0}
\]

(8)

and

\[
\frac{B}{Z_L} = \frac{1}{sC} \frac{\cosh(\gamma l)}{Z_L} + \frac{Z_0}{Z_L} \frac{\sinh(\gamma l)}{Z_L}.
\]

(9)

In Eq. (7) to (9), \(Z_L\) is the load impedance of the wire and can be represented by

\[
Z_L = \frac{R_L}{sR_L C_L + 1}.
\]

(10)

As \(\cosh(\gamma l)\) and \(\sinh(\gamma l)\) can be expanded in Maclaurin series, we can get

\[
\cosh(\gamma l) = \sum_{n=0}^{\infty} \frac{(\gamma l)^{2n}}{(2n)!}
\]

(11)

and

\[
\sinh(\gamma l) = \sum_{n=0}^{\infty} \frac{(\gamma l)^{2n+1}}{(2n + 1)!}
\]

(12)

In a capacitively driven wire as described in Fig. 1(c), \(R_L\) is infinite. So we can get

\[
\frac{1}{Z_L} = sC_L
\]

(13)

With Eq. (8) to Eq. (13), we have
\[
H(s) = \frac{1}{A + \frac{B}{Z_L}} = \frac{1}{a_0 + a_1 s + \ldots + a_n s^n}, \tag{14}
\]

where \( s = 2\pi f \), \( f \) is the signal frequency. So we have

\[
H(s) = \frac{1}{a_0 + a_1 s + O(s^2)} \tag{15}
\]

where

\[
a_0 = \frac{C_c + C + C_L}{C_c},
\]

\[
a_1 = \frac{RC}{2} + \frac{RC^2}{6C_c} + \frac{RCC_L}{2C_c} + RC_L,
\]

\[
O(s^2) = \left(1 + \frac{C_L}{C_c}\sum_{n=2}^{\infty} \frac{(2n)!}{(2n)^n} + \left(\frac{C}{C_c} + sRC_L\right)\sum_{n=2}^{\infty} \frac{(2n)!}{(2n + 1)!} + \frac{R^2CC_Ls^2}{6}\right). \tag{16}
\]

In typical applications, a transceiver system includes the driver, wire and the receiver as described in Fig. 3. In this paper, the length of interconnect is chosen to be 10 mm. The parameter of the wire is calculated based on Taiwan Semiconductor Manufacturing Company (TSMC) 1.0 V 1P9M 90 nm CMOS low-K technology. The total interconnect parameters are derived as in [12]. We have

\[
R = 120 \text{ ohm/mm}, \quad C = 223 \text{ fF/mm}.
\]

The load of the global wire is from the input capacitance of a receiver such as the input capacitance of a sense amplifier or an equalizer. In this paper, we assume the load \( C_L \) is from a 100 fF capacitive equalizer. The ratio of \( C_c \) to \( C \) is set small to get a low swing output as in [7, 8, 9]. The signal frequency is assumed to be 2 GHz. So, in this paper, we have

\[
|a_0 + a_1 s| \gg |O(s^2)|. \tag{17}
\]

And, we can get the approximation of Eq. (15)

\[
A + \frac{B}{Z_L} \approx \frac{C_c + C + C_L}{C_c} + \frac{C}{C_c} \frac{RC}{6} s. \tag{18}
\]

The transfer function of the capacitively driven wire can be approximated as a dominant pole system as
From Eq. (19), we can find that capacitively driven wire acts as a low pass filter, just as the conventional wire. In a capacitively driven wire, the first order delay is about $\frac{RC}{6}$. It is well known that the first order delay of a conventional wire is $\frac{RC}{2}$. Compared to the conventional wire, the bandwidth is three times than the wire without a small coupling capacitor.

In the proposed wire that described in Fig. 1(e), $R_L$ is not infinite as in capacitively driven wire. Typically, it is small when compared to the wire resistance. So the load impedance of the wire and can be rewritten as:

$$Z_L = \frac{1}{sCL} + \frac{1}{RL}$$  \hspace{1cm} (20)

And Eq. (7) is

$$H(s) = \frac{sRLC_c}{b_0 + b_1s + b_2s^2 + \ldots + b ns^n + \ldots}$$  \hspace{1cm} (21)

The resistance to ground introduces a zero and also influences the distributions of poles in the system. This make the wire a band pass filter as:

$$H(s) = \frac{sRLC_c}{1 + R_L C_c S_0 s + R_L C_s S_1 s^2 + R_L C_O(s^3)}.$$  \hspace{1cm} (22)

In Eq. (22), two parameters $S_0$ and $S_1$ are used to make the expression easy for reading, where

$$S_0 = 1 + \frac{C}{C_c} + \frac{C_L}{C_c} + \frac{R}{R_L} + \frac{RC}{2 R_L C_c}, \quad S_1 = \frac{RC}{2} + \frac{RC^2}{6C_c} + \frac{R C L}{2 C_c} + \frac{R C L C_c}{6R_L C_c} + \frac{R^2 C}{24 R_L C_c},$$

$$O(s^3) = \frac{s^3 R^2 C^2}{24} + \sum_{n=3}^{\infty} \frac{(-1)^n}{(2n)!} \left( \frac{C_L}{C_c} + \frac{1}{sRLC_c} \right)^n s^3 + \sum_{n=3}^{\infty} \frac{(-1)^n}{(2n+1)!} \left( 1 + \frac{C}{C_c} + sRCL + \frac{R}{R_L} \right)s.$$  \hspace{1cm} (23)

In Eq. (22), the $R_L$ could affect the choice of higher order terms to keep the accuracy of transfer function. In most cases, we can not get a simple approximated model as in the capacitively driven wire. Therefore, simulation is supplemented to demonstrate the bandwidth performance.

### 2.2 Bandwidth simulation

HSPICE simulations are performed for the conventional, capacitively driven and new proposed capacitive-resistively driven wires. In order to explorer the wire performance, we first ignore the driver impedance in this section and keep the other parameters as that in Section 2.1. As analyzed in Section 2.1, the conventional and capacitively driven wires act as low pass filers. The capacitive-resistively driven wire performs like a band pass filter. 3-dB bandwidth is taken as the wire bandwidth in this paper for performance analysis, which is described in Fig. 4(a).

In the simulation, the 3-dB bandwidth of the 10 mm conventional wire is 132.24 MHz. When the coupling capacitor having the size of $C/10$, 3-dB band-
width of the capacitively driven wire is 418.63 MHz. As analyzed in Section 2.1, the bandwidth is about three times than that in a conventional wire. When the size of the coupling capacitor is C/10 and the size of resistor to ground is R/10 in Fig. 1(e), 3-dB bandwidth of the capacitive-resistively driven wire is 865.49 MHz. However, the size of the coupling capacitor could affect the performance of the wire. Simulations are applied to explore this problem. In Fig. 4(b), the coupling capacitor is chosen to be from C/10 to C for a capacitively driven wire. When the ratio of \( \frac{C_c}{C} \) decreases, the bandwidth of the wire increases accordingly. We can also find that swing of the output signal decreases with the bandwidth increasing. To keep a reasonable swing at the output node, the ratio of Cc to C should be carefully selected. The simulation results of the proposed capacitive-resistively driven wire are shown in Fig. 4(c). Five groups of simulation have been carried out. In the simulations, the coupling capacitors having a size of C/10, C/20, C/30, C/40 and C/50 are selected. For each coupling capacitor, we increase the ratio of R to RL for observing the change in bandwidth and signal swing. If the ratio of C to Cc is 35 as proposed in [7], we find that the bandwidth and swing are 473.35 MHz and −34.5 dBV in Fig. 4(b). To keep a similar signal swing, the bandwidth is about 757 MHz in the new design. This happens when the coupling capacitor is C/10 and the ratio of R to RL is 5. Compared to the capacitively driven wire, the bandwidth is increased by about 50%.

Fig. 4. Simulation results: (a) Bandwidth calculation, (b) Bandwidth with capacitively driven wire, (c) Bandwidth with proposed wire.
3 Design optimization discussion

From Fig. 1, we can find that the difference between the proposed capacitively wire and the wire in [10] is only the location of the resistance to ground. As discussed in section 2, the resistor to ground can introduce a zero to the wire and improve its bandwidth. From this point, there may be other locations on the wire that may bring similar or even better performance. Simulations are performed to explore the influence of location of the resistor to ground and coupling capacitor on capacitive-resistively driven wire. In the simulations, the wire parameter and the load is kept the same as that in section 2. In order to make the simulation results more realistic, the driver impedance is set as 45 ohm, which is the output impedance of an inverter consisting of a 10u/0.1u pMOS transistor in TSMC 90 nm CMOS low-K technology.

3.1 Optimization for the location of resistor to ground

As presented in Fig. 5(a), we first put the coupling capacitor at the transmitter side and change the locations and value of resistance to observe the bandwidth variation.

Fig. 5. Simulation setup: (a) Optimization for the location of resistor to ground (b) Optimization for the location of coupling capacitor.

From the result of the Fig. 4(b) (c), in order to get a reasonable swing, the size of the coupling capacitor is selected as C/10 and the size of the resistor to ground is selected having a size of R, R/5, R/10, R/20 and R/30. Simulation results are presented in Fig. 6. In Fig. 6, when the location of the resistor changes, the bandwidth has two peaks for each resistor to ground. One peak is near the transmitter side, the other is near the receiver side. The location of the peaks changes with the size of the resistor. We can also observe that a smaller resistor to

Fig. 6. Bandwidth changes with the location of resistor to ground.
ground can achieve a larger bandwidth improvement before and after the location optimization.

3.2 Optimization for the location of coupling capacitor

According to [12], the location of the coupling capacitor can be optimized to improve the bandwidth in capacitively driven wire. In order to verify this optimized design methodology for capacitive-resistively driven wire, as in Fig. 5(b), we put the resistor to ground at the receiver side and change the locations and value of the coupling capacitor to observe the bandwidth variation. With the same consideration in Section 3.1, the size of the resistor to ground is selected as $R/10$ and the size of the coupling capacitor is selected having a size of $C/5$, $C/10$, $C/15$, $C/20$ and $C/30$. In Fig. 7, we find that the bandwidth can still change with location of the coupling capacitor on capacitive-resistively driven wire. The wire can be optimized by properly placing the coupling capacitor.

![Fig. 7. Bandwidth changes with the location of coupling capacitor.](image)

3.3 Optimization for both resistor and capacitor

From the results of Section 3.1 and 3.2, we can find that both the resistor to ground and coupling capacitor can be independently adjusted to optimize the design of capacitive-resistively driven wire. In order to explore whether the two optimization methods can be applied together, we first put the coupling capacitor at its optimized location and location of the resistor is changed to observe the bandwidth change.

Simulation results are described in Fig. 8. In this simulation, the coupling capacitor is located at the $1/4$ the wire length from the transmitter. In Fig. 8, when the resistor is put more close to the transmitter than the coupling capacitor, as the resistor to ground is at the left of the coupling capacitor in Fig. 5, the wire behaviors as a low pass filter. When the resistor moves toward the receiver, the resistor begins to locate at the right of the coupling capacitor, the wire behaviors as a band pass filter and the bandwidth is dramatically improved. From Fig. 8, we can find when the coupling capacitor is at the optimized location, the location of the resistor can still be optimized to improve the bandwidth of the wire. In other words, the two methods can be used together to optimized the design the capacitive-
resistively driven wire. However, there are some limitations in real circuit design. For example, for design considerations, the parameter of the capacitor and resistor to ground is limited to get a reasonable swing. The size of the capacitor and resistor should be easy for implementation. It is not easy to design a small resistor. So, an optimization Algorithm 1 is proposed as:

\begin{algorithm}
\caption{Capacitive-resistively driven wire optimization}
\begin{algorithmic}
\For{$C_{\text{coupling}} = C/50 : C/10$}
\For{$\text{Location } C \text{ coupling} = 0\% : 100\%$}
\For{$R \text{ to ground} = R/30 : R$}
\For{$\text{Location } R \text{ to ground} = 0\% : 100\%$}
{Get the 3-dB bandwidth}.
\EndFor
\EndFor
\EndFor
\EndFor
\end{algorithmic}
\end{algorithm}

3.4 Time domain simulation
In order to further verify our design optimization methodology, a transceiver circuit is implemented to achieve time domain simulation. The circuit structure is from [10], including the driver circuit, capacitive-resistively driven wire, equalizer and sense circuit as described in Fig. 9. The driver is an inverter consisting of a 20u/0.1u pMOS and 10u/0.1u nMOS transistor. M1 and M3 are 3u/0.1u nMOS transistors working as the resistance to ground. Inverter I2 and M2 are auto DC bias circuits. The inverter is consisting of a 4u/0.1u pMOS and 2u/0.1u nMOS transistor. M2 is a 0.4u/0.1u nMOS transistor. The receiver in Fig. 9(b) is a double tail sense amplifier from [8]. The coupling capacitor Cc1 and Cc3 have a size of 200fF and the equalizer Cc2 and Cc4 have a size of 100fF. By changing the location of the coupling capacitor and the resistor to ground, the input signal to sense amplifier before and after optimization is compared. In the implementation before optimization, the coupling capacitor is at the transmitter side, so as the resistor to ground. When the input bit rate is 2 Gb/s and the number of PRBS is $2^{12}$, the eye diagram of the input signal of the sense amplifier is presented in Fig. 10(a). We optimize the design by moving the coupling capacitor to the location which is 1/5 the wire length from the transmitter side. And the resistor to ground is moved to 3/10 the wire length from the transmitter side. The eye diagram of input signal of the sense amplifier is present in Fig. 10(b).
Fig. 9. Transceiver circuit for time domain simulation: (a) Transceiver circuit; (b) Double tail sense amplifier.

Fig. 10. Eye diagram of the received signal: (a) Eye diagram before optimization at 2 Gb/s; (b) Eye diagram after optimization at 2 Gb/s; (c) Eye diagram before optimization at 2.5 Gb/s; (d) Eye diagram after optimization at 2.5 Gb/s.
When the input bit rate is 2.5 Gb/s, the eye diagram of the input signal of the sense amplifier before optimization is presented in Fig. 10(c). In order to optimize the design at 2.5 Gb/s bit rate, we keep the location optimization as that in the simulation for 2 Gb/s bit rate and additionally reduce the coupling capacitor Cc1 and Cc3 from 200 fF to 150 fF. The eye diagram of input signal of the sense amplifier after optimization is present in Fig. 10(d). Compared Fig. 10(a) to Fig. 10(d), although the input data rate is increased by 25%, the optimized design can still keep the similar eye opening. If the sense amplifiers have the same threshold as 30 mV, in this implementation, the optimized design can achieve a 2.5 Gb/s, compared to 2 Gb/s before location optimization.

4 Conclusion

This paper proposed a new capacitive-resistively driven wire design style. Performance of the proposed wire is analyzed and an optimization methodology is proposed. HSPICE simulation environment is setup to validate our analysis. Simulation results show that the location of coupling capacitor or resistor to ground can be optimized to improve the 3-dB bandwidth of the wire. A transceiver circuit is also implemented to validate our design methodology in time domain. In this circuit, by applying our optimization algorithm, the data rate can be improved from 2 Gb/s to 2.5 Gb/s. The bandwidth and time domain simulation results show that the proposed circuit can be applied in high speed global communication.

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