Experimental Design of SRAM Type FPGA Single Particle Effect

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Abstract. The performance design of SRAM type FPGA single particle has been interrupted by its logical function failure, resulting in damage to its normal storage function and storage data. This research carries out the experimental design and discusses its feasibility based on the SRAM type FPGA single particle effect research to better improve the storage unit structure and capacity.

1. Introduction
SRAM (Static RAM) type FPGA (field programmable gate array) single particle can satisfy the diversity, repetitiveness, flexibility, and efficiency and can show the value of its experimental design at the same time.

2. Analysis of the necessity of experimental design
Affected by the energetic particle, the internal storage state of the FPGA processed by SRAM is not stable. The logic state of internal memory allocation is often flipped by the data transmission which will cause error. In the field of space flight, it can cause failure.

Fault tolerance and technology based on SRAM type FPGA single particle includes SEU shield, the structural design of anti radiation, a new anti radiation CMOS process, so it is necessary to improve the capacity and reduce the cost; The corresponding experimental design research focuses on the recovery of the back-end SEU flip effect, and analyzes the design plan and the necessary of design [1].

3. Basic survey of experimental design
3.1 Configuration principle
SRAM type FPGA single particle experiments rely on millions of configuration in the latch to store a value, at the same time in detail, the minimum group configuration read and write units and configure the frame column to achieve the configuration of the command word with the function of information command and configuration frame necessary.

The Configuring frame addressing is guided by the location and data of the block address (BA), the major address (MJA) and the minor address (MNA). The study of interior design according to the experimental design for the configuration of the 32bit configuration register, realizes the input of FDRI into FAR and control the configuration, refresh, and read back of COL [2].
3.2 Experimental performance analysis

3.2.1 Scrubbing. The main reason of failure of FPGA function is a bit configuration data in the flip. Once the recovery measures are taken inappropriately which causes the accumulated turn of several or more bit, it can not only cause the logic function disorder after the success of electric distribution, but the layout and implementation of a series of support is not up to the design requirements.

3.2.2 Read back comparison. The normal operation of FPGA depends on the accurate data of the isolated data after the completion of the configuration, that is to ensure the processing of the real time data such as LUT, RAM, SRL16 and BRAM in the memory of the sub unit structure. The realization of configuration function is the basic connection position on Select MAP or JTAG configuration interface. The original configuration and FPGA configuration information in the configuration latch is the fault-tolerant processing by FPGA single particle flip.

3.2.3 BRAM fault tolerant design. Whether RAM is a single port or a FLASH setting parameter, BRAM (Block RAM) is a special RAM area embedded in FPGA, and the dimensions and sizes of the configuration are also realized through the variables of each parameter. From the operational level, the application and error calculation realizes the fault-tolerant algorithm BRAM calculation, in addition to real-time detection data through experimental design, storage and processing. The Lanzhou heavy ion accelerator 55 Me V/ 58Ni Xilinx 5,500,000 ion pair carried out the typical system test based on flip gate field programmable gate array (FPGA) single particle effect protection design [3].

3.3 Experimental design process

3.3.1 The design method of SRAM type FPGA single particle fault injection effect. SRAM type FPGA single particle fault injection effect is mainly based on the initial stage, initial stage and final stage, mainly related to fault database, fault call module, fault input device, test results and results of file transfer and evaluation system. The extent of the impact mainly relates to the fault configuration files for FPGA single particle model, different types of fault configuration files, object files drive fault and fault file download, the output signal recovery module and docking with the normal signals and fault according to the test results of the system influence target [4]. The experimental design is shown in Figure 1.

![Figure 1 SRAM FPGA single event effect fault injection flow chart](image-url)
3.3.2 FPGA anti SEU fault tolerant design process. FPGA anti SEU design to read -- error detection; Scrubbing -- error correction; BRAM self correction macro - special treatment in several stages. From the performance analysis and completion of the functional needs of the user, the main strategy design method relates to a storage chip with high anti radiation performance of Asic or anti fuse FPGA. The core control chip side and the embedded configuration format realize the reasonable mechanism the circuit and ensure that the design process and meet the requirements of the users especially in various functional modules, including channel selection, control logic, many CPU control linkage mode selection and error correction circuit. Shown in Figure 2.

![Figure 2](image_url)  
**Figure 2** Structure diagram of FPGA anti SEU three mode redundancy system

3.4 The design feasibility analysis
The space particle radiation environment involves many aspects, high-energy charged particles flow component 85% protons, 12.5% alpha particles from 1.5% elements lithium to iron nuclei. The earth's radiation belts and the outer radiation belt radiation zone consists of electrons, and energetic particles of solar proton events burst can make fatal fault on the large scale integrated circuit computer star. The test results show that the functions and the performance indexes of the rail telemetry, remote control, tracking and other aspects meet the mission requirements, and do not have any problems or need to ground intervention. This technique can also be applied to other low grade devices and other types of FPGA, DSP (Digital Signal Processing, a digital signal processing LSI star) single load protection [5]. In the analysis of sensitivity and the effect based on RAM type FPGA single particle effect, SEU SRAM FPGA sensitive to reinforce and fault-tolerant design as a shielding layer to achieve the read -- error detection; Scrubbing -- error correction; BRAM self correction macro - special treatment in several stages [6-7].

In the study of system design, the design of Scrubbing node cannot use SRL16 and distributed RAM to avoid causing loss of real-time refresh state initialization and configuration processing. In the connector JTAG and Select MAP, IO is set to CCLK in linkage analysis, and maximize the feasibility of the design. By calculating the configuration in the FPGA layout, the model of circuit fault propagation simulation is closer to the actual circuit code bit flip results, which finds out the most easily lead to a failure of cellular proliferation calculated separately related configuration compared to LUT, and realizes the average degree of optimization for the application effect of 19.89%.

4. Conclusion
SRAM type FPGA single particle effect in this experiment, the storage machine design can be achieved through the design of the key and fault tolerance and its design principle. Whether the functional studies or the structure system, it is necessary in the study of adaptive characteristics of circuit to achieve the desired purpose, realize overall design of anti SEU memory function, and meet the sensitivity requirements and structure after improvement.
5. Reference

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