III-N heterostructures for monolithic integration of enhancement/depletion-mode high-electron-mobility transistors

D S Arteev¹, A V Sakharov¹, A E Nikolaev¹, W V Lundin¹ and A F Tsatsulnikov²

¹Ioffe Institute, 26 Politekhnicheskaya, 194021 St. Petersburg, Russia
²Submicron Heterostructure for Microelectronics, Research & Engineering Center, RAS, 26 Politekhnicheskaya, 194021 St. Petersburg, Russia

E-mail: ArteevDS@mail.ioffe.ru

Abstract. Simulation analysis of III-N two-dimensional electron gas-based structures that could be used for stable monolithically integrated enhancement/depletion-mode circuits was carried out. Three different designs were proposed and analysed, including a novel p-GaN/AlN-GaN SPSL/GaN, which is expected to have lower ON-state resistance and higher transconductance than conventional normally-off GaN-based transistors.

1. Introduction

The development of semiconductor electronics has completely changed the world we live in. To a large extent, the rapid progress of technology has been made possible by the invention and continuous improvement of silicon transistors. However, nowadays silicon-based devices have almost reached their limits. Therefore, great efforts are being made to find new materials for higher-performance electronics. Wide-bandgap semiconductors, in particular, gallium nitride (GaN) and its alloys, are considered to be “the silicon of the future” for power and highly-efficient electronics [1].

Modern GaN high-electron-mobility transistors (HEMT) are based on III-nitride heterostructures. Two-dimensional electron gas (2DEG) is induced at the heterointerfaces due to the polar nature of the wurtzite crystalline structure of III-materials and acts as a conduction channel [2, 3]. These devices are usually “normally-on” (or depletion-mode/D-mode), i.e. they conduct electric current even at zero bias at the gate electrode, while normally-off (or enhancement-mode/E-mode) transistors are preferable for lower energy consumption and safe operation in power electronic systems. There are several approaches to achieve normally-off GaN HEMT: fluorine implantation below the gate electrode [4], local thinning of the barrier layer under the gate [5], introduction of a p-type cap layer [6] or a combination of the last two methods [7]. Further details on the normally-off GaN-based HEMT technology can be found in [8]. Implementation of both normally-on and normally-off transistors on one wafer has a great potential for low-power consuming and high-functioning integrated circuits and devices. However, ion implantation and etching with subsequent regrowth may introduce additional defects, causing degradation of crystalline quality and unstable operation [9]. Thus, achieving high-performance normally-off HEMT is a challenging task.

In this paper, we present a simulation study of various structures that could potentially be used for stable monolithically integrated enhancement/depletion-mode HEMT circuits and some experimental results for one of them.
2. Simulation
The design of the heterostructures is based on the following requirements:

- An AlN interlayer should be inserted between a barrier layer and a GaN channel to avoid mobility degradation due to alloy disorder scattering [10]. We selected a 0.75 nm nominal thickness as it is usually used in our D-mode HEMTs
- Normally-on HEMT and inter-electrode regions of normally-off HEMT should be achieved by means of etching only, without a subsequent regrowth process
- An AlN etch-stop layer should be implemented to improve etch uniformity

One-dimensional simulation of the structures was carried out by solving the Poisson and Schrödinger equations self-consistently using Silvaco TCAD. The spontaneous and piezoelectric polarization charges induced at the heterointerfaces, scaled with the factor of 0.8 due to their screening by charged fixed defects and partial stress relaxation, were taken into account in the simulation. The buffer layer was assumed to be p-type with a hole concentration of $1 \times 10^{14}$ cm$^{-3}$ (in practice, it is compensated by deep impurities like Fe or C). The gate was considered an ohmic contact in the case of a p-doped cap layer and a Ni Schottky contact with a work function of 5.15 eV, otherwise. The epitaxial layer schematics of the investigated structures are shown in figure 1. A critical parameter for E-mode HEMT is $R_{ON}$, that depends on conductivity in the regions with an etched-off top layer, so every structure was simulated in three variations – a “full” structure with all layers, a structure with an etched cap but with a remained AlN etch-stop layer (“etch1” structure) and a structure without both cap and etch-stop layers (“etch2” structure). To facilitate comparison between different structures, we assumed that Fermi level pinning due to the surface states of the etched inter-electrode regions of normally-off HEMTs is absolutely identical to the one at the metal-semiconductor interface with a metal work function of 5.15 eV.

![Figure 1. Epitaxial layer schematics of the proposed structures.](image)

3. Results
First, a p-GaN/AlN/AlGa$_{0.17}$N/AlN/GaN structure (figure 1(a)) with an acceptor density [Mg]=$10^{19}$ cm$^{-3}$ in a 40 nm GaN cap layer was proposed and simulated. The case when the Fermi level lies below the conduction band minimum (corresponding to a 2DEG density < $10^{12}$ cm$^{-2}$) was chosen as an off-state criterion. The calculated band diagram shows that at a zero gate voltage the conduction channel is absent while applying 2 V of positive bias results in the formation of a potential well with a channel 2DEG density of ~ $6 \times 10^{12}$ cm$^{-2}$ (figure 2(a)). The calculated 2DEG density of the associated “etch1” structure is $8.1 \times 10^{12}$ cm$^{-2}$, while the “etch2” structure demonstrates a 2DEG density of $5.7 \times 10^{12}$ cm$^{-2}$. Based on this design, a structure was already grown and a transistor was fabricated. Its normally-off operation mode was experimentally proved [11], and the obtained data were in a good agreement with the calculated ones.
Sometimes it may be preferable to avoid using Mg doping since it can have a negative impact on the stability and reliability of the device [12, 13]. A possible solution is to use unintentionally-doped InGaN instead of p-GaN as a cap layer for polarization engineering [14]. Thus, the structure with the same design except for the cap layer was proposed and simulated. The calculated dependence of the 2DEG density at zero gate bias on the thickness and composition of the InGaN cap is shown in figure 3a. Symbols represent the critical thickness values calculated with different models (the data are taken from [15]). As one can see, the In$_{0.05}$Ga$_{0.95}$N cap is insufficient to obtain a normally-off operating mode. An InGaN cap with a higher indium content potentially allows achieving normally-off operation but is it difficult to grow a non-relaxed InGaN layer of a required thickness due to the large lattice mismatch between GaN and InN although E-mode HEMT with 5 nm In$_{0.2}$Ga$_{0.8}$N was reported [16]. Nonetheless, a bias-dependent simulation of the structure with an unintentionally-doped 15 nm In$_{0.15}$Ga$_{0.85}$N cap layer was carried out for comparison (figure 3b). A 2DEG density at a +2 gate voltage is slightly lower than in the p-GaN structure, and the dependence of the 2DEG density on the gate voltage is flatter, which may be an advantage for some applications. As for the 2DEG densities of the etched structures, they are exactly equal to the ones of the p-GaN cap structure, since the design of underlying layers is completely identical.

![Figure 2](image1.png)

**Figure 2.** Band diagram and electron concentration of the “standard” normally-off structure at 0V and +2 V gate voltages (a) and the associated etched structures at zero gate bias (b). Here and throughout zero energy corresponds to the Fermi level in the quantum well.

![Figure 3](image2.png)

**Figure 3.** (a) The dependence of the 2DEG density at zero gate bias on the thickness and composition of the InGaN cap layer. The solid circles and open squares are the critical thickness values calculated with different models (the data are taken from [15]). (b) Band diagram and electron concentration of the normally-off structure with a 15 nm In$_{0.15}$Ga$_{0.85}$N cap at 0V and +2 V gate voltages.

Trying to find the way to improve the ON-state resistance ($R_{ON}$), a novel design with a p-GaN cap layer and a 0.75 nm/0.75 nm AlN/GaN short-period superlattice (SPSL) as a barrier layer (instead of an AlGaN layer) was proposed. The feasibility of epitaxial growth of GaN/AlN SPSL was already demonstrated [17]. The device with no ternary alloys in the design could potentially have better
electrical properties due to the total absence of alloy disorder scattering. Subnanometer-thick layers were proposed to avoid the formation of multiple 2DEG channels [18]. In the case of the AlN/GaN SPSL barrier, the top AlN layer also serves as an etch-stop layer, so the requirement is met. The structures with 2, 3, 4 and 5 SPSL periods (referred as “S2”, “S3”, “S4” and “S5”, respectively) were simulated (figure 4). As one can see, structures S2, S3 and S4 demonstrate normally-off operation, while S5 is normally-on with a zero gate bias 2DEG density of ~3.9×10^{13} cm^{-2}. The bias-dependent simulation showed that an increasing number of SPSL periods resulted in a negative threshold voltage shift and the curve of 2DEG density versus the gate voltage becomes flatter in the on-state region (figure 5(a)). Then, the associated etched structures were simulated, and it was found that etching both the p-GaN cap and top AlN layer (i.e. the “etch 2” structure ) does not result in the normally-on operation mode in the case of S2, while S3 and S4 become normally-on for both “etch 1” and “etch 2” variations (figure 5(b)). The 2DEG density of etched S3 and S4 varies from 8×10^{12} to 1.2×10^{13} cm^{-2} and from 1.3×10^{13} to 1.5×10^{13} cm^{-2}, respectively, making them promising for the fabrication of GaN-based normally-off HEMT with low R_{ON} and a complementary pair of D-/E-mode HEMTs on one wafer.

4. Conclusion

One-dimensional simulation analysis of GaN HEMT-based structures that could be used for stable monolithically integrated enhancement/depletion-mode circuits was carried out. Three different designs, including a novel p-GaN/AlN-GaN SPSL/GaN, were proposed and analyzed. The optimal number of 0.75 nm/0.75 nm AlN/GaN SPSL periods to provide the normally-off operation mode was found to be 3 or 4. Such structures are expected to have lower ON-state resistance and higher transconductance than the conventional p-GaN cap or InGaN cap E-Mode HEMTs.

Figure 4. Band diagram and electron concentration of S2 (a), S3 (b), S4 (c) and S5 (d) structures at 0V and +2 V gate voltages.

Figure 5. (a) 2DEG density of “full” structures versus gate voltage. (b) 2DEG density of “full” and associated “etched” structures at zero gate bias.
References

[1] Chen A 2018 Gallium nitride is the silicon of the future The Verge https://www.theverge.com/2018/11/1/18051974/gallium-nitride-anker-material-silicon-semiconductor-energy

[2] Ambacher O et al. 1999 J. Appl. Phys. 85 3222

[3] Khan M A, Hove J M V, Kuznia J N and Olson D T 1991 Appl. Phys. Lett. 58 2408

[4] Cai Y, Zhou Y, Lau K and Chen K 2006 IEEE Trans. Electron Devices 53 2207

[5] Lanford W, Tanaka T, Otoki Y and Adesida I 2005 Electron. Lett. 41 449

[6] Hu X, Simin G, Yang J, Khan M A, Gaska R and Shur M S 2000 Electron. Lett. 36 753

[7] Chen K J, Haberlen O, Lidow A, Tsai C L, Ueda T, Uemoto Y and Wu Y 2017 IEEE Trans. Electron Devices 64 779

[8] Roccaforte F, Greco G, Fiorenza P and Iucolano F 2019 Materials 12 1599

[9] Bisi D, Meneghini M, Stocco A, Cibin G, Pantellini A, Nanni A, Lanzieri C, Zanoni E and Meneghesso G 2013 2013 Proc. European Solid-State Device Research Conf. (ESSDERC) September 16-20, 2013 Bucharest (s.l.: s.n.) 61

[10] Smorchkova I P, Chen L, Mates T, Shen L, Heikman S, Moran B, Keller S, Denbaars S P, Speck J S and Mishra U K 2001 J. Appl. Phys. 90 5196

[11] Kukhtyaeva O B, Egorkin V I, Zemlyakov V E, Zaitsev A A, Kapaev V V, Tsatsulnikov A F, Nikolaev A E and Sakharov A V 2019 Book of Abstracts 6th Int. Sch. Conf. “Saint Petersburg OPEN 2019” on Optoelectronics, Photonics, Engineering and Nanostructures April 22-25, 2019 Saint Petersburg ed A E Zhukov (Saint Petersburg: Academic University Publishing) 494

[12] Wuerfl J et al. 2011 Microelectron. Reliab. 51 1710

[13] Meneghini M, Hilt O, Wuerfl J and Meneghesso G 2017 Energies 10 153

[14] Mizutani T, Ito M, Kishimoto S and Nakamura F 2007 IEEE Electron Device Lett. 28 549

[15] Holec D, Costa P, Kappers M and Humphreys C 2007 J. Cryst. Growth 303 314

[16] Ito M, Kishimoto S, Nakamura F and Mizutani T 2008 Phys. Status Solidi C 5 1929

[17] Khan M A, Kuznia J N, Olson D T, George T and Pike W T 1993 Appl. Phys. Lett. 63 3470

[18] Wośko M, Paszkiewicz B, Vincze A, Szymański T and Paszkiewicz R 2015 Phys. Status Solidi B 252 1195