A fully autonomous power management interface for frequency up-converting harvesters using load decoupling and inductor sharing

M Tom, O Paul and T Galchev
Microsystem Materials Laboratory, IMTEK, University of Freiburg
Georges-Köhler-Allee 103, 79110, Freiburg, Germany
Email: tzeno.galchev@imtek.de

Abstract. This paper presents the design and simulation results of a self-starting electrical interface circuit for Parametric Frequency Increased Generator (PFIG) vibrational energy harvesters. A significant challenge with these types of harvesters is the ring down of the transducer, introducing an exponential decrease in efficiency when interfaced with standard passive rectifiers. This work aims to address these challenges by interfacing a standard active rectifier to a buck-boost stage in order to decouple the load and always provide an optimal impedance to the transducer. Because PFIG harvesters have two outputs, an inductor sharing technique allows the hardware to be reused. The active buck-boost power management circuit is designed for XFAB’s 0.35 µm 2P5M CMOS process. It can provide an efficiency between 75% - 93% for input voltages in the range of 0.5 - 2 V, reaching its maximum efficiency at 1.8 V. The active power consumption of the power converter is 800 nW. The system can start from as low as 800 mV of input voltage and 3 µW of input power.

1. Introduction
Advances in semiconductor technology over the past decade have led to sensor systems with increased functionality while the overall power consumption has been reduced. Additionally, improvements in low-power electronics and power management techniques for energy harvesters are predicted to lead to energy autonomous stand-alone sensor systems. One area of interest is in developing autonomous wearable and implantable systems. Human motion is a potential source of renewable energy, however it is particularly challenging to harvest due to its variability. Previously, a vibration harvester architecture was introduced, called the Parametric Frequency Increased Generator (PFIG) [1-2], particularly suited toward converting low-frequency and variable amplitude vibrations. However, due to the nature in which PFIGs operate, specialized power management techniques are needed which can deal with the alternating and decaying output signals. Furthermore, as energy harvesters are scaled down, reduced electromechanical coupling leads to lower output voltages and power levels. Therefore, future power management techniques must be able to address these technical issues while consuming nearly negligible power.

This paper discusses the design and simulation results of an electrical interface circuit for extracting power from PFIG harvesters. This type of harvester has two outputs, and therefore an architecture was developed that allows for energy from both outputs to be extracted, stored, and managed effectively while sharing and reusing hardware components in order to keep the overall system size small. One of
the main tasks of the power management system is to decouple the load from the harvester in order to allow energy transduction to take place in an optimized way regardless of the variable load presented to the system. Both piezoelectric and electromagnetic transducers can be approximated as having a resistive source impedance while in resonance, which means that they will deliver optimal power to a matched resistive load [3]. This is also true in the case of an unforced ring-down, as is the case with PFIG harvesters. In this work, the behavior of a matching load resistor is emulated using a non-inverting discontinuous conduction mode buck-boost converter. While the circuit in this paper is designed for interfacing to a piezoelectric PFIG, the same concept can be applied to electromagnetic implementations.

![Block diagram of the PFIG power management interface](image)

**Figure 1.** Block diagram of the PFIG power management interface

### 2. System architecture

The architecture of the proposed piezoelectric harvesting system is described in figure 1. The PFIG has two transducers and therefore the electrical circuit should be able to extract and combine the energy from both. As illustrated in figure 1, two separate active rectifiers are attached to the output of each of the two transducers. They are based on the design presented in [6] and their job is to convert the initially alternating voltage to DC. A single buck-boost converter is then shared between the two
transducers. Digital control is used to time-share the buck-boost converter. Since, the duty cycle of the converter is very small, the rising and falling edges of the clock signal are used to switch between the two harvester sources.

\[ i_p(t) \quad C_P \quad v_p(t) \quad i(t) \quad C\text{ RECT} \quad V\text{ RECT} \quad \text{NVC Active diode} \quad \text{Piezoelectric harvester Rectifier} \]

**Figure 2.** Piezoelectric transducer connected to an active rectifier and load.

### 2.1. Piezoelectric harvester model
Piezoelectric transducers can be approximately modeled in the electric domain as an ideal current source in parallel to a parasitic capacitance \( C_P \) and resistance \( R_P \) as shown in figure 2 [3]. Generally, \( R_P \) is very large compared to the impedance of \( C_P \) and therefore it is neglected. When connected to a rectifier, the maximum rectified voltage, \( V_{\text{RECT}} \), occurs during no-load scenario and is equal to the open-circuit voltage, \( V_{\text{OC}} \), given by

\[ V_{\text{OC}} = \frac{I_P}{\omega C_P}, \]

where, \( I_P \) is the amplitude of the alternating current and \( \omega \) is the frequency of vibration. It has been shown [4] that peak power is extracted, when \( V_{\text{RECT}} \) is half of \( V_{\text{OC}} \) and this maximum power corresponds to:

\[ P_{\text{RECT max}} = \frac{C_P \omega V_{\text{OC}}^2}{2\pi} \quad (1) \]

### 2.2 Rectifier
The rectifiers are implemented by combining a negative voltage converter with an active diode as previously shown in [6]. In this way the voltage drop is reduced to a few millivolts, compared with the large voltage drop (> 0.25 V) associated with a diode implementations. This is very important for miniaturized implementation, where the output voltages are typically small.

### 2.3 Buck-boost converter and optimal power extraction
The DC-DC converter is used to optimize \( V_{\text{RECT}} \) and thereby track the maximum power point of each PFIG transducer [3, 5]. Operating the buck-boost converter in a discontinuous conduction mode creates the impedance match. The time averaged input resistance, \( R_{\text{IN}} \), can be derived by formulating an expression for the average input current, \( I_{\text{IN}} \) (which is the inductor current \( I_L \) averaged over one switching cycle) and diving it by the input voltage \( V_{\text{RECT}} \) leading to the following formulation:

\[ R_{\text{IN}} = \frac{2L_f \text{CLK}}{D^2} \quad (2) \]

As can be observed from equation 2, the input impedance depends only on the inductor value \( L \), the duty cycle \( D \), and the switching frequency \( f_{\text{CLK}} \), and is independent of input or output voltage. The proposed buck-boost converter has five switches \( S1-S5 \). Switches \( S1 \) and \( S2 \) are used to extract energy from the rectified output of each of the PFIG transducers, while the remaining switches are shared. In order to improve efficiency at low voltages, switches \( S1 \) and \( S2 \) are implemented by a parallel combination of NMOS and PMOS transistors. Switches \( S3 \) and \( S4 \) are implemented using NMOS transistors and switch \( S5 \) is realized using PMOS.

### 2.4 Control circuit
The converter control unit uses a digital control loop in-order to minimize the active power consumption [5]. The control loop has a 5 bit up/down counter, whose value determines the on-time of switch \( S5 \). In-order to achieve zero current switching, the counter always tries to settle to the optimum
value by checking whether the present pulse value is higher or lower than optimal. This decision is made by a clocked comparator, which monitors node voltages $V_L$ and $V_{BUF}$.

2.5 Clock generator
An on-chip clock for synchronization is generated using an RC relaxation oscillator. The signal is generated by the constant charging and discharging of a capacitor through two reference current sources. The relaxation oscillator designed in this work generates a clock of 2.5 kHz. The clock generator consumes less than 150 nW during active operation.

2.6 Start-up circuit
In order to achieve fully autonomous operation, the harvester should have a start-up mechanism to initially charge the buffer capacitor, $C_{BUF}$ from a completely discharged state. The start-up circuit selectively uses switch $S4$, MOSFET diode $M_{P1}$, and inductor $L$ to create a boost converter, which in-turn charges $C_{BUF}$. The clock signal for the start-up procedure (CLK_STR) is generated directly from the mechanical input source using the arrangement shown in figure 1.

![Image of phase 1 and phase 2 with voltages and time scale](image)

**Figure 3.** Transient plot showing the start-up of the system when coupled to a PFIG. The following parameters are used:
- $I_p = 25 \mu A$, $C_p = 25 \text{nF}$,
- $f_p = 200 \text{Hz}$, $C_{RECT} = 1 \mu F$,
- $P_{IN,MAX} = 2.4 \mu W$,
- $L = 62 \mu H$,
- $C_{BUF} = 100 \text{nF}$.

3. Results
The architecture described in figure 1 was designed and simulated for the 0.35 µm CMOS process offered by XFAB. Each piezoelectric output of the PFIG is modeled to have $C_p = 25 \text{nF}$ and an operating frequency of 200 Hz. The start-up process can be explained in two phases. In phase 1, the buffer capacitor, $C_{BUF}$, initially charges passively through a diode. In phase 2, once $V_{BUF}$ reaches the MOSFET threshold voltage, charging continues using the start-up boost-converter described in section 2.6. This operation continues until $V_{BUF}$ reaches 1.2 V after which normal operation begins. During the start-up phase, all of the control circuits are disabled. Start-up transients are shown in figure 3, illustrating the two phases. With this arrangement, the harvester was able to start from input voltages as low as 800 mV with as little as 3 µW of input power.
The efficiency of the buck-boost converter during normal operation was analyzed by varying the input voltage between 0.5 - 2 V. Figures 4-5 show plots of power efficiency as a function of rectified input voltage, where the first range is more appropriate for low-impedance electromagnetic harvesters (figure 4) and the second for higher voltage and higher output impedance piezoelectric implementations (figure 5). The active power consumption of the converter is as low as 800 nW.

### Table 1: Performance comparison of previously published work

| Reference | Impedance matching | Converter efficiency | Rectified input voltage |
|-----------|--------------------|----------------------|-------------------------|
| This work | Yes                | 75% - 93%            | 0.5 - 2.0 V             |
| [7]       | No                 | 58% - 86% (end to end) | > 0.8 V                |
| [8]       | Yes                | 65% - 79%            | 1.5 - 5.0 V             |
| [5]       | Yes                | 75% - 85%            | 2.0 - 5.0 V             |
| [9]       | Yes                | 40% - 60%            | 0.6 - 2.0 V             |

### 4. Conclusion

A fully autonomous electrical interface circuit was developed for Parametric Frequency Increased Generators in XFAB’s 0.35 μm CMOS process. The designed buck-boost converter was able to achieve efficiencies in the range of 75% - 93% for input voltages in the range of 0.5 - 2 V, reaching its maximum efficiency at 1.8 V. The active power consumption of the power converter is 800 nW. The system can start from as low as 800 mV of input voltage and 3 μW of input power.

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