AsyncTaichi: On-the-fly Inter-kernel Optimizations for Imperative and Spatially Sparse Programming

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Fig. 1. Top left: In existing parallel imperative programming systems (such as CUDA and Taichi [Hu et al. 2019]), computational kernels are eagerly launched, leaving a tiny room for the optimizer to optimize beyond a single kernel. Bottom left: In this work, we accumulate kernels in an execution buffer, only flushing the execution queue when necessary. More importantly, we leverage a domain-specific inter-kernel optimizer to automatically conduct performance optimizations beyond a single kernel, especially for spatially sparse computation. We dynamically build a tailored data-flow graph ("state-flow graph") of kernels for easy analysis, so that computation kernels can be optimized at an inter-kernel level just in time. Right: After a suite of domain-specific and general-purpose optimization passes including list generation removal, sparse data structure activation elimination, fusion, and dead store elimination, kernels are much better optimized compared to the reference intra-kernel optimization system. As a result, our inter-kernel optimized programs run 1.87× faster on GPUs, without the user modifying any of the computation code. Our evaluation suite covers computations on Eulerian grids, Lagrangian particles, meshes, and automatic differentiation.

Leveraging spatial sparsity has become a popular approach to accelerate 3D computer graphics applications. Spatially sparse data structures and efficient sparse kernels (such as parallel stencil operations on active voxels), are key to achieve high performance. Existing work focuses on improving performance within a single sparse computational kernel. We show that, a system that looks beyond a single kernel, plus additional domain-specific sparse data structure analysis, opens up exciting new space for optimizing sparse computations. Specifically, we propose a domain-specific data-flow graph model of imperative and sparse computation programs, which describes kernel relationships and enables easy analysis and optimization. Combined with an asynchronous execution engine that exposes a wide window of kernels, the inter-kernel optimizer can then perform effective sparse computation optimizations, such as eliminating unnecessary voxel list generations and removing voxel activation checks. These domain-specific optimizations further make way for classical general-purpose optimizations that are originally challenging to directly apply to computations with sparse data structures.

Without any computational code modification, our new system leads to 4.02× fewer kernel launches and 1.87× speed up on our GPU benchmarks, including computations on Eulerian grids, Lagrangian particles, meshes, and automatic differentiation.

CCS Concepts: • Software and its engineering → Domain specific languages: • Computing methodologies → Parallel programming languages: Physical simulation.

Additional Key Words and Phrases: Sparse Data Structures, GPU Computing.

1 INTRODUCTION

Spatially sparse data structures such as VDB [Museth 2013] and SPGrid [Setaluri et al. 2014] have been effective tools to improve performance and memory efficiency in various 3D computer graphics applications. While existing work in sparse data structure libraries and compilers [Gao et al. 2018; Hoetzlein 2016; Hu et al. 2019; Wu et al. 2018] have significantly improved sparse data structure performance within a single computational kernel, performance optimization opportunities remain abundant when considering multiple consecutive sparse computation kernel as a whole. For example,
high-level knowledge of data structure sparsity patterns can often be extracted from the context around a sparse computation kernel. Such knowledge can help improve run-time performance of sparse data structure accesses, because the compiler may be able to infer whether the accessed voxel is active or not, thus saving sparsity checking overheads at run time.

Optimizing across function and kernel boundaries is a well-developed technique in traditional ahead-of-time compilers (see, for example, gcc WHOPR [Briggs et al. 2007]), and functional array-based parallel JIT systems, especially deep learning systems such as TensorFlow [Abadi et al. 2016] and JAX [Bradbury et al. 2018]. However, two major challenges exist when applying the idea of inter-kernel optimization to spatially sparse computation programs.

Firstly, sparse data structures in graphics need to support dynamic topology. Operations on these data structures usually come with not only value modifications but also topology changes. Traditional compiler optimization tools for dense arrays with constant topology may not directly apply here.

Secondly, graphics computations on sparse data structures are often imperative instead of functional, and side effects such as in-place modifications make imperative programming less “pure” and harder to optimize than functional programming. The reason why graphics programmers practically pick imperative rather than functional programming paradigm is two-fold: 1) sticking to imperative programming brings maximum compatibility with existing graphics algorithms, and 2) the tremendous amount of data in sparse computation implies programmers typically cannot afford to create a second copy of the data structures as in functional programming.

As a result, classical optimizations, such as fusion, cannot be naturally used here, since the data structure topology might have changed between two kernels on sparse data structures. Note that this is not an issue for programming systems with dense, immutable arrays. While tools for analyzing dense array programs are well established [Knob and Sarkar 1998], their counterparts in spatially sparse array computations are largely underexploited. Deep learning frameworks usually avoid some of the aforementioned challenges by adding constraints to the computation model, such as allowing only immutable data types to simplify code analysis. Although these constraints are often naturally satisfied in deep learning use cases, they may limit the programming flexibility in graphics (especially simulation) code.

Taichi [Hu et al. 2019] is an imperative and spatially sparse domain-specific programming language that aims to achieve both high performance and high productivity. In this work, we concretely base our discussions on Taichi and strive to develop an automatic inter-kernel optimization system for spatially sparse computation.

**Design principles.** With productivity and performance in mind, our system is practically designed following the guidelines below:

- **Transparent to users.** We wish users can get the benefits of inter-kernel optimizations for free. No code modification should be needed in the computational kernels for users to leverage our optimizations.

- **Just-in-time (JIT) compilation and optimization.** JIT compilation is widely adopted by many Python-based computational frameworks (TensorFlow [Abadi et al. 2016], PyTorch [Paszke et al. 2019], JAX [Bradbury et al. 2018]). It helps achieve a good balance between developer productivity and performance. However, JIT compilation alone usually cannot exploit the performance to its full extent. By accumulating the JIT-compiled kernel and building a state-flow graph on the fly, the Taichi runtime is able to uncover more opportunities for optimization.

  - **Problems of all scales matter.** Graphics applications cover a wide range of problem sizes. For example, a particle simulation may cover from 2 thousand to 235 million [Hu et al. 2021] particles. For small-scale tasks, compilation time may be the bottleneck; for large scale tasks, computation time is more important. Our asynchronous execution engine enables parallel compilation to reduce the JIT compilation delay.

  **Our solution.** We propose a domain-specific data-flow analysis model of imperative and sparse programs, to analyze programs with partial and in-place updates and those with sparse data structures. “States” in our formulation refer not only to numerical values stored in data structures, but also to domain-specific data descriptions, such as the topology of the sparse data structures. We build a state-flow graph (SFG) on-the-fly consisting of pending kernels to depict kernel relationships. The rich expressiveness of SFGs allows us to conduct domain-specific inter-kernel optimizations, such as fusing kernels on dynamic sparse data structures, eliminate unnecessary voxel list generation tasks for parallel iterations on the sparse data structures, and accelerate the sparse data structure access.

  Imperative parallel programming systems often eagerly execute computational tasks, leaving little room to analyze and optimize beyond a single kernel. To enable the optimizer to see beyond a single kernel at a time, we built an asynchronous execution engine that maintains a window of kernels, leaving room for performance optimizations before launching the kernels. The execution engine also enables parallel compilation, which significantly reduces the JIT compilation time.

  We show that SFGs combined with the asynchronous engine open up space for inter-kernel optimizations on spatially sparse computations, such as removing element list generation kernels when the topology is unchanged, and demoting data structure activations when the compiler can infer such high-level information. These domain-specific sparse computation optimizations further make way for classical inter-kernel optimizations such as kernel fusion and dead store eliminations. For example, on our MGP CG benchmark (section 8.4), we find that our optimizations lead to 5× fewer GPU kernel launches, and on our MLS-MPM [Hu et al. 2018] benchmark, our optimizer is able to automatically fuse the G2P and P2G kernels, leading to an efficient G2P2G kernel [Wang et al. 2020].

  We summarize our contributions as follows:

1. A domain-specific data-flow model to analyze imperative spatially sparse computation. The resulted state-flow graphs (SFGs) serve as a high-level intermediate representation (IR) of imperative, parallel, and spatially sparse programs.

2. An asynchronous task execution engine that exposes inter-kernel optimization opportunities and enables parallel compilation;

3. Most importantly, an inter-kernel optimizer for asynchronous spatially sparse computation. The optimizer can conduct
domain-specific optimizations such as list generation removal and sparse data structure activation demotion. Meanwhile, it can also carry out general-purpose inter-kernel optimizations such as dead store elimination and kernel fusion;

(4) A systematic study of the resulted system. Based on the benchmarks, we show our inter-kernel optimizer delivers 1.87x (geometric mean) wall-clock time improvements and 4.02x fewer GPU kernel launches compared to the reference system [Hu et al. 2019]. All these can be achieved without the programmer modifying a single line of kernel code.

We partially reuse the compiler infrastructure of Taichi [Hu et al. 2019]. Our source code is attached to the submission, and key files in the compiler implementation are listed in the supplemental document.

2 RELATED WORK

Spatially sparse computation. The idea of leveraging spatial sparsity in graphics originates from popular sparse data structures including VDB [Hoetzlein 2016; Museth et al. 2013; Wu et al. 2018] and SPGrid [Gao et al. 2018; Setaluri et al. 2014]. While these data structures have demonstrated effective computation and storage benefits over dense arrays, writing programs that leverage them is not an easy task. Taichi [Hu et al. 2019] provides a language abstraction that allows using these data structures as if they are dense, and runtime systems that automatically handle parallel voxel iteration and memory management. These designs benefit the end users, but may end up with more computation. These redundant jobs would need an inter-kernel analysis system to optimize.

Another thread of work on sparse computation is sparse linear algebra languages, such as TACO [Chou et al. 2018; Kjolstad et al. 2017], which can effectively generate kernels for Einstein summations on sparse matrices and tensors. Instead of explicitly building the sparse matrices, some simulators use matrix-free computations, which are often the more effective ways for high-performance linear algebra solves in physical simulations (see, for example [Liu et al. 2018]).

Sparse tensors in deep learning frameworks. Sparse tensors in ML frameworks such as PyTorch are typically implemented in sparse matrix formats such as the Compressed Sparse Row (CSR) and the "Coordinate" (COO) formats (e.g., torch.sparse). Just like dense tensors in deep learning frameworks, sparse tensors there are immutable. More importantly, sparse tensors in deep learning frameworks have a fixed topology, and the sparse matrix formats lack sufficient support for random accesses. These features make operations on them easier to analyze and optimize. In contrast, Taichi supports hierarchical sparse tensors with dynamic topology, which needs a domain-specific dataflow model to optimize.

Array data-flow analysis. The static-single assignment (SSA) form has been a very popular IR structure. SSA forms are designed for scalar variables, and it cannot directly represent array states, where partial updates may happen. Array SSA forms have been proposed and successfully adopted in parallelization [Knobe and Sarkar 1998] and array privatization [Maydan et al. 1993]. However, related work in this topic is mostly focused on dense arrays. Our high-level IR system represents not only array partial updates, but also the topology changes in sparse arrays.

Whole-program optimization (WPO). WPO is also known as Interprocedural optimization (IPO). For ahead-of-time compilation, IPO typically happens at link time, so sometimes it is also called link-time optimization (LTO). Many existing compilers, such as gcc, MSVC, and clang, already support LTO and WHO (see, e.g., gcc WHOPR [Briggs et al. 2007]). While WPO is extensively explored in classical compiling systems, it is still underexploited for spatially sparse computation. The unique computational pattern in sparse computation brings higher complexity and the need for a unified high-level intermediate representation for analysis and optimization.

Computational graph optimization in deep learning frameworks. A feed-forward deep neural (DNN) network can be naturally represented as directed acyclic graphs (DAG). This leads to a straightforward mapping between DNNs and the computational graph: immutable, dense feature maps directly map to the graph edges, and operators (such as convolutions, max pooling, and element-wise add) maps to the graph nodes. Consequently, modern deep learning frameworks such as TensorFlow [Abadi et al. 2016], PyTorch [Paszke et al. 2019], ONNX [Bai et al. 2019], Theano [Team et al. 2016], MLIR [Lattner et al. 2021]) have widely adopted the computational graph to represent the DNN models. High-level optimizations on the computational graph have been a popular feature in deep learning frameworks. The HLO IR of XLA and PyTorch GLOW [Rotem et al. 2018] are representative examples. Based on the computational graph, traditional computer optimizations such as operator fusion, dead code elimination (DCE), common subexpression elimination (CSE) can be applied. Tensor Comprehensions [Vasilache et al. 2018] and Stripe [Zerrell and Bruestle 2019] accelerate deep neural networks using the polyhedral model and graph optimizations such as fusion. We refer the readers to [Li et al. 2020] for a good survey.

In deep learning frameworks such as TensorFlow [Abadi et al. 2016], every operation creates a new, immutable buffer (“tensor”), and DNNs are essentially data flow of feature maps. In graphics applications, however, we have to adopt an imperative programming paradigm and support in-place updates, mostly because graphics programmers have been accustomed to using imperative programming (e.g., C++, CUDA, and GLSL) for decades.

Our system is similar to these systems in that a high-level graph-based IR is used, yet the high-level IR must consider its partial updates, sparsity, and "megakernel" (i.e., many-in-many-out, hundreds of instructions per kernel) nature of sparse computation code.

GPU code optimization. Extensive research has been done on code optimization for GPUs. For example, Hong et al. [2018] optimize SASS via emulation and identifying bottlenecks. Filipović et al. [2015] optimize CUDA kernels via kernel fusion on operations in the forms of map, reduce, and demonstrated speed up on dense BLAS operations. Bo et al. [2018] proposed an automatic fusion framework for image processing DSLs. However, an on-the-fly inter-kernel optimization system on GPU imperative programming models that
provides maximum flexibility for general-purpose computation is still missing.

*Physical Simulation DSLs.* Developing high-performance physics solvers is challenging, and a lot of low-level engineering is needed to exploit the capabilities of modern parallel processors. High-level DSLs models simulations as meshes (List [DeVito et al. 2011]), sparse linear algebra [Kjolstad et al. 2016], and relational data models [Bernstein et al. 2016].

A lower-level system that is more closely related to our work is the Taichi programming language [Hu et al. 2019]. Taichi is a DSL with first-class support for sparse data structures. In the next section, we briefly cover core Taichi features related to this work.

3 TAICHI BACKGROUND

Taichi [Hu et al. 2019] is a programming language for spatially sparse and differentiable visual computing. As a domain-specific language embedded in Python, Taichi’s just-in-time compiler transforms compute-intensive kernels (“Megakernels”, similar to a _global_ GPU kernel in CUDA) into parallel executables. Users can flexibly launch the kernels using Python.

We refer the readers to [Hu 2020] for an overview of the Taichi programming language. Key Taichi features related to this work are described below.

3.1 Data-oriented programming

A field is a key concept in Taichi that represents data. A field is essentially a one- to eight-dimensional tensor. Each element of the tensor can be a scalar (e.g., density), a small vector (e.g., velocity), or a small matrix (e.g., stress tensor). Internally, a field in Taichi is flat: field elements are always accessed via an $x[i, j, k]$-style syntax, regardless of its data layout. Internally, however, data are organized in hierarchical tree structures, described via structural nodes (SNodes). The leaf layer stores the actual numerical value, while the intermediate layers act as containers storing the cells of the next layer. Note that there is a duality between a container and a cell: The cell of an intermediate layer becomes the container of its next layer. See Fig. 2 as an example.

Commonly used SNodes in Taichi are dense, bitmasked, pointer, and dynamic [Hu et al. 2019]. They can easily compose into complex data structures that are dense or sparse.

Note that the field shapes are known at compile-time, allowing the compiler to easily conduct alias analysis.

3.2 Spatially sparse programming

A field in Taichi can be either dense (similar to a CUDA array) or spatially sparse (such as a VDB [Museth 2013] or SPGrid [Setaluri et al. 2014]). The support for spatial sparsity [Hu et al. 2019] is a unique feature of Taichi. Most 3D graphics data (especially those stored on the voxel grids) are spatially sparse, and Taichi has first-class support for sparse data structures to leverage this property for acceleration.

To make sparse data structures as intuitive to use as dense data structures, various designs are made on the syntax, the compiler and the runtime:

1. **Sparse struct-for loops** allow users to iterate over the active voxels of the sparse data structures conveniently. For example, the following code loops over a 3D sparse field:

   ```python
   for i, j, k in x:
       x[i, j, k] += 1
   ```

   While iterating over only active parts of a sparse data structure improves performance, implementing such an iteration in parallel is highly non-trivial, since the sparse data structure trees are often highly unbalanced. Instead of recursively looping on the tree, Taichi handles this by a process called list generation.

2. **List generation:** The Taichi runtime maintains a list of active elements for each SNode materialized in the program. During the sparse field traversal, Taichi will re-generate the content of the lists from top to bottom. The list generation procedure at each layer is implemented as a unique GPU kernel. For a given layer, the list generation procedure takes as input the parent SNode list, finds out the active cells in each container in the parent’s list (the mask state), and appends them to the list of the current layer. By induction, when this process is carried out for all layers, we will have all the active voxels of the sparse field. Such list generation (Fig. 2, left branch) procedure is the key mechanism to achieve load-balanced parallel sparse-for loops[Hu et al. 2019].

3. **Activation on write** ensures sparse data structure nodes are implicitly activated on writing. For example, the following
code generates a $2 \times 2 \times 2$ downsampling of a higher-resolution sparse field $y$ from a

for $i, j, k$ in $x$:
  $y[i // 2, j // 2, k // 2] += x[i, j, k]$

Note that the corresponding voxels of $y$ may not be active before this for loop. Taichi will automatically activate $y[i // 2, j // 2, k // 2]$ and zero-fill the voxels. See Figure 3 for an example.

Fig. 3. Execution result of simple program $\text{for } i \text{ in } x$: $y[i // 2] += 1$. $y[1]$ and $y[3]$ are activated on write. Because dense nodes cannot be only partially active, $y[0]$ and $y[2]$ are also activated.

4 A STATE-FLOW FORMULATION OF IMPERATIVE SPARSE COMPUTATION

In imperative programming, $\text{Program} = \text{State} + \text{Compute}$. Compared to traditional computation on dense arrays, in spatially sparse computation, “state” refers to not only the numerical values of fields, but also the auxiliary data structures to support sparsity. Similarly, “compute” also means more than GPU kernels that operate on voxel data, because iterating over sparse data structures in parallel implicitly leads to auxiliary computations such as list generation and node activation. These additional complexity create more challenges in modeling and analyzing spatially sparse programs.

For now, let us assume we know the whole execution history of a Taichi program. Drawn inspiration from traditional data-flow analysis, we reformulate the imperative computation scheme of Taichi into a collection of states and tasks. To systematically optimize imperative GPU programs, especially those with spatial sparsity support, we formulate a Taichi program as a state-flow graph (SFG), a domain-specific data-flow graph on spatially sparse computation. As a data-flow graph, SFG is a directed acyclic graph (DAG) with nodes being tasks and edges being states. This results in a state flow formulation and a high-level intermediate representation (IR). Scalar data-flow analysis is well studied in optimizing compilers (see, for example, [Khedker et al. 2017]), and SFG is an extension of data-flow analysis to handle auxiliary states such as lists in spatially sparse computation.

States. States split the holistic description of a Taichi program into a suitable granularity for analysis and optimization. For SNodes that are spatially sparse, we must decompose the holistic descriptions of their data, topology, and auxiliary structures into the following kinds of states:

- A value state simply represents the collection of numerical values stored in the field. Note that in the data structure trees of Taichi, only the leaf nodes (i.e., place SNodes) store numerical values.

Value states are the most basic states. They have the same meaning as those in data-flow analysis, and are useful in almost all GPU programming systems. It is worth noting that in sparse data structures, every voxel has a numerical value, even if the voxel is inactive - in that case, the inactive voxel has an ambient value 0.

- A mask state of an SNode records the activation information of all its cells (Fig. 4, right). Mask states must be handled as first-class primitives in our SFG system for domain-specific optimizations. Mask by itself is not a piece of data materialized in the memory, but a unified abstraction whose state could be inferred via different ways for each kind of the sparse SNode. For example, a bitmask SNode maintains a list of integers as the bitmask metadata, one bit for each cell. Therefore, the active mask contains those cells whose corresponding bits are activated. Another example is the pointer SNode. The elements of such a SNode are just pointers, hence non-null slots comprise the active mask state.

- A list state of an SNode represents the data structure nodes maintained by the runtime system. Recall that Taichi needs to generate/consume data structure node lists for load-balancing parallel iterations over sparse data structure nodes. List generation tasks take the mask state of the current SNode and the list state of the parent SNode to generate the list of the current SNode. Lists are consumed by (parallel) struct-fors. See [Hu et al. 2019] for more details on load balancing and parallel fors on unbalanced trees.

- An allocator state represents the state of Taichi’s memory allocator. For computation that allocates/deallocates sparse data structure nodes, the allocator states are marked as modified.

A state is tagged with a version number. Every time a state is modified within a task, its version number is incremented, with the underlying data buffer of the SNode mutated in-place. Doing so allows Taichi to track the latest writer (owner) of a given state, thereby enables many opportunities for optimization (more on this in section 6).

The relationship between value, mask, and list states is depicted in Fig. 4.

Tasks. A Taichi kernel may be decomposed into multiple parallel tasks (GPU kernels). Without loss of generality, we assume that a Taichi kernel corresponds to a single task and generates a single GPU kernel\(^2\). Each Taichi task has input edges (input states), output edges (modified states). It also maintains its metadata, such as loop ranges. These edges and metadata will be used for inter-kernel optimization.

4.1 State-flow chains

Now let us focus on a single state. For example, we use value state $S$ (Fig. 5), which is manipulated by kernels (tasks) $f, g, p, h, q$. Note that $f, h$ and $q$ read and write the value state $S$, yet $g$ and $p$ only reads the value of $S$. Clearly, only the latest writer holds the most up to date version of a state, while readers only fetch the latest state without resulting in a new version. If we only consider the writers, we get a chain structure for each state, with a few branches for readers. Fig. 5 provides a concrete example.

\(^2\)We use the term “task” and “kernel” interchangeably for a serial/parallel execution job on GPUs.
4.2 State-flow graphs

A Taichi program can easily have hundreds of states. Here we introduce state-flow graphs (SFGs), which are essentially state-flow chains sticking together, or unioning their nodes and edges (Fig. 6). SFGs completely describe the relationship between tasks in Taichi. Since unions of DAGs following the same topological order are still DAGs, SFGs are DAGs too.

The SFG serves as the IR for inter-kernel optimizations. The SFG formulation allows us to use well-established graph theory languages for compiler optimization. For example, our task fusion optimization uses reachability analysis in graphs (section 6.4).

Whenever a task is inserted into the execution queue, we dynamically create an SFG node and create the corresponding dependency edges. SFGs have two useful properties:

1. Order independency. Any topologically ordered task sequence leads to the same program behavior.
2. Reconstruction invariance, corollary of “order independency”. Any topologically ordered task sequence of G constructs the same graph G.

“Reconstruction invariance” is particularly useful when manipulating the graph nodes. For example, to remove a node from SFG, simply topologically sort the SFG nodes, remove the node from the sorted list, and rebuild the SFG. This frees us from worrying about how to handle edges that are connected to the removed node, or to update the latest set of owners of the affected states in the system.

5 LAZY AND ASYNCHRONOUS KERNEL LAUNCHES

In existing parallel programming languages such as CUDA, kernels are ahead of time (AOT) compiled and launched immediately once called on the host. However, we need two more execution mechanisms to make inter-kernel optimizations work: just-in-time (JIT) compilation and (kernel-level) lazy evaluation.

JIT compilation. The issue with AOT compilation is that, at launch time, optimizers only have access to low-level assembly code (e.g., PTX or SASS), which is too fine-grained and fragmented for further optimizations. Fortunately, Taichi not only provides a JIT system,
but also allows to lower the IR halfway to a level that is very suitable for inter-kernel optimizations (see Fig. 1, bottom left, where inter-kernel optimizations happen at the middle-end IR).

**Asynchronous launching.** In CUDA, GPU kernel execution is asynchronous, but GPU kernel launches are still eager. The eager launching mechanism prevents cross-kernel optimization from happening, since the system only "sees one kernel at a time." Therefore, to make the SFG practically useful, we need to hold the SFG nodes from executing before inter-kernel optimizations.

We developed an asynchronous execution engine for GPU programs. The existing Taichi system eagerly launches the kernels, but we can modify the system, making it asynchronous, and maintain a list of kernels to compile and run lazily. This opens up opportunities for inter-kernel optimizations detailed in the following section.

**By-product: parallel compilation.** A drawback of JIT compilation is its compilation time. Note that ahead of time compilation does not have this issue. In fact, as Taichi becomes more widely adopted, the compiler needs to deal with programs with increasing instructions and optimization passes, in extreme cases compilation can take up to 70% of program end-to-end run time. In the previous eager execution scheme, a serial thread is used to compile and launch these kernels. In contrast, since the asynchronous execution engine sees multiple kernels at a time, parallel compilation can be done easily, which can significantly reduce wall-clock time spent on the compilation. The effectiveness of parallel compilation is evaluated in section 8.7.

## 6 Optimize Across Kernel Boundaries

With the state-flow graph IR that describes the task relationships, and the asynchronous execution engine that saves the tasks from being executed too early, we can finally conduct analysis and optimizations on the state-flow graph. In this section, we discuss four effective inter-kernel optimizations on spatially sparse computation programs.

### 6.1 A minimal example

Here we show a trivial optimization example of two Taichi kernels.

As shown in Fig. 8, since \( \mathbf{x} \) is a sparse data structure, Taichi needs to generate an active list of \( \mathbf{x} \) to know which elements of \( \mathbf{x} \) need to be looped over. So there are 3 tasks per kernel in the original Taichi system. Note that the kernels are lightweight here, the running time of list generation tasks is comparable to the essential computation time. If the kernel on the right succeeds the kernel on the left of Fig. 8, in our system, we can perform some analysis to know that the mask state of \( \mathbf{x} \) is not changed, fuse the two kernels into one, and finally get Fig. 9 after optimizations. In this case, we reduce the number of generated tasks from 6 to 3. Kernel fusion is not new, but fusing kernels that operate on \( \text{sparse} \) data structures is a unique challenge in Taichi, since the iteration over active elements implicitly depends on the mask of the sparse data structures.

Even if the bodies of both kernels cannot be optimized in the same way as this example, we can still remove some list generation tasks and reduce running time. This can be a significant improvement for small kernels where the list generation time is comparable to the real computation time.

Common GPGPU patterns and Taichi’s sparse computation model motivates us to apply the following domain-specific and general-purpose compiler optimizations:

- List generation removal
- Activation demotion
- Task fusion
- Dead store elimination

The remainder of this section details these optimizations.

### 6.2 List generation removal

This is the easiest whole program optimization, yet it leads to significantly higher performance for sparse computations in certain cases. A list generation task is idempotent in the sense that, if its input parent list state and the mask state is the same, it will always produce the same list state. Because of this property, if no modifying task is launched between two struct-for loops over the same SNode, the state versions in the SFG will stay the same. Thus the list generation tasks associated with the later loop can be safely eliminated.

List generation removal not only saves unnecessary execution time on generating the sparse element lists, but also opens up opportunities for other optimizations. For example, if two struct-for tasks are using the same list after list generation removal, a task fusion may fuse the tasks.

### 6.3 Activation demotion

Recall that Taichi has an activation-on-write mechanism. It is often the case that the sparse element was already activated before the task execution, so the element activeness was checked to avoid unnecessary activation. This extra check not only creates diverging instruction flow on CPU/GPUs that harms performance, but also creates a modification to the corresponding mask state, creating obstacles for list generation removal. Therefore, we should try to demote activating accesses to non-activating accesses.

Fortunately, many activations can be demoted, by analyzing the task contexts. If two struct-for tasks are identical, the loop lists are the same, and the activation statement in the second task depends only on the loop indices, then the activation in the second task can be removed.

This optimization is remarkably effective for repeated access patterns such as \{1 // 2\}. For example, in the restriction (downsample) operator of multigrid solvers, it is common to have the following pattern (Fig. 10):

```plaintext
for i, j in x:
y[i // 2, j // 2] += x[i, j] * 0.25
```

Our activation elimination optimizer can successfully infer that if the mask of \( \mathbf{x} \) has not been changed, then the mask of \( \mathbf{y} \) will not change either. This avoids false-positive mask state modifications, and can further bring down the list generation kernel tasks by 6.7x in the MGPCG example.
6.4 Task fusion

Task fusion is an effective optimization to improve locality and reduce the number of kernels launches. Without list generation removal, we cannot fuse the two struct-for tasks in Fig. 7a because they take as input two different lists (different versions of the list state of the pointer SNode). Fortunately, after removing the list generation task in Fig. 7b, we can fuse the tasks, resulting in Fig. 7c. The pattern of loops in Fig. 7 is very common in spatially sparse programming, and we need list generation removal to open up space for task fusion. We use the SFG to find pairs of tasks to fuse, and this can be time-consuming when there are too many tasks. Please
see the supplemental document for details about the fusing criteria and the algorithm for efficiently finding all fusible pairs of tasks.

6.5 Dead store elimination

We can also perform some general-purpose inter-kernel data-flow analysis. For example, `ti.clear_all_gradients()` may excessively zero-fill unrelated gradient fields, which can be eliminated with data-flow analysis.

For convenience, a user may frequently zero-fill fields in Taichi to ensure data are correctly re-initialized. This is a typical source of dead stores. For such cases where a field is completely overwritten, our optimizer can eliminate the previous dead store:

```python
@ti.kernel
def clear():
    for i in x:
        x[i] = 0
        y[i] = 0

@ti.kernel
def inc_x():
    for i in x:
        x[i] += 1
for i in x:
    print(x[i])
clear()
# After DSE, y[i] = 0 in this kernel is eliminated
inc_x()
clear()
```

7 IMPLEMENTATION DETAILS

The inter-kernel optimizations are relatively simple to implement, but extra attention was paid to the infrastructure to support these optimizations. In this section, we briefly cover implementation details that we empirically found to directly impact performance.

7.1 Asynchronous Execution Engine

We implement an asynchronous execution engine that performs SFG optimizations and parallel compilation.

All tasks invoked from the Python side are initially accumulated inside a queue, until either an implicit synchronization event (e.g., data transfer between the device and the host), or an explicit call to flush (explained in the next paragraph) happens. Upon such events, the tasks are popped off the queue to construct an SFG instance. This SFG instance goes through the various kinds of optimizations mentioned in Section 6. Once the tasks in the graph are finalized, they are sent to the JIT compilation workers running in parallel, then the backend device.

Flushing. While the more tasks are deferred, the more information is retained for the SFG to optimize, it is usually undesirable to solely depend on the implicit synchronization events to flush the task queue, since this can easily cause starvation on either CPU or GPU side. To provide experienced users with more control over the asynchronous execution engine, we provide a simple API, `ti.async_flush()`, to flush the tasks to the SFG optimizer and then the GPU device. This API is non-blocking, which allows for overlapped execution between CPU and GPU. For most of the usage cases, our system is configured to periodically flush the tasks automatically. While this simple strategy could lead to sub-optimal executions, in practice, we have found this to yield sufficient performance. Note that setting the flushing period to 1 effectively turns off the asynchronous execution.

Partial SFG Garbage Collection. To further mitigate the loss of information potentially caused by flushing or synchronization, each time an optimized SFG instance is sent for execution, Taichi does a partial garbage collection by preserving those nodes that are the latest owners of the states. As new tasks get launched, these nodes will become the roots in the new SFG instance. This enables the system to capture the information it needs for certain types of optimizations. For example, assuming one preserved SFG node is the latest owner of an SNode’s mask state, and a new sparse struct-for loop task reading that SNode is launched. If the mask state has not been modified in between, the SFG optimizer can infer that it is safe to remove the list generation tasks preceding the struct-for task.

7.2 IR handle and IR bank for caching compilation

Since a kernel can be launched many times with the same IR, we store all IRs into an IR bank to avoid repeated passes on the IR and to improve the asynchronous compilation performance. We use IR handles to access IRs in the bank. An IR handle consists of a pointer to the IR and the hash of the IR. We assign an IR handle to each task, and whenever we are going to do any modification to the IR, we check if we have already done it in the IR bank, where we cache the result of IR optimization passes such as fusion, activation elimination, and dead store elimination. If the result is not cached, we copy the IR on write to avoid corrupting the IR in the bank, do the modification, store the modified IR into the bank, and then cache the mapping from the IR handle before modification to the IR handle after modification into the bank. We also cache some data that do not need to modify the IR into the bank, such as the task’s metadata.

7.3 Intra-kernel data-flow optimizations

To achieve better performance after task fusion, we need an optimization pass on the task after fusion. As Taichi IRs are inherently hierarchical, we build a data-flow graph for data-flow analysis, to perform inter-kernel optimizations, including store-to-load forwarding, dead store elimination, and identical store/load elimination. For example, assuming one preserved SFG node is the latest owner of an SNode’s mask state, and a new sparse struct-for loop task reading that SNode is launched. If the mask state has not been modified in between, the SFG optimizer can infer that it is safe to remove the list generation tasks preceding the struct-for task.

8 EVALUATION

In this section, we systematically evaluate our system on microbenchmarks and large-scale end-to-end test cases.
Metrics. On each test case, we evaluate the performance with five metrics:

1. Wall-clock time (inter-kernel optimizer time included);
2. Backend (GPU or CPU thread pools) execution time;
3. Number of tasks launched;
4. Number of instructions emitted to the code generator;
5. Number of tasks compiled.

Each case is executed multiple times on GPU (CUDA) and CPU (x64), with a synchronization after each run in asynchronous mode, and the total metrics over all runs are recorded.

Benchmark cases. We constructed 10 simple yet indicative microbenchmarks (tens of lines of code each) to unit-test specific inter-kernel optimizations. Four complex test cases (hundreds of lines of code each) test the behavior of our optimizer on real-world programs, including computational physics tasks on regular sparse grids (section 8.2), hybrid Lagrangian-Eulerian schemes (particles and grids, section 8.3), multi-resolution sparse grids (section 8.4), and triangular meshes (section 8.5).

8.1 Microbenchmarks

We constructed 10 microbenchmark cases to unit-test the system. The results are promising: without code modification, the new system leads to 3.73× fewer kernel launches on GPUs and 2.5× speedup on our benchmarks. More details on the microbenchmarks are discussed in the supplemental document.

8.2 MacCormack advection

In this benchmark case, we use the MacCormack advection scheme [Selle et al. 2008] with RK3 path integration. We follow the recent trends to use collocated grids (see, e.g., [Gagniere et al. 2020; Nielsen and Bridson 2016]) to improve cache line utilization. On a 3D unit grid, we advect three scalar fields of physically uncorrelated quantities over a sparsely populated vector field defined over a tube domain (see the supplemental document for more details). We use a multi-kernel implementation to keep the flexibility to use different schemes (stable fluid/MacCormack, possibly combined with decaying/sourcing) for different channels. Noticing the program is memory-bound, we expect an at most 3× speedup when the three physical fields are advected together because of the improved cache line utilization when they are adjacent in memory. Our results show that our optimizer is able to achieve approximately 2.92× and 2.80× performance boost on CUDA and CPU, respectively, which is very close to the theoretical 3× acceleration. The number of launched tasks is reduced by 14.8× on both backends. Compared to manually fused advection on different channels, our system automatically detects fusible patterns. This provides more coding flexibility and reduces the mental burden on developers.

We present an ablation study of four inter-kernel optimization passes in Table 3. The improved performance and the reduced number of launched tasks in this benchmark mainly attribute to the task fusion and the list generation removal optimization.

8.3 Moving Least Squares Material Point Method (MLS-PM)

Fig. 11 evaluates our system in more challenging cases where both particles and grids are used, where we benchmark against [Wang et al. 2020] (setup details are in the supplemental document).

To achieve the best performance, we use two grids and swap them before each substep. We also hint our optimizer that the values stored in the pid (particle ID) field is a permutation of all active indices in the particle SNode (see the supplemental document for more details). Then our optimizer fuses G2P and P2G into a single G2P2G task (Fig. 12), which is the main source of optimization.

We use a field to store the affine velocity around the particle (see [Jiang et al. 2015]) between the G2P and P2G tasks. After fusing into a single G2P2G task, the dead store elimination pass further concludes that we do not need to store the intermediate result in the global field, which leads to further improved performance. Our system achieves a 1.32× performance boost on CUDA over the original Taichi system. The performance speedup due to fusion matches the originally reported number in [Wang et al. 2020]4. We also benchmark against a manually fused G2P2G version implemented in the original Taichi system to mimic an optimized larger-scope megakernel with static fusion, and our system is 1.005× faster than it on CUDA, indicating our automatic fusion system performs as fast as manual fusion.

An ablation study of four inter-kernel optimizations is listed in Table 4. In the microbenchmarks, there is a small-scale MPM test case (mpm,splitted) that simply fuses per-particle operations and grid boundary conditions, leading to 1.1× speed up.

4Note that even in our implementation with G2P2G, Wang et al. [Wang et al. 2020] (wall-clock time 5.004 s on CUDA) is still 2.12× faster than our system, because of their AOSOA acceleration data structure, which is outside the scope of this work. In their hand-engineered CUDA version, AOSOA+G2P2G is 2.1× faster than G2P2G, which aligns well with the observations on our system.
Table 1. Benchmarks against the original Taichi system [Hu et al. 2019] without inter-kernel optimizations. The baseline system and applications are tuned against state-of-the-art manually engineered CPU and GPU implementations, as detailed in [Hu et al. 2019]. Benchmarks are done on a system with a quad-core Intel Core i7-6700K CPU with 32 GB of memory, and a GTX 1080 Ti GPU with 12 GB of GRAM. The geometric mean all benchmarks: the wall-clock speed up is $1.87 \times$ (CUDA) / $1.33 \times$ (x64) and the reduction of task launched is $4.02 \times$. Commands to reproduce all the numbers are included in sections detailing each experiment.

Table 2. Geometric mean results of the 10 microbenchmark cases. Numbers are ratios between the reference system [Hu et al. 2019] and ours with inter-kernel optimizations.

Table 3. An ablation study on the MacCormack advection benchmark. The main optimization comes from task fusion. In this case, disabling list generation optimization transitively disables fusion, therefore degrades the performance. [Reproduce: python3 benchmark_advec.py -d 3 -r 256 -n 100 -a [–no-lgr] [–no-ad] [–no-fusion] [–no-dse]]

Table 4. An ablation study on the MLS-MPM benchmark. The main optimization comes from task fusion and dead store elimination. Note that without list generation removal, we cannot perform task fusion, and other optimizations will take much more time. [Reproduce: python3 benchmark_mpm.py -n 2 -a [–no-lgr] [–no-ad] [–no-fusion] [–no-dse]]

8.4 Multigrid preconditioned conjugate gradients (MGPCG)

Multigrid algorithms have frequent sparse data structure operations on grids of multiple resolutions. We test our system on a complex MGPCG Poisson solver. We use a sparsely populated region in a $1024 \times 1024$ (2D) and $256 \times 256 \times 256$ (3D) grid. We follow the MGPCG solver design in [Hu et al. 2019]. In the 2D case, for example, our optimizer is able to bring down the number of tasks launched from 3,183,900 to 2,411,488 (only 21% of the original number). This is because the restriction, smoothing, and prolongation operations lead to 820, 912 redundant list generation tasks, which are reduced to 8004 (2% of the original) by our list generation removal and activation demotion (Fig. 13). Note that the CUDA speed ups ($2.49 \times$ in 2D and $1.44 \times$ in 3D) are much higher than the x64 speed up ($1.12 \times$ in 2D and $1.07 \times$ in 3D), likely because parallel task launches on GPUs are relatively more expensive than that on CPUs, and the majority of the speed ups in this benchmark case is from eliminating small
We implemented MLS-MPM [Hu et al. 2018] with Lagrangian forces [Jiang et al. 2015]. In the simulation, the structure is modeled using a mesh of 160K triangles, and a NeoHookean hyperelastic model (Fig. 14). The force $f_i$ on the particle $i$ is by definition

$$f_i = -\frac{\partial L(x)}{\partial x_i}.$$  

where $L(x)$ is the Lagrangian.

Since manually deriving the partial derivative on the right hand side is error-prone, we rely on Taichi’s automatic differentiation system [Hu et al. 2020]. The key optimization opportunity is the following code:

```python
with ti.Tape(total_energy):
    compute_total_energy()
```

The code above does the forward computation of total energy $L(x)$, and then automatically evaluates for $x\.grad$, which is essentially $\frac{\partial L(x)}{\partial x}$. In the majority of the cases where we only need the gradient rather than the total energy itself, the result of the total energy $L$ is not used. By looking at a long window of kernels, our optimizer can automatically eliminate the forward computation, only doing the backward gradient evaluation. Inter-kernel dead store elimination plays the most important role in this benchmark case.

An interesting observation is that our system gets a significantly higher speedup on CUDA than x64. This is because the particle-to-grid (P2G) transfer step plays different roles in the total time consumption. Note that P2G requires atomic add, which is a relatively cheap operation on CUDA (native hardware support) yet expensive operation on x64 (needs software read-modify-write using hardware CAS). As a result, when our inter-kernel optimization is on, P2G takes 51% run time on x64, yet only 7% on CUDA. This means the forward total energy computation, which is optimized out, occupies a smaller fraction on x64 (since P2G remains the bottleneck), hence a smaller speedup.

8.6 Relationships to JAX

Fusion is an effective optimization in both Taichi and JAX. The common high-level idea is to fuse CPU/GPU kernels to improve data locality and reduce kernel launches. However, due to different application domains and design decisions, fusion plays a more important role in JAX than in Taichi. Here we show a texture manipulation example (Fig. 15) that lies at the intersection of application domains of Taichi and JAX.

We implemented the program using both Taichi and JAX. It turns out that Taichi without fusion, Taichi is 52.4x faster than JAX, but with fusion Taichi is only 3.3x faster than JAX. We implemented

![Fig. 13. The key computational patterns in one iteration of the multigrid preconditioner. Note that in a single Poisson solve, once the sparse multigrid hierarchy is initialized, it will never change its topology. Our optimizer is able to infer the this property, since activation demotion will learn that the restriction kernels, starting from the second iteration, does not additionally activate any new voxels. The majority of list generations can also be removed.](image)

![Fig. 14. The AutoDiff test case: a hyper-elastic material falls down, hits an obstacle, and finally land on the ground. The nodal forces are computed using automatic differentiation. We use a low-resolution simulation here to better visualize the mesh structure.](image)

| Ablation | List / Total tasks | GPU time (s) |
|----------|--------------------|--------------|
| Reference [Hu et al. 2019] | 420912/1057560 | 7.776 |
| No list generation removal | 420912/827303 | 7.232 |
| No activation demotion | 10524/227104 | 2.213 |
| No task fusion | 8004/231695 | 2.156 |
| No dead store elimination | 8004/224585 | 2.098 |
| All optimizations on | 8004/224565 | 2.098 |

8.5 AutoDiff: nodal forces from energy gradients

We implemented MLS-MPM [Hu et al. 2018] with Lagrangian forces [Jiang et al. 2015]. In the simulation, the structure is modeled using a mesh
Table 6. An ablation study on the AutoDiff benchmark. The main optimization comes from dead store elimination. Fusion helps, to some extent, when evaluating and clearing the gradients. Since the data structures are all dense in this benchmark, list generation and activation demotion lead to no performance boost. [Reproduce: `python3 benchmark_autodiff.py -a [–no-lgr] [–no-ad] [–no-fusion] [–no-dse]`]

| Ablation                        | Tasks     | Wall-clock/GPU time (s) |
|---------------------------------|-----------|-------------------------|
| Reference [Hu et al. 2019]      | 65674     | 2.256/2.214             |
| No list generation removal      | 42454     | 1.386/1.191             |
| No activation demotion          | 42454     | 1.383/1.188             |
| No task fusion                  | 54064     | 1.411/1.121             |
| No dead store elimination       | 48424     | 2.305/2.082             |
| All optimizations on             | 42454     | 1.377/1.181             |

Fig. 15. The texture generation test case: the source pattern is rotated and scaled separately using bilinear resampling, and then alpha blended into a final image.

Table 7. The GPU kernel execution time of the texture generation test case with/without fusion in Taichi and JAX. Taichi with fusion is our system, and Taichi without fusion is the original Taichi system [Hu et al. 2019]. JAX without fusion is JAX without the `@jit` decorator. [Reproduce `nvprof -print-gpu-trace python3 benchmark_texture_gen.py -a; nvprof -print-gpu-trace python3 benchmark_texture_gen_jax.py [–no-jit]`]

| Framework                   | with fusion (ms) | without fusion (ms) |
|-----------------------------|------------------|---------------------|
| Taichi                      | 0.306            | 0.467               |
| JAX                         | 1.005            | 24.626              |

- **Analysis difficulty.** Fusion in JAX is easier compared to that in Taichi. This is because 1) fusion in JAX works only on pure functions and in-place mutating updates of arrays are not supported, and 2) most JAX operations are tensor expressions that take holistic arrays as inputs and outputs (e.g., $a = b + c$) while Taichi kernels are often finer-grained array manipulations (e.g., $a_{i,j} = b_{i,j} + c_{j,3i}$). These two reasons make it easy to model the computational graph using a feed-forward DAG, without the need for relatively more complex data-flow modeling as in Section 4.

8.7 Discussions

**Productivity.** An attractive feature of our system is users get a performance boost for free, simply by turning on an option to let the system conduct inter-kernel optimizations.

**Parallel compilation.** Delay caused by compilation time may lead to potential performance issues in JIT systems. Fortunately, in our asynchronous execution engine, we have a whole buffer of kernels to compile, and parallel compilation significantly reduces this compilation delay. For example, in the 2D $1024 \times 1024$ MGPCG benchmark, we find the time of the first iteration, which is compilation delay as no kernels are compiled and cached, improves from 9.0s to 3.7s after switching to the asynchronous engine, a 2.43x improvement. See Fig. 16 for a visualization of the multithreading behavior of the asynchronous optimization and execution engine.

**Behavior on CPUs.** Interestingly, on CPU, the performance boost is less significant compared to GPUs. Initial investigations show three reasons:

1. When using the CPU backend, the optimizer and executor share the same processor, meaning the optimization process itself may slow down the execution. This issue does not exist on the GPU backend, since optimization overlaps with the GPU kernel execution time.

2. On CPU computation itself occupies a bigger fraction of the execution time. For example, in the AutoDiff example, we find 51% of the execution time was spent on scattering force contributions to nodes, which needs expensive software-emulated atomic add. On GPUs, atomic add is hardware-native and is much faster. When the task is fully memory-bound, e.g., the MacCormack advection benchmark, we do achieve a close to ideal 3x speed up on CPUs, similar to the behavior on GPUs.

3. Some of our performance boost comes from eliminating kernels. Compared to the actual computation, kernel launching is expensive on GPU but relatively cheap on CPU.

**Wall-clock time v.s. backend time.** In most cases, our wall-clock time is within 103% of the execution time, which indicates that our multi-threaded optimization and compilation system is able to keep GPU busy. However, in the 2D MGPCG example, we find wall-clock time to be 1.75x higher than the execution time. This is an engineering limitation of our work: some optimization passes, such as kernel fusion, still takes a longer time than expected on GPUs.

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More details on the JAX GitHub.
We have presented an inter-kernel optimization system for parallel, imperative, and spatially sparse computation. In our benchmark cases, we achieved an 1.87x wall-clock time performance improvement, without users changing any computation code. We believe our system can alleviate the low-level performance engineering burden on programmers, achieving higher-performance spatially sparse computation without harming code modularity and readability.

Future work. While our optimizer improves the runtime performance of spatially sparse computation, it does not automatically eliminate the storage cost of intermediate fields. This is partly due to a limitation of Taichi: it materializes the entire data structure before executing any kernel, then no fields can be created or destroyed. To address this problem, Taichi needs a system extension to support dynamic creation and destruction of fields. A tailored optimizer can then be designed.

Meanwhile, there are many unexplored kernel metadata we can extract for sparse computation. For example, a colored Gauss-Seidel solver may only use the “white” cells in a checkerboard pattern. These features may enable further inter-kernel optimization opportunities in physical simulation and numerical linear algebra.

REFERENCES

Martin Abadi, Paul Barham, Jianmin Chen, Zhifeng Chen, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Geoffrey Irving, Michael Isard, Manjunath Kudlur, Josh Levenberg, Rajat Monga, Sherry Moore, Derek G. Murray, Benoit Steiner, Paul Tucker, Vijay Vasudevan, Pete Warden, Martin Wicke, Yuan Yu, and Xiaoqiang Zheng. 2016. TensorFlow: A system for large-scale machine learning. In 12th USENIX Symposium on Operating Systems Design and Implementation (OSDI 16). 265–283. https://www.usenix.org/system/files/conference/osdi16/osdi16-abadi.pdf

Junjie Bai, Fang Lu, Ke Zhang, et al. 2019. ONNX: Open Neural Network Exchange. https://github.com/onnx/onnx

Gilbert Louis Bernstein, Chunmaye Shah, Crystal Lemire, Zachary Devito, Matthew Fisher, Philip Levis, and Pat Hanrahan. 2016. Edb: A DSL for physical simulation on CPUs and GPUs. ACM Trans. Graph. 35, 2 (2016), 21:1–21:12.

James Bradbury, Roy Frostig, Peter Hawkins, Matthew James Johnson, Chris Leary, Dougall Maclarum, George Necula, Adam Paszke, Jake VanderPlas, Skye Wanderman-Milne, and Quoc V. Nguyen. 2018. Jax: Composable transformations of Python-NumPy programs. http://github.com/google/jax

Reynolds Briggs, Doug Evans, Brian Grant, Robert Hundt, William Maddox, Diego Novillo, Seongbaur Park, David Sehn, Ian Taylor, and Ollie Wild. 2007. WHOPR: fast and scalable whole program optimizations in GCC. Initial Draft 12 (2007).

Stephen Chu, Fredrik Kjolstad, and Saman Amarasinge. 2018. Format abstraction for sparse tensor algebra compilers. Proceedings of the ACM on Programming Languages 2, OOPSLA (2018), 1–30.

Zachary DeVito, Niels Joubert, Francisco Palacios, Stephen Oakley, Montserrat Medina, Mike Barrientos, Erich Eilen, Frank Ham, Alex Aiken, Karthik Duraisamy, et al. 2011. Lustre: A domain specific language for building portable mesh-based PDE solvers. In International Conference for High Performance Computing, Networking, Storage and Analysis. 9.

Jiri Filipovic, Matáu Madzin, Jan Fousek, and Laděk Matyska. 2015. Optimizing CUDA code by kernel fusion: application on BLAS. The Journal of Supercomputing 71, 10 (2015), 3934–3959.

Steven W Gugenberger, David AB Hyde, Alan Marquez-Razon, Chenfunliang Jiang, Zhiheng Ge, Xuchen Han, Qi Guo, and Joseph Teran. 2020. A Hybrid Lagrangian/Eulerian Collocated Advection and Projection Method for Fluid Simulation. arXiv preprint arXiv:2003.12227 (2020).

Ming Gao, Xinlei Wang, Kai Wu, Adre Pradhana-Tampubolon, Efthychios Sifakis, Yukel Cem, and Chenfunliang Jiang. 2018. GPU Optimization of Material Point Methods. ACM Trans. Graph. (Proc. SIGGRAPH Asia) 37, 4 (2018), 102.

Rama Kurth Hoetzlein. 2016. Gvdr: Raytracing sparse voxel database structures on the GPU. In Proceedings of High Performance Graphics. Eurographics Association, 109–117.

Changwen Hong, Aravind Sukumar-Rajam, Jinping Kim, Prashant Singh Rewat, Sriman Krishnamoorthy, Louis-Noel Pouchet, Fabrice Rastello, and P Sadasivan. 2018. Gpu code optimization using abstract kernel emulation and sensitivity analysis. In Proceedings of the 39th ACM SIGPLAN Conference on Programming Language Design and Implementation. 736–751.

Yuanming Hu. 2020. The Taichi programming language. In ACM SIGGRAPH 2020 Courses. 1–50.

Yuanming Hu, Luke Anderson, Tzu-Mao Li, Qi Sun, Nathan Carr, Jonathan Ragan-Kelley, and Frédo Durand. 2020. DiffTaichi: Differentiable Programming for Physical Simulation. ICLR (2020).

Yuanming Hu, Yu Fang, Ziheng Ge, Ziyin Qu, Yixun Zhi, Andre Pﬂadenhauer, and Chenfunliang Jiang. 2018. Moving least squares material point method with displacement discontinuity and two-way rigid body coupling. ACM Trans. Graph. (Proc. SIGGRAPH Asia) 37, 4 (2018), 150.

Yuanming Hu, Tzu-Mao Li, Luke Anderson, Jonathan Ragan-Kelley, and Frédo Durand. 2019. Taichi: A language for high-performance computation on spatially sparse data structures. ACM Transactions on Graphics (TOG) 38, 6 (2019), 201.

Yuanming Hu, Jiadong Liu, Xuanda Yang, Mingkuan Xu, Ye Kuang, Weiwei Xu, Qiang Dai, William T. Freeman, and Frédo Durand. 2021. QuanTaichi: A Compiler for Quantized Simulations. ACM Transactions on Graphics (TOG) 40, 4 (2021).

Chenfanfu Jiang, Craig Schroeder, Andrew Selle, Joseph Teran, and Alexey Stomakhin. 2015. The affine particle-in-cell method. ACM Transactions on Graphics (TOG) 34, 4 (2015), 1–10.

Uday Khedker, Amitabha Sanyal, and Bageshri Sathe. 2017. Data flow analysis: theory and practice. CRC Press.

Fredrik Kjolstad, Shoab Kamil, Stephen Chou, David Lugato, and Saman Amarasinghe. 2017. The tensor algebra compiler. Proceedings of the ACM on Programming Languages 1, OOPSLA (2017), 1–29.

Fredrik Kjolstad, Shoab Kamil, Jonathan Ragan-Kelley, David J. W. Levin, Shinjiro Sueda, Desai Chen, Etienne Vouga, Danny M. Kaufman, Guetar Kanwar, Wojciech Matusik, and Saman Amarasinghe. 2016. Simt: A language for physical simulation. ACM Trans. Graph. 35, 2, 2016:1–20:21.

Kathleen Knoke and Vivek Sarkar. 1998. Array SSA form and its use in parallelization. In Proceedings of the 25th ACM SIGPLAN-SIGACT symposium on Principles of programming languages. 107–120.

C. Lattnner, M. Amini, U. Bondhugula, A. Cohen, A. Davis, J. Pliemar, R. Riddle, T. Shipman, N. Vaslach, and O. Zinenko. 2021. MLIR: Scaling Compiler Infrastructure for Domain Specific Computation. In 2021 IEEE/ACM International Symposium on Code Generation and Optimization (CGO). 2–14. https://doi.org/10.1109/CGOS1591.2021.9370308

Mingzhen Li, Yi Liu, Xiaoyuan Liu, Qingxiao Sun, Xin You, Hai long Yang, Zhonghui Luan, and Depei Qian. 2020. The Deep Learning Compiler: A Comprehensive Survey. arXiv preprint arXiv:2002.03794 (2020).

Haixiang Liu, Yuanming Hu, Bo Zhu, Wojciech Matusik, and Efthychios Sifakis. 2018. Narrow-band Topology Optimization on a Sparsely Populated Grid. ACM Trans. Graph. (Proc. SIGGRAPH Asia) 37, 6 (2018), 251:1–251:14.

Dror E. Maydan, Saman P. Amarasinghe, and Monica S. Lam. 1993. Array-data flow analysis: theory and practice. ACM Trans. Program. Lang. Syst. 3, 2 (1981), 1–27.

Ken Metueth. 2013. VDB: High-resolution sparse volumes with dynamic topology. ACM Trans. Graph. 32, 3 (2013), 27.

Ken Metueth, Jeff Lait, John Johanson, Jeff Budsberg, Ron Henderson, Mihai Alden, Peter Cucka, David Hill, and Andrew Pearce. 2013. OpenVDB: an open-source data structure for voxel data. ACM Trans. Graphics (Proc. SIGGRAPH Asia) 32, 4 (2013), 9.

Michael B. Nielsen and Robert Bradson. 2016. Spatially adaptive FLIP fluid simulations in Infroth. In ACM SIGGRAPH 2016 Talks. ACM, 41.

Adam Paszke, Sam Gross, Francisco Massa, Adam Lerer, James Bradbury, Gregory Chanan, Trevor Killeen, Zeming Lin, Natalia Gimelshein, Luca Antiga, Alban Desmaison, Andrew Kopf, Edward Yang, Zachary DeVito, Martin Raison, Alykhan Tejani, Sasank Chilamkurthy, Benoit Steiner, Lu Fang, Junjie Bai, and Soumith Chintala. 2019. PyTorch: An Imperative Style, High-Performance Deep Learning Library. In Advances in Neural Information Processing Systems 32. H. Wallach, H. Larochelle, A. Beygelzimer, F. d’Alchê-Buc, E. Fox, and R. Garnett (Eds.). Curran Associates, Inc., 8024–8035. http://papers.neurips.cc/paper/9015-pytorch-an-imperative-style-high-performance-deep-learning-library.pdf

Bo Qin, Oliver Reiche, Frank Hanung, and Jurgen Teich. 2018. Automatic kernel fusion for image processing applications. In Proceedings of the 21st International Workshop on Software and Compilers for Embedded Systems. 76–85.

Nadav Rotem, Jordan Fix, Saleem Abdurabos, Garret Catron, Summer Deng, Roman Dzhabarov, Nick Gibson, James Hegeman, Meghan Lele, Roman Levenstein, et al. 2018. Glow: Graph lowering compiler techniques for neural networks. arXiv preprint arXiv:1805.00978 (2018).

Andrew Selle, Ronald Fedkiw, Byungmoon Kim, Yingjie Liu, and Jarek Rossignac. 2008. An unconditionally stable MacCormack method. Journal of Scientific Computing 35, 2-3 (2008), 350–371.
Fig. 16. **Top:** In our asynchronous execution engine, multiple compilation threads simultaneously compile optimized IR to executable kernels, maximizing JIT benefits. Timelines are gathered from the MGPCG example, where our parallel compilation system leads to a 2.43x shortened program start-up time. **Bottom:** At later stages of program execution, most possible inter-kernel optimized kernels are already compiled and cached, so the compilation threads are mostly idle. Still, our multithreading framework allows the inter-kernel optimizer to overlap with the launcher thread and GPUs, making sure no GPU starvation happens. Timelines are gathered from the MLS-MPM example.
AsyncTaichi: On-the-fly Inter-kernel Optimizations for Imperative and Spatially Sparse Programming (Supplemental Document)

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1 MICROBENCHMARK CASES

Here we describe the cases in the microbenchmarks.

The case chain_copy contains 2 kernels \( y[1] = x[1] + 1 \) and \( z[1] = y[1] + 4 \), like Fig.8 in the main paper. They are fused in asynchronous mode.

 increments contains 10 inc() kernels \( x[i] += 1 \) in Fig.8 in the main paper.

 fill_array contains 10 kernels, all filling a 1-D dense array with the same constant value. With task fusion, only 1 task is launched in these cases instead of 10 tasks. The running time is nearly 10x faster.

 sparse_saxpy contains some kernels performing saxpy (Scalar Alpha X Plus Y) operations among sparse tensors. The performance boost of execution time comes from the elimination of list generation and task fusion. Sometimes the wall-clock time is slower than the synchronous mode because of the overhead of the asynchronous engine.

Fig. 1. Microbenchmarks results. "Sync" refers to the reference system [Hu et al. 2019]. "Async" refers to our system with asynchronous execution and inter-kernel optimizations.

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autodiff computes a loss function as reduction on an array and accumulates the gradients to another array 10 times. With dead store elimination, the forward tasks computing the loss function should be eliminated except for the last one, so the number of launched tasks reduces by roughly a half.

 stencil_reduction performs stencil and reduce operations on a tensor. They are common operations in computer graphics.

 mpm_splitted contains some substep() kernels in an MPM program [Hu et al. 2018].

 simple_advection performs semi-Lagrangian advection 10 times. The performance boost comes from activation elimination and task fusion.

 deep_hierarchy is a multi-resolution program downsampling in 4 levels. 

 multires is a multi-resolution program downsampling in 4 levels.

2 DETAILS IN TASK FUSION

Fusing criteria. We fuse tasks A and B when all the following criteria are satisfied:

(1) There is no path of length \( \geq 2 \) between A and B in the SFG. If we fuse tasks A and B when there is a path \( A \rightarrow C \rightarrow B \), C can neither depend on the fused task nor become its prerequisite, leading to a contradiction.
(2) Either both tasks are serial, or both tasks are parallel with the same loop ranges (if the tasks’ type is range-for) or the same SNode (if the tasks’ type is struct-for).

(3) If $A \rightarrow B$ are connected via a SNode in the SFG, both tasks need to access the SNode in an element-wise manner. Failing to do so may lead to data races. For example, if there is an edge $A \rightarrow B$ (corresponding to some SNode) in the SFG, we need every accesses to that SNode in both tasks are at the same address, and that address is unique per iteration of the loop. When not every accesses on the SNode are on the same address, we may bump into a racing condition if we fuse the tasks, for example,

```python
for i in x:
    x[1] = 1
for i in x:
    x[1 + 1] = 2
```

The access to $x[1 + 1]$ at the $i$-th iteration is racing with $x[1]$ at the $(i + 1)$-th iteration when fused. If we access some address which is not unique per iteration of the loop, we may also bump into a racing condition if we fuse the tasks. Example:

```python
for i in x:
    y[0] = 0
for i in x:
    y[0] += x[i]
```

These two tasks compute the sum of $x$ and store it in $y[0]$, but if we fuse the tasks, they will store only one element in $x$ to $y[0]$ because the access of $y[0]$ is not unique per iteration of the loop.

(4) When there are multiple tasks that can be fused together, we introduce a compilation option `async_max_fuse_per_task` with a default value 1, and greedily fuse each task no more than that times per iteration of the task fusion optimization pass. In this way, when there are $n$ tasks that can be fused together, we will perform the task fusion optimization for $O(\log(n))$ iterations, and avoid fusing $n$ tasks one by one into a huge task. This makes the intra-kernel optimizations after task fusion faster, and utilizes the IR bank better when there are duplicated tasks. See section 7.2 in the main paper for more details.

To find all fusible pairs of tasks efficiently, we compute the transitive closure of the SFG using bitsets. For pairs of tasks without edges, we group tasks by the tasks’ type, loop range (if the type is range-for), or the SNode (if the type is struct-for). For each group, we use the transitive closure to find which pairs of tasks do not have any path to each other quickly; for each edge $A \rightarrow B$ in the SFG, we check if there is a task $C$ such that $A$ has a path to $C$ and $C$ has a path to $B$ using the transitive closure. The two cases above cover the criterion “there is no path of length $\geq 2$ between $A$ and $B$”. Then we apply the other criteria to find if the pair of tasks is fusible, and greedily fuse them.

3 INTRA-KERNEL DATA-FLOW OPTIMIZATIONS

We apply the traditional control-flow analysis to optimize within kernels. We build a control-flow graph along with the hierarchical IR, and perform analysis on the graph. With the help of control-flow analysis, we perform optimizations including store-to-load forwarding, dead store elimination, and identical load/store elimination. These optimizations motivate task fusion as it greatly simplifies fused tasks.

We also utilize control-flow analysis to help compute task meta information. Since stores to a SNode may only partially modify a value state, the resulting value state (which contains the modified and unmodified part) may need a read from the previous version of the value state. We use control-flow analysis to detect which SNodes do not need a read from the previous version of the value state.

Fig. 2 shows the effect of data-flow optimization on 360 Taichi test cases. Although these test cases are relatively simple, data-flow optimization still leads to 16% fewer instructions.

4 EVALUATION

4.1 MGPCG at different scales

To evaluate our system on problems of different scales, we scan the problem size and plot the wall-clock time and backend time in Fig. 3. Most of the optimizations come from eliminating fragmented kernels caused by list generation. As the problems scale up, these kernels occupy relatively less time, hence we observe the performance boost to be more significant at lower resolutions. An ablation study of four inter-kernel optimization passes is listed in Table 5 in the main paper.
4.2 MacCormack advection benchmark setup
This benchmark is carried out on a 3D unit grid of 256³ cells. We advect three scalar physical fields (temperature, color, and density) over a sparsely populated vector field defined over a tube domain with inner radius 0.32 and outer radius 0.45. The statistics of the first five frames are discarded to exclude the effects of the JIT compilation.

4.3 MLS-MPM benchmark setup
As shown in Fig. 4, we seed a uniform cube of 16, 777, 216 (256³, on GPU) or 2, 097, 152 (128³, on x64 CPUs) fixed corotated particles into a grid of size $1 \times 1 \times 1$, with the distance between each two adjacent particles 1/512. Each particle is a cube of length 1/512, with $\rho = 10^3$, $E = 2 \times 10^4$, $\nu = 0.4$. The gravity is $g = 9.8$. Each frame consists of 400 substeps, with time step size $\Delta t = 10^{-4}$s. We benchmark the time of the second frame (i.e., the 401st to the 800th substeps). The ground is set to be at $z = 1/32$, and to make the cube touch the ground in the second frame, we set the initial $z$-coordinate of the center of the bottom-most particles to be 49/1024. The $x$ and $y$ coordinates of the center of the cube are set to be the center of the grid.

Fig. 4. The falling cube in our MLS-MPM benchmark. The cube’s initial position is higher than the one we used in the benchmark for better visualization.

4.4 Compiler hints in MLS-MPM
In MLS-MPM, the G2P task writes the values in the particle SNode, and the P2G task reads the values in the particle SNode. Since both tasks are parallel, it is challenging to infer that there will be no racing conditions if we fuse the two tasks together. Therefore, we hint our compiler with a simple statement (in mpm_solver.py):

```python
p = ti.loop_unique(p, covers=self.particle)
```

where $p$ is the particle ID in one iteration of the loop in the G2P task. This statements means that $p$ is unique per iteration of the loop, and the set of its value among all iterations of the loop covers all active indices in the particle SNode (so the values stored in the $p\text{id}$ (particle ID) field is a permutation of all active indices in the particle SNode). With this hint, we can infer that there will be no racing conditions if we fuse the G2P and P2G tasks together since different iterations of these tasks access different addresses. We further analyze that the $c$ field (affine velocity around the particle), as a component in the particle SNode, is fully written in the G2P task (or the fused G2P2G [Wang et al. 2020] task), so we do not need to write to this field until the last G2P task.

5 KEY SOURCE CODE FILES
We partially reuse the existing Taichi system, with key modifications listed below:

- The SFG data structure and some optimization passes are implemented in taichi/program/state_flow_graph.[h/cpp];
- The asynchronous execution engine is implemented in taichi/program/async_engine.[h/cpp];
- The IR bank and some of the optimization passes are implemented in taichi/program/ir_bank.[h/cpp].
Other low-level implementation details are scattered in the whole Taichi codebase.

REFERENCES
Yuanming Hu, Yu Fang, Ziheng Ge, Ziyin Qu, Yixin Zhu, Andre Pradhana, and Chenfanfu Jiang. 2018. A moving least squares material point method with displacement discontinuity and two-way rigid body coupling. ACM Trans. Graph. (Proc. SIGGRAPH Asia) 37, 4 (2018), 150.
Yuanming Hu, Tzu-Mao Li, Luke Anderson, Jonathan Ragan-Kelley, and Frédo Durand. 2019. Taichi: a language for high-performance computation on spatially sparse data structures. ACM Transactions on Graphics (TOG) 38, 6 (2019), 201.
Xinlei Wang, Yuxing Qiu, Stuart R Slattery, Yu Fang, Minchen Li, Song-Chun Zhu, Yixin Zhu, Min Tang, Dinesh Manocha, and Chenfanfu Jiang. 2020. A massively parallel and scalable multi-gpu material point method. ACM Transactions on Graphics (TOG) 39, 4 (2020), 30–1.