ARENA: Asynchronous Reconfigurable Accelerator Ring to Enable Data-Centric Parallel Computing

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Abstract—The next generation HPC and data centers are likely to be reconfigurable and data-centric due to the trend of hardware specialization and the emergence of data-driven applications. In this paper, we propose ARENA – an asynchronous reconfigurable accelerator ring architecture as a potential scenario on how the future HPC and data centers will be like. Despite using the coarse-grained reconfigurable arrays (CGRAs) as the substrate platform, our key contribution is not only the CGRA-cluster design itself, but also the ensemble of a new architecture and programming model that enables asynchronous tasking across a cluster of reconfigurable nodes, so as to bring specialized computation to the data rather than the reverse. We presume distributed data storage without asserting any prior knowledge on the data distribution. Hardware specialization occurs at runtime when a task finds the majority of data it requires are available at the present node. In other words, we dynamically generate specialized CGRA accelerators where the data reside. The asynchronous tasking for bringing computation to data is achieved by circulating the task token, which describes the dataflow graphs to be executed for a task, among the CGRA cluster connected by a fast ring network. Evaluations on a set of HPC and data-driven applications across different domains show that ARENA can provide better parallel scalability with reduced data movement (53.9%). Compared with contemporary compute-centric parallel models, ARENA can bring on average 4.37× speedup. The synthesized CGRAs and their task-dispatchers only occupy 2.93mm² chip area under 45nm process technology and can run at 800MHz with on average 759.8mW power consumption. ARENA also supports the concurrent execution of multi-applications, offering ideal architectural support for future high-performance parallel computing and data analytics systems.

Index Terms—Compute-Flow-Architecture, Runtime Reconfiguration, Asynchronous Parallel Execution, Abstract Machine Model.

1 INTRODUCTION

With the slowing down of Moore’s Law [51], future computer systems will need to resort to domain-specific accelerators for continuous performance scaling [27], [63] under the same power envelope. This is especially the case for HPC and data centers, as we are quickly entering an era of extreme heterogeneity [71], characterized by cluster nodes integrating a multitude of cooperating accelerators [33], [38], [43], [61].

While integrating domain-specific accelerators (DSAs) into HPC and data centers provides considerable efficiency gains [33], [38], [55], [64], it leads to enormous complexities as well. First, DSAs can only be economically designed for ubiquitous computational patterns in applications, while the workloads currently running in HPC and data centers are converging towards mixed workloads that include scientific simulation, machine learning, data analytics, etc. Second, managing various (typically loosely coupled) accelerators across many nodes significantly complicates programming models and the software infrastructure. In both HPC and data centers, the accelerators typically need to be shared among multiple users, often using multiple nodes for applications with divergent characteristics. Since we could not design hardware accelerators for all seen and unseen kernels, reconfigurable architecture, which allows specialization after system deployment and even during system execution, promises to be a wise solution. While Field Programmable Gate Arrays (FPGAs) have already been deployed at large scale in some data centers [61], they may suffer from limited frequency and energy-efficiency compared with ASICs, as well as long reconfiguration time (e.g. in milliseconds) due to bit-level reconfigurability. Coarse-grained reconfigurable arrays (CGRAs), which integrate highly optimized functional units (rather than fundamental lookup tables or LUTs) and offering reconfigurability at the word-level, emerge as a promising alternative choice [60]. The rapid reconfiguration [24] makes dynamic formalization of hardware accelerators at runtime becomes feasible, and even plausible.

Conventional large-scale HPC clusters implicitly assuming homogeneous node-configuration and bulk-synchronous-parallel (BSP) execution model suffer from three low-utilization challenges regarding per-node data locality: (1) unbalanced data distribution among homogeneous nodes may lead to unbalanced workload and poor utilization; (2) If data is not locally available, during the long-time remote data fetching, the compute units can be idle; (2) Even worse, these idle units or idle nodes cannot be reclaimed for other tasks despite the node may hold their desired data. As emerging workloads become more dynamic and data-driven, decentralized asynchronous task management is highly desired, while data locality becomes a crucial factor for the system design [18], [27], [63]. This is largely due to the observation that the energy cost of data-movement significantly outweighs the energy cost of computing them [34], [40], [50], which is particularly the case when migrating
data through the interconnect network (e.g., the power budget is ∼5.5 watts per full bi-directional NVLink port [1]). While software solutions such as active messages [16], [17] and remote procedure call (RPC) mitigate the problem by pushing computation to the nodes where data resides, they suffer from considerable overhead due to the lack of architectural support. Existing applications however still widely adopt the BSP model [14], [69] alternating phases of (parallel) local computation with phases of global communication. Note that the BSP model implicitly assumes that the majority of the time can be spent in easily parallelizable computation phases, with limited data movement. However, the exponential growth in the availability of data and the emergence of new applications, radically changed the balance.

ARENA can provide better parallel scalability with reduced data movement (53.9%) and bring 2.17× and 4.37× speedup over traditional compute-centric approach with and without CGRA acceleration. The CGRA-based ARENA prototype only costs 2.93nm² chip area in 45nm and can work at 800MHz with 759.8mW power consumption per node, showing significant advantages over the present architectural design in the current HPC and data centers.

2 Motivation
Scientific simulation, where linear solvers iterate on data organized in dense (structured sparse) matrices or tensors, typically easy to divide in equally sized tiles, represents the premier HPC workload [5], [6], [56], [68], [73]. However, emerging HPC applications, targeting areas such as power grid dynamics [4], seismic risk assessment [49], urban systems simulation, and microbiome analysis [8], will likely combine together traditional scientific simulation with advanced data analytics and machine learning. The datasets for these applications are much less structured, and thus more difficult to organize in regular and partitionable data structures. Applications will alternate phases of scientific simulations with regular behaviors, to phases where the computation happens on sparse data structures (e.g., sparse matrices, graph traversal) that induce unpredictable fine-grained data accesses and irregular behaviors. This scenario provides a clear opportunity for adaptability to diverse behaviors with reconfigurable hardware, while at the same time makes the current HPC programming models inadequate. In the following, we describe three major existing multi-node computing paradigms to motivate the ARENA design.

2.1 Baseline-1: Compute-Centric BSP Execution Model
HPC systems typically rely on the classical Bulk Synchronous Parallel (BSP) programming model in which a process is assigned to a processor or an entire node, and communication typically happens through message passing with libraries such as MPI. In the BSP model, the computation proceeds as a series of global supersteps: concurrent computation, where every participating nodes perform parallel computations on local data; communication, where nodes exchange data among them (with various, algorithm dependent, patterns); and barrier synchronization, to align execution of nodes.

The BSP model assumes that data are partitioned and distributed across nodes and rarely moves, to facilitate the local computation super-steps. Otherwise, the message-passing based communication super-steps would dominate the execution time. While this model works well for applications with easily partitionable data, regular computation, and limited, structured communication, it starts to experience significant limitations when workloads exhibit irregular behaviors (skewed data distributions, high synchronization intensity, irregular communication patterns). For these reasons, we consider the BSP model as Compute-Centric.

Consider as an example an application with the (hierarchical) task graph in Figure 2(a), where the computation is split into 4 high-level tasks, each one executing task-partitioned computational kernels where the subtasks require
data from other nodes. When employing a BSP model, both the data allocation and the distribution of the high-level tasks are fixed for the entire application execution. Hence, if a subtask needs data available in another node, it needs to initiate a communication phase, load the remote data, and synchronize to avoid hazards. Despite the latest high-performance designs can exploit mechanisms such as remote-direct-memory-access (one-sided communication, not requiring a blocking receive with implicit synchronization from the remote node), prefetching and data migration, when these remote accessing are frequent, the bandwidth requirements may trigger additional data-centric procedure calls, following the data-centric execution model. While FPGAs potentially allow acceleration of kernels (e.g., FFT, GEMM), this approach matches with an offload accelerator model - tasks and computational kernels do not move in the system. On the other hand, a reconfigurable architecture potentially allows to dynamically adjust the configuration at runtime, being able to accelerate divergent tasks with the computation proceeds. Despite the potential, the excessive reconfiguration overheads (typically in milliseconds) makes such an approach very costly.

Limitations – Reconfigurable accelerators make it possible to accelerate a more diverse workload, but current practice in heterogeneous HPC still leverages the offload model. The lack of low-latency runtime reconfiguration also limits the chances of large-scale task migration across the whole system. On the other hand, the data-centric execution model allows different tasks to work concurrently, requiring a blocking receive with implicit synchronization from the remote node, prefetching and data migration, even more data movement and synchronization, as the actual data distribution and access patterns are unknown before runtime.

Limitations – While compute-centric BSP long remains the standard model in HPC, its adoption in emerging HPC applications may be limited by data movement and synchronization. HPC practitioners have introduced asynchronous multi-task runtimes to tackle the limitations of the BSP model. Besides migrating data blocks where the computation occurs, these runtimes often allow tasks to migrate where the data reside, via approaches such as active messages and remote procedure calls, following the data-centric models.

2.2 Baseline-2: Reconfigurable accelerators in HPC

Reconfigurable accelerators have been deployed at a massive scale in data centers to provide application-specific acceleration with improved power-/area-efficiency [30], [60], [61]. Some institutions have also started hosting clusters with FPGA to perform research in HPC [2].

However, accelerators in HPC installations still generally adopt the BSP model, where a part of the local computation is offloaded to the accelerator itself. This also requires gathering desired data by the running tasks offloaded for execution. While FPGAs potentially allow acceleration of workloads more diverse than conventional accelerators such as GPUs, their current usage in HPC application often entails static configuration for accelerating a small amount of kernels (e.g., FFT, GEMM). This approach matches with an offload accelerator model - tasks and computational kernels do not move in the system. On the other hand, a reconfigurable architecture potentially allows to dynamically adjust the configuration at runtime, being able to accelerate divergent tasks with the computation proceeds. Despite the potential, the excessive reconfiguration overheads (typically in milliseconds) makes such an approach very costly.

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2.3 Baseline-3: Data-Centric Software Approaches

Many programming models have been leveraged or designed to allow data-centric execution on multi-node systems. SSMP [55] can operate on shared memory machines and support dynamic detection of dependencies between tasks. The implicitly shared memory management and dependence detection improve the programmability at the cost of increased synchronization overhead. Remote procedure call (RPC) achieves near-data-computation based on prior knowledge about the exact distribution of data. X10 [21] and Chapel [20] allow the programmers to control where to place the data and tasks. Similarly, Legion [12] enables explicit, programmer-controlled movement of data and placement of asynchronously spawned tasks, based on locality information. Legion employs a Cilk-like [15] algorithm for locality-aware task stealing.
Towards data-centric programming, MapReduce programmers think in a data-centric fashion: they focus more on handling the sets of data records, rather than managing fine-grained threads, processes, communication, and coordination [9]. However, MapReduce constrains its usage to batch-processing tasks, which falls in the BSP scope. To accommodate the emerging data-driven applications with irregular and unpredictable data access patterns, data-centric execution with asynchronous task-spawn should be enabled with hardware support. Meanwhile, the synchronization and task dependencies should be specified by the programmers to eliminate the unnecessary performance and energy overhead rather than forced by the programming model (e.g., remote procedure need to return to local in RPC, all the spawned tasks of the same ancestor need to join eventually in Legion). Besides the data locality, the runtime should also consider the computing resource utilization when reconfigurable accelerators are deployed and shared by multi-users in HPC/data-center environments.

Limitations – The high-level software framework and runtime facilitate the asynchronous execution of tasks and attempt to take advantage of data locality. Unfortunately, existing frameworks based on software solutions incur considerable overhead. The lack of hardware reconfiguration also limits the benefit from application-specific design and heterogeneity.

2.4 Compute-Flow ARENA Execution Model

We propose ARENA to address the limitation of the three aforementioned baseline. ARENA includes a novel programming model targeting asynchronous data-centric execution paradigm. As shown in Figure 2, all the configurable nodes in ARENA are connected by a ring network to bring the specialized computation to the data rather than the reverse to minimize data movement. Each reconfigurable node mainly contains a CGRA (detailed in Section 4.3) that supports real-time reconfiguration and simultaneous execution of multi-tasks.

3 ARENA PROGRAMMING MODEL

Being the interface between software and hardware, the ARENA programming model defines a list of API functions in Table 1. On one hand, in order to program an ARENA abstract machine, a software programmer has to define their user-logic as task functions, and rely on the User APIs to operate the abstract machine. Please note that although in this work we use CGRAs as the hardware testbed, it is only one of the possible instantiations of the ARENA abstract machine model (AMM). On the other hand, in order to support ARENA software and run ARENA program, an alternative architecture has to support the Hardware Abstract Functions here.

3.1 ARENA Programming Interface

To program an ARENA abstract machine, the programmers first partition their application into tasks and register the defined tasks to the ARENA runtime. Ideally, the partition can separate the working set into a bunch of continuous data segments, where each task accounts for a segment.

TABLE 1: ARENA programming and hardware APIs.

ARENA does not limit the granularity of a task, which can be extremely fine-grained or coarse-grained. While ARENA works perfectly when the data is locally available for a task, we understand this is not always feasible. When remote data access is inevitable, the application can either spawn a new task for the remote data, or explicitly initiate the data-movement through the data-transfer-network.

Fig. 3: Example of programming SSSP in ARENA.
Figure 3 shows an example on how to solve the single-source shortest path (SSSP) problem using a breadth-first search (BFS) kernel. The design traverses associated vertices until the shortest path(s) from a source node to all the other nodes are found. Without losing generality, we assume the graph, represented as an adjacency matrix, is distributively stored on all nodes and each node holds $SIZE/NODES$ vertices (rows) of the entire graph (the adjacency matrix is in $SIZE \times SIZE$, an initial value of $\infty$ indicates a connected edge while 0 implies no connection).

ARENA enables asynchronous data-centric execution by dynamically spawning new task-tokens among the nodes. Currently, all tasks need to be registered at the beginning. During runtime, task-tokens are circulating among all nodes in the ring. In case a node confirms it has the data required by a task-token (indicated by the starting & ending addresses $TASK_{start}$ and $TASK_{end}$) as well as sufficient hardware resources for runtime hardware specialization implied by the task-token, it takes out the token from the task-token-stream and executes it. A task will be executed by the CPU if no hardware specialization is provided. New tasks for remote nodes can be generated or spawned at any node. We currently rely on the programmer to determine the granularity of a spawned task (in other words, the data-range a spawned task designated). Fine-grained tasks facilitate asynchronous execution but increase scheduling overhead in the runtime. We discuss this tradeoff in detail in Section 3.2.

This is in contrast with the conventional compute-centric approach demanding frequent data communication and synchronization [19]. As each node maintains the vertex status locally, and no prior knowledge about vertex distribution is asserted, repeated all-to-all communications are essentially desired for broadcasting vertex updating information to associated nodes on the present frontier. Figure 4 shows the performance gain of ARENA for the SSSP application.

### 3.2 ARENA Runtime Support

Figure 4 and 5 illustrate the workflow of ARENA runtime executed per-node and the pseudo-code of the workflow, respectively. As can be seen, multiple tasks (marked with different colors) can be asynchronously executed in parallel. Note, the runtime can be supported by CPUs, GPUs, DSPs, or any other fixed or reconfigurable hardware substrate given the substrate realize the Hardware Abstract Functions and support the Base Constructs.

We describe the runtime process below: Primarily, the task queues (line 3) and local data range (line 7) are initialized. We then proceed with 6 steps: **Step-(1):** All the incoming task tokens from the proceeding node will be appended to the RecvQueue (line 8). **Step-(2):** A token popped from the RecvQueue will be processed in the Filter, where a task can be split into multiple tasks, which are either buffered in the WaitQueue for local execution, or forwarded to the SendQueue, wait for being conveyed to the next node (line 21, 22). The logic is: (I) if the task data range is irrelevant to the node’s local data range, it is forwarded to SendQueue as it is; (II) if the task data range is a subset of the node’s local data range ($local_{start} \leq TASK_{start} \leq TASK_{end} \leq local_{end}$), implying the local availability of all the needed data for the task, the token will be pushed into WaitQueue for future execution; (III) if the data range indicated by the task is a superset of the node’s local data range ($ TASK_{start} \leq local_{start} \leq local_{end} \leq TASK_{end}$), it suggests that the task might be too coarse-grained. We split the task into three portions and spawn three new tasks. The one with data range $local_{start}$ to $local_{end}$ will be buffered in WaitQueue for local processing; the other two tasks are redirected to SendQueue; (IV) finally, if the task data range is partially aligned with the node’s local data range, two new tasks will be spawned. The aligned part is buffered in WaitQueue while the mismatch part is forwarded to SendQueue. **Step-(3):** The runtime checks whether there is available resources for the token at the top of the WaitQueue to be executed (line 26). **Step-(4):**
If so, the runtime verifies whether the task needs to incur any inevitable remote data access. If yes, the data will be acquired from the objective remote nodes (line 50) through the Data-Transfer-Network. **Step-(5):** when all demanding data are available, the task is issued to the computing resources for execution (line 55). **Step-(6):** As new tasks can be generated locally in a node during the task execution, to avoid too many tasks flooding the system, a CoalescingUnit (line 55) is designed to aggregate the newly generated tasks if the boundaries of their data-ranges coincide each other, and whether alternative key parameters (e.g., task-token carried partial-reduction variables) are the same. This can avoid the scenario that too many generated fine-grained tasks saturate the task-token network and the associated buffers. Finally, the runtime on a particular node terminates when the TERMINATE token has been continuously received, and there is no pending tasks in the local WaitQueue (line 22).

4 ARENA CGRA-Cluster Architecture

Our ARENA prototype in this work is built upon a CGRA cluster interconnected by a fast ring network. Figure 6(a) shows the overall design — multiple reconfigurable nodes are connected in a ring topology. Each node incorporates a microcontroller (e.g., a simplified CPU), a task dispatcher, a CGRA, a network interface (NIC), a DMA unit, and local memory storage. At runtime, task tokens are circulating along the ring. The dispatcher can split, offload, and forward a task token based on the data range as already discussed. We adopt the ring network topology to simplify the routing strategy and provide sufficient bandwidth for delivering the small-sized task tokens (~21 bytes) with up to 16 nodes evaluated in this paper. The ring network can also provide near optimal bandwidth for most collective communication [54], and can be easily built upon various physical network topology. We leave the exploration of alternative multi-node topology as a future work.

4.1 Task Token

A task is represented by a task token in ARENA, which can be dynamically spawned, executed, delivered, and split. Figure 6(b) shows the general format of the task token which comprises 7 fields: TASK<sub>id</sub> indicates the task will be executed, which is registered by the user (using ARENA_task_register()) before launching the ARENA runtime. During execution, the reconfigurable node will be dynamically configured (see Section 4.3) based on TASK<sub>id</sub>, TASK<sub>start</sub> and TASK<sub>end</sub> together describe the data range for the task. PARAM refers to a token-carried return value that is typically initialized by its parent task. This field is useful when performing collective operations (e.g., reduction and accumulation). For unavoidable remote data access, we use REMOTE<sub>start</sub> and REMOTE<sub>end</sub> to indicate the starting and ending addresses. FROM<sub>node</sub> labels the node where its parent task locates. Each task token thus requires 21 bytes in our prototype architecture (i.e., 4-bit for TASK<sub>id</sub> and FROM<sub>node</sub>, 4-byte each for the other fields).

4.2 Task Dispatcher

ARENA’s task dispatcher mainly includes a task FilterLogic and three queues as shown in Figure 7. The FilterLogic can offload, split, and convey a task token based on the data requirement (see Section 3.2). The NIC handles remote data requests from the task tokens in the WaitQueue. The WaitQueue will be acknowledged when the required remote data arrives at the data memory. The CGRA controller will then pop the acknowledged task token from the head of WaitQueue and reconfigure the CGRAs accordingly.
4.3 Reconfigurable CGRA Nodes and Toolchain

To achieve rapid dynamically reconfiguration, an ARENA node is prototyped with CGRA. The on-chip configuration memory is used for conserving the control signals for each task. The intra-node CGRA consists of 64 tiles connected in a mesh network. A scratchpad data memory conserves the data required for the computation. Note that both the control signals and the data are pre-loaded by the CPU/micro-controller through the DMA unit before launching the ARENA runtime. The CGRA communicates with the Task Dispatcher through the CGRA controller. The controller can offload tasks and coalesce spawned tokens through the Coalescing Unit.

**CGRA Tile** – As shown in Figure 7 each CGRA tile contains a functional unit, a scratchpad control memory, a crossbar switch, and three sets of registers. The functional unit supports all the basic operations (e.g., add, mul, shift, select, branch, load, store, etc). Control-divergence (i.e., existence of multiple control flow paths) inside the loop kernel is supported through partial predication [32]. The functional unit also supports the spawn operation (i.e., generate a new task token and issue to the CGRA controller), which is unique in ARENA. If sufficient information is available (\(TASK_{id}, TASK_{start}, \) and \(TASK_{end}\)), a new token can be spawned in a single cycle; otherwise, two cycles are required to encode additional information (i.e., PARAM, \(REMOTE_{start}\), and \(REMOTE_{end}\)). The FROM\(_{node}\) filed will be automatically filled by the CGRA Controller. In Figure 7 there are 4 tiles being able to spawn new tasks (marked in green). The leftmost tiles are connected to two 4-port scratchpad data memory banks. The functional unit can be configured to perform different operations at each cycle based on the control signals from the control memory. The CGRA tiles are granular to support the simultaneous execution of multiple tasks. Specifically, all the tiles are partitioned into 4 groups and a task can be executed by 1, 2, and 4 groups, dynamically managed by the CGRA controller.

**Control Memory** – The control signals of all the tasks are initially pre-loaded into the control memory. At runtime, tiles iterate over a subset of the control signals to execute specific tasks based on the \(TASK_{id}\) in the task token. Each tile requires a 480-byte control memory in our prototype to support all application tasks evaluated in this paper (Section 5). Each task has three execution modes powered by different tile groups. It takes only 8 cycles for the CGRA controller to reconfigure specific tile groups by using the data network to forward the \(TASK_{id}\) systolically through the array from right to left.

**CGRA Controller** – The CGRA Controller can launch a task (using the task token at the head of WaitQueue) to be executed by different groups of the CGRA tiles. Based on the current CGRA utilization status and the data requirement of the target task, the CGRA controller allocate an appropriate number of groups for a waiting task. For example, if the data range required by the target task is less than a quarter of the local data range (i.e., \(TASK_{end} - TASK_{start} < (LOCAL_{end} - LOCAL_{start})/4\)), only one available group (i.e., 2x8 CGRA tiles) will be allocated to the task. When the target task works on more than half of the local data range (i.e., \(TASK_{end} - TASK_{start} > (LOCAL_{end} - LOCAL_{start})/2\)), the CGRA controller attempts to allocate all the four groups (i.e., entire 8x8 CGRA tiles) when available (otherwise, two groups are allocated). In addition, there are four queues in the controller to temporarily hold the spawned task tokens, which would be coalesced by the Coalescing Unit if any two of them imply continuous task data range and share the same \(TASK_{id}\) and PARAM. When there are insufficient slots in the queues, the CGRA controller stops fetching tokens from the WaitQueue in the Task Dispatcher. Deadlock can be avoided by providing a memory attached to the CGRA controller for storing the over-spawned task tokens.

**Compiler Toolchain for CGRA** – Figure 8 shows the development procedure for ARENA using CGRA cluster as the backend. As already mentioned, the CGRA cluster is just one design choice; the ARENA execution model can be realized on alternative back-ends in case the HAF APIs (Table 1) are realized. For example, on a CPU cluster backend, we can adopt MPI non-blocking primitives [29] to realize HAF APIs. We use this as one of our baselines in the evaluation. Here, to support the CGRA-cluster backend, an LLVM [42] based design automation toolchain is developed. In particular, a kernel that typically includes a multi-level nested loop is described as a task. As shown in Figure 8 to synthesize an appropriate mapping for a task on the allocated CGRA tiles, the nested loop is first vectorized with a factor that can fully leverage relatively larger CGRA tiles (e.g., 8x8 tiles) in the vectorization pass. Then, the remaining loops are flattened, generating the Control-Data Flow Graph (CDFG) representation, which is an extension of DFG with control dependence edges. We implemented a heuristic method [39] to map the CDFG on various combinations of the tiles (i.e., 2x8, 4x8, and 8x8 tiles) and produce their control signals.

**5 Evaluation**

**5.1 Environment Setup**

The ARENA runtime is evaluated on traditional CPU HPC clusters and our proposed CGRA-based ARENA cluster. For the latter, we extend the Structural Simulation Toolkit (SST) [62] to model a multi-node cluster based on MPI. We model the network topology and package transmit switch in SST using the MACRELS Analytic Model [70]. The token transmit network is modeled as 1D Torus Ring. We implement the task dispatcher, CGRA, and CGRA controller in PyMTL [47], which can report cycle-accurate simulation results for a single node. To obtain the cycle-level simulation result, we implement the dispatcher interface in SST to handle the task...
tokens. Finally, we feed the single-node result to SST and generates synthesizable Verilog for power, area, and timing analysis. The detailed simulation parameters are listed in Table 2.

| Technology     | 45nm          |
|----------------|---------------|
| Network Interface | 80 Gb/s     |
| Network Topology  | 1D Torus Ring|
| Network Switch   | 1 per node, 1us hop latency |
| Dispatcher       | Filter logic, 8-entry receive queue, 8-entry wait queue, 8-entry send queue |
| CPU (baseline)   | 2.6GHz, 20MB 3-level Cache, Out-of-order, x86 |
| CGRA             | 8 × 8 CGRA, 480-byte control memory per tile, 2-bank 4-port 32KB scratchpad data memory, 4 × 4-entry queue for spawned task tokens, Coalescing unit |

TABLE 2: RTL and simulation parameters for ARENA.

Applications – We evaluate ARENA using representative HPC and data-analytics workloads: The single-source shortest paths (SSSP) problem (see Section 3.1) is a key subroutine in many data-intensive graph computations. General Matrix Multiply (GEMM) is the core function of linear algebra and deep learning workloads. We assume the matrices are distributed among nodes. Sparse-matrix-vector multiplication (SPMV) is the fundamental kernel in many scientific & data applications. Here, the distributed matrix is in the Compressed Sparse Row (CSR) format. DNA sequence alignment (DNA) leverages Needleman-Wunsch (NW) algorithm to search the best-matched protein sequences with respect to the target pattern. A Graph convolutional network GCN inference application on the Cora dataset is also evaluated, representing emerging irregular machine learning workloads. We assume the adjacency and feature matrices are distributed among nodes. Finally, an N-body simulation application for simulating dynamical particle system is demonstrated, representing traditional scientific simulation workloads. Again, the particle information (e.g., accelerations, velocity, position, collision, etc) are distributively stored and required to be updated per iteration at runtime.

The conventional compute-centric parallel implementations of all the evaluated applications are developed based on state-of-the-art algorithms or derived from the widely-used benchmark suites [22, 59]. For example, the SSSP application is implemented based on [21]. The GCN model is extracted from PyTorch Geometric [28]. The DNA application leverages the NW algorithm from Rodinia [22]. Regarding the ARENA implementation, all the applications are programmed following the ARENA programming models for data-centric asynchronous execution with runtime hardware specialization. Note that GCN and NBody contain numeric distinct functional tasks.

5.2 Evaluation Results

We show the benefits of the data-centric programming model, CGRA hardware acceleration, and the entire ARENA system.

Programming Model – We first show the performance effectiveness of ARENA’s data-centric programming model. Figure 9 illustrates the normalized speedups for conventional compute-centric and ARENA’s models (Both are software implemented based on MPI) with respect to a serial implementation on a single CPU node (i.e., baseline). As can be seen, ARENA’s data-centric execution model shows higher speedups and better scalability in general. This is mainly due to the elimination of synchronization, and the minimization of data communication. On average, ARENA’s data-centric model outperforms the compute-centric counterpart by 1.61× (i.e., 7.82/4.87) in a 16-node cluster. Specifically, the kernels with higher data parallelism (e.g., SSSP, GEMM, and SPMV) can gain better scalability for both models; for kernels with limited data parallelism such as DNA, the compute-centric model exhibits lower scalability due to massive data dependency and costly remote communication. In this condition, ARENA achieves better scalability by streaming task tokens over the nodes to minimize data movement.

Figure 10 illustrates the normalized data movement breakdown for ARENA’s data-centric model with respect to the compute-centric model for all applications in a 4-node cluster. Compared with the compute-centric HPC cluster, ARENA can eliminate on average 53.9% data movement without any prior knowledge about the data distribution, leading to substantial improvement in energy efficiency. We also observe different data movement patterns across applications. For example, SSSP posts considerable task movement, as it spawns massive fine-grained tasks with discrete data ranges, which are hard to coalesce. Regarding DNA, the compute-centric implementation is based on OpenMP where all threads are sharing the same copy in global memory [22]. The sub-blocks workload distribution to threads following a zig-zag manner incurs frequent data movement. In ARENA, the data dependency only exits on the edge of the sub-block, which can be explicitly labeled by the parent tasks using the ARENA User-APIs (i.e., \texttt{REMOTE}_{E_{start}} and \texttt{REMOTE}_{E_{end}} in ARENA_task_spawn()), therefore minimizing data movement. Finally, GEMM and NBody comprise coarse-grained tasks and the task-flows require data streaming among the nodes, leading to little task movement or essential data movement as shown in the figure.

CGRA Speedup – Figure 12 shows the normalized speedup of the evaluated applications running on different configurations or combinations of ARENA’s CGRA tile groups (each group is a 2x8 CGRA) with respect to the single node CPU baseline. In general, a larger CGRA tile configuration leads to higher speedups. For DNA, however, the loop-carried data dependency limits the data parallelism, as well as the obtainable speedups (1.7× speedup at most). On average, 1.3×, 2.4×, and 3.5× speedups are achieved by ARENA’s 2x8, 4x8, and 8x8 CGRA across all the applications and kernels. The 2x8 CGRA exhibits the optimal area-efficiency, showcasing the advantages of runtime hardware specialization.

Overall System – The normalized speedup of ARENA is shown in Figure 11. As can be seen, ARENA maximizes the overall performance by leveraging a data-centric execution model and CGRA in a synergistic and integrated fashion. Instead of fixing the CGRA configuration for each workload, ARENA dynamically allocates and configures the CGRA tiles specifically for a particular task based on the task-carried specification (obtained based on data requirement of the task), as well as the current CGRA resource availability. On average, the compute-centric execution model using the entire CGRAs for each kernel obtains 10.06× speedup on a 16-node cluster, whereas ARENA achieves 21.29× speedup. In other words, ARENA is 2.17× better than the compute-centric with CGRA.
Fig. 9: Normalized speedup for compute-centric and ARENA's data-centric execution models running on different multi-CPU clusters w.r.t. a serial implementation on a single node.

Fig. 10: Normalized data movement breakdown in data-centric model w.r.t. the compute-centric model.

support. This implies ARENA can leverage the CGRAs in a more efficient way. Compared with Figure 9, we can see that ARENA with CGRAs also gains better scalability (from 1.61 × to 2.17 × on a 16-node cluster). The performance of DNA does not improve much due to limited acceleration from CGRA. Finally, the compute-centric execution of GEMM does not scale well because synchronization over a larger amount of data creates serious performance bottlenecks.

5.3 RTL Timing, Area and Power

We evaluate the timing, area, and power consumption of ARENA's CGRA-cluster (e.g., CGRAs, CGRA controllers and task dispatchers) using the synthesized Verilog HDL code from PyMTL. We use Synopsys Design Compiler, Cadence Innovus, and Synopsys PrimeTime PX in order to synthesize, place, route, and estimate the power consumption of the designs. We use FreePDK45 with the Nangate standard cell library. Figure 13 illustrates the obtained chip layout. The area and power of the 32KB scratchpad data memory are estimated based on CACTI-6.5. The chip area is 2.19mm x 1.24mm and the operating frequency is 800MHz @ 45nm with an average 759.8mW power consumption.

6 RELATED WORK

We summarize related work regarding the ring network, clusters of reconfigurable architecture, and the task-based execution model in a ring network.

Ring Network. The ring network has been adopted in real multi-processors design [11] (e.g., Intel Xeon-Phi [23]) and logically studied for efficient collective communication [8], [10], [44], [45], [46], [72]. On the one hand, the ring network provides simple routing mechanism to better-utilize the link bandwidth for fast communication [11]. On the other hand, the ring network has been criticized for easy saturation due to linear increased latency with more node [7], [35], [46]. Previous works [8], [45], [46], [72] extend the ring concept to form local-rings network among a subset of nodes, known as routerless network. In ARENA, we avoid the saturation problem through: (a) a routerless task execution model among nodes; and (b) the dynamically task allocation and dispatching mechanism.

Reconfigurable Hardware Cluster. Clusters incorporating reconfigurable devices such as FPGAs [26], [41], [61], [65] and CGRAs [36], [60], [66] have already been showcased by existing works [48], [67]. On one hand, Putnam et al. from Microsoft propose the reconfigurable Catapult fabric [61], where each instantiation consists of a 6x8 2D torus of Xilinx Stratix-V FPGAs. Every FPGA is connected to a CPU server via PCI-e and directly links to other FPGAs through the SAS cables. This 1632-node FPGA cluster has been adopted for document ranking of the Bing search engine. Nearly 95% performance increase has been demonstrated with only a 10% extra power budget. However, each FPGA in Catapult is specialized to a single application kernel during runtime. Reconfiguration takes several milliseconds. Even reloading models without changing the computation logic can take up to 250 microseconds. On the other hand, the data-centric execution model allowing different tasks working on the same set of data in an HPC node requires rapid dynamic reconfiguration. Gazzano et al. propose R-Grid, a complete grid infrastructure for distributed high-performance computing using dynamically reconfigurable FPGAs [26]. Knodel et al. virtualize the FPGA resources and propose adapted service models in a cloud context [41]. Tafard et al. discussed how FPGAs of a cloud data center can be flexibly connected based on a logical kernel and a mapping file [65]. Zhang et al. adopt a cluster of six Xilinx VC709 FPGA for cooperative convolutional neural network inference [75]. Regarding to the CGRAs, the SambaNova DataScale system incorporates 8 reconfigurable-dataflow-units (RDUs) derived from Plasticine [60], claiming higher performance than a thousand GPUs for training extremely large deep-learning models. PPA [57] exploits pipeline parallelism in streaming applications to create a CGRA-like pipeline to execute streaming media applications. Samsung proposes to adopt the CGRA cluster for medical volume image rendering [36]. HammerBlade [66] aims at designing a rack-scale cluster for ML and Graphs. Their ASIC is composed of general-purpose cores and specialized CGRAs (e.g., Chimera [74]).

Asynchronous Task Execution. The asynchronous tasks...
 execution has been studied in many graph processing frameworks [13], [52], [53]. They propose software-level data-centric approaches to implement irregular graph kernels on multi-node clusters [52] and GPUs platform [52]. The work that is most relevant to ARENA is Groute [13], which is an asynchronous runtime environment for processing irregular graphs. In Groute, the GPUs form a logical ring network with each GPU conserves a worklist. Tasks are encapsulated as messages passing along the ring. ARENA is motivated by Groute. However, Groute is a pure software implementation based on general-purpose GPUs, thus cannot benefit from hardware specialization. Additionally, for Groute, the routing policy, which specifies the action when input is received, as well as memory consistency and ownership, are all defined and maintained by the users, which can be complicated, tedious and error-prone (e.g., imagine if data dependency occurs at runtime, users have to manually locate them and fetch in corresponding tasks). In ARENA, these are designed and supported by hardware. Furthermore, global coordination and work counting in Groute are centralized and managed by the CPU whereas in ARENA, all of them are distributedly processed.

7 CONCLUSION

In this paper, we propose an asynchronous-reconfigurable-accelerator-ring architecture for next generation data-driven high-performance computing. Through the co-design of architecture and programming model, ARENA is able to bring computation tasks in the form of CGRA-specialized hardware accelerators to the data, rather than the reverse as in contemporary compute-centric and dataflow architectures, significantly improving performance and reducing data movement.

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