Practical design and simulation of silicon-based quantum dot qubits

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Spins based in silicon provide one of the most promising architectures for quantum computing. A scalable design for silicon-germanium quantum dot qubits is presented. The design incorporates vertical and lateral tunneling. Simulations of a four-qubit array suggest that the design will enable single electron occupation of each dot of a many-dot array. Performing two-qubit operations has a negligible effect on other qubits in the array. Simulation results are used to translate error correction requirements into specifications for gate-voltage control electronics. This translation is a necessary link between error correction theory and device physics.

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Quantum computation would enable huge speedups of certain very hard problems, such as factorization. However, quantum computing is essentially an analog method. As such, the problem of errors creates a serious challenge. Advances in error correction algorithms have produced well-justified optimism that this challenge will be overcome. However, existing error correction algorithms require low error rates. Thus, hardware design will be critical to the creation of a working quantum computer.

The purpose of this paper is to address hardware design challenges in a specific materials system: silicon quantum dots. There are two reasons to analyze this system in detail. First, spins in silicon have long coherence times. Second, classical silicon electronics has demonstrated fast operation and a proven record of scalable integration. Indeed, several spin-based qubit designs have emerged that are compatible with silicon. The full benefit of existing silicon technology may be used to greatest advantage in spin qubits based in quantum dots. Previous calculations of the exchange coupling in coupled quantum dots with idealized potentials have demonstrated the promise of such structures for quantum computation. However, there are important questions that can only be addressed in the context of an explicit physical design and realistic simulations.

In this paper, we present an explicit design for quantum dot qubits in silicon-germanium heterostructures. To determine whether it will be possible to build and operate such a device, we perform realistic simulations of four coupled qubits. The simulations are self-consistent: they include the full three-dimensional electrostatics, and the Hamiltonian is solved via exact diagonalization. These simulations allow us to answer several questions. First, we find that it is possible to couple neighboring quantum dot qubits without any significant perturbation of secondary qubits. Second, the coupling can be strong, enabling GHz operation rates. Most importantly, these simulations allow us to translate gate volt-
Qubits are useful only if operations can be performed on them. For the structure we describe here, the operations are performed by controlling the exchange coupling on them. For the structure we describe here, the operation greater than 1 meV throughout the operating range for the four-qubit device of Fig. 1(b), and we find stabilizations, because of the large difference in energy scales: $J/E_{\text{trip}} < 5 \times 10^{-4}$.

Figure 3 shows a map of the exchange coupling $J$ as a function of gate voltages $V_{\text{in}}$ and $V_{\text{out}}$, computed numerically for the double-dot device of Fig 1(a). The back-gate is grounded. The envelope function approximation used here is reasonable for quantum dots of size $\sim 50 \text{ nm}$. The overall trends in Fig. 3 are consistent with previous studies, which use more idealized confinement potentials. However, because the magnetic field is zero in this work, the exchange coupling does not cross zero, in contrast with results for high magnetic fields. Nonetheless, $J$ can be made arbitrarily small by raising the electrostatic barrier between the qubits. Raising such a barrier creates an asymptotic approach to zero that is extremely robust.

The data in Figures 2 and 3 are for two qubits. It is conceivable that adding additional qubits would cause at least one qubit to become unstable or suffer an undesired coupling with a neighboring qubit during the manipulations described by Fig. 3. Fortunately, this is not the case. Fig. 4 shows the electron density in a four-qubit device for two extreme cases, in which the exchange coupling is either (a) very small or (b) very large. Between Fig. 4(a) and (b), the inner pair of electrons each move by 21.5 nm, whereas the outer electrons move by only 0.5 nm. This motion corresponds to a change in $J$ for the inner pair from approximately $10^{-19} \text{ eV}$ to $0.4 \mu\text{eV}$. We can estimate the $J$ coupling between the fourth and “fifth” electrons in Fig. 4 (using periodic boundary conditions). We obtain approximately $10^{-19} \text{ eV}$ for Fig. 4(a), and this number decreases by only a factor of 0.8 in Fig. 4(b).
Thus, any pair of qubits can be manipulated independently of any other pair. This independence is due, in part, to screening effects arising from the various gates.

The results of Fig. 3 allow us to consider errors in quantum gates. It is important to remember that errors arise in quantum computing not just from decoherence but also from the inevitable misapplication of quantum gates. Such misapplications will arise, for example, from uncertainties in the applied gate voltages. Fault-tolerant techniques have been developed for correcting errors, but these are only effective below an error threshold of one accumulated error in $10^4$ operations. Thus, it is critical to know the error rate expected during the application of quantum gates.

Here we calculate the error rate in $J$ as a function of the uncertainty or noise in the voltage pulses used to manipulate the quantum dots. Accurate gate control involves two steps: (i) initial characterization of the exchange coupling between pairs of qubits, and (ii) precise implementation of the gate operations. For this discussion, we assume perfect characterization, and we focus on step (ii). As a prototype for gate operations we consider $\sqrt{\text{SWAP}}$, as implemented with a voltage pulse $V_s(t)$. In principle, the particular shape of $V_s(t)$ is arbitrary, although it must satisfy the following relation:

$$\int_{\tau_s} J[V_s(t)] dt = \pi \hbar / 2. \quad (1)$$

Here, $\tau_s$ is the switching time, and the function $J(V)$ was computed in Fig. 3. To be specific, we consider low and flat voltage pulses, such that errors in the pulse width are diluted to acceptable levels.$^{18}$

What are the error levels that can be tolerated in the applied gate voltages? For a flattop pulse of height $J = \pi \hbar / 2 \tau_s$, fault tolerant computation requires that the pulse height uncertainty $\delta V$ should satisfy

$$\delta V < 10^{-4} J \left| \frac{\partial J}{\partial V} \right|^{-1}. \quad (2)$$

It is important to note that the magnitude of $\delta V$ depends on classical control electronics, while $J$ and $\partial J/\partial V$ are implementation-specific. To evaluate gating errors, it is therefore necessary to work with a realistic device design. By fitting the exponential dependence of $J(V)$ in Fig. 3, Eq. (2) yields the requirement $\delta V / V < 5 - 8 \times 10^{-6}$ for the double qubit device of Fig. 1(a). We can compare this figure to published specifications for state-of-the-art control electronics. For sub-kHz pulses (approaching DC), extremely high voltage accuracy can be achieved, and the requirement can be met. For sub-MHz pulse generators, the desired accuracy levels fall nearly within the specifications of off-the-shelf electronics.$^{19}$ For GHz operation, over three orders of magnitude improvement in pulse height uncertainties will be required to meet the requirements of fault tolerant computation.$^{20}$ We point out that decoherence constraints may indeed require spin-based silicon qubits to operate in the GHz regime.

In conclusion, we have described and simulated a realizable design for a SiGe quantum dot quantum computer. A prominent feature of this device is the backgate, which enables tuning of the number of electrons in each quantum dot. We have directly addressed the issue of scalability through simulations of a four-qubit device. Qubit interactions are found to be very robust, particularly as a consequence of Coulomb screening provided by the back-gate. Our calculations show that a key challenge for solid-state spin-based quantum computation is to develop devices in which the exchange coupling is relatively insensitive to gate voltage uncertainty. At a simple level, the quantum dot structures should be optimized to increase $J/|\partial J/\partial V|$, which sets the scale for gate voltage accuracy requirements. The ultimate goal should be to “digitize” the gating function $J(V)$, such that $\partial J/\partial V$ goes to zero at appropriate working points.$^{21}$

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Due to strain effects, the six-fold degeneracy of the silicon conduction band in the quantum well is lifted, so that only the [001] bands are populated. The envelope function approximation can be used to describe lateral variations of the wave function when the confinement potential varies slowly with respect to atomic distances, for quantum dots of size \( \sim 50 \) nm, the approximation should be reasonable. In the vertical direction, however, the band edge has sharp discontinuities at the quantum well interfaces. For this case, an extension of Ref. \[25\] to quantum wells shows that the envelope function approximation remains accurate, although the fine structure of the wavefunction (i.e., the Bloch function) should be modified to accommodate intervalley scattering. Symmetry allows two possible valley-coupled wavefunctions: \( \Psi_{z} = F_{z}(\phi_{z} \pm \phi_{-z}) \), where \( \phi_{z} \) and \( \phi_{-z} \) are the appropriately modified Bloch functions at the [001] and [001] band minima. The envelope functions in these two directions are equal, \( F_{z} \equiv F_{\pm} \). Perturbation theory gives the energy splitting for the two eigenstates \( \Psi_{z} \), although a complete treatment of the interface physics is still lacking. Using the estimate given in Ref. \[25\] \((\alpha \approx 0.5 \) Å\) we predict a valley splitting of \( \Delta E > 0.06 \) meV \((0.7 \) K\) for our heterostructure—more than 10 times our dilution fridge temperature. By optimizing the heterostructure to increase the electric field in the quantum well, it is possible to increase \( \Delta E \) significantly. At low temperatures then, all electrons should be in the valley-split ground state, with no interference effects of the type discussed in Ref. \[25\].

\[ \text{The } 10^4 \text{ estimate assumes two-qubit operations between any pair of qubits. In a linear qubit array with only nearest neighbor couplings, a more restrictive threshold may be appropriate.} \]

\[ \text{Using the estimate } T_2 > T_2^2 \approx 0.5 \text{ ms for bulk silicon, the fault-tolerant error threshold suggests a maximum pulse length of } 0.1 \mu \text{s. For a flat-top pulse of width } 0.1 \mu \text{s, we estimate a minimum pulse edge of } 10 \text{ ps to satisfy adiabatic gating requirements. Such a pulse must be produced with less than } 10^{-4} \text{ relative error in its duration. Such accuracy is currently beyond the limits of commercial pulse generation technology.} \]

\[ \text{Estimates are based on specifications for pulse amplitude jitter in PB-4 and PB-5 sub-MHz pulse generators from Berkeley Nucleonics Corporation (http://www.berkeleynucleonics.com).} \]

\[ \text{Specifications from the Agilent Technologies 8133 and 81100 families of GHz pulse generators are listed as } \delta V/V < 0.01 \text{ (http://www.agilent.com).} \]

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