Abstract
A small-signal equivalent circuit for graphene field-effect transistors is proposed considering the explicit contribution of effects at the metal-graphene interfaces by means of contact resistances. A methodology to separate the contact resistances from extrinsic parameters, obtained by a de-embedding process, and intrinsic parameters of the circuit is considered. The experimental high-frequency performance of two different GFET technologies is properly described by the proposed small-signal circuit. The correct detachment of contact resistances from the internal transistor enables to study their impact on the intrinsic cutoff frequency of the devices under study.

Index Terms
GFET, small-signal circuit, contact resistance, high-frequency.

I. INTRODUCTION
Small-signal characterization of graphene field-effect transistors (GFETs) has enabled the demonstration and immediate parametric assessment at high-frequency (HF) of this emerging technology [1]-[8]. One of the key device parameters to be considered in GFETs is the contact resistance $R_c$ related to bias-dependent potential barriers at the metal-graphene (MG) interfaces and additional interface layers [9]-[12], i.e., $R_c$ is the series combination of a bias-dependent resistance and a bias-independent resistance. The separation of these effects is not trivial [11]. In general, values of $R_c$ can be obtained either by test structure characterization [1], [2], [7], by analytical models [6], by S-parameters measurements [3], [4], [8], by I-V-based extraction methods [12] or by a fitting process [5]. Regardless of the method to obtain it, in small-signal equivalent circuits (ECs) of GFETs, the extracted $R_c$ has been usually either considered in the extrinsic part of the model only [1], [3], [5] or included in the intrinsic circuit [2], [4], [7]. It must be noticed that standard de-embedding procedures with test dummy patterns can not subtract the total effect of $R_c$ from the intrinsic device. Hence, either intrinsic or extrinsic circuit elements compensate the impact of $R_c$ by overestimating or underestimating other parameters, respectively, depending on where $R_c$ has been considered in the small-signal model.

The contribution from the source contact resistance $R_{sc}$ and drain contact resistance $R_{dc}$ has been generally embraced by $R_c$ in a symmetrical manner, i.e., $R_{sc} = R_{dc} = R_c/2$ [1], [4], [6]. This symmetrical distribution of effects is a good initial approximation but the real conditions can differ since the potential barrier at each MG interface, represented by $R_{sc/dc}$, can vary depending on the operating bias point.

In contrast to other approaches where $R_c$ is lumped either in the extrinsic [1], [3], [5] or intrinsic [2], [4], [7] part of the EC, in this work a straightforward method considering asymmetric contact resistances in the EC separated from the intrinsic and extrinsic networks has been presented. The proposed approach has been validated with experimental data from two GFET technologies.

II. EQUIVALENT CIRCUIT AND PARAMETER EXTRACTION
The small-signal EC considered in this work is shown in Fig. 1. Non-negligible device contact resistances have been considered in this EC. This approach has been useful as well for small-signal EC describing the HF performance of other emerging transistors [13] and it has been followed for the first time in GFETs here. The intrinsic elements are between the $g_s$, $s_x$, and $d_i$ nodes. Source and drain contact resistances including the contribution of a potential barrier at the MG interfaces are between $s_x$ and $s_x$ nodes and $d_i$ and $d_x$ nodes, respectively. Extrinsic parasitic elements are between $g_{sc}$, $s_x$ and $d_x$ and the access points of the device G, S and D, respectively. Conventional de-embedding techniques do not eliminate the impact of contact resistances on the intrinsic parameters. This effect should be removed in order to obtain an accurate description of the intrinsic device.

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The parasitic effects of the metallic access lines and pads are represented by the gate/source/drain parasitic inductance \( L_{gs/sa/da} \), the gate/source/drain parasitic resistance \( R_{gs/sa/da} \) and the gate-to-source/gate-to-drain/drain-to-source parasitic capacitances \( C_{gsx/gdsx/dsx} \). The intrinsic transistor consists of the gate-to-source/gate-to-drain/drain-to-source capacitances \( C_{gs/gd/ds} \), the intrinsic output resistance \( 1/g_{ds} \) and the voltage-controlled current defined by the intrinsic transconductance \( g_m \) and the intrinsic gate-to-source voltage \( V_{gs} \). In the context of graphene devices in general, the contact resistances \( R_{sc/dc} \) embrace both external and internal device phenomena \([9]-[12]\) and their impact on the intrinsic device performance can not be separated by standard de-embedding procedures. The extraction of the small-signal parameters used here has been introduced elsewhere \([13]\) for a different low-dimensional transistor technology. This methodology is applied in this work to two GFET technologies and it is summarized as follows.

Extrinsic outer-parasitic capacitances \( (C_{gsp1/gsp2/dsp1}) \) can be obtained from the admittance matrix \( Y_{open} \), associated to the HF characterization of an open dummy structure using the same architecture and materials as the active device. Similarly, the extrinsic parasitic inductances \( (L_{gs/sa/da}) \) and parasitic resistances \( (R_{gs/sa/da}) \) are calculated from the HF impedance matrix \( Z_{short} \), of short dummy structures. The HF characterization of a pad dummy structure yields an admittance matrix \( Y_{pad} \) from which the inner-parasitic capacitances \( (C_{gsp2/gsp2/dsp2}) \) are obtained. The de-embedded admittance matrix \( Y_{dem} \), including the impact of \( R_c \), is related to the raw extrinsic admittance matrix \( Y_{raw} \) by using \( Y_{open}, Z_{short} \) and \( Y_{pad} \) in a three-step parasitic de-embedding method \([13], [14]\).

In order to characterize correctly the intrinsic GFET, the contribution of the contact resistances should be removed from \( Y_{dem} \) since their impact has not been eliminated by the de-embedding methodology: the dummy structures do not include the potential barriers at the MG interfaces. This non-trivial approach is performed here, under the condition of linear matrices, by following the matrix algebra explained in \([13]\) after identifying the corresponding blocks and connection topologies of the intrinsic transistor and contact resistances as shown in Fig. 2. This procedure is summarized as follows: the impedance matrix of the intrinsic transistor including only the contribution of the drain contact resistance \( Z_{r,Rdc} \), obtained by removing the impedance matrix of \( R_{sc} \) from \( Z_{dem} \), has been transformed into its \( ABCD \)-representation in order to obtain the intrinsic device matrix by multiplying it by the inverse \( ABCD \)-matrix of the remaining contact resistance, i.e., \( ABCD_{Rsc}^{-1} \). The intrinsic \( ABCD \)-matrix is then transformed into the intrinsic admittance matrix \( Y_1 \).

The intrinsic admittance matrix, obtained after the removal of \( R_c \) from \( Y_{dem} \), enables the reliable calculation of each intrinsic element of the EC. An initial value for \( R_{sc/dc} \), required for this procedure, can be set by considering a symmetrical disposal of \( R_c \), the value of which can obtained by one of the methods listed in Section \([13]\). The asymmetric condition of \( R_c \) is achieved by an additional optimization step involving a correct description of experimental \( S \)-parameters.

1\( Y_{dem} \) represents the admittance parameters of a device without the contribution of elements outside the nodes \( g_s, d_s \) and \( s_s \) in the EC, i.e., without parasitic outer/inner capacitances, inductances and access resistances. \( Y_{dem} \) here is equivalent to \( Y_{INT} \) in \([14]\) if \( R_c = 0 \).
Two different top-gate bilayer graphene FETs fabricated on SiC substrates with gate lengths of 60 nm \[3\] and 80 nm \[7\] and gate widths \(w_{gs}\) of 2 × 8 μm and 2 × 15 μm, respectively, have been characterized using the small-signal model proposed here. Fabrication details of each device can be found in \[15\] for the shortest device \[3\] and in \[16\] for the largest one \[7\]. Table I lists the parameter values of the EC in Fig. 1 extracted here for each device as well as values reported in the corresponding references where different topologies and effects than the ones included here have been considered, e.g., the contribution of the MG-interface related effects have not been included explicitly in the ECs associated to \[3\] and \[7\] (see discussion below).

| Parameter          | Ref. \[3\] | This Work | Ref. \[7\] | This Work |
|--------------------|------------|-----------|------------|-----------|
| \(g_m\) (mS)       | 20         | 20.3      | -38        | -10.7     |
| \(g_{ds}\) (mS)    | 70         | 71.1      | 31         | 87.4      |
| \(C_{gd}\) (pF)    | 4          | 3.9       | 4.4        | 5.9       |
| \(C_{gs}\) (pF)    | 13         | 3.9       | 9.7        | 5.9       |
| Contact resistances| \(R_{sc}\) | 5          | 3.2        | -         | 5.5       |
| \(R_{dc}\) (Ω)     | 7          | 4.5       | -          | 16        |
| \(C_{gd1}\) (pF)   | 3          | 3         | 0.7        | 0.7       |
| \(C_{gd2}\) (pF)   | -          | 1.8       | -          | 0.5       |
| \(C_{gs1}\) (pF)   | 6          | 6         | 8.2        | 8.2       |
| \(C_{gs2}\) (pF)   | -          | 7.9       | -          | 17        |
| \(L_{ga}\) (pH)    | 12         | 12        | 7.8        | 7.8       |
| \(L_{as}\) (pH)    | 12         | 12        | 7.8        | 7.8       |
| \(L_{da}\) (pH)    | 30         | 30        | 40         | 40        |
| \(R_{sc}\) (Ω)     | 2          | 2         | -          | 57        |
| \(R_{dc}\) (Ω)     | -          | 1.8       | -          | 0         |
| \(R_{g}\) (Ω)      | -          | 2.6       | -          | 0         |

The reference \(R_c\) value of the 60 nm-long device \[3\], obtained via cold-FET measurements \[8\], has not been used here since it does not embrace the impact of lateral fields on the potential barrier at MG interfaces \[18\]. Instead, \(R_c\) value, obtained with TLM and corresponding to a \(R_c\cdot w_g\) of 123Ω·μm for such device \[3\]. The approach adopted in this work implies lower \(R_{sc}\) and \(R_{dc}\) than in the reference EC as well as the incorporation of access parasitic resistances. On the other hand, for the 80 nm-long device, the reference \(R_c\) value, obtained with the transfer length method (TLM), has not been explicitly included in the EC presented in \[7\] and hence, the impact of the MG interface effects on the device has been embraced by other internal parameters. In contrast, such \(R_c\) value, obtained with TLM and corresponding to a \(R_c\cdot w_g\) of 645Ω·μm, has been used here in the proposed EC. The explicit incorporation of \(R_c\) and its non-symmetrical distribution in our approach yields different values of some of the extracted small-signal elements in comparison to the reported ones in both reference works.

Intrinsic parameters of the EC in Fig. 1 have been calculated from \(Y\)-parameters (see Eqs. (5)-(9) in \[13\]) by using the \(R_e\) separation method (cf. Fig. 2) towards a correct description of the experimental de-embedded \(S\)-parameters by the intrinsic device and considering asymmetric contact resistances\[1\]. Available values of extrinsic parameters reported in the corresponding work (obtained by a de-embedding process discussed in Section II) have been used here while the remaining extrinsic parameter values have been obtained with a computer-aided least-square error-function \[17\] optimization towards a correct description of experimental raw \(S\)-parameters.

### III. VALIDATION WITH EXPERIMENTAL RESULTS

The small-signal equivalent model proposed here using the EC in Fig. 1 and the extracted values reported in Table I for both devices under study \[3\], \[7\] describes well the experimental \(S\)-parameters of each GFET as shown in Fig. 3. Similar results have been obtained for other GFET \[8\] (not shown here) using the proposed methodology.

The experimental extrinsic transit frequency \(f_{t,e}\) and extrinsic maximum oscillation frequency \(f_{\text{max.e}}\) reported in the corresponding references have been also described with the model proposed here as demonstrated in Fig. 4 where the small signal current gain \(h_{21}\) and the unilateral power gain \(U\) versus frequency have been shown for each device. The small-signal circuit proposed in \[3\], yielding a \(f_{t,e}\) and \(f_{\text{max.e}}\) of \(\sim 72\) GHz and \(\sim 110\) GHz, respectively, is not capable to reproduce the corresponding experimental figures of merit (FoM) of 70 GHz and 120 GHz, respectively. In contrast, the approach considered here, including a more precise extraction and distribution of \(R_c\), and hence a more accurate description of extrinsic and intrinsic networks, is a more efficient and reliable method to obtain an accurate HF modeling of such device as shown in Figs. 4a,c.

\(^2\)The starting values to obtain this asymmetric disposal of \(R_c\) are the ones obtained with an \(I-V\)-based extraction method for \[3\] and with TLM for \[7\] as discussed above.
Intrinsic FoM can be useful to indicate the HF material capabilities and performance projections for optimized technologies. In contrast to other studies where the impact of contact resistance effects from the intrinsic transistor and from the bias-independent de-embedded extrinsic elements. In dependent potential barriers associated to MG interfaces has been presented here. An extraction methodology enables to separate the contact resistance effects from the intrinsic transistor and from the bias-independent de-embedded extrinsic elements. In contrast to other works, this approach enables a more exact quantification of intrinsic and extrinsic parts of the equivalent circuit.

IV. CONCLUSION

A small-signal equivalent circuit for GFETs with contact resistances embracing the effect of material layers and the bias-dependent potential barriers associated to MG interfaces has been presented here. An extraction methodology enables to separate the contact resistance effects from the intrinsic transistor and from the bias-independent de-embedded extrinsic elements. In contrast to other works, this approach enables a more exact quantification of intrinsic and extrinsic parts of the equivalent circuit. The proposed model has been verified with experimental S-parameters and HF FoM of two different GFET technologies.

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