Performance analysis of Cu/CNT-based TSV: impact on crosstalk and power

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Abstract
This paper presents a new approach to implement a compact resistance–inductance–capacitance–conductance (RLCG) model for carbon nanotube (CNT) and Cu-based differently shaped through-silicon vias (TSVs) in 3-D ICs. The model primarily comprises the effect of bump, inter-metal dielectric, and eddy currents. Using the proposed model, a mathematical formulation for the coaxial-, cylindrical-, and tapered-based via parasitics is derived using the concept of partial inductance, sectioning the via laterally into infinitesimally thin slices and triangular inter-tube assemblage, respectively. The analytical model is validated against fabrication-based experimental results and subsequently employed for crosstalk-induced delay, peak noise, and power losses analysis. Additionally, for the further validation, the S parameter for the $Pi$-based model is derived, and compared with an electromagnetic simulator to benchmark the proposed model. The consistency between the analytical and EM simulation-based results further confirms the validity of the proposed model. A significant improvement in the power losses, crosstalk, and peak noise can be observed using the CNT-based tapered TSV compared to the Cu-based via structures. Additionally, it is shown that, irrespective of via height, the average crosstalk-induced delay, peak noise, signal transmission, and reflection loss of the TSV with tapered-shaped 15-shell CNT bundle are reduced by 22.82, 27.80, 47.63 and 33.71%, respectively, compared to the Cu.

Keywords Crosstalk-induced delay · Eddy effect · Single-walled carbon nanotube (CNT) · 3-D IC · Mean time to failure (MTTF) · Resistance–inductance–capacitance–conductance (RLCG) model · Through-silicon via (TSV)

1 Introduction

Three-dimensional (3D) ICs provide a promising alternative to yield reduced area, improved performance, and higher bandwidth system on chip (SoC) by vertically stacking multiple dies [1]. Through-silicon via (TSV) is primarily preferred to establish a vertical interconnection between the dies fascinating excessive concern due to their decent competencies to offer a large number of I/Os, high density, and low-cost heterogeneous integration [2, 3]. In order to fulfill the aforementioned requirements, researchers primarily used Cu as a potential filler material during the via-last fabrication process [4]. However, at deep submicron regime, Cu confronts major limitations of the surface and grain boundary scatterings due to a smaller mean free path (mfp) in the range of 40 nm [5]. Therefore, a single- and multi-walled carbon nanotube bundle (SWB and MWB) has been emerged as a potential filler material due to its low resistivity and a larger mfp of several micrometers [6]. Using the Cu and CNT bundle-based TSVs, several researchers [7] have investigated cylindrical-shaped vias due to their uniform structure, high breakdown voltage, and design simplicity. However, compared to the cylindrical-shaped TSVs, a coaxial via provides a unique structure to mitigate the substrate noise due to the presence of a guard ring [8]. Nevertheless, the production of these coaxial-shaped TSVs is immensely complex and expensive as the Cu and the oxide layer have to be deposited twice to form the guard ring. Furthermore, compared to the cylindrical and coaxial via, the metal and oxide deposition in the case of a tapered-shaped
TSV primarily requires less time due to its reduced cross-sectional area. Additionally, few other benefits such as less reflection noise and signal loss, less space, and straightforward fabrication process associated with the tapering shape recently draw a wide attention of the research community toward the modeling of tapered-based TSVs [9].

Earlier, Liu et al. [10] implemented a Cu-based cylindrical TSV using an accurate physical parameters of filler material surrounded by an oxide layer, depletion layer, and the silicon substrate. Herein, resistance and inductance of Cu-based cylindrical TSVs were calculated by considering the MOS effect using a Fourier–Bessel expansion method. However, the model did not consider the overall capacitive impact of the isolation layer. Meanwhile, different via structures such as cylindrical, tapered, and coaxial were analyzed for insertion and reflection losses by considering the aforementioned capacitive effect. However, parasitic modeling of different via shapes was ignored [11]. Later, Xu et al. [12] demonstrated parasitic modeling in terms of a closed-form expression by considering a coaxial-shaped TSV. The authors converted an EM solved scattering (S) matrix to the transmission (ABCD) matrix while neglecting the adverse effect of capacitive/inductive coupling. In order to mitigate these coupling capacitance issues in coaxial TSVs, the researchers in [13] and [14] proposed the parasitic modeling of a tapered structure using conical modal basis functions and numerical moment method. Herein, the analysis was carried out by considering the potential of a circular-striped TSV, extracting the Green’s function, meshing and obtaining the parasitics for the different shapes. However, the analysis carried in [13] and [14] restricted their research related to the Cu-based conventional filler material without considering the effect of emerging material. Later, Zhao et al. [15] proposed CNT-based cylindrical TSV modeling by using the concept of Poisson’s equation in cylindrical coordinate and complex conductivity. Herein by virtue of effective complex conductivity, the CNT kinetic inductance is evaluated. However, the researchers in [15] used a cylindrical-shaped CNT-based TSV that possesses less conductivity due to its uniform structure and an increase in the via capacitance. Therefore, in recent, Hu et al. [16] consider the electrical modeling of coaxial-type guarded CNT-based TSV for an improved conductivity. In order to obtain the TSV impedance, a RLGC model is proposed using the concept of partial element equivalent circuit. The analysis carried in [16] has used coaxial via comprising of CNT-based vertically aligned TSV and Cu guard ring that can create a serious electromigration and coupling capacitance issues. In order to mitigate issues associated with CNT-based coaxial via, Rao et al. [17] considered tapered-shaped via bundle. The analysis carried in [17] examined electrical and bidirectional vertical signal delay characteristics by using the Elmore RC method. However, the model did not consider all the parasitic components of the TSV, such as the via coupling capacitance in the inter-metal dielectric (C_{IMD}) layer and between the bumps (C_{bump}). Therefore, an extensive analysis and a novel modeling are required for a CNT-based optimal TSV shape by incorporating all significant via parasitics.

This paper analyzes for the first time a closed-form expression of the parasitics and its RLGC model of Cu-, SWB-, and MWB-based different TSV shapes by considering the effect of bump and inter-metal dielectric (IMD) layer. These closed-form expressions of the Cu-based via model primarily consider the eddy effect occurred due to the Faraday’s law of induction. As per the law, the magnitude of induced electromotive force (EMF) generates a circulating eddy current into the silicon substrate. Herein, considering the impact of eddy current, the closed-form expressions of bump, via, IMD inductance, resistance, and capacitance are derived using the concept of partial inductance, slicing TSV with numerous pieces, and the Taylor series expansion of the infinite differential parallel capacitance, respectively.

Furthermore, the number of CNTs for the different shapes of the bundle can be obtained using the concept of triangular inter-tube arrangement. Additionally, using an accurate Pi-type transmission line model, the closed-form expression has been derived for the S11 and S21 power losses. The primary reason behind using a Pi-type network is that the shunt compensation for reactive power and power factor correction is easy to accomplish. The S parameters obtained using the Pi-based transmission line model are validated against the structural EM simulations for different TSV shapes. In order to further validation, the via parasitics are compared with a fabricated test model of a cylindrical-shaped TSV up to 40 GHz of the operating frequency. A CMOS driver is employed to investigate and compare the crosstalk-induced delay, peak noise, and power losses of the Cu-, SWB-, and MWB-based Pi-type TSV network. The analysis has been performed by considering an accurate physical dimensions of TSV at 22 nm technology due to its higher device density, reduce operating voltage, and drive down power consumption [18].

The paper is organized in the following sections: Sect. 1 outlines the current research review and provides brief summaries of the work. Section 2 presents the physical structure of different TSVs and bumps, its RLGC model using Cu, and bundled CNT under the consideration of eddy effect. Additionally, an analytical model expression is established for the Cu- and CNT-based cylindrical, coaxial, and tapered TSVs in the aforementioned section. Furthermore, Sect. 3 demonstrates a comparative analysis of Cu and bundled CNT-based TSVs for different via shapes. Finally, Sect. 4 summarizes a brief conclusion.
2 TSV and bump structure

This section presents an equivalent electrical model of different TSV configurations and their physical parameters incorporating Cu, SWB, and MWB as filler materials. The closed-form expressions are obtained for both AC and DC resistances, inductances, and capacitances by considering semi-analytic and analytic expressions of the via parasitic. Consequently, a novel equivalent electrical modeling of different shapes of TSV is proposed under the consideration of the eddy resistance, IMD, and microbump. In order to examine the accuracy, the model parasitics are validated against experimental measurements and fabricated test samples as presented in the following subsection.

2.1 Physical configuration of bump

The cross-sectional view of the parallel via with two bumps and IMD lines present at the top dies is illustrated in Fig. 1a. The microbumps, separated by an underfill layer, are primarily placed between the vias that connect the stacked dies. The IMD layer is used to provide an isolation between the bumps and the lossy silicon substrate. The physical model of the bumps associated with IMD layer (shown in Fig. 1a) is primarily designed at 22 nm technology. For the proposed tapered-shaped microbump, the geometrical parameters $P_{\text{via}}$, $h_{\text{bump}}$, $\theta_{\text{bump}}$, and $h_{\text{IMD}}$ represent the center-to-center distance between the via, height of the bump, tapering angle, and the IMD layer height, respectively. Furthermore, Fig. 1b delineates the analytical model of tapered bump that demonstrates the framework of computing the bump parasitic values. The $r_{a_{\text{bump}}}$ and $r_{b_{\text{bump}}}$ in Fig. 1b represent the lower and upper radii of the bump, respectively. The vertical position $x$ in infinitesimally thin sliced bump utilizes the geometric parameters that can provide an approximate evaluation of the parasitic. Thus, the location of point $x$ in relation with bump height ($h_{\text{bump}}$) and radius ($r_{b_{\text{via}}}$) can be represented as

$$x = h_{\text{bump}} - \tan\theta_{\text{bump}} \times r_{b_{\text{bump}}}$$

However, the closer proximity of IMD and microbump creates mass transport of electron when stressed by high current and thereby the electromigration failure. The electromigration-induced mean time to failure (MTTF) is a critical parameter for estimating the life span of the bump. The current analysis is used to build the distribution map as the EM life span of bump is dependent on the current density. Additionally, researchers have discovered other EM driving mechanisms, such as thermal gradients. A comprehensive EM life span computation considering these current density and thermal gradients parameters necessitates modeling of the gradual failure in a microbump. As a result, this work exclusively employs the Black’s equation to estimate the MTTF while focusing on the impact of current distribution and thermal gradients on the EM life span. Therefore, in order to identify the appropriate bump shape in terms of MTTF analysis, a black equation is required.

$$\text{MTTF} = A \frac{1}{j^2} \exp \left( \frac{E_a}{KT} \right)$$

where current density $(j)$ and temperature $(T)$ in the aforementioned equation can be obtained using the structural analysis of the bump and the other parameters, i.e., Boltzmann’s constant $(K)$, activation energy $(E_a)$, and proportionality constant $(A)$ can be described in [19].

A comprehensive analysis of MTTFs for the spherical-, cylindrical-, and tapered-shaped bumps is summarized in Table 1. It is observed that the overall improvement of MTTF of the tapered bump is 3.21% compared to the cylindrical and spherical, respectively. The MTTF is primarily improved due to the reduced effect of lower solder volume

| Bump radius (µm) | Spherical bump  | Cylindrical bump | Tapered bump |
|------------------|-----------------|------------------|--------------|
|                  | Temp (°C) | MTTF (h) | Temp (°C) | MTTF (h) | Temp. (°C) | MTTF (h) |
| 2.5              | 294.25  | 75.17    | 295.35  | 72.83    | 293.35  | 77.15    |
| 3.0              | 296.45  | 70.57    | 297.45  | 68.58    | 295.75  | 72.00    |
| 3.5              | 297.75  | 68.00    | 299.05  | 65.53    | 297.65  | 68.19    |
| 4.0              | 299.65  | 64.43    | 301.05  | 61.93    | 299.15  | 65.35    |
that can provide less joule heating and better reliability. Therefore, a tapered-shaped bump can be preferred for modeling of the TSVs in terms of the improved MTTF.

### 2.2 Physical configuration of TSV

This subsection demonstrates a thorough insight of the TSV configuration and quantitative values of TSV parameters that will eventually be used in the electrical modeling of the different via configurations. The top and perspective view of a cylindrical, coaxial, and tapered TSVs is illustrated in Fig. 2a, b and c, respectively, and the via physical parameters are summarized in Table 2. Figure 2b shows the physical configuration of tapered TSV, where \( r_{a,\text{via}} \) and \( r_{b,\text{via}} \) are the lower and upper radii, respectively; \( h_{\text{via}} \) is the height; and \( \theta_{\text{via}} \) is the tapering angle. The tapered via degenerates to the cylindrical shape (see Fig. 2a) when tapering angle \( \theta_{\text{via}} = 90^\circ \). In order to provide DC isolation and to prevent leakage between the TSV and the substrate, a metal–insulator–semiconductor (MIS)-based TSV is primarily preferred. Herein, the TSV is enclosed by an insulating material such as a liner (typically \( SiO_2 \)) and a depletion layer that resembles the MOS structure. Therefore, the performance of a TSV is primarily dependent on the proper selection of the filler material. In general, Cu is used as a via filler material due to its low resistivity and silicon compatibility. However, in recent, the demand of technology scaling primarily draws the attention of the researchers toward the use of emerging SWB and MWB as filler material in TSV. Apart from this, a physical configuration of a coaxial TSV is shown in Fig. 2c that possesses a metal via enclosed by a benzocyclobutene (BCB) layer and a metal ring that employs high immunity to noise coupling and well-controlled characteristic impedance.

### 2.3 RLGC modeling

Using the physical configuration of different TSV shapes, an equivalent circuit model of a Cu- and CNT-based signal-ground TSV pair is demonstrated in Figs. 3 and 4.

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**Table 2** Model symbol, parameters, and its value [20–22]

| Parameter                        | Symbol | Values       |
|----------------------------------|--------|--------------|
| TSV height                       | \( h_{\text{via}} \) | 20-80 µm     |
| Cylindrical TSV radius           | \( r_{\text{via}} \) | .52 µm       |
| TSV Pitch                        | \( P_{\text{via}} \) | 3.82 µm      |
| IMD height                       | \( h_{\text{IMD}} \) | 1.18 µm      |
| Oxide thickness                  | \( t_{\text{ox}} \) | .105 µm      |
| Bump radius                      | \( r_{\text{bump}} \) | 2.5–4 µm     |
| Bump height                      | \( h_{\text{bump}} \) | 2.76 µm      |
| Depletion layer width            | \( t_{\text{dep}} \) | .691 µm      |
| Tapered slope angle              | \( \theta \) | 89°          |
| Coaxial TSV inner radius         | \( r_{\text{inner}} \) | .28 µm       |
| Coaxial TSV ring thickness       | \( t_{r} \) | .12 µm       |
| Coaxial TSV insulating layer thickness | \( t_{\text{ins}} \) | .12 µm       |
| Tapered TSV upper radius         | \( r_{b,\text{via}} \) | .52 µm       |
| Tapered TSV lower radius         | \( r_{a,\text{via}} \) | .17 µm       |
| Tapered bump upper radius        | \( r_{b,\text{bump}} \) | 2.5 µm       |
| Tapered bump lower radius        | \( r_{a,\text{bump}} \) | 2.45 µm      |

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![Fig 2](image-url) Perspective and top view of TSV structure: **a** cylindrical, **b** tapered, and **c** coaxial.
respectively. For an accurate analysis of the proposed model, the impact of skin effect and eddy loss has been considered.

In order to analyze the RLGC parameters, a Pi-based lumped model is considered. It is fairly obvious that as long as an entity’s physical dimensions is less than one-tenth of its wavelength, it can be classified as electrically small owing to these TSVs which can be accurately considered as lumped circuit [20]. Additionally, the total lengths of the TSV interconnects are shrinking to the tens of micrometers order as the fabrication technology headways. Since the height of the via is in the micrometer range corresponding to the wavelength of a few hundreds of gigahertz, a lumped-based circuit is preferred. Hence, using the lumped-based network in Figs. 3 and 4, the equivalent parasitic expressions for the Cu- and CNT-based TSV are discussed in the following subsections.

### 2.3.1 Cu-based TSV

This subsection presents a RLGC model of cylindrical-, tapered-, and coaxial-based signal-ground paired MIS-based via structure as shown in Fig. 3. The model primarily comprises of a via and bump resistance \( R_{\text{cu\_via}} + R_{\text{bump}} \) and inductance \( L_{\text{cu\_via}} + L_{\text{bump}} \), insulator and bump capacitance \( C_{\text{TSV\_bump}} \), underfill and IMD capacitance \( C_{\text{underfill\_IMD}} \), silicon substrate conductance \( G_{\text{si}} \), and capacitance \( C_{\text{si}} \), and eddy resistance \( R_{\text{eddy\_loss}} \). The skin effect is taken into consideration for the TSV high-frequency model. As a result, AC resistances of the via are computed using the concept of skin depth. For the cylindrical- and coaxial-shaped TSVs, the expressions for the via resistance \( R_{\text{cu\_via}} \) are provided in [23], and [12], respectively. Furthermore, for tapered via, the DC resistance can be calculated using (3) by substituting the bump with the TSV physical parameter, and the AC resistance can be calculated using [23]. In order to calculate the DC resistance of tapered solder joint, the bump can be distributed into infinite number of small cylindrical components with a height of \( dx \). Hence, the total bump resistance \( R_{\text{bump}} \) can be presented by integrating infinitesimally thin slice along the bump height and can be calculated as

\[
R_{\text{bump}} = \int_{0}^{\delta_{\text{bump}}} \frac{h_{\text{bump}}}{\pi \left( \frac{h_{\text{bump}} - x}{\tan \theta_{\text{bump}}} \right)^2} \, dx
\]

(3a)

\[
R_{\text{bump}} = \frac{4 \delta_{\text{bump}} h_{\text{bump}}}{2 \pi \rho_{b\_bump} \left( \frac{2 h_{\text{bump}}}{\tan \theta_{\text{bump}}} - \frac{2 h_{\text{bump}}}{\tan \theta_{\text{bump}}} \right)}
\]

(3b)

Here, \( \delta_{\text{bump}} = 1.09 \times 10^{-6} [\Omega \cdot \text{m}] \) represents Resistivity of bump. Additionally, the eddy resistance, which is predominantly caused by high-frequency eddy current, is appropriately accounted in the proposed model. The expression of eddy resistance of cylindrical and coaxial TSVs can be obtained using the Maxwell equation and vector potential Green’s function. Thus, the eddy resistance of cylindrical and coaxial TSVs can be formulated as

\[
R_{\text{eddy\_loss}} = \frac{\omega \times \mu_{0} \times \mu_{s\_via} \times h_{\text{via}}}{4} \left[ \text{Re} \left( H_{0}^{(2)} \left( \frac{1 - j}{\delta_{i}} \left( r_{\text{via}} + t_{\text{ox}} + t_{\text{dep}} \right) \right) \right) \right]
\]

(4)
where as for tapered TSV we can substitute \( r_{via} \) in expression (4) with \( \sqrt{a_{via}^2 + c_{via}^2} + \beta^2 \).

Where \( \beta = \tan \theta_p \), \( a_{via} = 90 - \theta_{via} \), and \( \mu_r = 1 \) represents relative permeability of via.

The opposing magnetic field property in the via and bump produces inductance that tends to oppose changes. The inductance of TSV is computed by integrating the total magnetic flux penetrating the surface enclosed by the current loop. For the cylindrical and coaxial TSV, the expression for magnetic flux penetrating the surface enclosed by the current loop. For the cylindrical and coaxial TSV, the expression for magnetic flux penetrating the surface enclosed by the current loop.

The inductance of TSV is computed by integrating the total magnetic flux density along the via (as shown in Fig. 1 (b)) which is represented as

\[
\psi_{\text{bump}} = \int_{r_{a,\text{bump}}}^{r_{b,\text{bump}}} \frac{mr+c}{r} B\,dx + \int_{r_{b,\text{bump}}}^{\infty} B\,dx
\]

\[
L_{\text{bump}} = \frac{\psi_{\text{bump}}}{I} = \frac{-\mu_0 \times \mu_r}{4\pi} \left[ h_{\text{bump}} \times \ln \left( \frac{r_{b,\text{bump}}}{r_{a,\text{bump}}} \right) + f(r_{a,\text{bump}}) + f(r_{b,\text{bump}}) \right]
\]

The signal-ground TSV pair also possesses an insulating and bump capacitance due to the presence of oxide, depletion, and IMD layers. The aforementioned capacitances are primarily dependent on the thickness of the insulating layers and can be formulated for cylindrical, tapered, and coaxial TSVs as given in [14, 20], and [8], respectively. Furthermore, the bump capacitance for cylindrical via can be expressed as

\[
C_{\text{bump}} = \frac{e_0 \varepsilon_r \times \pi \times \left( r_{a,\text{bump}}^2 - (r_{via} + t_{ox} + t_{\text{dep}})^2 \right)}{h_{\text{IMD}}}
\]

where as for analysis of \( C_{\text{bump}} \) for tapered and coaxial via one can replace \( r_{via} \) in (8) with \( r_{b,\text{via}} \) and \( r_{inner} + t_r + t_{\text{ins}} \) respectively.

The IMD layer is formed due to post-metallization of TSV during the fabrication process. Additionally, in order to reduce leakage between the bump, the underfill layer is used. Therefore, the effect of capacitance through IMD \( (C_{\text{IMD}}) \) and underfill layers \( (C_{\text{underfill}}) \) needs to be considered. The underfill and IMD capacitance of TSVs can be computed by integrating infinitesimally parallel capacitance which is expressed as expression (9) through (13)

\[
C_{\text{underfill}} = \int_{0}^{h_{\text{underfill}}} \frac{2\pi e_0 \varepsilon_{r,\text{underfill}}}{\cosh^{-1} \left( \frac{p_{\text{via}}}{2(r_{a,\text{bump}} + t_{\tan \theta_{bump}})} - 1 \right)} \, dx
\]

\[
C_{\text{underfill}} = 2\pi e_0 \varepsilon_r \left( \frac{h_{\text{bump}}}{\cosh^{-1} \left( \frac{p_{\text{via}}}{2(r_{a,\text{bump}} + t_{\tan \theta_{bump}})} - 1 \right)} - 4 \times r_{a,\text{bump}}^3 \left( \frac{p_{\text{via}}}{2(r_{a,\text{bump}} + t_{\tan \theta_{bump}})} - 1 \right)^2 \left[ \frac{p_{\text{via}}}{2(r_{a,\text{bump}} + t_{\tan \theta_{bump}})} - 1 \right] \right)
\]

where

\[
f(r_{a,\text{bump}}) = \sqrt{r_{a,\text{bump}}^2 + h_{\text{bump}}^2} - h_{\text{bump}}
\]

\[
f(r_{a,\text{bump}}) = \sqrt{r_{a,\text{bump}}^2 + h_{\text{bump}}^2} - h_{\text{bump}}
\]

Here, \( \mu_r = 1 \) represents relative permeability of bump.

However, for \( f(r_{b,\text{bump}}) \) one can replace \( r_{a,\text{bump}} \) with \( r_{b,\text{bump}} \) in expression (7) for obtaining the total bump inductance of (6).
and for coaxial via, \( f(P_{via}, r_{via}) \) can be written as,

\[
\cosh^{-1}\left[\frac{p_{via}^2}{2(r_{inner} + t_{ins} + t_r + t_oa)^2} - 1\right] = \frac{r_{via}}{r_{inner} + t_{ins} + t_r + t_oa} \approx \frac{r_{via}}{2}\frac{r_{via}}{r_{inner} + t_{ins} + t_r + t_oa} \quad (12)
\]

For tapered via, \( C_{IMD} \) are in relation with \( \alpha_{via} \), is defined as,

\[
C_{IMD} = 2\pi f_{\phi, IMD} \left\{ \frac{h_{IMD}}{\cosh^{-1}\left[\frac{p_{via}^2}{2(r_{via})^2} - 1\right]} - \left[\left(\frac{h_{IMD}}{r_{via}}\right)^2 \tan \alpha_{via} \times p_{via}\left(\frac{2(t_{oas} + t_{ias})^2 - p_{via}^2}{2(t_{oas} + t_{ias})^2} - p_{via}\right) \right] \right. \\
\left. \left(\frac{h_{IMD}}{r_{via}}\right)^2 \tan \alpha_{via} \times p_{via}\left(\frac{2(t_{oas} + t_{ias})^2 - p_{via}^2}{2(t_{oas} + t_{ias})^2} - p_{via}\right) \right] \right\} \quad (13)
\]

2.3.2 CNT-based TSV

This subsection presents different bundle topologies (SWB and MWB) and its physical structures such as tapered, cylindrical, and coaxial as depicted in Fig. 5. For the CNT bundle, the radius of SWCNT (\( r_{CNT} \)) is considered as 0.5 nm, while the radius of MWCNTs are represented as \( r_{CNT1}, r_{CNT2}, \ldots, r_{CNTn} \), where \( r_{CNT1} \) and \( r_{CNTn} \) are the inner and outermost shell radius, respectively. The SWB/MWB, placed above the ground plane with a height \( H_{ground} = 100 \mu m \), primarily consists of a number of SWCNTs/MWCNTs with length \( L_{CNT} = 20 \mu m \) and inter-shell/inter-CNT distance \( S_{CNT} = 0.34 \) nm. Using the aforementioned physical parameters and triangular inter-tube arrangement (Fig. 6), the RLG model of SWB/MWB is proposed in Fig. 4. When modeling the RLG parameters of a CNT-based via bundle, the effect of the nanoparticle electric and magnetic properties is appropriately considered, while modeling of the bump, IMD, and insulating capacitance is kept constant. The CNT-based via bundle parasitic is predominantly determined by the number of CNTs in bundle.

The total number of SWCNTs (\( N_{CNT} \)) in a bundle is proportional to volume of bundle and inversely proportional to triangular arrangement. The volume of triangular arrangement of CNT bundle as shown in Fig. 6 can be expressed as

\[
V_{\Delta} = \frac{\sqrt{3}}{4} \times (2r_{CNT} + S_{CNT})^2 h_{via} \quad (14)
\]

Thus, using the concept of volumetric triangular arrangement the total number of CNTs (\( N_{CNT} \)) for the different bundle shapes can be primarily expressed as,

For cylindrical

\[
N_{CNT} = \frac{4\pi \times r_{via}^2}{\sqrt{3} \times (2r_{CNT} + S_{CNT})^2 h_{via}} \quad (15)
\]

For tapered

\[
N_{CNT} = \frac{\pi}{3} \times \left( r_{via}^2 \times r_{b, via}^2 + r_{a, via} \times r_{b, via} \right) \quad (16)
\]

For coaxial

\[
N_{CNT} = \frac{\pi}{4} \times \left( r_{via}^2 \times r_{b, via}^2 + r_{a, via} \times r_{b, via} \right) \quad (17)
\]

The via parasitics depend on the number of conducting channel that can be modeled using the effect of spin and sublattice degeneracy of carbon atoms. Thus, the conducting channels (\( N_i \)) for CNT bundle (SWB and MWB) can be presented as

\[
N_i \approx 2k_i r_{CNT} + k_2, \quad 2r_{CNT} > d_T/T \approx 2/3, \quad 2r_{CNT} \leq d_T/T \quad (18)
\]
where \( r_{\text{CNT}_i} \) represents the radius of \( i \)th shell in CNT bundle and \( k_1, k_2, d_T \) are equivalent to \((3.87 \times 10^{-4}) \text{nm}^{-1} \text{K}^{-1}, 0.2 \) and 1300\( \text{nm·K} \), respectively, at room temperature (\( T = 300 \text{K} \)).

The total number of conducting channel in a CNT bundle (SWB and MWB) defined using the sum of conducting channels of each shell (in case of MWCNT)/each CNT (in case of bundle) is represented as

\[
N_{\text{Total}} = \sum_{i=1}^{N_{\text{SWB}}} N_i
\]  

(19)

If the height of the via bundle is greater than the mean free path, the TSV bundle will often exhibit scattering resistance, that is caused by static impurity scattering, defects, and acoustic phonon scattering. Hence, the total bundle resistance can be expressed as

\[
R_{\text{bundle}} = \frac{h \times h_{\text{via}}}{4e^2 \times \lambda_{\text{mfp}} \times N_{\text{Total}}}
\]  

(20)

where \( h \) and \( \lambda_{\text{mfp}} \) are the Planck’s constant and the electron mean free path, respectively, and can be obtained from [24].

The bundle inductance \( L_{\text{bundle}} \) associated with kinetic (\( L_K \)) and magnetic inductance (\( L_M \)) is primarily appeared due to kinetic and magnetic energy. Additionally, the bundle quantum capacitance (\( C_{\text{bundle}} \)) is defined based on the finite density of states at Fermi energy and can be obtained from [24].

The via resistance \( (R_{\text{via}}) \) and inductance \( (L_{\text{via}}) \) computed through (3) and (6) are validated with fabrication-based experimental results given in [25, 26] as depicted in Fig. 7. It is observed that the via resistance is in well agreement with the experimental result with an average error of 7.35% only. Similarly, the via inductance is also in close approximation with experimental result with an average deviation of 6.35%.

### 3 Crosstalk and Power loss analysis

This work presents a comparative exploration of Cu- and CNT-based different via bundle shapes using the coupled driver-via-load (DVL) setup at 22 nm technology. The TSV line in the DVL arrangement primarily represents the \( RLCG \) model. Using the setup as mentioned, the cylindrical, coaxial, and tapered via bundles are examined in terms of crosstalk-induced delay, peak noise, insertion, and reflection losses for Cu- and CNT-based TSVs. The simulation setup comprises of aggressor and victim via lines wherein the switching activities of aggressor line generate peak noise to the grounded victim line due to cross-coupling capacitance, i.e., termed as functional crosstalk. Similarly, dynamic crosstalk refers to the crosstalk-induced delay caused by the simultaneous switching of both via lines in the opposite (out-phase) or same (in-phase) direction [27]. Furthermore, the insertion loss (S12) typically occurs when part of a signal power is dissipated while travelling from source to load. Additionally, the return loss (S11) refers the amount of signal power reflected from the source end. Incorporating the \( RLCG \) into the CMOS-based driver–receiver circuit, the aforementioned delay and losses can be discussed in the following subsection.

#### 3.1 Crosstalk-induced delay analysis

A comparative analysis for crosstalk-induced delay is demonstrated for Cu-, SWB-, and MWB-based different via shapes using the proposed \( RLCG \) networks as presented in Figs. 3 and 4. A CMOS driver at 22 nm technology is used to drive the via lines of the \( RLCG \) model. Using the industry standard circuit simulation, the in-phase and out-phase crosstalk-induced delays are investigated for coaxial, cylindrical, and tapered via with different filler materials such as Cu, SWB, 2-shell, 10-shell, and 15-shell MWB as depicted in Fig. 8a and b, respectively. It is observed that the in-phase
and out-phase crosstalk-induced delays are considerably reduced for 15-shell MWB compared to the Cu, SWB, 2-, and 10-shell MWB TSVs. It is due to the lower quantitative values of the coupling capacitance that is primarily governed by the number of neighboring CNTs in the bundle. Furthermore, for a fixed bundle radius, the number of neighboring CNTs for the 15-shell MWB is lesser compared to SWB and MWB with 2 and 10 shells, resulting in reduced coupling capacitance and eventually producing lesser crosstalk. It is evident that compared to other via shapes, the tapered TSV has relatively lesser crosstalk delay due to the lesser cross-sectional area that primarily reduces the overall capacitive effect in terms of $C_{\text{via}_{\text{total}}}$, $C_{\text{total}_{\text{dielectric}}}$, and $C_{\text{si}}$ as observed in Table 3. Apart from this, the out-phase delay has more adverse effect in comparison with the in-phase transition irrespective of TSV shapes and height. This phenomenon can be occurred due to the Miller’s effect that predominantly governed by the coupling capacitance between the neighboring via bundle. Therefore, considering an overall out-phase delay, a 15-shell MWB-based tapered TSV outperformed by 11.29, 8.26, 5.57 and 2.58% w.r.t. Cu, SWB, and 2- and 10-shell MWB, respectively. The reason behind is that for a fixed via volume, the tapered-based MWB has lesser number of MWCNTs in comparison with SWCNTs that reduces the overall conducting channels in a bundle. It substantially reduces the cumulative effects of equivalent capacitance and resistance. Therefore, the results indicate that the 15-shell tapered-based MWB possesses an improved dynamic crosstalk compared to the Cu and other CNT bundle-based different TSV shapes at 22 nm technology.

Furthermore, the percentage improvement in crosstalk-induced delay for a 15-shell MWB w.r.t. to the other filler materials at a via height of 20 μm and 80 μm is summarized in Table 4. It is perceived that the overall out-phase delay improvement is 77% lesser in comparison with the in-phase delay (as summarized in Table 4). The reason behind this is that the out-phase produces a larger delay over in-phase due to the Miller capacitive effect that drives the coupling capacitance to virtually double by a factor of two. Therefore, the relative changes on smaller delay (i.e., in case of in-phase) can appear to be more significant because a small absolute change in the number can result in a large percentage improvement. Additionally, from Table 4, it can be inferred that when the via height increases from 20 to 80 μm, the worst case crosstalk delay (i.e., out-phase) worsens by 5.8% in case of 20 μm, while it enriched by 8.5% in 80 μm scenario. It is due to the fact that the MWCNT concentration rises in case of higher TSVs and hence the conductivity becomes a significant physical component influencing the crosstalk-induced delay. Furthermore, MWB-based higher TSVs are more effective since their conductivity increases for more number of CNTs and thus results in significant improvement in crosstalk-induced delay. In conclusion, the via height influenced the improved crosstalk-induced delay for 15-shell MWB, which is attributed to the reduction in phonon scattering due to a smaller contact interface area for MWB-based higher TSVs [28].

### 3.2 Peak noise

The primary reason of logic malfunctions in the integrated circuits is inadvertent peak occurrence on the victim line. An analysis of a percentage improvement in peak noise of a tapered-based MWB having 15-shell MWCNTs w.r.t. other filler materials is demonstrated in Table 5. It is evident that a considerable reduction in peak noise is observed for 15-shell MWB in comparison with the other filler materials. The primary reason behind this reduced effect is due to the fact that the bundle comprises of MWCNTs with larger shells.
| TSV filler material and shape | Parasitic                          | Parasitic                          | Parasitic                          | Parasitic                          | $C_{\text{total, dielectric}}$ (fF) | $N_{\text{total}}$ | $C_{\text{bump}}$ (fF) | $C_{\text{TSV}}$ (fF) | $C_{\text{Q^{bundle}}}$ (nF) |
|------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|-------------------------------------|----------------|----------------|----------------|----------------|----------------|
| Cu                           | Cylindrical                        | 516                                | 7.97                               | 9.17                               | 3.49                                | .33           | 1.93           | -              | .14            | 9.03           |
|                              | Coaxial                            | 719                                | 1.42                               | 4.82                               | 3.49                                | .33           | 1.93           | -              | .14            | 4.68           |
|                              | Tapered                            | 1220                               | 13.36                              | 3.28                               | 2.28                                | .21           | 1.90           | -              | .14            | 3.14           |
| SWB                          | Cylindrical                        | 177                                | 51.81                              | 9.17                               | 3.49                                | .33           | 1.93           | 727,200        | .14            | 9.03           |
|                              | Coaxial                            | 254                                | 51.90                              | 4.81                               | 3.49                                | .33           | 1.93           | 507,800        | .14            | 4.68           |
|                              | Tapered                            | 371                                | 52.05                              | 3.27                               | 2.28                                | .21           | 1.90           | 347,590        | .14            | 3.14           |
| MWB-2 shell                  | Cylindrical                        | 239                                | 50.02                              | 9.16                               | 3.49                                | .33           | 1.93           | 320,000        | .14            | 9.03           |
|                              | Coaxial                            | 343                                | 50.24                              | 4.80                               | 3.49                                | .33           | 1.93           | 223,400        | .14            | 4.68           |
|                              | Tapered                            | 502                                | 50.57                              | 3.26                               | 2.28                                | .21           | 1.90           | 152,900        | .14            | 3.14           |
| MWB-10 shell                 | Cylindrical                        | 501                                | 48.19                              | 9.15                               | 3.49                                | .33           | 1.93           | 36,150         | .14            | 9.03           |
|                              | Coaxial                            | 717                                | 50.11                              | 4.79                               | 3.49                                | .33           | 1.93           | 25,240         | .14            | 4.68           |
|                              | Tapered                            | 1049                               | 53.06                              | 3.25                               | 2.28                                | .21           | 1.90           | 17,270         | .14            | 3.14           |
| MWB-15 shell                 | Cylindrical                        | 519                                | 48.99                              | 9.14                               | 3.49                                | .33           | 1.93           | 23,625         | .14            | 9.03           |
|                              | Coaxial                            | 743                                | 51.94                              | 4.77                               | 3.49                                | .33           | 1.93           | 16,495         | .14            | 4.68           |
|                              | Tapered                            | 1086                               | 56.43                              | 3.24                               | 2.28                                | .21           | 1.90           | 11,291         | .14            | 3.14           |

$R_{\text{via,total}} = R_{\text{cu,via}} + R_{\text{bump}} + R_{\text{eddy,loss}}$, for Cu

$L_{\text{via,total}} = L_{\text{cu,via}} + L_{\text{bump}}$, for Cu

$C_{\text{total, dielectric}} = C_{\text{underfill}} + C_{\text{IMD}}$

$C_{\text{via,total}} = \left( C_{\text{Q^{bundle}}} \left( C_{\text{TSV}} + C_{\text{bump}} \right) \right) / \left( C_{\text{Q^{bundle}}} + C_{\text{TSV}} + C_{\text{bump}} \right)$, for CNT

$C_{\text{TSV}} = (C_{\text{ox}} C_{\text{dep}}) / (C_{\text{ox}} + C_{\text{dep}})$

$R_{\text{via,total}} = R_{\text{bundle}} + R_{\text{bump}}$, for CNT

$C_{\text{via,total}} = C_{\text{TSV}} + C_{\text{bump}}$, for Cu

$L_{\text{via,total}} = L_{\text{bundle}} + L_{\text{bump}}$, for CNT
carries lesser current than a SWB and Cu due to effect of fractional conductance and reduced number of conducting channel \((N_{\text{Total}})\). Sanvito et al. \cite{29} stated that MWCNT’s outermost shell reflects not only even/odd conductance quantum multiples, but also fractional and non-integer quantum conductance values as a result of their inter-wall interaction. The cumulative effect of both the inter-wall interaction and reduction in number of conducting channel \((N_{\text{Total}})\) can increase the bundle resistance \((R_{\text{bundle}})\) because of its inverse relation (as shown in Eq. 20). It also results in a reduced quantum capacitance \((C_{Q_{\text{bundle}}}^{\text{bundle}})\) value as a result of direct dependency. Hence, the overall via capacitance \((C_{\text{via,total}}^{\text{via,total}})\) decreases, resulting in low loss leakage due to an increased impedance \((Z = 1/jC_{\text{via,total}}^{\text{via,total}})\) that lowers the inadvertent peak.

It is also discerned from Table 5 that the peak noise rises for an increase in via physical dimensions, i.e., TSV heights. This is primarily due to the quantitative values of via parasitic, i.e., \(R_{\text{via,total}}, L_{\text{via,total}}, C_{\text{via,total}}\) increases for higher via dimension as observed from expressions (3) through (20). Additionally, Table 5 depicts the overall improvement in peak noise for the tapered-based TSV in comparison with the cylindrical- and coaxial-shaped TSVs. This is due to the fact that the tapered TSVs possess reduced area from top to bottom that creates lower quantitative values of the TSV parasitic such as silicon substrate capacitance \((C_{\text{Si}})\) and insulating and deletion capacitance, i.e., \(C_{\text{TSV}}\). Finally, from Table 5, it can be concluded that irrespective of via height, the tapered-based 15-shell MWB possesses average improvement of 20.7% peak noise in comparison with the other filler materials.

Table 4 Percentage improvement in crosstalk delay using 15-shell MWCNT-based tapered TSVs for different via heights

| TSV Heights | Filler material | % improvement in crosstalk induced delay of tapered-shaped 15-shell MWB-based TSV in comparison with |
|-------------|----------------|-----------------------------------------------------------------------------------------------|
|             |                | In-phase (%) | Out-phase (%) |
| 20 µm       | Cu             | 65.5        | 11.0          |
|             | SWB            | 53.5        | 7.2           |
|             | MWB—2 shells  | 46.3        | 3.6           |
|             | MWB—10 shells | 35.0        | 1.7           |
| 80 µm       | Cu             | 16.4        | 12.7          |
|             | SWB            | 13.9        | 10.4          |
|             | MWB—2 shells  | 11.6        | 8.2           |
|             | MWB—10 shells | 9.2         | 2.9           |

Table 5 Percentage improvement in peak noise using 15-shell MWCNT-based-tapered TSVs for different via heights

| TSV Height (µm) | % improvement in peak noise for 15-shell MWB-based tapered TSV in comparison with |
|-----------------|-------------------------------------------------------------------------------|
|                 | Tapered TSV                                                                  |
|                 | Cu (%) | SWB (%) | MWB 2-shell (%) | MWB 10-shell (%) |
| 20               | 40.00  | 28.57   | 26.82           | 23.07            |
| 40               | 29.41  | 23.56   | 21.31           | 18.64            |
| 60               | 20.76  | 18.37   | 15.01           | 10.68            |
| 80               | 21.05  | 19.64   | 11.76           | 4.25             |

Fig. 9  \( S \) parameter comparison of Cylindrical, Coaxial and Tapered TSV for different filler material a Cu, b SWB, and c MWB 15-shell
4 Conclusion

An analytic or semi-analytic mathematical expressions were derived for the differently shaped Cu, SWB and MWB (2, 10, and 15 shells)-based TSVs by presenting a π-based equivalent RLGC model. In order to validate the equivalent model, scattering (S) parameters were compared to the results obtained through structural EM simulation. For several test cases of different frequencies, a negligible average deviation of the scattering parameters S21 and S11 was observed as 0.004 dB and 0.7 dB, respectively. Additionally, via compatible differently shaped bump (cylindrical, tapered, and spherical) was analyzed in terms of MTTF reliability.

It can be seen that the MTTF encouragingly improved for the tapered-shaped bump due to its lower volume fraction and coefficient of thermal expansion (CTE). In addition to MTTF analysis, an improved performance of 15-shell MWB has been observed in comparison with Cu, due to its reduced number of neighboring CNT that correspondingly decreases the cross-coupling capacitance. Furthermore, compared to other shapes of TSVs, i.e., coaxial and cylindrical, the tapered via possesses lower parasitic values due to its reduced cross-sectional area. Finally, the electrical characteristics of the tapered via are computed and compared with that of coaxial and cylindrical via. It reveals that irrespective of via height, the 15-shell MWB-based tapered TSV exhibits a reduced crosstalk delay of 8.27 and 3.85%, peak noise of 40.53 and 26.59%, insertion loss of 16.24 and 10.56%, and reflection loss of 3.60 and 2.60% with respect to cylindrical and coaxial, respectively. Therefore, it can be concluded that the 15-shell-based tapered MWB provides an improved signal integrity and power loss.

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Declarations

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