A Demodulation Circuit For Analog Front End Of Passive Tag Chip

Qinglong Li, Yong Xu*, Qiao Li, Kun Peng, Xian Zhang
School of Communication Engineering, Army Engineering University of PLA, Nanjing, China
xu_yong99@163.com

Abstract. The demodulation circuit designed in this paper is suitable for the analog front end of passive UHF RFID tag chip, which can handle ASK signals with large changes in amplitude, modulation depth and signal frequency. Its performance meets the requirements of standards ISO/IEC 18000-6C and GB/T 29768-2013. Envelope detection circuit and limiter circuit are simple in structure and do not consume power. The comparison reference voltage is taken according to the average value of the envelope high and low levels, and is less affected by the dynamic changes of the input signal. Changing the width-to-length ratio of the MOSFETs in the feedback path of the comparator can adjust the hysteresis, with strong noise suppression and controllable sensitivity. The demodulator is implemented with TSMC 0.18 μm standard CMOS process. The simulation results show that the ASK signal modulation depth that the demodulator can handle is as low as 30%, and the maximum pulse width demodulation error is only 0.43%.

1. Introduction
Radio frequency identification (RFID) technology relies on radio waves to realize non-contact data exchange and target identification between reader and tag chip. The ultra-high frequency (UHF, 300 MHz ~ 3 GHz) radio frequency system has the characteristics of long identification distance, fast transmission speed and small antenna size[1]. The current international mainstream standards and national standards for UHF RFID systems are ISO/IEC 18000-6C and GB/T 29768-2013, respectively. It can be known from the two standards that the system forward link signal is a wave modulated by amplitude keying (ASK) with a modulation depth of 30% to 100%, and the baseband signal frequency is 40 kHz to 160 kHz.

The structure of the tag chip demodulator is generally a low-pass filter followed by a comparator. Its comparison reference voltage takes half of the envelope peak voltage. This circuit has a simple structure but cannot demodulate ASK signals with a modulation depth of less than 50%. Some schemes are voltage-compensated envelope detector followed by peak detection circuit. Although this type of circuit improves the demodulation sensitivity, the structure of the detection circuit is complex and requires a working power supply[2]. This paper designs a UHF RFID demodulator with no power consumption for the first two sub-circuits and based on average detection. It can handle RF signals with large changes in amplitude, modulation depth and signal frequency. The circuit performance meets the requirements of ISO/IEC 18000-6C and GB/T 29768-2013.

2. Design of UHF RFID Signal Demodulator
The structure of the UHF RFID signal demodulator designed in this paper is shown in Figure 1.
The received radio frequency signal \textit{RFIN} modulated by amplitude keying (ASK) is transmitted to the envelope detector to extract the envelope \textit{VENV} of the modulated signal. The limiter circuit can avoid circuit abnormalities caused by large envelope signals. The limiting voltage \textit{VLIM} is divided into two lines: one is connected to the comparator; the other is transmitted to the reference voltage generator to generate the comparison reference value \textit{VAVE}. The comparator compares \textit{VLIM} and \textit{VAVE} to determine the high or low level, and finally outputs the digital signal \textit{DOUT}.

2.1 Envelope Detector

As shown in Figure 2, a better scheme to extract ASK signal envelope is voltage multiplier plus low-pass filter[3]. The circuit structure is very simple, does not require additional power supply, does not consume power, and is suitable for use in passive tag chips.

![Envelope detector circuit](image)

Capacitors C1, C2 and MOSFETs M1 and M2 in Figure 2 form a one-stage voltage doubler rectifier circuit. When the value of \textit{RFIN} is less than the threshold voltage \textit{V_{TH}} of the MOSFET, that is, \(-V_{TH} < \textit{RFIN} < V_{TH}\), both M1 and M2 are cut off. When \textit{RFIN} is in the negative half cycle and \textit{RFIN} < \(-V_{TH}\), M2 is turned on, and the current flows from Ground through M2 to charge C1. Assuming that the peak value of \textit{RFIN} is \textit{V_M}, the voltage on C1 will be \(V_{C1} = -(V_M - V_{TH})\) at this time. As the input voltage rises, M2 will be cut off, and according to the conservation of charge, the voltage on C1 will remain unchanged. When \textit{RFIN} > \textit{V_{TH}}, M1 turns on and \textit{RFIN} starts charging C2. When \textit{RFIN} reaches the peak value of the positive half cycle, the ideal voltage value of C2 should be:

\[
V_{C2} = V_M - [-(V_M - V_{TH})] - V_{TH} = 2(V_M - V_{TH})
\]

When \textit{RFIN} gradually drops from the peak value of the positive half cycle to \textit{RFIN} < \textit{V_{TH}}, M1 is cut off and C2 discharges through R1. Since the charging time constant \(\tau_1 = R_{on1} \cdot C2\) is much smaller than the discharge time constant \(\tau_2 = R1 \cdot C2\), \textit{V_{C2}} is better maintained near the peak value of the positive half cycle of \textit{RFIN}. \textit{V_{C2}} is \textit{VENV}.

The simulation result of the envelope detection circuit given in the second row of Figure 6 shows: the passive and power-free voltage doubler rectifier and low-pass filter structure successfully extract the envelope of the radio frequency signal.

2.2 Limiter

When the distance to the reader is closer, the energy received by the tag is larger. The limiter circuit can avoid the abnormality of the subsequent circuit caused by the large envelope signal. As shown in Figure 3, the entire limiter circuit is not connected to a working power source and has no energy consumption.
Diode-connected N-MOSFETs M1~M4 are connected in series to form a voltage detection channel. Resistor R1, R2 and N-MOSFETs M5, M6 form a charge leakage path[4].

When $V_{ENV}$ is low, the gate-source voltage $V_{GS5}$ of M5 is less than its threshold voltage $V_{TH5}$, so $V_{GS6}$ must be less than $V_{TH6}$. At this time, M5 and M6 are both in the cut-off state and the output voltage $VLIM$ is equal to the input voltage $V_{ENV}$. When $V_{GS5} > V_{TH5}$ and $V_{GS6} < V_{TH6}$, M5 is on and M6 is off. The resistance R1 and the equivalent resistance $r_{O5}$ of M5 divide the input voltage. At this time, the output voltage is:

$$VLIM = V_{ENV} \cdot \frac{r_{O5}}{R_1 + r_{O5}} \quad (2)$$

When $V_{ENV}$ rises continuously so that $V_{GS6} > V_{TH6}$, both M5 and M6 are turned on. The output voltage is:

$$VLIM = V_{ENV} \cdot \frac{r_{O5}[(R_2+r_{O6})]}{R_1 + r_{O5}[(R_2+r_{O6})]} \cdot \frac{r_{O6}}{R_2 + r_{O6}} \quad (3)$$

Figure 4 shows the simulation results of the limiter circuit. When the input voltage is 0~1.5 V, the output voltage is approximately equal to the input voltage. When the input voltage is 1.5~8 V, the output voltage is limited to 1.8 V.

Figure 4. Simulation results of limiter
2.3 Reference Voltage Generator

Divide $VLIM$ into two lines: one is connected to the comparator; the other is connected to the reference voltage generator to generate the average voltage $VAVE$. If you want to demodulate radio frequency signals with different amplitudes and different modulation depths, the reference voltage used for comparison should be dynamically determined according to the high and low levels of $VLIM$. The reference voltage generator based on peak value $V_{peak}$ and valley value $V_{val}$ detection satisfies this requirement well. Its circuit structure is shown as in Figure 5[5]. The operational amplifier in the circuit can adopt a general operational amplifier structure.

![Reference voltage generator circuit](image)

**Figure 5.** Reference voltage generator circuit

The operational amplifiers OPA1 and OPA2 form a voltage follower through a deep negative feedback loop. OPA1, P-MOSFET M1 and capacitor C1 jointly detect the peak value $V_{peak}$. N-MOSFET M3 adjusts the amount of current in the channel. OPA2, N-MOSFET M2 and capacitor C2 can detect the valley value $V_{val}$ of $VLIM$. Equivalent resistors R1 and R2 divide the peak and valley voltages to determine the average voltage $VAVE$, that is:

$$VAVE = \frac{1}{2} (V_{peak} + V_{val}) \quad (4)$$

At the initial moment, the voltages on capacitors C1, C2 and C3 are all zero. When the input terminal $VLIM$ is high level, the voltage of the inverting terminal of OPA1 and OPA2 is greater than their in-phase terminal. Therefore, both operational amplifiers output low level. M1 turns on and M2 turns off. $VDD$ charges C1, C2 and C3 through M1. Because OPA1 is a voltage follower, the C1 voltage $V_{peak}$ will be equal to the input voltage $VLIM$. M2 cut-off makes the negative feedback loop of OPA2 open and cannot form a voltage follower. The C2 voltage $V_{val}$ is divided by R1 and R2. Because the resistances of the equivalent resistors R1 and R2 are relatively large, the charging time constant is large, so $V_{val}$ rises slowly. According to the KVL theorem, the C3 voltage $VAVE$ conforms to equation (4).

The input voltage $VLIM$ changes from high level to low level. The voltage $V_{peak}$ of the energy storage capacitor C1 is greater than $VLIM$, so that the operational amplifier OPA1 outputs a high level. So M1 is cut off. The negative feedback loop of OPA1 is open, making $V_{peak}$ no longer follow $VLIM$ changes. C2 voltage $V_{val}$ is also greater than $VLIM$, making OPA2 output a high level. Then M2 is turned on. C1, C2 and C3 are discharged through M2. Since the discharge time constants of C1 and C3 are much greater than the signal period, the input level $VLIM$ has already become high before $V_{peak}$ and $VAVE$ drop in time. Because the on-resistance of M2 is small, the discharge time constant of C2 is small. So $V_{val}$ quickly drops to a low level. Due to the voltage follower principle, $V_{val}$ remains near the low level. Similarly, the equivalent values of R1 and R2 show that $VAVE$ satisfies equation (4).
The simulation result of the reference voltage generator is shown in the third row of Figure 6: The actual $V_{AVE}$ (dashed line) generated is successfully placed between the high and low levels of $V_{LIM}$.

![Figure 6. Simulation result of reference voltage generator](image)

### 2.4 Hysteresis Comparator

Ripple voltage input to an ordinary single-threshold comparator will produce back and forth jitter at the output. The hysteresis comparator has the ability to suppress noise whose amplitude is within the range of hysteresis $\Delta V$. The structure of the hysteresis comparator designed in Figure 7 is a two-stage amplifier followed by a two-stage inverter[6].

![Figure 7. Hysteresis comparator circuit](image)

The differential input MOSFETs M1 and M2 have the same specifications. Now assume that $V_{AVE}$ is grounded. When the input voltage $V_{LIM}$ is far less than 0, the relationship between the gate-source voltage of M1 and M2 is: $|V_{G_{S1}}| \ll |V_{G_{S2}}|$. Then M2 turns on and M1 turns off. The turned-on M2 causes M7 and M8 to turn on, but M1 cutoff makes M5 and M6 cut off and makes M7 in the deep linear region. So there is $I_9 = I_2 = I_8$. (I_2, I_8, and I_9 are the drain-source currents of MOSFETS M2, M8, and M9, respectively.). At this time, M3 is off and M4 is on, and the comparator outputs a low level.

The input voltage $V_{LIM}$ gradually increases from low to high, causing $|V_{G_{S2}}|$ to continue to decrease. Then M1 gradually leaves the cut-off state. The ultimate role of M7-M8 mirroring is to:

$$I_7 = \frac{(W/L)_7}{(W/L)_8} \cdot I_8$$  \hspace{1cm} (5)

$(W/L)_7$ and $(W/L)_8$ in formula (5) are the conductive channel width-to-length ratios of MOSFET M7 and M8, respectively. When the rising $V_{LIM}$ makes M1 gradually turn on and makes $I_1$ increase to the mirror value $I_7$, the output of the comparator switches from low to high. Therefore, When $I_1 = I_7$, the
input voltage difference \( (V_{LIM} - V_{AVE}) \) is the positive turning point. This point is the upper threshold voltage \( V_+ \), so:

\[
V_+ = V_{LIM} - V_{AVE} = V_{GS2} - V_{GS1} \quad (6)
\]

From \( I_1 = I_7, I_2 = I_8, I_9 = I_1 + I_2 \) and equation (5), the following equation can be derived:

\[
I_1 = \frac{I_9}{1 + \left(\frac{W/L}{W/L_7}\right)} \quad (7)
\]

\[
I_2 = \frac{I_9}{1 + \left(\frac{W/L}{W/L_8}\right)} \quad (8)
\]

From equations (6) to (8) and the current formula of the saturation region of the P-MOSFET (where \( \mu_p \) is the surface electron mobility of the P-MOSFET, \( C_{OX} \) is the gate capacitance per unit area):

\[
V_+ = \frac{2I_9}{\mu_p C_{OX} (W/L)_1 \sqrt{1 + \left(\frac{1}{1 + \left(\frac{W/L}{W/L_8}\right)}\right)}} \quad (9)
\]

Similarly, the lower threshold voltage can be derived as:

\[
V_- = \frac{2I_9}{\mu_p C_{OX} (W/L)_1 \sqrt{1 + \left(\frac{1}{1 + \left(\frac{W/L}{W/L_6}\right)}\right)}} \quad (10)
\]

The bias current \( I_9 \) of the circuit is provided by the current mirror M9. If the aspect ratio of M1 (M2) has been determined, the upper and lower threshold voltages and hysteresis can be determined by changing the aspect ratios of M5, M6, M7 and M8. Figure 8 shows the simulation result of the hysteresis response of the comparator: the designed hysteresis of this circuit \( \Delta V \) is 20 mV.

![Figure 8. Hysteresis response of comparator](image)

### 3. Circuit Layout

In order to reduce the mutual interference between circuit devices, each sub-circuit and each amplifier are arranged as independent module units. There are two guard rings around each unit: the inside is the P guard ring connected to the ground, and the outside is the N guard ring connected to the power supply. The combination of inner P and outer N forms a PN junction wall around the outside of the module to protect the inside of the module from external noise. The capacitors, resistors, P-MOSFETs and N-MOSFETs in each module unit should be arranged separately. A P guard ring connected to the ground is arranged around each capacitance area, resistance area and N-MOSFET area. This protects the holes in the P substrate in the ring from being injected by electrons outside the ring. In addition, the P-ring of
the N-MOSFET area can also be used as the substrate of the MOSFET. An N-ring connected to the power supply is arranged around the P-MOSFET area: This not only protects the electrons in the N-well in the ring from being absorbed by the holes outside the ring, but also serves as the substrate of the P-MOSFET.

The current mirror controls the current of each branch by changing the width-to-length ratio of each MOSFET. In order to obtain an accurate proportional current, the MOSFET in the current mirror should adopt interdigital structure. Such as hysteresis comparator M5-M6, M7-M8, M9-M10 and M11-M12. Each MOSFET that needs to be matched should have the same channel length. The matching of the two MOSFETs uses the ABBA symmetrical interdigital structure and the three uses ABCCBA.

Because the MOSFET on the differential input terminal is extremely sensitive to signals, the accuracy of the one-dimensional interdigital structure is insufficient. The two-dimensional co-centroid array has better consistency, symmetry, dispersion, compactness and directionality. M1-M2 and M3-M4 in the hysteresis comparator are differential input pairs. The channel lengths of these MOSFETs that need to be matched should be the same. The two-dimensional high-precision matching MOSFET's fingers should be divided into two rows: the layout of the first row is ABBA and the second row is BAAB to form an ABBA cross-coupled pair.

Figure 9 shows the demodulation circuit layout of the tape-out.

4. System Simulation of Demodulator
The pre-simulation and post-simulation of the whole circuit use cadence spectre. The working power supply of the circuit is 1.8 V during simulation. The carrier of the radio frequency signal is a sine wave of 915 MHz. The simulation conclusion is obtained by observing and measuring the output signal and calculating the maximum deviation. Figure 10 shows the simulation results of ASK signals with three different amplitudes, modulation depths and pulse frequencies. The widths of the three input pulse signals are 3.125us, 6.25us and 12.5us respectively. The actual measured output pulse width is 3.116us, 6.277us and 12.499us respectively. Thus, The pulse width errors are -0.29%, 0.43% and -0.01%, respectively.

Protocols ISO/IEC 18000-6C and GB/T 29768-2013 use PIE and TPP to encode baseband data respectively. Both of these codes can be converted into non-return-to-zero (NRZ). Now arbitrarily give three groups of 8-bit NRZ baseband data, and use different depths to modulate the carrier to generate ASK signals. Use them as incentives for the circuit. The output response is shown in Figure 11: The baseband signal is accurately and completely demodulated by this circuit.
The demodulation circuit designed in this paper with good dynamic performance and extremely low demodulation error has been applied to an ultra-low power label chip that has been taped out. The position of the demodulation module in the chip is shown in the photomicrograph in Figure 12.
5. Conclusion
The envelope detection circuit and limiter circuit in this paper do not need power supply and consume no power, so they are suitable for passive tags. The reference voltage generator can generate the corresponding average value reference voltage according to the high and low level of the signal envelope, so its dynamic adaptation performance is better. Finally, after the judgment of a hysteresis comparator with strong noise suppression, it can demodulate ASK radio frequency signals with various amplitudes, various modulation depths and various code rates. Reasonable layout technology minimizes device mismatch and parasitic effects, so the circuit has a good front-end consistency. The circuit is implemented using TSMC 0.18 μm standard CMOS process. The simulation results of ASK signal combinations of various amplitudes, modulation depths and pulse frequencies show that the maximum error of the signal pulse width is only 0.43%. The demodulator can accurately and completely process the PIE and TPP encoding of the protocol ISO/IEC 18000-6C and GB/T 29768-2013. This circuit has been used as a demodulation module in passive tag chips and successfully taped out.

6. References
[1] A. El Boutahiri, M. El Alaoui, K. El Khadiri, A. Tahiri, and H. Qjidaa, "Design of new power generating circuit for passive UHF RFID tag," International Journal of Power Electronics and Drive Systems, vol. 9, no. 3, pp. 1389-1397, 2018.
[2] D. Yongqian, Z. Yiqi, L. Xiaoming, and L. Weifeng, "A UHF RFID chip solution with new oscillator calibration scheme and 16k bits EEPROM," IEICE Electronics Express, vol. 13, no. 13, pp. 20160472-20160472, 2016.
[3] L. Yang, J. Li, M. Tang, L. Cai, J. Li, and M. Zheng, "A high-sensitivity ASK demodulator for passive UHF RFID tags with automatic voltage limitation and average voltage detection," in 2015 IEEE 11th International Conference on ASIC (ASICON), Chengdu, China, 2015, pp. 1-4: IEEE.
[4] S. Haddadian and J. C. Scheytt, "Analysis, Design and Implementation of a Fully Integrated Analog Front-End for Microwave RFIDs at 5.8 GHz to Be Used With Compact MIMO Readers," IEEE Journal of Radio Frequency Identification, vol. 4, no. 4, pp. 476-490, 2020.
[5] Y.-L. Tsai, J.-Y. Chen, B.-C. Wang, T.-Y. Yeh, and T.-H. Lin, "A 400MHz 10Mbps D-BPSK receiver with a reference-less dynamic phase-to-amplitude demodulation technique," in 2014 Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, HI, USA, 2014, pp. 1-2: IEEE.
[6] S. Li et al., "A~20 dBm Passive UHF RFID Tag IC With MTP NVM in 0.13-μm Standard CMOS Process," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4566-4579, 2020.