Heterogeneous Sparse Matrix-Vector Multiplication via Compressed Sparse Row Format

Phillip Allen Lane¹,*, Joshua Dennis Booth²

Abstract
Sparse matrix-vector multiplication (SpMV) is one of the most important kernels in high-performance computing (HPC), yet SpMV normally suffers from ill performance on many devices. Due to ill performance, SpMV normally requires special care to store and tune for a given device. Moreover, HPC is facing heterogeneous hardware containing multiple different compute units, e.g., many-core CPUs and GPUs. Therefore, an emerging goal has been to produce heterogeneous formats and methods that allow critical kernels, e.g., SpMV, to be executed on different devices with portable performance and minimal changes to format and method. This paper presents a heterogeneous format based on CSR, named CSR-k, that can be tuned quickly and outperforms the average performance of Intel MKL on Intel Xeon Platinum 8380 and AMD Epyc 7742 CPUs while still outperforming NVIDIA’s cuSPARSE and Sandia National Laboratories’ KokkosKernels on NVIDIA A100 and V100 for regular sparse matrices, i.e., sparse matrices where the number of nonzeros per row has a variance ≤ 10, such as those commonly generated from two and three-dimensional finite difference and element problems. In particular, CSR-k achieves this with reordering and by grouping rows into a hierarchical structure of super-rows and super-super-rows that are represented by just a few extra arrays of pointers. Due to its simplicity, a model can be tuned for a device and used to select super-row and super-super-rows sizes in constant time.

1. Introduction
Sparse matrix-vector multiplication (SpMV) has remained one of the most important kernels in high-performance computing (HPC) due to its use in applications such as machine learning and iterative solvers (e.g., Conjugate Gradient (CG) and GMRES for partial differential equations (PDEs)) [13]. Modern systems are composed of numerous heterogeneous compute units, e.g., many-core CPUs, GPUs, and FPGAs. Each compute unit has different microarchitecture properties that influence how they access and process data. Due to SpMV’s importance and shift in system design, a need exists for a heterogeneous format, i.e., a data structure that can be efficiently utilized by different compute units, for SpMV. This SpMV format needs to exist in a manner that requires only minor adjustments that can be done quickly when switching between compute units. Overall, the problem of constructing such a format is difficult. Even on many-core systems, optimizing the performance of SpMV requires tuning given the sparse matrix, microarchitecture of the hardware, and the number of SpMV operations the application will execute [14][18][23]. Optimizing on accelerators, such as GPUs, can be even more difficult and many of the optimization choices utilized for many-core systems, such as blocking and base format, are completely different. In this work, we propose extending the well-known many-core system CSR-k [14][15] format to be heterogeneous for both parallel many-core systems and GPUs as this format is both flexible enough and compatible with many already standard interfaces that utilize CSR format.

SpMV, i.e., Ax = y where A is a sparse coefficient matrix and x, y are dense vectors, is well-known to be a notoriously difficult kernel to optimize because of its memory bandwidth requirements [5][11][18]. The primary challenge in optimizing SpMV is its relatively poor performance on devices due to low computational intensity, i.e., the number of floating-point operations per memory load is low. Recalling the general algorithm for SpMV, for each row (i) of A the nonzero elements are multiplied by their corresponding elements in x and added together for a single element in y (yi). Each of these nonzeros in a row results in three loads (i.e., aij, xj, and yj) and one store must occur per multiply-add operation. Additionally, there exists little data reuse as each aij is only used once and yj is only used for each row. Making matters even more difficult, the one array that does see reuse (i.e., x) might be accessed effectively at random, depending on the structure of the matrix. This makes it extremely difficult for cache structures to consistently hold relevant data, and places SpMV firmly on the bandwidth-limited roofline of the roofline model [27]. As such, SpMV may only see a small fraction of the peak performance of a compute device because a very proportionally large amount of time is spent waiting for memory accesses [17].

Currently, SpMV formats such as coordinate list (COO) and compressed sparse row (CSR) [12][21] are used to reduce the memory overhead of storing sparse data. This reduction aids large sparse matrices to better fit into the main memory and may reduce the number of loads needed to keep data in higher cache levels. However, they are not designed in consideration of parallel processing and the complex microarchitecture of modern devices, such as nonuniform memory accesses

¹Corresponding author
Email addresses: phillip.lane@uah.edu (Phillip Allen Lane), joshua.booth@uah.edu (Joshua Dennis Booth)
²Graduate Student
³Assistant Professor of Computer Science

Preprint submitted to Elsevier
January 9, 2023
(NUMA) on many-core systems. A second challenge is the complexity of the optimization. This complexity comes in the form of the time to optimize and overhead in the size of the data structure. For example, the process of autotuning SpMV was popular in the early 2000s [1][23], and the cost for tuning SpMV on many-core systems by constructing complex multi-level block structures could be amortized over the length of the application. However, both the computational device and the number of concurrent threads could theoretically change per iteration of the application in modern heterogeneous systems, and the cost of autotuning would be too high on such systems.

Therefore in this paper, we extend CSR-k for heterogeneous systems. CSR-k has shown in the past to be a very efficient format on early-generation multicore systems and is relatively easy to understand and store as it is an extension to the highly used CSR format. Due to being a direct extension of the CSR format, the values can be accessed by other packages that require CSR format without converting once the sparse matrix has been placed in CSR-k format. Moreover, the tuning time is far smaller than other methods (e.g., pOSKI [1][23]) as the parameter space is much smaller, and, as we observe in the paper, the tuning can be done in constant time after training a simple model. We note that the goal of CSR-k is for a performance portable heterogeneous format. Therefore, the performance goal is to be on par with the state of the art and not necessarily better for every device and sparse matrix structure.

This paper provides the extension of CSR-k for heterogeneous systems, in particular CPUs and GPUs, in the following manner:

- An overview of the implementation changes needed for CSR-k on NVIDIA GPUs
- The first model-driven selection of tuning parameters for the CSR-k format to provide constant-time parameters
- A comparison of CSR-k to KokkosKernels [10], NVIDIA’s cuSPARSE, CSR5 [18], and TileSpMV [20] on Volta and Ampere
- A comparison of CSR-k to Intel MKL and CSR5 [18] on Xeon Platinum 8380 and Epyc 7742
- A demonstration of the ability of CSR-k to offer portable performance on regular matrices and limitations of CSR-k with irregular matrices.

2. Background and Related Work

In this section, we present some of the most common implementation formats for SpMV on CPU and CPU/GPU heterogeneous formats. Through this presentation, we outline the strengths and weaknesses of each and their current state.

2.1. Formats for CPU

Though many SpMV formats have been studied [9][12][14][21][24][25], two standard formats have become popular for SpMV due to reducing memory overheads and their relative ease of understanding, i.e., Coordinate list (COO) and Compressed Sparse Row (CSR). COO is the most straightforward format for storing a sparse matrix. The COO format contains three arrays (i.e., col_idx, row_idx, and vals) each array is the length of the number of nonzeros (NNZ) in the sparse matrix. However, several drawbacks exist for utilizing COO on many-core systems. These drawbacks include the overall storage required is $3 \times NNZ \times 32$ bits if we consider 32 bit integers and single-precision floating-point values, and the format itself does not provide any ordering of how the nonzero values should be processed. As a result, a SpMV of a sparse matrix that is stored in COO based on a random permutation of col_idx and/or row_idx would have poor performance, and lock or atomic operations would be needed for parallel implementations.

CSR is designed to be a more space-efficient data structure than COO. It does this by blocking nonzero elements into shared rows. The format contains three arrays (i.e., row_ptr, col_idx, and vals). The row_ptr array provides the running cumulative sum of the nonzero elements in each row and hence has size $m + 1$ for an $m \times n$ sparse matrix. The col_idx provides the column index and the vals provides the values for each of the nonzero elements. As such, the CSR requires $(2 \times NNZ + m + 1) \times 32$ bits of data. Figure 1 provides an example of this format in black (ignoring sr_ptr and ssr_ptr).

![Figure 1: Example of the CSR-3 data structure with the super-row pointer (sr_ptr) and super-super-row pointer (ssr_ptr). Super-rows and super-super-rows are shown in the matrix above. They contain the continuous sums of the number of rows and super-rows, respectively. This is similar to how row_ptr contains the continuous sum of nonzeros per row.](image)

Sparse blocked based formats, such as Block Compressed Sparse Row (BCSR) [19][25] or Unaligned Block Compressed Sparse Row [24], take the idea of CSR into a second dimension. Nonzero elements are grouped together in two-dimensional blocks that are normally dense. Many sparse matrices from finite-element analysis often exhibit this dense block substructure. These blocks are next grouped together in some outer blocking structure, such as by row in BCSR. These can be highly optimized due to the number of different parameters they provide, e.g., the number of rows and columns in a block. However, the performance of BCSR depends on grouping together nonzero elements into a block, therefore BCSR is not ideal for many
sparse matrices. Though these formats can reduce the memory needed to store the sparse matrix, the true advantage of these formats is having smaller structures and memory access patterns that better fit the hierarchical cache memory structures in many-core systems. In particular, these small dense blocks can better fit into L1 or L2 caches.

In the application space, SpMV formats are hard to separate from reorderings. Sparse reorderings permute nonzero elements, and these reorderings can provide better memory accesses [8], improve iteration counts of sparse iterative solvers [2], and can provide better groupings of nonzeros, such as those taken advantage of by many block based formats and supernodes in sparse direct methods [8]. An example of these orderings includes reorderings that reduce the bandwidth around the diagonal, i.e., orderings that pull nonzero elements toward the diagonal, such as spectral orderings [4] and Reverse Cholesky-McKee (RCM) [6]. Therefore, it is almost always the case that some reordering is applied to the sparse matrix in conjunction with selecting a storage format.

### 2.2. CSR-k

One CSR based format that has shown to greatly improve parallel performance and be more aware of the hierarchical cache structure is CSR-k [14, 15]. CSR-k is a multilevel data structure for storing sparse matrices based on CSR. This format utilizes both multilevel structures that better fit the cache structure of many-core systems and multiple levels of reorderings to reduce the envelope or band size for a level. In particular, the \( k \) represents a small integer \( \geq 2 \) that defines the number of additional arrays that store data about rows (i.e., the number of additional arrays equals \( k-1 \)). We explore the choice of \( k \) as a parameter in Section 6.2. Figure 1 provides an example of CSR-3. As noted before, the standard three arrays of CSR (i.e., vals, col_idx, and row_ptr) exist in CSR-3. CSR-3 has two additional arrays. These arrays are \( s r_{\text{ptr}} \) and \( ssr_{\text{ptr}} \) that contain pointers to the super-rows and the super-super-rows. Super-rows are groups of contiguous rows, and the array is compressed in a similar manner to how row_ptr compresses information on the number of contiguous nonzeros in a row. As an example from Figure 1, the SR 0 contains two rows (2), the SR 1 contains three rows (2 + 3), the SR 2 contains two rows (2 + 3 + 2), and finally SR 3 contains two rows (2 + 3 + 2 + 2) to provide \( ssr_{\text{ptr}} = \{0, 2, 5, 7, 9\} \). This method is extended up to super-super-rows that group together contiguous super-rows, i.e., SSR 0 contains two SRs and SSR 1 contains two SRs to provide \( ssr_{\text{ptr}} = \{0, 2, 4\} \). As a result, the CSR-k format’s only memory overhead is the storage of these additional arrays.

For completeness, we provide the pseudocode for SpMV with CSR-3 on a many-core system in Listing 1. Lines 4-5 parallelize the outermost for loop, which iterates over super-super rows (e.g., \( \text{num\_ssr} = 3 \) in Fig 1). In lines 6-9, the bounds for one super-super-row are fetched and iterated across (e.g., \( ssr_{\text{ptr}} \) in Fig 1). Similarly, lines 10-13 fetch the bounds for one super-row and are iterated across (e.g., \( sr_{\text{ptr}} \) in Fig 1). Finally, lines 14-21 implement the actual work in a similar manner to a CSR-based kernel.

```plaintext
Listing 1: CSR-3 CPU kernel

1 function SpMV3(num_ssr, ssr_ptr[]) {
2     sr_ptr[], r_ptr[], col_idx[];
3     vals[], x[], y[])
4 #pragma omp parallel for
5 for i = 0 to num_ssr
6     let ssr_start = ssr_ptr[i + 1]
7     let ssr_end = ssr_ptr[i + 1]
8     for j = ssr_start to ssr_end
9         let sr_start = sr_ptr[j]
10        let sr_end = sr_ptr[j + 1]
11        let temp = 0.0
12        for k = sr_start to sr_end
13            let r_start = r_ptr[k]
14            let r_end = r_ptr[k + 1]
15            temp += vals[l] * x[col_idx[l]]
16        } y[k] = temp
17    }
```

Listing 2: Band-k

```plaintext
Listing 2: Band-k

1 function BandK(Gk, k) {
2     for i = 0 to k - 1
3         From G_{k+i} from G_i using graph coarsening
4         Reorder G_{k+i} using
5         weighted bandwidth limiting ordering
6     }
7     for i = k to 2
8         Expand node G_i to G_{i-1}
9         Reorder its corresponding vertices
10        in G_{i-1} with weighted bandwidth
11        limiting ordering
12    }
13 for i = 1 to k
14 Use reordering of G_i to determine
15 super-rows of A
18 }
```
in Listing 2. The sparse matrix is first converted into a graph $G$. The graph is coarsened in multiple levels determined by $k$ (i.e., lines 2-6, Fig 2b). Each coarsened level is reordered using a weighted bandwidth limiting ordering (i.e., lines 7-14, Fig 2c). Additionally, nodes are reordered within each of these coarsened nodes using a bandwidth limiting ordering. This process normally produces an ordering with a band slightly wider than that produced by RCM, but better fits the format structure (i.e., Fig 2d). As such, we utilize the standard Band-$k$ format for our extension as well. Moreover, the multiple levels of the coarsened-band ordering aim to help with load imbalance.

2.3. Formats for GPU

One notable format has a long history of being pushed on GPU, namely ELLPACK (ELL) format [16] and its derivatives. ELL format is a blocking format, which takes an $m \times n$ sparse matrix and stores it as two $m \times k$ dense matrices, where $k$ is the number of nonzeros in the densest row of the sparse matrix. One matrix stores the nonzeros shifted left, padded on the right with zeros. The other matrix stores their corresponding columns also padded with zeros. ELL and its many variants were used heavily for GPU-based SpMV in the early days of GPGPU, due to its friendliness to vector architectures [19, 26], but suffer from the issue of excess memory overhead. For instance, if an irregular sparse matrix had the densest row containing 40 nonzeros, but an average nonzero count of 10, the ELL format would incur a 300% memory overhead.

2.4. Heterogeneous Formats

Heterogeneous formats are those that are designed to fit multiple different computational devices. These have become popular due to the importance of heterogeneous computing systems. Several popular formats stand out in this area. The first is the use of blocked sparse format on GPU devices. Eberhardt and Hoemmen [9] demonstrate that BCSR is a reasonable format for both many-core CPUs and GPUs when the sparse matrix contains some block substructure. However, a specialized algorithm for SpMV on GPU must be reworked for the particular device such as their by-column algorithm in order to outcompete NVIDIA’s built-in sparse matrix library cuSPARSE. On the other hand, Liu and Vinter [18]’s CSR5 introduces a CSR based format that utilizes a number of tiles to improve performance on both many-core CPUs and GPUs. These tiles are of size $\sigma$ by $\omega$ and are autotuned to better fit the SIMD nature of the device. The elements in the col_idx are ordered in a way to fit these tiles and additional vectors (i.e., a title pointer and a title descriptor with lengths that are based on the choice of $\sigma$ and $\omega$) are kept for title information along with a bit-flag vector the length of the number of nonzeros in the sparse matrix. Therefore, the format is tuned to the device, and storing the spare matrix for additional devices would require keeping additional title pointers and title descriptors. Utilizing this format, CSR5 can obtain on average the maximum performance of either standard CSR or the autotuned pOSKI [1] on many-core CPU systems and is able to obtain on average the maximum performance of all tests kernels on GPUs. Lastly, work by Aliaga et al. [3] examines the use of a compressed COO format. They demonstrate a truly heterogeneous format that can be stored in the same format for both many-core CPUs and GPUs. This format’s performance on CPU is on average better than Intel MKL’s CSR utilizing 16 AMD Epyc cores and is better on NVIDIA V100 and A100 than cuSPARSE’s COO. This format compresses values into integer values using a look-up table and requires bit-wise computation to determine blocking.

3. CSR-$k$ for Exploiting Multidimensional Block Structure in NVIDIA GPUs

In this section, we provide an overview of how to extend CSR-$k$ for NVIDIA GPUs utilizing CUDA. We note that there is nothing different in the storage format of CSR-3 for a GPU and the storage format of CSR-3 for a CPU that is introduced in the previous section. The difference is how we interpret the hierarchical levels within CSR-$k$ and how this optimally gets implemented in the GPU algorithm. As noted before, the multiple levels in the CSR-$k$ for a CPU can be interpreted as blocking sets of rows into super-super-rows and super-rows that better fit the hierarchical level cache structure on many-core systems. The algorithm implementation of this is straightforward with each level providing an additional level of for-loops over the super-super-rows and super-rows. Listing 1 provides an example of this code for CSR-3 on a CPU.

However, NVIDIA GPUs utilizing CUDA do not have the same types of hierarchical level cache structure as a CPU. Figure 3 provides a representation of the memory and execution structure of a NVIDIA GPU. The GPU has a large (e.g., 80 GB) shared global memory consisting of HBM2 or HBM2E high-bandwidth memory for higher end systems, a shared L2 cache, and a memory layer that can be partitioned as a private
L1 data cache or shared memory for each streaming multiprocessor (SM). We also note that these caches (such as the L1 data cache) are much smaller per thread than a traditional CPU cache. For instance, AMD Rome (e.g., AMD Gen2 Epyc) has 32 KB per core of private L1 data cache, while the NVIDIA Ampere A100 has 192 KB per SM of L1 data cache. Since each SM has 64 32-bit floating-point units (FP), that equates to an average of 3 KB/thread, though this cache is shared across all FP execution units in an SM. Additionally, how these resources are scheduled is fundamentally different than a CPU. Each thread on a CPU can be fixed or pinned to a particular computational core and remain there until it has completed its work. In the CSR-k case, this work could be the execution of a particular set of super-rows. However, 32 threads are blocked together to form a warp on these GPUs. It is more convenient to think of this warp as a single SIMD intrinsic on CPUs. Groups of these threads/warps combine to form a thread block, and a thread block supports at most 1024 threads. These thread blocks are assigned to an SM and will not migrate to other SMs (i.e., they are fixed or pinned). Therefore, it is easier to think of each block as an assignment of a core to a super-row. This mapping only goes so far as each SM may have multiple thread blocks and the order of execution of these thread blocks is unknown. These blocks are further coarsened into a grid. Due to how the scheduler is implemented, the most efficient CUDA kernels are mapped into a computational grid or cube. This allows better exploitation of the 3D nature of CUDA blocks and the grid. Utilizing this structure often aids in better data locality, since the CUDA runtime is able to schedule threads close in a block closer on the die. Using this cubic environment, we can map multilevel data structure efficiently to a 2D or 3D block.

Therefore, we can utilize the hierarchical structure of the GPU even if not directly related to the cache level size for CSR-k, and in the next section, we justify super-super-row and super-row sizes based on this argument if we utilize CSR-3 format. As such, we will primarily focus on a $k = 3$ for these NVIDIA GPUs. We start by assuming that an SM is a core or shared-memory computational area in a standard CPU with a shared memory cache, i.e., the L1 data cache, even though each SM may have multiple blocks mapped to it and contains multiple dispatch units. This rationality is reasonable as a core may work on multiple super-super-rows and these super-super-rows should be issued as a chunk. Therefore, we can view a single block as a super-super-row each being assigned to an SM. As such, we build a grid of these blocks, i.e., a 1D grid. We note that a single block can only support up to 1024 threads, which will put a cap on the maximum size of our super-super-rows. Within a block, the next level (i.e., super-row) loop can be mapped to the $y$-dimension and the row can be mapped to the $x$-dimension to form 2D blocks. We note that the order that $x$- and $y$-dimensions are structured in the code is important for GPU dispatch. Warps are grouped first by thread adjacency in the block $x$-dimension, then the $y$-dimension, then the $z$-dimension. Therefore, organizing the threads that work on the inner loops (which work on spatially adjacent data) along the $x$-dimension first is important for data locality. We call this base code GPUSpMV-3.

Figure 4 provides a diagram of the CSR-3 format’s layout in terms of CUDA thread blocks. As such, super-super-row 0 (SSR 0) will map onto Block 0. The $y$-dimension of the block will be mapped on the super-row (SR), e.g., $y_0$ maps to SR0 and $y_1$ maps to SR1. The accompanying pseudocode is provided in Listing 3. We note that this code is relatively simple and easy to implement in CUDA as it relies on the simple CSR-3 structure and CUDA block parallel functions.

The last for-loop, i.e., the inner product of the sparse matrix row and the vector, (Line 19-21 in Listing 3) in the algorithm provides an additional level of possible parallelism from across the row (i.e., both the multiply-add operations and the sum reduction). The original CSR-k paper did not consider this level of parallelism because of overheads with aligning and data movement for SIMD intrinsics in the test hardware. As noted in the last section, CSR5 explicitly lays out its tiles for these SIMD operations but at the cost of the complexity of the format. This level of parallelism is important and needs to be addressed in GPU codes. However, if the number of nonzeros per row is relatively small (e.g., $< 8$), utilizing this level of parallelism would reduce the available number of overall threads to a block and would require the overhead of utilizing part of the L1 data cache for shared memory. Through experimentation, we discovered that 8 nonzero elements per row is what is required to improve performance with parallelization at this level. We denote the algorithm with the parallelism of the last level as GPUSpMV-3.5, and pseudocode is provided in Listing 4. Fig-
4. Tuning Optimal Structure

4.1. GPU

When tuning CSR-k for CPUs normally a low cost autotuning method is needed, and the original paper notes how expensive this autotuning is compared to pOSKI. Autotuning on a GPU opens up many new parameters, such as block dimensions and if the inner product should be parallelized (e.g., GPUSpMV-3 vs GPUSpMV-3.5). However, there exist some standards that can help guide this tuning, and these standards can even be reduced to a closed form heuristic formula that can determine the super-row and super-super-row sizes in constant time for a given sparse matrix after some initial tuning on a given device.

The first of these standards is based on the relationship between the number of threads and block size. Remember that only 1024 threads can be used per block and that 32 threads are launched at a time in a warp. Therefore, the dimensions of the block should be based on multiples of 32. The second of these standards is having enough work to keep each thread busy while limiting the working memory size of each thread so accesses are not hitting slower caches or main memory. Additionally, making more threads is more likely to amortize any imbalance in work each thread might have. The average amount of work a single row must compute (in GPUSpMV-3) is based on the average row density, i.e., \(rdensity = \frac{NNZ}{N}\) where \(NNZ\) is the number of nonzeros and \(N\) is the number of rows. Additionally, we have experimentally determined as noted before that serial computation of the inner product per row only makes sense when \(rdensity < 8\). Based on these two facts and common block dimensions used in GPUs, we only need to consider the following cases:

**Case 1:** \(rdensity \leq 8\)
The block dimensions are set as \(8 \times 12\).

**Case 2:** \(8 < rdensity \leq 16\)
The block dimensions are set as \(4 \times 8 \times 12\).

**Case 3:** \(16 < rdensity \leq 32\)
The block dimensions are set as \(8 \times 8 \times 8\).

**Case 4:** \(32 < rdensity\)
The block dimensions are set as \(16 \times 8 \times 4\).

We can interpret these values as follows. In Case 1, four rows along the \(y\)-dimension (i.e., \(8 \times 4\) threads) would make up a warp. Since the \(y\)-dimension corresponds to a super-row in GPUSpMV-3, a single warp would have four super-rows. This may seem like a lot of work, but the \(rdensity\) is relatively small in this case. On the other hand, in Case 4, two rows along the \(y\)-dimension would make up a warp due to the number of nonzeros in a single row needing to be computed.

Once these standard block sizes are set, empirical runs can be completed with different sizes of super-rows and super-super-rows over a suite of sparse matrices. We can use these runs with the following modeling method to determine a closed form heuristic for the selection of super-super-row and super-row 
sizes in the future. Using these test runs, we perform a logarithmic regression over the dataset, with the $x$-values being $rdensity$ and the $y$-values being the optimal super-super-row or super-row sizes. The $SSRS$ (super-super-row size) and $SRS$ (super-row size) parameters are tuned independently. That is, during testing, all reasonable combinations of $SSRS$ and $SRS$ are tested (some set of representative sizes between 4 and 48 for GPU) and the regression is performed twice: one on the optimal $SSRS$ parameters, and one on the optimal $SRS$ parameters. The specific set of combinations for $SSRS$ and $SRS$ tested are described as follows:

$$(SSRS, SRS) \in \left( \bigcup_{i=2}^{5} \{2^i, 1.5 \cdot 2^i\} \right)^2$$

where $\phi^2$ is shorthand for the set Cartesian product $\phi \times \phi$.

Finally, since the logarithmic regression tends to yield a formula that drops much below optimal when $rdensity$ becomes large, the coefficient of the natural logarithm was lowered by hand to better fit the optimal $SSRS$ and $SRS$ with high $rdensity$.

From this method, we achieve the following formula for tuning on the NVIDIA Volta:

$$SSRS = [8.900 - 1.25 \cdot \ln(rdensity)]$$
$$SRS = [10.146 - 1.50 \cdot \ln(rdensity)]$$

where $[x]$ represents rounding-to-nearest, half towards positive infinity operation.

These numbers would have to be derived for each different machine that has considerable microarchitecture differences. For NVIDIA Ampere, a slight tuning is required and provides:

$$SSRS = [9.175 - 1.32 \cdot \ln(rdensity)]$$
$$SRS = [20.500 - 3.50 \cdot \ln(rdensity)].$$

Similarly, the coefficient of the natural logarithm is lowered so that $SSRS$ and $SRS$ do not drop too low on higher density rows. The constant term is unchanged in both instances.

After the initial $SSRS$ and $SRS$ are determined, they can be further tuned based on $rdensity$. In particular, the $SSRS$ and $SRS$ need to be updated to account for their derivation from the original assumption of utilizing GPUSpMV-3 to GPUSpMV-3.5, in addition to accounting for the changing block dimensions as $rdensity$ grows. As such, they are modified on Volta:

Case 1: $rdensity \leq 8$
Tune SSRS and SRS no further.

Case 2: $8 < rdensity \leq 16$
$$SSRS = [SSRS \times 1.5]$$
$$SRS = SRS \times 2.$$  

Case 3: $16 < rdensity \leq 32$
$$SSRS = SSRS \times 4$$
$$SRS = \lfloor SSRS / 2 \rfloor.$$  

Case 4: $32 < rdensity$
$$SSRS = SSRS \times 5$$
$$SRS = \lfloor SSRS / 2 \rfloor.$$  

For Ampere, they are modified as:

Case 1: $rdensity \leq 8$
Tune SSRS and SRS no further.

Case 2: $8 < rdensity \leq 16$
Tune SSRS no further.
$$SRS = SSRS \times 4.$$  

Case 3: $16 < rdensity \leq 32$
$$SSRS = [SSRS \times 2.5]$$
$$SRS = SSRS \times 3.$$  

Case 4: $32 < rdensity$
$$SSRS = SSRS \times 2$$
$$SRS = SSRS \times 2.$$  

4.2. CPU

When running CSR-2 on a CPU, the kernel is much less dependent on having optimal $SSRS$ and $SRS$ within a narrow window for good performance. Additionally, the added complexity of the cache hierarchy in CPUs, as opposed to GPUs, makes tuning much more difficult to do optimally, as there is no clear correlation between optimal $SSRS$/$SRS$ and known matrix attributes without analyzing matrix structure. Due to these combinations of factors, we find that in an ideal scenario, each matrix would be tuned individually, using a set of representative $SRS$ between 8 and 3072, which are specified as the set:

$$SRS \in \left[ \bigcup_{i=3}^{11} \{2^i, 1.5 \cdot 2^i\} \right].$$

The combined effect of larger caches on CPU and using CSR-2 instead of CSR-3 means that much higher $SRS$ are often preferred. Namely, most matrices on CPU using CSR-2 prefer $SRS$ in the range of 40-1000, as opposed to most matrices on GPU using CSR-3 preferring $SSRS$/$SRS$ in the range of 4-12.

If constant-time tuning is preferred at the expense of performance, we have found that taking the geometric mean of optimal $SRS$ across a representative dataset yields decent performance. For instance, one might use a $SRS = 96$ for all matrices on CPUs to yield performance that is often "good enough."

5. Test Setup

5.1. Test Systems

The test setup consists of four systems. **GPU Systems.** System 1 is used for GPU testing and has two Xeon E5-2650v4 CPUs ("Broadwell") with 12 cores each, and contains several NVIDIA V100 GPUs ("Volta"). These GPUs contain 32 GB of main memory and a peak memory bandwidth of 900 GB/s. System 2 is also used for GPU testing and has two Epyc 7713 CPUs ("Milan" or "Zen 3") with 64 cores each, and contains NVIDIA A100 GPUs ("Ampere"). These GPUs contain 40 GB of memory and a peak memory bandwidth of 1555 GB/s. On both GPU systems, only one GPU is used. **CPU Systems.** System 3 is for CPU testing. It contains two Epyc 7742 CPUs ("Rome" or "Zen"
Table 1: Benchmark suite. ID identifies regular vs. irregular, SY is the percentage of pattern symmetry, N is the outer dimension in millions, NZ is the number of nonzeros per million, MAX is the maximum number of nonzeros per row, and R is the row density.

| ID | SY      | Matrix          | N (M) | NZ (M) | MAX   |
|----|---------|-----------------|-------|--------|-------|
| r1 | 1.0     | belgium_osm     | 1.44  | 3.10   | 10    | 2.15  |
| r2 | 1.0     | netherlands_osm | 2.22  | 4.88   | 7     | 2.20  |
| r3 | 1.0     | roadNet-TX      | 1.39  | 3.84   | 12    | 2.76  |
| r4 | 1.0     | roadNet-CA      | 1.97  | 5.53   | 12    | 2.81  |
| r5 | 1.0     | roadNet-PA      | 1.09  | 3.08   | 9     | 2.83  |
| r6 | 1.0     | hugetrace-00000 | 4.59  | 13.76  | 3     | 3.00  |
| r7 | 1.0     | hugetric-00000  | 5.82  | 17.47  | 3     | 3.00  |
| r8 | 1.0     | debr             | 1.05  | 4.19   | 4     | 4.00  |
| r9 | 1.0     | venturi_level3   | 4.03  | 16.11  | 6     | 6.00  |
| r10| 1.0     | rajat31          | 4.69  | 20.32  | 1.2K  | 4.33  |
| r11| 1.0     | G3_circuit      | 1.59  | 7.66   | 6     | 4.83  |
| r12| 1.0     | ecology1         | 1.00  | 5.00   | 5     | 5.00  |
| r13| 1.0     | 333SP            | 3.71  | 22.22  | 28    | 5.98  |
| r14| 1.0     | AS365            | 3.80  | 22.74  | 14    | 5.98  |
| r15| 1.0     | NACA0015         | 1.04  | 6.23   | 10    | 5.99  |
| r16| 1.0     | M6               | 3.50  | 21.00  | 10    | 6.00  |
| r17| 1.0     | NLR              | 4.16  | 24.98  | 20    | 6.00  |
| r18| 1.0     | delaimuy_n20     | 1.05  | 6.29   | 23    | 6.00  |
| r19| 1.0     | delaimuy_n21     | 2.10  | 12.58  | 23    | 6.00  |
| r20| 1.0     | delaimuy_n22     | 4.19  | 25.17  | 23    | 6.00  |
| r21| 1.0     | atmosmodL        | 1.49  | 10.32  | 7     | 6.93  |
| r22| 1.0     | atmosmodM        | 1.49  | 10.32  | 7     | 6.93  |
| r23| 1.0     | atmosmodD        | 1.27  | 8.81   | 7     | 6.94  |
| r24| 1.0     | atmosmodJ        | 1.27  | 8.81   | 7     | 6.94  |
| r25| 1.0     | thermal2         | 1.28  | 8.58   | 11    | 6.99  |
| r26| 1.0     | Curl/Curl_3      | 1.22  | 13.54  | 13    | 11.11 |
| r27| 1.0     | Curl/Curl_4      | 2.38  | 26.52  | 13    | 11.14 |
| r28| 1.0     | Stocf-146s       | 1.47  | 21.09  | 18    | 14.34 |
| r29| 1.0     | Transport        | 1.60  | 23.48  | 15    | 14.66 |
| r30| 1.0     | packing...       | 2.15  | 34.98  | 18    | 16.30 |
| r31| 1.0     | af_shell10       | 1.51  | 52.26  | 35    | 34.65 |
| r32| 0.0     | Hamrle3          | 1.45  | 5.31   | 9     | 3.81  |
| r33| 0.9     | circuit5M_dc     | 3.52  | 14.87  | 24    | 4.22  |
| r34| 0.9     | memchup          | 2.71  | 13.34  | 27    | 4.93  |
| r35| 0.9     | Freescale1       | 3.43  | 17.05  | 25    | 4.97  |
| n1 | 1.0     | com-Youtube      | 1.13  | 5.98   | 28.8k | 5.27  |
| n2 | 1.0     | kkt_power        | 2.06  | 12.77  | 90    | 6.19  |
| n3 | 1.0     | FullChip         | 2.96  | 26.62  | 2.3M  | 8.91  |
| n4 | 1.0     | circuit5M        | 5.56  | 59.13  | 10.71 | 11.14 |
| n5 | 1.0     | av-Skitter       | 1.70  | 22.19  | 35.5k | 13.08 |
| n6 | 1.0     | rgg_n_2_20_s0    | 1.05  | 13.78  | 36    | 13.14 |
| n7 | 1.0     | rgg_n_2_21_s0    | 2.10  | 29.88  | 37    | 13.82 |
| n8 | 1.0     | cancer14         | 1.51  | 27.13  | 41    | 18.02 |
| n9 | 1.0     | dgreen           | 1.20  | 26.51  | 97    | 18.22 |
| n10| 1.0     | nv2              | 1.45  | 37.48  | 84    | 25.78 |
| n11| 1.0     | nlpkt80          | 1.06  | 28.19  | 28    | 26.54 |
| n12| 1.0     | Hook_1498        | 1.50  | 59.37  | 93    | 39.64 |
| n13| 1.0     | dieFilterV2real  | 1.16  | 48.54  | 25    | 41.94 |

5.2. Tested Libraries

For GPU experiments, GUPUSpMV-3 and GUPUSpMV-3.5 are both implemented in C++ with CUDA and compiled with the NVIDIA NVHPC compiler using compilation tools version 11.4. Our CSR-k SpMV implementations are compared against cuSPARSE v11.4, KokkosKernels v3.4.1 [10], CSR5 [13], and TileSpMV [20]. NVIDIA’s cuSPARSE is an optimized sparse linear algebra library written for use on NVIDIA GPUs. It provides SpMV implementations in several formats, and we compare it against the library’s CSR implementation. NVIDIA’s cuSPARSE is part of the CUDA runtime, so all runs are performed using CUDA runtime 11.4, which has support for both Volta and Ampere GPUs. KokkosKernels is a computational mathematics library published by Sandia National Laboratories. It supports sparse and dense linear algebra, among other kernels, on both CPUs and GPUs. The goal of KokkosKernels is to provide performance portable code to multiple parallel run-time libraries without requiring the user to code in the different libraries. KokkosKernels is compiled for the SM_70 compute architecture, which is supported by our Volta GPUs. The tested version of KokkosKernels does not support building for multiple GPU architectures (e.g., SM_70 and SM_80), and therefore will only be tested on Volta.

CSR5 is tested on both Volta and Ampere and is compiled with the same compiler used for GUPUSpMV. We were unable to use the -gencode flag the default make has to specify the GPU architecture because the implementation uses several functions that are deprecated for SM_70 and onwards, which includes both of our GPU test beds. TileSpMV is tested on Ampere and is compiled with the same compiler used for GUPUSpMV. TileSpMV is a format for sparse matrices that stores tiles of the matrix in one of seven formats: CSR5, ELL, HYB, COO, dense column, dense row, and dense. A decision tree classifies each tile into one of the storage formats. At runtime, optimized device kernels are chosen on a per-tile basis to match the storage format of a given tile. It is important to note that TileSpMV is not advertised as a heterogeneous solution. As such, it is not tested on CPUs. We do not test it on Volta, as we use it for a replacement for KokkosKernels.

For CPU experiments, we utilize Intel MKL v19.1.3 on system 3 and Intel MKL v19.1.1 on system 4. Intel MKL (Math Kernel Library) is a computational mathematics library that supports highly-optimized sparse linear algebra on CPUs. CSR-k is compiled on system 3 with the AMD Optimizing C Compiler (AOCC) v2.3.0 with -03 optimization and -march=znver2. CSR-k is compiled on system 4 with the Intel v19.1.1 compiler with -03 -ipo optimization and -march=icelake-server. Additionally, OpenMP scheduling parameters are set to static scheduling for CSR-k on systems 3 and 4. CSR5 is also tested on systems 3 and 4, using the same compiler configurations as CSR-k. We compile the AVX2 version of the compiler.
sion of CSR5 for both systems 3 and 4. Despite system 4 supporting AVX512, the AVX512 implementation of CSR5 uses extensions that are not supported in our Ice Lake CPU (namely, AVX512ER and AVX512PF).

5.3. Test Suite

For our test suite, we consider all sparse square matrices with the outer dimension ranging from 1 to 6 million and having less than 60 million nonzeros from the SuiteSparse collection [7]. This provides a total of 64 sparse matrices with various sparsity patterns. Table 1 provides a list of these sparse matrices along with a categorization (ID), percentage of the symmetric pattern (SY), outer dimension (N) given in millions, number of nonzeros (NZ) given in millions, the maximum number of nonzeros in a row (MAX), and the average number of nonzeros in a row (i.e., row density) (R). Matrices within the table are categorized into two levels of groups: regular vs. irregular and symmetric vs. nonsymmetric. The group of regular vs. irregular is similar to the grouping done in the analysis of CSR5 [13], and provides a way to judge if the number of nonzeros in a row varies from the average. As such, sparse matrices whose number of nonzeros do not vary greatly from the average are considered regular, while sparse matrices whose number of nonzeros vary greatly from the average are considered irregular. While the analysis of CSR5 used the maximum and the minimum number of nonzeros in a row to approximate this grouping into regular vs irregular, we calculated the variance of the number of nonzero in a row (σ²) and used the value of σ² = 10 to be the point of classifying into the two groups of regular and irregular. Next, we classify the groups of regular and irregular into symmetric and nonsymmetric. Any matrix that does not have a 100% (1.0) symmetric sparsity pattern is considered nonsymmetric. While this classification may not be interesting to formats like CSR5, we believe that this is an interesting factor for us as our reordering algorithm considers the symmetrical pattern of the matrix during the coarsening and reordering phases. Lastly, matrices within the two levels are sorted based on their average number of nonzeros per row.

Additionally, we want to note that matrices from different application areas tend to be placed within a certain category of regular vs. irregular and symmetric vs. nonsymmetric. For example, sparse matrices from the solution of large PDEs utilizing finite-difference or finite-element methods such as those from computational fluid dynamics (atmosmod, StocF-1465), triangulations (de launay), or thermal problems (termal2) tend to be symmetric in pattern and regular. On the other hand, matrices from areas such as circuit simulations (Hamrle3, memchip, FullChip) or graph analysis (wiki-Talk, sz-stackoverflow) tend to be more nonsymmetric and irregular.

For KokkosKernels, cuSPARSE, and MKL, all sparse matrices are first reordered utilizing RCM obtained from MATLAB’s symrcm. As noted before, RCM provides improved convergence for some iterative solvers (e.g., CG) and improves performance due to reducing the stride of irregular accesses. We opt to feed CSR-k with matrices in their natural ordering to demonstrate the efficacy of the Band-k algorithm [2]. CSR5 and TileSpMV are fed matrices in their natural ordering, as the original papers do not specify the use of bandwidth-reducing reorderings. The rationale for this choice is twofold. The first is that CSR5 and TileSpMV are complex enough formats that already look for clusterings of nonzeros for tiles and therefore impose some ordering themselves. This is unlike cuSPARSE, KokkosKernels, and MKL, which use simple formats that can benefit from reordering. The second is that our Band-k algorithm is part of our CSR-k algorithm and we feed CSR-k the same nature ordered matrices, therefore it would be a better comparison as we are directly comparing how we form block structures via super-rows and them using their tiling.

5.4. Test Methodology

For GPU tests, data is copied ahead of time to the GPU, and only the SpMV kernel execution time is measured. This is done to accurately model the behavior of iterative solvers, which should not re-copy the data each iteration. For both CPU and GPU tests, 20 runs are performed and the results are averaged via arithmetic mean. On CPU tests, 5 untimed warmup runs are performed, because MKL appears to take 1-2 iterations before reaching maximum performance.

6. CPU Performance and k Selection

In this section, we verify the ability of CSR-k to improve performance on CPUs. This is necessary as the original paper was printed over eight years ago (2014), and the design of CPUs has changed. In particular, the three design changes have been increased core count on a single socket, different caching structures (e.g., multiple segmented shared caches as in Rome), and different hardware reuse techniques (e.g., newer Intel systems). Additionally, we wish to re-investigate the impact of the selection of the k for CSR-k. In keeping with the format of other heterogeneous formats presentation, we present the performance as the GFlop/s.

6.0.1. CPU Performance

Figure 6 presents the four bar graphs with performance measured in GFlop/s. The top two bar graphs [a] and [b] present the performance on the Intel Ice Lake system for the regular and irregular groups. We divided the symmetric and nonsymmetric sparse matrices within the bar graph with a vertical black dashed bar, and we present the average performance for each method within the category (i.e., within regular or irregular including both symmetric and nonsymmetric) as a horizontal dash line. This system is most like the one the original CSR-k work was presented on. For the regular category, we find that CSR-2 provides the highest average GFlop/s at ~ 44.1 with CSR-3 and CSR5 closely behind at ~ 38.5 and ~ 35.3 (i.e., ~ 14.5% and ~ 24.9% improvement). Overall CSR-2 does better in this group except in a couple of cases such as: 1.) the first five with an average row density of less than three; 2.) the very nonsymmetric Hamrle3; 3.) deb. In the case of the irregular sparse matrices on Ice Lake, the gap between CSR-2 and CSR5 closes with an average of ~ 32.2 GFlop/s and ~ 28.8 GFlop/s, respectively (i.e., ~ 11.8% improvement). In general, we notice that CSR5 is better than CSR-2 in very irregular matrices.
and those with nonsymmetric structures, such as those from the Wikipedia grouping and webbase-1M.

We next consider the performance on the Rome system and CSR5. This system is of importance due to how different it is from the Intel system in terms of cache size and structure. In particular, Rome is set up as a cluster of 16 core complexes (CCXs), each consisting of 4 cores that share an L3 cache. The latency for accessing the L3 cache from a core’s own CCX is very low (i.e., around 39 clock cycles) while accessing a remote L3 can be slower than the main memory. Additionally, Rome has less L1 data cache and L2 cache per core while having over 4x as much L3 cache. We notice that the gap between the performance of CSR-2 and CSR5 is more pronounced on this system. For the category of regular matrices, CSR-2 can obtain an average performance of ∼ 37.2 GFlop/s while CSR5 only obtains ∼ 37.2 GFlop/s (i.e., ∼ 95.7% improvement). Moreover, the only two sparse matrices in this group that CSR5 can outperform CSR-2 on are debr and hamr1e3. We additionally observe better behavior of CSR-2 for the category of irregular matrices on Rome. CSR-2 is able to obtain an average performance of ∼ 22.1 GFlop/s (i.e., ∼ 65.1% improvement) As with the Intel Ice Lake system, CSR5 does seem to handle irregular and nonsymmetric matrices better than CSR-2. However, the performance gap is much smaller on the AMD Rome system with CSR-2 outperforming CSR5 in all cases except for the sparse matrix of circuit5M. Based on these results, we can validate that CSR-k is still a valid method on CPUs. We do note that if the matrix is known to be very nonsymmetric or very irregular, CSR5 would be a better choice in particular on the Intel Ice Lake system.

6.1. Scalability

For completeness, we also present the scalability in terms of speedup relative to MKL for our two CPU systems. The geometric mean of all 64 speedups (i.e., a speedup for each sparse matrix) is presented. This analysis helps to determine if there are unforeseen overheads (e.g., the use of parallel data structures or synchronizations) that may plague an implementation at a different number of cores. Figure 5 presents this scalability study. We observe that on both systems, all SpMV methods are about the same using 4 cores. On both systems, CSR-2, CSR-3, and CSR5 close (i.e., ∼ 8 – 12x) at 16 cores; however, Intel MKL does not do well on the AMD Rome system. When utilizing the full chip, the spread of scalability starts to widen with CSR-2 performing better than CSR5.

6.2. Selection of k

Like the validity of the CPU performance of the original work, the selection of k should also be validated. In the original work, the choice of k is made based on the number of discrete cache levels in the hardware and not on the sparse matrix, which the original work makes based on their own experimental tests. Therefore, the choice of k for our two systems (Ice Lake and Rome) should be 2, based on the observations of the original work. We did additional runs with k = 3 (i.e., CSR-3) to validate if this choice is something that could be set independently of the sparse matrix. Figure 6 presents the performance of CSR-3 for both systems and both categories. From this data, CSR-2 always outperforms CSR-3 on average. On the Ice Lake system, CSR-3 is never able to outperform CSR-2 even with the additional cost of tuning both the super-row and super-super-row size. On the Rome system, CSR-3 does seem to perform better but is still not able to outperform CSR-2. Therefore, we validate the same observation they made for the CPU systems.

In the next section, we present the GPU performance. Based on our algorithm and our view of the CUDA memory system, we likewise predict that CSR-3 will be sufficient. We note that we also test CSR-2 on the GPU, and we find that in a couple of matrices CSR-2 slightly outperforms CSR-3. We do not include all of the CSR-2 results for the GPU in the figures due to readability of the bar graphs but do present the listing of matrices outperformed by CSR-2 in the text. However, the number of sparse matrices that are outperformed by CSR-2 is so few that we would generally recommend CSR-3, and why we presented CSR-3 for GPU as our main algorithm.

7. GPU Performance

In this section, we analyze the performance of CSR-3 on Volta and Ampere GPUs. We tune the super-super-row and the super-row sizes based on the automatic analysis tuning in Section 4. We compare these results to both the CSR representation format in cuSPARSE and KokkosKernels for the Volta and only cuSPARSE on the Ampere due to KokkosKernels’s current compiler limitations. We test against the state of the art format of CSR5 on both Volta and Ampere as this is a true
Figure 6: Performance on CPU
(a) GFlop/s on Volta regular matrices

(b) GFlop/s on Volta irregular matrices

(c) GFlop/s on Ampere regular matrices

(d) GFlop/s on Ampere irregular matrices

Figure 7: Performance on GPU
heterogeneous format. As a replacement for KokkosKernels on Ampere, we test on the state of the art (non-heterogeneous) format of TileSpMV. Similar to the last section, we utilize GFlop/s as our primary measurement of performance.

Figure 7 presents the performance measurements on GPU. Results for the regular and irregular categories are present in 7a and 7b for the Volta system. Again, the average performance for a method within the regular and irregular categories is presented as a dashed line. In the regular category, CSR-3 achieves an average of ~98.4 GFlop/s while CSR5 achieves ~93.0 GFlop/s (i.e., ~5.8% improvement). Similar to CSR-2 vs. CSR5 on the CPU system of Ice Lake, CSR5 does better than CSR-3 on the first five sparse matrices with an average row density of less than three. We also observe that KokkosKernels does well in this group and is the fastest on the next two sparse matrices, i.e., hugetrace-00000 and hugetrace-00000, while CSR-3 does very poorly on these. We believe this is an artifact of how the KokkosKernels implementation is tuned as the CSR-3, CSR5, and cuSPARSE implementations perform very similarly to each other and KokkosKernels is the only outlier. The choice of the best method is much less cut and dry on Volta than in the CPU systems. One example of this is AS365, M6, and NLR where both cuSPARSE and KokkosKernels outperform CSR-3 and CSR5. However, the tables are opposite for CurlCurl_3 and hmr1el3. We also observe that CSR-3 is less sensitive to the nonsymmetric nature of hmr1el3 on this system. Considering the irregular category of sparse matrices on the Volta system, cuSPARSE (~98.2 GFlop/s) and CSR5 (~88.15 GFlop/s) outperform CSR-3 (~47.9 GFlop/s) on average. We note that CSR-3 is particularly bad on irregular sparse matrices with a very low average row density (i.e., the first five matrices). However, we also note that these five matrices have some of the largest maximum nonzero row counts which makes them some of the most irregular matrices. This is likely due to the fact that the selection between GPUSpMV-3 and GPUSpMV-3.5 is based on average row density, so the very dense rows are being computed in serial. A potential avenue for future work could include selecting based on maximum row density for such highly irregular matrices, which would allow for aforementioned dense rows to be computed in parallel. As the average row density increases (and likewise the irregularity decreases) in our test suite, CSR-3 starts to perform better.

Additionally, CSR-2 runs are done to compare the sensitivity of the selection of k (not pictured in the figure). CSR-2 was able to outperform CSR-3 by more than 5% in four cases (wiki-Talk, patents, as-Skitter, debr, and FullChip). Similar to the previous time, CSR-2 outperforms CSR-3 but does not equate to much since the largest outperformance is on sparse matrices that CSR-3 already performs very poorly on. For example, CSR-2 outperforms CSR-3 by 17% on wiki-Talk but this is still not enough to be close to either cuSPARSE or CSR5. Therefore, we conclude that CSR-3 be an ideal choice if the user knew the sparse matrix was regular on the Ampere system.

8. Overall Observations About a Heterogeneous Format

The primary goal of any heterogeneous format is to have a portable format that scales well across multiple different systems. In particular, our goal is to have a format that scales across CPUs and GPUs. As seen in the previous two sections, both CSR5 and CSR-k are not perfect homogeneous formats, and almost all have some limitations as we are optimizing over such a large array of systems and sparse structures. In our observations, we see that CSR5 is limited in its performance on both Ice Lake and Rome CPU systems with CSR-2 outperforming CSR5 by as much as ~95.7% on AMD Rome CPUs for regular matrices and as little as ~11.8% on Intel Ice Lake CPUs for irregular matrices. On GPUs, CSR-3 can still outperform CSR5 but only by a small margin and only in the category of regular sparse matrices. In particular, CSR-3 can outperform CSR5 by at most ~10.5% on the Ampere system for regular matrices. However, CSR-3 is unable to keep up with CSR5 at all in the category of irregular matrices on GPU systems. Therefore, the right choice of which package to use would be based on the primary use of the package. If the choice is for a package that will be used on GPU most often and needs to support various matrix structures, then CSR5 is a clear winner. However, if the choice is for a package within a sparse iterative linear solver designed for PDEs (e.g., CG) that might equally be executed on CPU or GPU then CSR-k makes sense as it has better performance on the CPU systems and slightly better performance than CSR5 on GPU systems for regular matrices that are common in these types of applications.

9. Conclusion

An efficient heterogeneous format for SpMV is required by modern high-performance computing. This format needs to be
easy to tune and provide portable performance across devices. This paper presents CSR-$k$ as a heterogeneous format solution for SpMV, and in particular, for the use on regular matrices, i.e., sparse matrices where the number of nonzeros per row has a variance $\leq 10$. This kind of sparse matrix is common in the solution of PDEs and could be used in a SpMV driven sparse iterative solvers such as CG. This CSR-based format is easy to understand, can be tuned quickly, and can be used as-is by library calls that require a standard CSR format. Moreover, we present a method to tune CSR-3 in constant time for a particular sparse matrix utilizing an autotuned formula model. Using tuned CSR-2, the format method outperforms CSR5 and Intel MKL on Intel Ice Lake and AMD Rome Systems on average over our whole test suite of regular and irregular matrices. This improvement can be as high as $\approx 95.7\%$ against CSR5 on AMD Rome. Our CSR-3 version for GPU outperforms CSR5 by at most $\sim 10.5\%$ on the Ampere systems for regular matrices but fails to outperform for irregular matrices on GPU systems. Therefore, we demonstrated that CSR-$k$ is an ideal heterogeneous format for many-core CPUs and NVIDIA GPUs when dealing with regular matrices that tend to be symmetric or close to symmetric in their sparsity pattern.

Acknowledgement
This work was made possible in part by support from the Alabama Supercomputer Authority, Sandia National Laboratories, and NSF2044633. This work used the Extreme Science and Engineering Discovery Environment (XSEDE), which is supported by National Science Foundation grant number ACI-1548562.

References
[1] pOSKI: Parallel optimized sparse kernel interface. URL [bebop.cs.berkeley.edu/poski/]
[2] The effect of ordering on preconditioned conjugate gradients. BIT Numerical Mathematics, 29:635–657, 1989.
[3] José I. Aliaga, Hartwig Anzt, Thomas Grützmacher, Enrique S. Quintana-Ortí, and Andrés E. Tomás. Compression and load balancing for efficient sparse matrix-vector product on multicore processors and graphics processing units. Concurrency and Computation: Practice and Experience, page e6515.
[4] Stephen T. Barnard, Alex Pothen, and Horst Simon. A spectral algorithm for envelope reduction of sparse matrices. Numerical Linear Algebra with Applications, 2(4):317–334, 1995.
[5] Shizhao Chen, Jianbin Fang, Donglin Chen, Chunfu Xu, and Zheng Wang. Adaptive optimization of sparse matrix-vector multiplication on emerging many-core architectures. In 2018 IEEE 20th International Conference on High Performance Computing and Communications; IEEE 16th International Conference on Smart City; IEEE 4th International Conference on Data Science and Systems (HPCCC/SmartCity/DSS), pages 649–658, 2018.
[6] E. Cuthill and J. McKee. Reducing the bandwidth of sparse symmetric matrices. In Proceedings of the 1969 24th National Conference, ACM ’69, page 157–172, New York, NY, USA, 1969. Association for Computing Machinery. ISBN 9781450374934.
[7] Timothy A. Davis and Yifan Hu. The university of florida sparse matrix collection. ACM Trans. Math. Softw., 38(1), dec 2011. ISSN 0098-3500.
[8] Timothy A Davis, Sivasankaran Rajamanickam, and Wissam M Sid-Lakhdar. A survey of direct methods for sparse linear systems. Acta Numerica, 25:383–566, 2016.
[9] Ryan Eberhardt and Mark Hoemmen. Optimization of block sparse matrix-vector multiplication on shared-memory parallel architectures. In 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pages 663–672, 2016.
[10] H. Carter Edwards and Christian R. Trott. Kokkos: Enabling performance portability across manycore architectures. In 2013 Extreme Scaling Workshop (xsw 2013), pages 18–24, 2013.
[11] István R egie and Mike Giles. Efficient sparse matrix-vector multiplication on cache-based gpus. In 2012 Innovative Parallel Computing (InPar), pages 1–12, 2012.
[12] Alan George and Joseph W. Liu. Computer Solution of Large Sparse Positive Definite Systems. Prentice Hall Professional Technical Reference, 1981. ISBN 0131652745.
[13] Michael A. Heroux, Padma Raghavan, and Horst D. Simon. Parallel Processing for Scientific Computing. Society for Industrial and Applied Mathematics, 2006.
[14] Humayun Kabir, Joshua Dennis Booth, and Padma Raghavan. A multilevel compressed sparse row format for efficient sparse computations on multicores. In 2014 21st International Conference on High Performance Computing (HiPC), pages 1–10, 2014.
[15] Humayun Kabir, Joshua Dennis Booth, Guillame Aupy, Anne Benoit, Yves Robert, and Padma Raghavan. STS-$k$: A multilevel sparse triangular solution scheme for numa multicores. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC ’15, New York, NY, USA, 2015. Association for Computing Machinery. ISBN 9781450337236.
[16] David Kincaid, Thomas Oppe, and David Young. Itpackv 2d user’s guide. URL [https://web.ma.utexas.edu/CNA/ITPACK/manuals/Itpack2d/]
[17] Orhan Kislal, Wei Ding, Mahnud Kademir, and Ilteris Demirkiran. Optimizing sparse matrix vector multiplication on emerging multicores. In 2013 IEEE 6th International Workshop on Multi-/Many-core Computing Systems (MuCoCoS), pages 1–10, 2013.
[18] Weifeng Liu and Brian Vinter. CSR5: An efficient storage format for cross-platform sparse matrix-vector multiplication. In Proceedings of the 29th ACM on International Conference on Supercomputing, ICS ’15, page 339–350, New York, NY, USA, 2015. Association for Computing Machinery. ISBN 9781450335591.
[19] Marco Maggioni and Tanya Berger-Wolf. Addell: An adaptive warp-balancing ell format for efficient sparse matrix-vector multiplication on gpus. In 2013 42nd International Conference on Parallel Processing, pages 11–20, 2013.
[20] Yuyao Niu, Zhengyang Lu, Meichen Dong, Zhaojun Jin, Weifeng Liu, and Guangming Tan. Tilespmv: A tiled algorithm for sparse matrix-vector multiplication. In Proceedings of the 2022 ACM/SPEC on International Conference on Performance Computing. ACM, April 2022.
[21] Richard Vuduc, James Demmel, and Kathrine Yelick. OSKI: A library of automatically tuned sparse matrix kernels. Journal of Physics Conference Series, 16:521–530, 01 2005.
[22] Richard W. Vuduc and Hyun-Jin Moon. Fast sparse matrix-vector multiplication by exploiting variable block structure. In Proceedings of the First International Conference on High Performance Computing and Communications, HPCC’05, page 807–816, Berlin, Heidelberg, 2005. Springer-Verlag. ISBN 3540293011.
[23] Richard Wilson Vuduc and James W. Demmel. Automatic Performance Tuning of Sparse Matrix Kernels. PhD thesis, 2003. AA3121741.
[24] F. Vázquez, G. Ortega, J.J. Fernández, and E.M. Garzón. Improving the performance of the sparse matrix vector product with gpus. In 2010 10th IEEE International Conference on Computer and Information Technology, pages 1146–1151, 2010.
[25] Samuel Williams, Andrew Waterman, and David Patterson. Roofline: An insightful visual performance model for multicore architectures. Commun. ACM, 52(4):65–76, April 2009. ISSN 0001-0782.