Design of a Memory Array Using Tail Transistor and Sleep Transistor Based 7T SRAM with Low Short Circuit and Standby Power

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Abstract. The display hardware concentrates on planning low power control gadgets due to the utilization of versatile battery-powered gadgets. Ultra low energy process of memory clusters has ended up undying due to its uses in low voltage calculation and communications. Stable SRAM process is valuable for the success of low-power due to parameter variations in scale-down technologies. In expansion to control utilization, the SRAM's get to time is another complex parameter due to the inevitable exchanging exercises utilized for distinctive squares, say SRAM cell, get to NMOS transistors, NMOS preload transistors, a yield sense enhancer and both decoders. It has been appeared that the tail transistor-based 6T SRAM cluster comes up short to realize solid standby control and less delay process. The proposed inactive arbitrary get to memory (SRAM) plan gives an approach towards diminishing the standby control scattering. The design uses a sleep transistor which helps in limiting the standby power by preventing the whole cell from working for unwanted operations. It is eligible for low power applications due to the supply voltage being 1.8V. The designed SRAM cell has single-ended write and reads operations, which can also reduce the total power dissipation and the tail transistor reduces the short circuit energy consumption. The design is verified with Cadence (45nm) and the power estimated as 4.6789pW, which is 78.2% of ordinary 6T SRAM block.

Keywords—static power dissipation; sleep transistor; tail transistor; short circuit power dissipation; sub-threshold current.

1. INTRODUCTION

Memories are the foremost valuable square in VLSI blocks. These are divided into two as ROM and RAM. The first one may be a straightforward based on transistor, it keeps information moreover without control circumstance as well with structure of transistors. Arbitrary get to memory basically contrasts from Studied as it were memory. No one can process any single process without the usage of Random access memory. RAM is further broken down into two forms. Energetic Slam employments a capacitor to spare information, charge within the capacitor can store a little data. Henceforth this begins rotting. In a noted moment slot the potential esteem gets to be low edge voltage of the switch. So, Measure needs a reviving circuit, which occasionally refreshes the put away voltage within the capacitor until that information is taken for the process and information is constrained. Inactive Slam employments as it were transistors to keep information (as a match of inverters), which doesn’t use any additional blocks. Some more issues related with the control dissemination in SRAM memory. To begin with one is as it were a data sequence for both studied and compose processes, which squandered the control when as
it were one process takes put as control of two operations. Moment one is superfluous exchanging action of all transistors processes, it disseminates high energetic control.

![Figure 1. Classic SRAM diagram](image)

One final hectic problem is brief circuit control dissemination, it happens while supply is directed specifically with VSS for a little sum of time being exchanged ON for a minor time period when move of one state to another. Control dissemination of this setup will be decreased by lessening this 3 problems a small. A customary classic setup is appeared in below diagram.

| Process   | Input | Output |
|-----------|-------|--------|
| 'low'     | 0     | 1      | 1      | 0      |
| Write 'high' | 1     | 0      | 0      | 1      |

Fundamental process of which is organized in below underneath (Table 1). Which will be carried out by distinctive plan methods, from this method or any other method utilized in a plan which control dissemination sum is diminished. In this paper, we use three techniques, i) separation of read and write operations ii) tail transistor and iii) sleep transistor.

2. RELATED WORK

An SRAM cell plan is characterized by three key parameters, number of transistors, plan innovation and the strategy utilized. Each plan comprises of a particular plan to lower the region, control, and delay parameters and these moreover shift the number of transistors, sometime transistor counts do not differ, and modifications are made in traditional SRAM cells. New design also needs improved new technology if available, at present many VLSI projects done with the help of tools like Cadence and Tanner with 45nm technology.

A moo control strategy was presented in 1993 centering on high-speed inactive Slam plans and fast, slow active circuit plans counting CMOS and BiCMOS are depicted. Poly silicon PMOS-load cells as a very useful cell of quick SRAMs but extra forms needed are yet a overwhelming issue for system of in-built Memories [11,12]. Use of slow and fast-voltage circuits, its activity timereduced near to BiCMOS SRAM. In any case, ECL helping circuits with CMOS blocks are perfect way of the most perfect path in very quick get to slots, in spite of the fact that it yet needs to control scattering. We
may choose is highly accessible quick get to tall control scattering or slower get to with moo control dissemination.

Inactive control utilization administration in CMOS Memories was proposed in 2001 centered on the particular precharge concept in arrange to decrease energetic control utilization. This method can diminish definitely inactive control utilization. Exploratory comes about gotten from a test circuit are given and compared to one utilizing substrate back predisposition. Gotten picks up are detailed for ROM, single and twofold port SRAM Memories. Specific precharge isn't as it were appropriate for energetic control decrease but moreover a great approach for inactive control diminishment.

In [5], conducting PMOS technique is used with 8Transistor design. Conducting PMOS helps in avoiding read failure and in [19], sleep transistor is used with 9 Transistor design. In standby mode, all 6 transistors of SRAM are switched and dissipate power, which is prevented by using extra 2 sleep transistors. In [10,16], sleep transistor logic was combined with the conducting PMOS design, which reduces the static power consumption along with successful read process.

In [1], supply voltage of 1V is used. Supply voltage is directly proportional to the power dissipation so, reduced power supply helps in low power VLSI design. In[3], Schmitt trigger design is used in order to reduce power consumption. In [13], 10Transister type with separated read and write operations is done as DCVSL design in order to reduce bit line leakage and reduce short circuit power by 18.11%.

In [4], tail transistor design type is used as modified 6T SRAM design by removing an NMOS from a cross coupled inverter set and using it as tail transistor. Whenever the transistors go to C region, both NMOS and PMOS transistors turn ON so VDD is directly connected to ground and creates a small short circuit power dissipation. By using tail transistor and input as EX-ORed output of read and write enable lines, short circuit power dissipation is reduced [9,20].

In [1,14], dual threshold voltage technique is employed with 7 Transistor design. To switch on NMOS and PMOS transistors, only 0.7 V and 4.3 V is enough respectively, the extra voltage given switched transistors unnecessarily. Dual threshold voltage is the concept of one supply is 0 to 2.5 V and another supply voltage is 5 to 2.5 V, which reduces the unnecessary switching actions of transistors hence reducing the power.

3. PROPOSED WORK

Using tail transistor reduced the short circuit power consumption and sleep transistor reduces the standby power dissipation.

Figure 2. Proposed 7T SRAM
At a small interval if, both PMOS and NMOS transistors turned ON then the Supply voltage is directed to VSS [17,22]. This caused the small but an effective power consumption called short circuit power consumption. In the tail transistor method, an NMOS is placed as a tail transistor above the ground and input of this NMOS is given as the output of the EX-OR gate, whose inputs are read and write lines [7,15]. If the inputs of the EX-OR gate are same and output is zero, which turned OFF the tail transistor [8]. Similarly due to the separation of read and write operations, the memory process is effectively regulated as well. The usage of sleep transistor is to turned OFF the complete cell for unnecessary operations by cutting VDD and ground. When isolated studied and compose operations, the control dissemination is diminished as nearly half of the control dissemination when the bit line utilized both get to transistors for studied and compose operations additionally one process should get to as it were one get to transistor to switch get to make less time of the memory process.

3.1. SRAM Array:

SRAM is utilized to keep a few information, comprises some amount of bits to specific get to slot.

![Figure 3.4x4 SRAM Array](image)

A Static RAM cell has 2 NOT gates and 2 get to transistors (totally 6) will save as it were one word of information interior it. The number of words have to be keep considerable sum of Static RAM block is utilized. This Static RAM blocks were put as a set as much required since getting to cluster is a straightforward handle. Consideration of a word cell is did by two dimensional strategy as row and push, this is appeared within the figure 3.

3.2. Sense amplifier:

Consider huge memory capacity as a rule the expanded bit-line parasitic capacitance. Sense enhancers are primarily utilized to study the substance of Smash, Measure and SRAM cells. They are exceptionally delicate to clamor and their plan suggests that they will give satisfactory commotion edges and give great quality of information that speak to the substance of a specific memory cell. There are two categories of sense intensifiers. The inactive sense intensifiers primarily utilized to distinguish rationale within the inactive RAMs and SRAMs and the energetic sense intensifiers basically utilized to spare vitality when moo control dissemination is required. Quick sense intensifiers are critical for accomplishing moo latency in numerous circuits, the foremost common space being bit-line perusing in Memories. With the approach of sub micrometer CMOS chips, interconnection is
getting to be a major source of on-chip delay, and quick sense enhancers are too likely to be required, e.g. as repeaters for high-speed signals which must navigate huge chips.

3.3. Decoder:

Decoder is used to reduce the number of input and output pins used in a chip. Decoder produces '2n' outputs from 'n' input lines. A simple block of decoder is shown in the below figure 4. Two different decoder blocks are used in the SRAM array design are row decoder and column decoder. Column decoder is incorporated with column mux, which also connected with sense amplifier. So, column decoder also sense output when read operation.

![Figure 4. Decoder](image)

Row decoder is simply connected with input address line, which only used to select the input row address.

3.4. Symbol Creation:

Symbol creation is used to reduce the complexity of creating schematic of big architectures. Symbols need to create for SRAM array design are inverter, AND gate, SRAM cell and sense amplifier.

![Figure 5. Symbol of 6T SRAM using tail](image)

![Figure 6. Symbol of proposed 7T SRAM transistor](image)
Figure 5 and 6 shows the schematic of 6T SRAM using tail transistor and proposed 7T SRAM respectively. Figure 7 shows the schematic of SRAM array.

4. SCHEMATIC IN CADENCE

Cadence could be a VLSI circuit investigation device for planning full custom coordinate’s circuits incorporates schematic passage, behavioral modeling, circuit recreation, custom format, physical confirmation, extraction and back explanation. It is utilized basically for analog blended flag, RF and standard cell plans but too memory and FPGA plans. RTL and GDS-II execution and signoff: Sort amalgamation, Joules control investigation, Innovus put and course, tempus timing signoff, Voltus control keenness and modus programmed test design era.

Figure 8. 4×4 SRAM array Schematic

The major advantage of the Cadence tool is only need to design the graphic model of a circuit in transistor level instead of verilog or VHDL code like another design tools (Ex: Xilinx, Quartus). The ultimate structure of a four×four SRAM setis appeared within the figure 8.

5. RESULT AND DISCUSSION

While input/output is empower, type in information input is composed within the Static RAM cell at the apportioned storage cell taken by push and column multiplexer. For simple understanding, compose and examined processes are done progressively in one line access. When perused process, the information type in within the past step is studied and held that same esteem until the following studied process. The ultimate yield appeared within below diagram, what appears the output type in
empower, Information in, push decoder inlets (r0, r1), column decoder inlets (c0, c1) and Information out. Control of the cluster plan is done by CADENCE by the different transistors accessible within the plan for all set of the inlet, push and column decoder inlets and yields.

![Figure 9. Result Waveform](image)

Delay is calculated between different parameters and the basic delay between the information input and information yield is organized between customary 6T SRAM and adjusted 6T SRAM.

|                      | Power     | Delay (μs) |
|----------------------|-----------|------------|
| Basic SRAM           | 5.9832pW  | 193        |
| 6T SRAM Using Tail Transistor | 4.6789pW  | 123        |
| Proposed 7T SRAM     | 4.0789pW  | 103        |

The table appears that the control utilization is decreased by 21.8% and delay is diminished by 36.26% in 6T SRAM utilizing tail transistor. In proposed 7T SRAM plan control utilization is diminished by 31.8% and delay is decreased by 46.62%.

6. CONCLUSION

This plan gives a moo control SRAM plan with 7 transistors versus the customary 6T SRAM plan. A 4x4 memory cluster too made utilizing the proposed 7T SRAM cell. The plan is recreated utilizing Cadence (45nm) and the control evaluated as 4.6789pW, which is 68.2% of routine 6T SRAM plan. End of the upgrades are ready to grow the memory cluster to more number of proposed 7T SRAM cells, supplant conventional FET with progressed FETs like FINFET and CNTFET to diminish the control utilization and to make strides the innovation to less than 45nm.
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