NGEMM: OPTIMIZING GEMM FOR DEEP LEARNING VIA
COMPILER-BASED TECHNIQUES

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ABSTRACT

Quantization has emerged to be an effective way to significantly boost the performance of deep neural networks (DNNs) by utilizing low-bit computations. Despite having lower numerical precision, quantized DNNs are able to reduce both memory bandwidth and computation cycles with little losses of accuracy. Integer GEMM (General Matrix Multiplication) is critical to running quantized DNN models efficiently, as GEMM operations often dominate the computations in these models. Various approaches have been developed by leveraging techniques such as vectorization and memory layout to improve the performance of integer GEMM. However, these existing approaches are not fast enough in certain scenarios.

We developed NGEMM, a compiler-based GEMM implementation for accelerating lower-precision training and inference. NGEMM has better use of the vector units by avoiding unnecessary vector computation that is introduced during tree reduction. We compared NGEMM’s performance with the state-of-art BLAS libraries such as MKL. Our experimental results showed that NGEMM outperformed MKL non-pack and pack version by an average of 1.86x and 1.16x, respectively. We have applied NGEMM to a number of production services in Microsoft.

Keywords Deep Learning · Training · Inference · Low-Precision · GEMM · Compiler

1 Introduction

In the past few years, deep neural networks (DNNs) have demonstrated great success in various domains such as natural language processing (Howard & Ruder, 2018; Radford et al., 2018), speech recognition (Deng et al., 2013; Anwar et al., 2015) and computer vision (Simonyan & Zisserman, 2014; Szegedy et al., 2015). The increasing size and complexity of DNN models have become an impediment to the deployment of these models on edge devices where latency is often a hard requirement. Even for cloud platforms like Azure, AWS and Google Cloud, where more computational resources are available, complex models such as BERT (Devlin et al., 2018) may still cause long service time and high cost for both training and inference.

Quantization has emerged to be an effective way to significantly improve the performance of DNN models by utilizing low-bit computations (Krishnamoorthi, 2018; Jacob et al., 2018; Rastegari et al., 2016; Han et al., 2015; Lin et al., 2016). By converting the weights and activations of a DNN model from high-precision floating point values to low-precision representations, quantization is able to reduce the model size and hence requires less memory for running the model. Smaller memory footprint can have better cache behavior, because more intermediate computation results can be kept in the cache for re-use. Moreover, computations on lower numerical representations such as 8-bit integers almost always need fewer clock cycles on contemporary general purpose CPUs and GPUs, compared with their high precision counterparts such as 32-bit floating point.
GEMM operations often dominate the computation for training or inferencing DNN models (Jia, 2014). Consequently, high performant integer GEMM has great impact to the efficiency of quantized DNN models, where high-precision floating point matrix elements are converted to low-bit such as 8-bit integers. Recently, there have been increasing efforts in developing high-performance low-precision GEMM libraries, such as FBGEMM (Daya Khudia & Deng., 2018), gemmlowp (Jacob et al., 2017) and MKL (Intel, 2019), where techniques such as vectorization, memory layout and various tiling schemes (Goto & Geijn, 2008; Van Zee & Van De Geijn, 2015) are applied to optimize GEMM computation. However, they are still not fast enough in certain scenarios.

We developed NGEMM, an optimized GEMM implementation for DNN models based on compiler techniques. NGEMM can provide high performance GEMM computation with different low-precision representations for various target machines. Our experimental results showed that NGEMM outperformed MKL non-pack and pack version by an average of 1.86x and 1.16x respectively. NGEMM has been used in a number of Microsoft production services (Chang et al., 2018; Microsoft, 2018).

In the rest of the paper, we will be focusing on Intel X86 CPUs, which are ubiquitous in modern computing systems. However, our methodology is widely applicable and not just specific to Intel CPUs.

## 2 Background

In this section, we briefly discuss the conventional approach to implementing low-precision GEMM.

### 2.1 Conventional Approach

Figure 1 shows the conventional approach (Rodriguez et al., 2018) to conduct low-precision GEMM. Matrix A is the weight matrix with size of \([M \times K]\), and is typically determined from the training. Matrix B is \([N \times K]\) input matrix, which contains the input data. Matrix C \([M \times N]\) is the result. In low-precision GEMM, matrices A and B are the ones with low numerical precision such as 8- or 16-bit, while matrix C is in higher precision like 32-bit. Throughout the example below, we will use unsigned 8-bit integers for matrix A and signed 8-bit integers for matrix B. Other integer types have similar processes.

\[^1\text{NGEMM is used as external custom functions for specific integer BLAS routines in our Halide-based inference engine (Chang et al., 2018), and is implemented as a rewriting pass in code generation of Nuphar Execution Provider in ONNX Runtime (Microsoft, 2018).}\]
In Figure 1, phases ①, ② and ③ are the typical phases to perform GEMM vector reduction, which computes the dot product of one row from matrix A and one column from matrix B to produce one element of matrix C. Phase ① shows the process of converting low-precision values to higher precision. VPMADDUBSW takes two 8-bit integer vectors, \( \mathbf{a}_{u8} = [a_0, a_1, ..., a_{i-1}] \) and \( \mathbf{b}_{u8} = [b_0, b_1, ..., b_{j-1}] \), which contain unsigned and signed integers loaded from matrix A and B, respectively. It then multiplies each unsigned 8-bit integer in \( \mathbf{a}_{u8} \) and the corresponding signed 8-bit integer in \( \mathbf{b}_{u8} \), produces a signed 16-bit integer. Lastly, it adds adjacent pairs of the 16-bit integers to generate another vector \( \mathbf{e}_{16} \):

\[
\mathbf{e}_{16} = [e_0, e_1, ..., e_{j-1}] = [a_0 \times b_0 + a_1 \times b_1, ..., a_{i-2} \times b_{i-2} + a_{i-1} \times b_{i-1}]
\]

After that, VPMADDWD takes \( \mathbf{e}_{16} \) and a unit vector \([1, 1, ..., 1]\) to perform horizontal reduction, which produces a signed 32-bit integer vector \( \mathbf{e}_{32} \):

\[
\mathbf{e}_{32} = [e_0, e_1, ..., e_{k-1}] = [e_0 + e_1 + e_2 + e_3, ..., e_{j-1} + e_{j-2}]
\]

\[
= [a_0 \times b_0 + a_1 \times b_1 + a_2 \times b_2 + a_3 \times b_3, ..., a_{i-4} \times b_{i-4} + a_{i-3} \times b_{i-3} + a_{i-2} \times b_{i-2} + a_{i-1} \times b_{i-1}]
\]

where each 32-bit value in \( \mathbf{e} \) comes from four 8-bit values, thus \( k = j/2 = i/4 \). The result of phase ① is a 32-bit integer vector \( \mathbf{e}_{32} \) with size of \( k \).

Note that the vector width (i.e. the number of cubes in the vector) in Figure 1 is just for illustration purpose. The actual width depends on the data type and target machine. For example, on an AVX-2 machine, where the vector width is 256 bits, the vector size \( k \) of \( \mathbf{e}_{32} \) is 8. In contrast, for an AVX512 machine, \( k \) becomes 16.

Phase ② repeats the computation in Phase ① multiple times for the rest of the bytes of the same row from matrix A and the same column from matrix B. Each repetition produces a 32-bit vector \( \mathbf{e}_{32} \), which will be accumulated using instruction VPADDD. This phase gives us: \( \mathbf{e} = \sum_{k} \mathbf{e}_{32} \).

Phase ③ sums all of the 32-bit integers within the vector using tree-reduction to generate one final element in matrix C (shown as the black cube). There are different ways to achieve this phase depends on instructions used. One approach is to use VPHADD, which is the instruction to horizontally add adjacent pairs of 32-bit integers. Depending on vector width, multiple VPHADD are needed to accumulate the integer values and generate the final value. The other approach is to utilize the VPSHFD instruction, which shuffles the 32-bit integers within the vector, with following VPADDD to accumulate corresponding values to generate the final result.

Finally, phase ① ② ③ are applied to all rows of matrix A and columns of matrix B to generate the whole matrix C. Although these phases change the common reduction order of GEMM, they are typically applicable in integer computation unless overflow happens due to a very large \( K \), which is rare for most DNN models, where \( K \) ranges from 100s to 1000s.

3 Methodology

3.1 Alternative Approach

The conventional approach described in the previous section is straightforward to perform low-precision GEMM computation. However, it is not optimal because the vector units are not fully used during the tree-reduction phase ③. Therefore, we present NGEMM, which has better use of the vector units by avoiding non-efficient vector computation such as tree-reduction.

Figure 2 shows the details of our NGEMM. We use the same configuration as that we used for the conventional approach: matrix A is the \([M \times K]\) weight matrix, matrix B is the \([N \times K]\) input matrix, and matrix C \([M \times N]\) is the result matrix. Matrices A and B are in low numerical precision, and matrix C has 32-bit full precision.

Similar to phase ① in the conventional approach, phase ① computes partial results from two vectors, \( \mathbf{a}_{u8} = [a_0, a_1, ..., a_{i-1}] \) and \( \mathbf{b}_{u8} = [b_0, b_1, ..., b_{j-1}] \), using VPMADDUBSW and VPMADDWD. However, the shapes of the loaded data are different from the conventional approach even with the same vector length. In this illustration, its shape is \([4 \times 2]\), which is determined by the vector width and the width of horizontal reduction in practise. For example, the shape is \([8 \times 4]\) for AVX2. Because both dimensions are shorter than the vector width, loads of \( \mathbf{a}_{u8} \) access non-contiguous memory, which may compromise memory bandwidth. To resolve the issue, we apply data layout transformation (see Sec 5.1.1) to force \( \mathbf{a}_{u8} \) to be fully contiguous in memory.
Furthermore, because vector $b_{i8}$ has shorter length than $a_{u8}$ ($p < i$), we broadcast $b_{i8}$ to $b'_{i8}$:

$$b'_{i8} = [b_0, b_1, \ldots, b_{p-1}, b_0, b_1, \ldots, b_{p-1}]$$

where $b'_{i8}$ has the same width as $a_{u8}$. For example, if $p = 4$, then $b'_{i8} = [b_0, b_1, b_2, b_3, b_0, b_1, b_2, b_3]$. Consequently, $c'_{i16}$ and $e'_{i32}$ will be as follows:

$$c'_{i16} = [c_0, c_1, c_2, \ldots, c_{j-1}]
= [a_0 \ast b_0 + a_1 \ast b_1, a_2 \ast b_2 + a_3 \ast b_3, \ldots,
\ast a_{i-4} \ast b_0 + a_{i-3} \ast b_1, a_{i-2} \ast b_2 + a_{i-1} \ast b_3]$$

$$e'_{i32} = [e_0, e_1, e_2, \ldots, e_{k-1}]
= [a_0 \ast b_0 + a_1 \ast b_1 + a_2 \ast b_2 + a_3 \ast b_3, \ldots,
\ast a_{i-4} \ast b_0 + a_{i-3} \ast b_1 + a_{i-2} \ast b_2 + a_{i-1} \ast b_3]$$

Figure 2 shows an example of $p = 2$ (two elements during load of matrix B) for simplicity, which is the 16-bit scenario:

$$a'_{i16} = [a_0, a_1, \ldots, a_{i-1}, a_i]$$
$$b'_{i16} = [b_0, b_1, \ldots, b_{0}, b_1]$$
$$c'_{i32} = [c_0, c_1, c_2, \ldots, c_{j-1}]
= [a_0 \ast b_0 + a_1 \ast b_1, a_2 \ast b_2 + a_3 \ast b_3, \ldots,
\ast a_{i-4} \ast b_0 + a_{i-3} \ast b_1, a_{i-2} \ast b_2 + a_{i-1} \ast b_1]$$

where only VPMADDWD is required in phase ❶ to accumulate to 32-bit.

The second phase ❷ accumulates all the partial results of $e'_{i32}$ to directly form the final result vector in matrix C.

Figure 2 also shows the two more partial results obtained by applying phases ❶ and ❷ to the same part of A but different two vectors of B. The same computation will be applied to the entire A and B and obtain the final result matrix C.
Compared with phases ➀ ➁ ➂ of the conventional approach, our approach only has phases ➀ and ➂ but missing the tree-reduction phase, which is implicitly finished through the vector additions in phase ➂.

Our presented approach is not limited to GEMM operations, but benefits other similar computations such as GEMV. Moreover, it is also applicable to GEMM operations with other types such as signed 16-bit or unsigned 8-bit integers.

It is worthwhile to mention that Intel adopted similar approach in MKL (Andres Rodriguez, 2018), which is contemporary work with our NGEMM.

### 3.1.1 Data Layout

We describe the data layout used by our approach in detail. The layout is mainly for the weight matrix in a DNN model, e.g. matrix A in our examples. Therefore, data marshalling can often be performed offline. For those uncommon cases where both matrices are inputs, we can simply perform online packing with extra overhead.

Figure 3 and Figure 4 demonstrates the two-level hierarchy of the layout used in NGEMM. Figure 3 shows various inner layouts in NGEMM, where the top row display the original vector access. Assuming the memory address grows horizontally, the original vector loads the contiguous elements from the memory. Vector width \( w \) depends on hardware instructions and data types as displayed in Figure 3:

\[
\frac{\text{InstructionWidthInBits}}{\text{DataTypeInBits}} = \begin{cases} 
\text{InstWidth}_{\text{AVX2}}/\text{Integer}_{8\text{bit}} = 32 \\
\text{InstWidth}_{\text{AVX2}}/\text{Integer}_{16\text{bit}} = 16 \\
\text{InstWidth}_{\text{AVX512}}/\text{Integer}_{8\text{bit}} = 64 \\
\text{InstWidth}_{\text{AVX512}}/\text{Integer}_{16\text{bit}} = 32 
\end{cases}
\]

The bottom row draws the inner layout, which determines the data access pattern for the matrix. Instead of accessing data from a single row or column, inner layout will first access \( h \) elements along \( K \) dimension and then move to next row, and repeat this process \( v \) times along \( M \) dimension. This kind of memory access forms a small zigzag pattern, which is known as Morton code (Morton, 1966). Usually, \( h \) and \( v \) are determined by hardware instructions and data type:

\[
h = \begin{cases} 
4 & \text{when 8bit integer} \\
2 & \text{when 16bit integer} 
\end{cases} \quad v = \frac{w}{h} = \begin{cases} 
8 & \text{when AVX2} \\
16 & \text{when AVX512} 
\end{cases}
\]

The size of \( h \) simply implies the number of elements needed to be accumulated to a single 32-bit value in phase ➀.

Figure 4 illustrates the outer layout pattern in NGEMM for weight matrix. The outer layout can be combined with loop optimizations such as loop tiling to deliver better performance. Loop tiling is a classic loop transformation technique to maximize parallelism and improve cache locality (Hong et al., 2016; Bao et al., 2017a,b). It has been widely adopted in various BLAS libraries to optimize intensive computation such as GEMM.

Figure 4(a) shows the outer layout without loop tiling applied, which iterate the inner layout pattern first through \( M \) dimension and then \( K \) dimension for the whole matrix. It is worth mentioning that if columns or rows are not multiple of \( h \) or \( v \), we simply pad 0-element, respectively.

Figure 4(b) shows the tiling with a tile size \( tk \)-by-\( tm \) combined with the layout for matrix A, where \( < tm, tn, tk > \) denote tiling sizes along \( < M, N, K > \) dimension of the GEMM. In our tiling scheme, \( tk \)-by-\( tm \) typically contains multiple \( h \)-by-\( v \). Thus the tiling size selection of \( < tm, tn, tk > \) becomes \( \beta v, tn, \alpha h > \), where \( tn \) is the tiling size along dimension \( N \). The outer layout then is to iterate the tile pattern through the whole matrix.

Moreover, we also apply inter- and intra-tile level optimizations. For inter-tile level, we perform loop unrolling to increase locality and reduce loop control overhead within a tile. For intra-tile level, different loop permutation can
be used, which corresponds to the outer layout iterate order described previously. Overall, the loop tiling size and permutation are a typical search-space-exploration problem, which can be solved by techniques such as auto-tuning.

### 3.2 Latency Analysis

In this part, we perform the latency analysis between the conventional approach and our NGEMM. Note, here, we only considers the computation cost, but ignores the cost of loads/stores, since after data layout transformation, memory accesses in the both methods have become contiguous.

Assume the matrix sizes are the same as previous section, i.e. $C_{M \times N} = A_{M \times K} \times B_{K \times N}$ with vector width $w$. The latency of the conventional approach can be calculated as follows:

\[
\text{Latency}_{\text{convention}} = M \times (K \frac{w}{w} \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2})) + \text{latency}(\mathbb{3})) \\
= M \times K \frac{w}{w} \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2})) + M \times (c_1 \log(w))
\]

where $\text{latency}(\mathbb{1})$ and $\text{latency}(\mathbb{2})$ are the total cost for phase $\mathbb{1}$ and $\mathbb{2}$ in the conventional approach respectively. Here, $c_1 \log(w)$ is the latency cost of tree-reduction computation $\text{latency}(\mathbb{3})$, and $c_1$ is constant parameter.

For our NGEMM with layout size $h \times v = w$, the latency is as follows:

\[
\text{Latency}_{\text{NGEMM}} = \frac{M}{w} \times \frac{K}{h} \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2})) \\
= M \times \frac{K}{w} \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2}))
\]

where latency(\mathbb{1}) and latency(\mathbb{2}) are the time cost of phase \mathbb{1} and \mathbb{2} in NGEMM. The speedup ratio between these two can be expressed as:

\[
\text{ratio}_{\text{speedup}} = \frac{\text{Latency}_{\text{convention}}}{\text{Latency}_{\text{NGEMM}}} = \frac{K/w \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2})) + (c_1 \log(w))}{K/w \times (\text{latency}(\mathbb{1}) + \text{latency}(\mathbb{2}))}
\]

(1)

where phases of \mathbb{1} \mathbb{2} and \mathbb{1} \mathbb{2} have the same latency cost, and their latency can be noted as $c_2$. Then equation (1) can be expressed as:

\[
\text{ratio}_{\text{speedup}} = 1 + \frac{c_1 \log(w)}{K/w \times c_2} = 1 + c_3 \cdot \frac{\log(w)}{l}
\]

(2)
where \( l = K / w \) represents the reduction dimension in the step of vector width of matrix multiplication, \( w \) is the vector width and \( c_3 = c_1 / c_2 \) is constant parameter.

From equation (2), we can observe that the speedup is relevant to reduction dimension and vector width. The longer vector width and the shorter reduction dimension will result in better speedup. It is worth mentioning that the trend of increasing vector width \( w \) continues in new generation of processors.

4 Implementation

We implemented single-threaded NGEMM by leveraging TVM (Chen et al., 2018) tensorize schedule primitive that replaces partial computation code with the corresponding intrinsics in LLVM (Lattner & Adve, 2004). It can be easily extended to support multi-threading by parallelizing the outermost loop. We modified TVM code to properly handle tail condition during code generation, which is important for certain loop transformation techniques (Bao et al., 2016a; Bao, 2018). Furthermore, we added several LLVM intrinsics that were not supported by TVM. It is worthwhile to mention that our NGEMM is not limited to TVM. The same techniques can be implemented in other compiler-based frameworks (Rotem et al., 2018; Google, 2019).

Layout The layout of the weight matrix has been prepacked offline, and the marshalled matrix is fed as a constant initializer to the inference runtime. NGEMM generates different layouts for the weight matrix based on numerical precision requirements and supported instruction sets.

Loop Optimization The optimal loop tiling sizes and permutation orders are determined through compiler auto-tuning. NGEMM generates the best choice based on matrix sizes, target machines and numerical precision.

Moreover, it is straightforward to explore more extensions such as operation fusion with the help of compiler techniques. DNN models have pre- and post-GEMM operations, which can be fused together with GEMM to increase cache locality and thus improve performance.

5 Evaluation

We evaluated NGEMM’s performance against MKLML in MKL-DNN v0.21. Our NGEMM was implemented in ONNX Runtime (Microsoft, 2018), using a custom version of TVM with LLVM 9.0.0. The experiments were conducted on a machine with 8-core 2.3GHz Intel Xeon E5-2673V4 processors where AVX2 is supported. The machine runs Ubuntu 16.04 and GCC 6.5. No frequency scaling (DVFS) related techniques were used in the experiments (Bao et al., 2016b; Farkas et al., 2000). The performance numbers were obtained by taking geometric means across repetitions after several warmup runs. The numbers include only function calls of MKL routines or our generated functions, without any ML framework overhead.

Figure 5 shows the speedups of NGEMM and MKL-PACK (the pack version with the routines cblas_gemm_s8u8s32_compute and the offline packing routines cblas_gemm_s8u8s32_pack) over non-pack MKL (the version with the routines cblas_gemm_s8u8s32) on various problem sizes with 8-bit integers. Similar to NGEMM, MKL-PACK applies packing to the weight matrix. In contrast, MKL does not do any packing. The last two bars in the figure are the geometric means of the speedups of NGEMM and MKL-PACK over MKL across all the problem sizes. NGEMM and MKL-PACK demonstrated 1.86x and 1.60x speedups compared to MKL, respectively.

As shown in the graph, NGEMM has better performance compared to MKL for all the problem sizes that we chose. NGEMM also shows about 1.16X speedups over MKL-PACK. Moreover, we observed a huge memory cost (about 12MB) with MKL-PACK for packing a \([512 \times 512]\) int8 weight matrix, whereas NGEMM consumed only 0.25MB, which is the size of the matrix.

It is worth mentioning that the actual performance benefits of NGEMM might vary for different deep learning models. Real models have computations performed by other ops such as element-wise ops, which consume considerable time. In our experiments with real production models, NGEMM could delivered up to 1.34X speedups over MKL without packing.

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2 This version of MKL fixed certain performance issues in previous versions.
3 Speedup numbers reported in the previous version include ONNX Runtime overhead.
Figure 5: Performance Speedups of NGEMM and MKL-PACK (single-threaded cblas_gemm_s8u8s32_compute with an offline process cblas_gemm_s8u8s32_pack) vs MKL (single-threaded cblas_gemm_s8u8s32) over different sizes

6 Related work

Many research studies have shown that low numerical precision can be applied to DNN models with minimal to no accuracy losses. Quantization techniques have been adopted by many DNN frameworks to improve training and inference performance. XLA (Accelerated linear algebra) is a compiler backend for TensorFlow, which supports various optimizations including quantization and generates machine instructions for different targets. Glow is a machine learning compiler, which consumes neural network graphs, performs high-level graph optimizations and low-level machine-dependent optimizations for diverse hardware targets. Glow also supports quantization with various bit-widths. TVM, another compiler stack for deep learning, compiles the model into low-level IR and performs loop optimizations. It supports multiple hardware backends and quantization with different bit-widths. Our work, NGEMM, incorporates with Microsoft ONNX Runtime.

Many BLAS libraries have implemented low precision GEMM for various architectures. Intel MKL (Math Kernel Library) provides well-tuned 8- and 16-bit GEMM kernels, which is widely adopted across many DNN frameworks as a CPU vendor library. NVIDIA cuBLAS library provides GPU counterparts on NVIDIA GPUs. FBGEMM is a reduced-precision linear algebra library for deep learning inference, and is integrated into Caffe2. Gemmlowp is a library that only supports low-precision GEMM. In addition to execution time, it is also optimized to minimize the power consumption, which is crucial for edge devices.

Other than TVM, which is used to implement our techniques in the paper, general-purpose code generation frameworks, and domain-specific languages, are also capable to adopt our techniques for optimizing GEMM routines.

7 Conclusion

In this paper, we present NGEMM, an optimized low-precision GEMM implementation based on compiler techniques. Compared to the conventional approach adopted by contemporary BLAS libraries, our approach does not require tree reduction and hence has better performance. We implemented a hierarchical layout for the weight matrix to further improve the latency. Our evaluation on various problem sizes demonstrate an average of 1.16X and 1.86X speedup over state-of-the-art MKL library with and without packing. A number of production models also show up to 1.34X speedup using NGEMM compared to MKL without packing.
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