Abstract

The size of deep neural networks has grown exponentially in recent years. Unfortunately, hardware devices have not kept pace with the rapidly increasing memory requirements. To cope with this, researchers have turned to techniques such as spilling and recomputation, which increase training time, or reduced precision and model pruning, which can affect model accuracy.

We present **OLLA**, an algorithm that optimizes the lifetime and memory location of the tensors used to train neural networks. Our method reduces the memory usage of existing neural networks, without needing any modification to the models or their training procedures.

We formulate the problem as a joint integer linear program (ILP). We present several techniques to simplify the encoding of the problem, and enable our approach to scale to the size of state-of-the-art neural networks using an off-the-shelf ILP solver. We experimentally demonstrate that **OLLA** only takes minutes if not seconds to allow the training of neural networks using one-third less memory on average. **OLLA** is available at https://github.com/facebookresearch/OLLA.

1. Introduction

Scale is a major force behind the accuracy improvements of machine-learning-based solutions [9], and both the depth and width of deep neural networks (DNN) are expanding exponentially [66] (Figure 1). This inflation in size increases the memory needed to store the weights of the neural network and the intermediate results (e.g., activations and gradients) generated during the training process. Compounding the problem, researchers are training neural networks on larger inputs, such as high-resolution images [22, 71], video [28], three dimensional point-clouds [14], long natural language sequences [75, 15, 21], and using larger batch sizes to increase efficiency [69].

Unfortunately, due to the slowing of Moore’s law, the memory capacity of hardware has only increased linearly over the last decade (Figure 2). Thus, the amount of memory available on the hardware used to train DNNs has not kept pace with the needs of deep learning. Furthermore, features powered by machine learning, such as automatic speech recognition [63] or keyboard suggestions [35], are being personalized by fine tuning models on-device. This means that model training is increasingly being pushed to even more memory constrained edge devices such as smartphones. As a result, memory is increasingly becoming a bottleneck that hinders progress, and researchers frequently mention memory scarcity as a limiting factor that impacts their work [47, 36, 12, 18, 15].

The research community has proposed several solutions to mitigate the problem. Data spilling [54] and recomputation of intermediate results [43] relieve memory pressure. Novel neural network architectures [40] use memory more sparingly. Strategies such as reduced precision training [76, 78, 45] and weight pruning [56, 24, 37] decrease memory requirements. However, these all come at the cost of decreasing the accuracy of the model, or increasing the time it takes to train it, or both [49, 7, 57].

Popular deep learning frameworks such as PyTorch [61] and TensorFlow [1] do not fully utilize the limited memory available. Similar to traditional dynamic memory allocators such as tcmalloc [32] and jemalloc [26], these frameworks maintain a pool of free blocks of memory at runtime. To serve memory requests, they look for a large enough memory block in the memory pool, or allocate it from the physical memory if none is available. This results in memory fragmentation when free memory blocks do not exactly match the size of an allocation request, which occurs frequently.
The memory capacity of NVidia datacenter GPUs (in gigabytes) has only increased tenfold over the last decade, which has not kept pace with the rapidly increasing size of deep neural networks. The x-axis is plotted on a linear scale.

Furthermore, DNN frameworks do not optimize tensor lifetimes. PyTorch [61] executes operations in the order in which they are defined in the program. TensorFlow [1] keeps a queue of operators that are ready to run, and executes them on a first-come, first-served basis. As a result, tensors can be allocated earlier than required, or freed later than necessary, wasting valuable memory.

Our method overcomes these two limitations of existing deep learning frameworks. We model the computations performed to train a deep neural network as a dataflow graph of operations. We analyze this graph to find a topological ordering of the nodes that adjusts the lifetime of the tensors generated by these operations to minimize the peak amount of memory that needs to be allocated (Figure 3). Furthermore, we find an optimal packing of these tensors, which minimizes memory fragmentation (Figure 4). We encode these two objectives as an integer linear program (ILP) that can be solved quickly by commodity solvers, and present OLLA (Optimization of the Lifetime and Location of Arrays), our algorithm for memory-optimal training of neural networks.

In addition to significantly reducing memory usage, our solution has four key strengths. First, it does not impact the accuracy of the predictions of the neural networks. Second, it requires no modification to the neural network or the training procedure. Third, it doesn’t increase training time. Fourth, it is orthogonal to and can be combined with other memory reductions techniques to further reduce the memory needs of a neural network.

Our work makes the following novel contributions:

- We formulate the problem of finding the lifetime and memory location of tensors that minimizes the peak memory required to train neural networks as a joint integer linear program.
- We demonstrate how to leverage domain knowledge to simplify the ILP formulation, which enables off-the-shelf solvers to quickly reduce the memory usage of large DNNs.
- We study empirically the practicality and effectiveness of our solution on a wide variety of DNNs, which achieves average memory savings exceeding 30% in a median time of less than 10 seconds.
- We provide an open source implementation of OLLA, which is available at https://github.com/facebookresearch/OLLA.

2. Background

2.1. Representing Neural Networks as Dataflow Graphs

Deep neural networks can be represented using dataflow graphs, as pioneered by TensorFlow [1]. The nodes of the graph encode the computations to be performed (e.g. matrix multiplications, convolutions, activation functions), while the edges represent the data (aka tensor or array) that is produced by an operation and transferred to consumer nodes.

Due to the producer-consumer relation between connected nodes, edges are oriented. Each edge has exactly one source, which is the operator that generated the corresponding tensor. Since a tensor can be consumed by more than one node, edges can have multiple sinks.

Operators can have multiple incoming (aka fanin) edges. Typically, one of these incoming edges will be the tensor generated by the previous layer, and another one will be a weight tensor. Similarly, operators can have multiple outgoing (aka fanout) edges: while most operations generate a single output tensor, some may create two or more. Operators with no fanout edges are used to model the final outputs of the neural network. Operators without fanin edges can model random
number generators, constants, weights, or initial inputs to the neural network.

In the remainder of this paper, we assume that the graphs are acyclic. In practice, this is not a significant limitation since recurrent neural networks such as LSTM [39] have been eclipsed by transformers [75]. Furthermore, their loops can be unrolled to avoid the problem altogether.

2.2. Optimizing Tensor Lifetimes

In order for an operator to run, all its input tensors must be resident in memory, and its output tensors must have been allocated so that they can be written to while the node executes. Additionally, to avoid recomputing tensors, once a tensor is generated it must be preserved in memory until all its consumers have been run.

We define the resident set RS(t) at a given time t as the set of tensors that need to be kept in memory at that point in the execution of the neural network. It comprises the tensors in the fanin and fanout of the operator that is scheduled for execution at timestep t, as well as all the other tensors that were previously generated but need to be kept in memory to be able to run subsequent operators. The peak resident set is the largest resident set over the execution of the network.

The order in which nodes are executed impact the lifetime of the tensors, and therefore the peak working set. Figure 3 illustrates a simple example where changing the operator ordering noticeably improves memory usage.

Among all possible node orderings, those prioritizing the execution of nodes that free large amounts of data while generating little output data themselves, are likely to be more efficient. However, as demonstrated in prior works [5, 8], finding an optimal scheduling for a generic DAG is an NP-complete problem, which cannot be solved with a simple greedy approach.

2.3. Optimizing Tensor Locations in Memory

Similar to malloc-style memory allocators, the tensor allocation schemes used by typical deep learning frameworks operate online and suffers from fragmentation. Indeed, free memory is often segregated into small blocks and interspersed by memory allocated to live tensors. As a result, a significant fraction of the total memory is effectively unusable because it is divided into pieces that are not large enough to fit a tensor. Figure 4 illustrates this phenomenon, and demonstrates that planning the location of each tensor ahead of time can significantly reduce the overall peak memory usage.

3. Formulation

We propose to take advantage of the predictability of neural network computations to proactively Optimize the Lifetime and Location of Arrays (OLLA).

We formulate the problem of optimizing the ordering of computations (which determines the tensor lifetimes) and the location of tensors in memory (which determines the amount of memory fragmentation) of generic data-flow graphs, including those used in neural network training. We encode the problem as an integer linear program, and use an off-the-shelf ILP solver to find a solution that minimizes the peak memory required to run the dataflow graph.

We solve the ILP problem ahead of time, before the training process starts. This results in a small one-time initial cost, which can be recouped over the duration of the training: as free space does not need to be found at runtime, our memory allocation and deallocation operations are much cheaper than that of a standard allocator, thus saving some time at each training step (section 5.7).

3.1. DNN representation

As mentioned in section 2.1, we model a neural network as a directed acyclic graph G = (V, E) with n nodes V = v1, ..., vn that represent the operators and the neural network, and m edges E = e1, ..., em that encode the tensors exchanged by operators. The size in bytes of the tensor represented by edge ei is denoted as Sl. The source vertex of edge e is denoted src(e). The set of sink vertices of edge e is denoted snks(e).

The set of edges in the fanout of a node v is denoted fo(v), while the set of edges in its fanin is represented as fi(v). We will also denote fi(e) the set of edges in the fanin of the source vertex of e. We represent by sib(e) the siblings to an edge e, that is the collection of edges that are driven by the same source vertex.

We model time as a discrete set of timesteps T = t1, ..., tn. A single operation typically runs per timestep, but it is possible for several operations to execute concurrently. Therefore, we need at most n timesteps to schedule a graph with n operations.
3.2. Encoding Tensor Lifetimes

We capture the execution of a neural network as a series of tensors being allocated or preserved over time. To do this, we use two sets of binary variables:

- A variable labeled $C_{e,t} \in \{0,1\}$ indicates whether or not the tensor $e$ should be created (i.e. allocated) at timestep $t$ by running its source vertex.
- A variable named $P_{e,t} \in \{0,1\}$ reflects whether tensor $e$ needs to be preserved in memory at timestep $t$ or whether it can be freed.

We leverage a set of linear constraints to ensure that the sequence of tensor creations and preservations reflects a valid execution sequence of the neural network corresponding to a feasible topological ordering of the DAG.

First, a tensor $e$ can either be created or preserved at each timestep $t$, but not both (equation 1). Note that it’s possible for both $C_{e,t}$ and $P_{e,t}$ to be false, which indicates that the tensor does not reside in memory at this point in time.

$$\forall e \in E, \forall t \in T \quad P_{e,t} + C_{e,t} \leq 1$$

Second, a tensor $e$ can be preserved in memory at timestep $t$ if and only if it was created or preserved at the previous timestep (equation 2).

$$\forall e \in E, \forall t \in T \quad P_{e,t} \leq P_{e,t-1} + C_{e,t-1}$$

Third, to ensure that the solver does not simply avoid running any of the operators, we force every tensor $e$ to be created once through equation 3.

$$\forall e \in E \quad \sum_{t \in T} C_{e,t} = 1$$

Fourth, a tensor $e$ can only be created by running its source operator $v$. In order to do so, all the tensors in the fanin of $v$ must be present in memory (equation 4).

$$\forall e \in E, \forall t \in T, \forall f \in fi(e) \quad C_{e,t} \leq P_{f,t}$$

3.3. Encoding Tensor Locations

To let our solver also optimize the placement of tensors in memory, we assign an integer variable $A_e \in [0,M]$ to each tensor $e$ that encodes its base address. Here, $M = \sum E P$, which corresponds to the worst case scenario where all the tensors reside concurrently in memory.

We also introduce two binary variables $a_{i,j} \in \{0,1\}$ and $b_{i,j} \in \{0,1\}$ for each pair of tensors $i$ and $j$. We constrain them through equation 6 in such a way that either $a_{i,j}$ or $b_{i,j}$ is equal to 1 if both tensors reside in memory concurrently at any point in time, but can be 0 otherwise.

$$\forall t \in T, \forall (i,j) \in E^2 \quad a_{i,j} + b_{i,j} \leq 1$$

$$a_{i,j} + b_{i,j} \geq live_{it} + live_{jt} - 1$$

where $live_{it} = C_{i,t} + P_{i,t}$
and $live_{jt} = C_{j,t} + P_{j,t}$

We use these variables to prevent the overlap of tensors that reside in memory at the same time in equations 7a and 7b.

$$\forall (i,j) \in E^2 \quad A_i + S_t - A_j \leq (1 - a_{i,j}) * M$$

$$\forall (i,j) \in E^2 \quad A_i - A_j - S_t \geq (b_{i,j} - 1) * M$$

If $a_{i,j}$ takes the value 1, equation 7a degenerates into $A_i + S_t \leq A_j$. This forces tensor $i$ to reside below tensor $j$ in memory. Similarly, equation 7b degenerates into $A_i \geq A_j + S_t$ when $b_{i,j}$ takes the value 1, which forces tensor $i$ to be placed above tensor $j$. On the other hand, if $a_{i,j}$ and $b_{i,j}$ take the value 0, equations 7a and 7b hold for any value of $A_i$ and $A_j$ in the range $[0,M]$. In other words, they don’t impose further restrictions on the location of $e_i$ and $e_j$.

Put altogether, constraints 6, 7a, and 7b ensure that tensors can share the same memory space if and only if their lifetimes do not overlap.

3.4. Minimizing Peak Memory Usage

We track the peak memory usage by introducing a variable peak_mem that we constrain as follow:

$$\forall e \in E \quad A_e + S_e \leq peak_{-}mem$$

We find the schedule of operators and memory location of tensors that optimizes the memory usage of the neural network by feeding program 9 to an ILP solver.

$$\arg \min_{C,PA} peak_{-}mem$$

subject to (1), (2), (3), (4), (5), (6), (7a), (7b), (8)

3.5. Decoding the ILP Result

Given a feasible solution to our ILP, we generate an optimized execution sequence of operations $ES = (s_1, ..., s_k)$ for the neural network using function 1.
All of the input tensors of a node must reside in memory for it to run at a given timestep. This means that all the operators in the immediate fanin of the node must have been run at least one timestep prior. As a result, we can identify the earliest timestep \( \text{ASAP}(v) \) (“as soon as possible”) during which a node \( v \) can run. \( \text{ASAP}(v) \) is the longest distance from \( v \) to an input of the neural network, which is computed in linear time using a simple depth first search traversal of the graph [3]. Using the same approach, we can also identify the latest timestep \( \text{ALAP}(v) \) (“as late as possible”) at which a node \( v \) can run, which is the longest distance from \( v \) to an output of the neural network.

A node \( v \) can only run within the span \([\text{ASAP}(v), \text{ALAP}(v)]\). Since tensors are created when their source node is run, a variable \( C_{e,t} \) will always be false outside the span of their source node (Equation 10).

\[
\text{SPAN}(v) = [\text{ASAP}(v), \text{ALAP}(v)]
\]
\[\forall e \in E, \forall t \notin \text{SPAN}(s(e)) \quad C_{e,t} = 0\] (10)

Furthermore, a tensor only needs to be preserved in memory until all its sink operators have run. This enables us to define the Maximum Useful Lifetime (MUL) range of a tensor, and set the variable \( P_{e,t} \) for a tensor \( e \) to false outside of this range (Equation 11).

\[
\text{MUL}(e) = [\text{ASAP}(s(e)), \max_{s \in \text{snks}(e)} \text{ALAP}(s)]
\]
\[\forall e \in E, \forall t \notin \text{MUL}(e) \quad P_{e,t} = 0\] (11)

Additionally, tensors must be preserved in memory from the time they are created until their last sink node has run. Therefore, \( P_{e,t} \) must always be true from the last timestep at which \( e \) can be created until the earliest timestep at which its last sink can run (Equation 12).

\[
\text{PRES}(e) = [\text{ALAP}(s(e)) + 1, \max_{s \in \text{snks}(e)} \text{ASAP}(s)]
\]
\[\forall e \in E, \forall t \in \text{PRES}(e) \quad P_{e,t} = 1\] (12)

This enables us to reduce the number of timesteps to track for each tensor. In the best case scenario, where a neural network is a linear sequence of operators, the span of each node \( v \) is reduced to a single timestep, and we can derive the values of all the \( C_{e,t} \) and \( P_{e,t} \) purely from the structure of the graph. However, in the opposite extreme case where a neural network consists exclusively of operators that can run in parallel, we cannot infer any of the values of the \( C_{e,t} \) and \( P_{e,t} \) variable. The structure of real neural networks lies somewhere between these two extremes.

### 4.2. Leveraging Precedence Constraints

We simplify our memory placement formulation by skipping constraints 6 7a and 7b whenever we can determine that two tensors can never reside in memory at the same time. We exploit two sufficient conditions to achieve this.

First, we leverage the Maximum Useful Lifetime ranges from our ASAP/ALAP analysis. If the MUL ranges of two tensors do not overlap, they will never be present concurrently in memory.

We complement this first condition with a precedence analysis. If a vertex \( v_2 \) is reachable from another vertex \( v_1 \) (i.e. if \( v_1 \) is in the transitive fanin of \( v_2 \)), the corresponding operator \( v_1 \) must be run before operator \( v_2 \). Therefore, if all the sink
vertices of an edge $e_1$ are in the transitive fanin of the source vertex of an edge $e_2$. $e_1$ and $e_2$ can only be present in memory if there is a vertex $v$ such that $e_1$ is one of the fanout edges of $v$ and $e_2$ is one of its fanin edges (Figure 5). We call this condition $\prec_{\text{prec}}$, and if either condition $\prec_{\text{prec}}$ or $e_2 \prec_{\text{prec}} e_1$ holds $e_1$ and $e_2$ can never reside together in memory.

We use a simple depth-first search (Function 2) to determine whether a vertex $v_2$ is reachable from a vertex $v_1$. We leverage memoization to ensure that answering the query for a pair $(v_1, v_2)$ yields to constant time queries for all future queries $(v, v_2)$ that involve a vertex $v$ on a path from $v_1$ to $v_2$.

**Function 2** IsInTransitiveFanin($v_1$, $v_2$, cache)

- Returns true iff $v_2$ can be reached from $v_1$.
- if $(v_1, v_2)$ in cache then
  return cache[$(v_1, v_2)$]
- end if
- for $f$ in $fi(v_2)$ do
  if src($f$) = $v_1$ then
    cache[$(v_1, v_2)$] ← true
    return true
  end if
  if IsInTransitiveFanin($v_1$, src($f$)) then
    cache[$(v_1, v_2)$] ← true
    return true
  end if
end for
- cache[$(v_1, v_2)$] ← false
- return false

4.3. Enforcing Early Memory Deallocations

Running a weight update operation enables the freeing of the corresponding gradient tensor. Applying these updates early reduces memory pressure, and conversely, there is no benefit to delaying their execution. To speed up the tensor lifetime optimization process, we prevent the solver from considering running these nodes late in the computation.

To achieve this, we look for a good anchor node, and add an edge of size 0 (which we call a control edge) from the gradient update node to this anchor node. The control edge forces the ALAP time of the gradient node to be less than that of the anchor node, but has no impact on memory usage since its size is 0. The anchor node must meet two criteria:

- Its level must be greater than that of the weight update node in the graph levelization [17]. This prevents the introduction of a loop through the control edge in the graph.
- A good anchor candidate must be scheduled early in the computation itself. We determine this by running the levelization on a copy of the DAG in which the directions of all the edges are reversed, and looking for a node with a high backward level.

We start the search for anchor nodes in the immediate fanin of the weight update vertex, and progressively expands the search radius until we find a suitable node as detailed in Functions 3 and 4.

**Function 3** EnforceEarlyWeightUpdates($G$)

- Adds control edges to $G$ to force the weight update nodes to run early. The pseudo code for FindCandidate is provided in Function 4.
- $fwd_{lvl} \leftarrow \text{ComputeLevelization}(G)$
- $bwd_{lvl} \leftarrow \text{ComputeReverseLevelization}(G)$
- for $v$ in gradient update nodes of $G$ do
  - $min_{fwd_{lvl}} \leftarrow fwd_{lvl} [v]$
  - $best_{bwd_{level}} \leftarrow -1$
  - $best_{anchor} \leftarrow \text{none}$
  - $search_{starts} \leftarrow \text{set} (v)$
  - $visited \leftarrow \text{hashtable} ()$
  - while not $best_{anchor}$ and len($search_{starts}$) > 0 do
    - $next_{starts} \leftarrow \text{set} ()$
    - for $v$ in $search_{starts}$ do
      - for $f$ in $fi(v)$ do
        - add src($f$) to $next_{starts}$
      end for
    end for
    - $search_{starts} \leftarrow next_{starts}$
  end while
  - for $src$ in $search_{starts}$ do
    - candidate, level $\leftarrow \text{FindCandidate}(src, fwd_{lvl}, bwd_{lvl}, min_{fwd_{level}}, visited)$
    - if level $> best_{bwd_{level}}$ then
      - $best_{bwd_{level}} \leftarrow$ level
      - $best_{anchor} \leftarrow$ candidate
    end if
  end for
  - if $best_{anchor}$ then
    - add control edge from $v$ to $best_{anchor}$
  end if
end for
We noticed empirically that OLLA is always able to fully eliminate memory fragmentation. Therefore, without losing optimality, we can divide the problem in two subproblems that are faster to solve sequentially.

We first look for the schedule of operations that leads to the smallest peak memory usage under the assumption that we will be able to locate tensors in memory later on without introducing any fragmentation. We compute this peak memory usage metric, \( \text{peak}_\text{mem}_\text{no}_\text{frag} \), by leveraging the \( C \) and \( P \) variables in equation 13:

\[
\forall t \in T \sum_{e \in E} (C_e,t + P_e,t) \times S_e \leq \text{peak}_\text{mem}_\text{no}_\text{frag} \tag{13}
\]

The problem of optimizing the lifetime of tensors without considering fragmentation is then formulated in equation 14:

\[
\begin{align*}
\text{arg min}_{C,P} & \quad \text{peak}_\text{mem}_\text{no}_\text{frag} \\
\text{subject to} & \quad (1), (2), (3), (4), (5), (13)
\end{align*}
\tag{14}
\]

4.4. Splitting the Problem

We measured the impact of OLLA on the memory usage of DNN training. We tried to answer the following questions:

- How effective are our two strategies of node reordering and address generation at reducing memory usage?
- How applicable is our approach? Can one reasonably expect to benefit from it on their use case, or is it more effective in some scenarios than others?
- How practical are our algorithms? Can they be applied to large neural networks in a reasonable amount of time?
We included the ResNet [36] and Transformer [75] models. We evaluated OLLA on a comprehensive set of neural networks. We implemented a system on top of PyTorch version 1.11 [61] with torchtext 0.12 and torchvision 0.12. We leveraged torch.FX to convert neural networks into executable sequences of operator calls, and reconstructed the computation graphs from the operator arguments. We encoded and solved the memory optimizations problems (9), (14) and (15) using Gurobi version 9.1.1 [34]. We translated the Gurobi results into optimized execution sequences and memory locations as described in section 3.5.

We ran all our experiments on a workstation featuring an Intel Xeon Gold 6138 CPU running at 2.0 GHz and a NVidia A100 GPU with 40GB of memory.

5.2. Methodology

We evaluated OLLA on a comprehensive set of neural networks. We included the ResNet [36] and Transformer [75] models as large as XLM-R [16] (2007 operators).

In addition to these models that were designed to run on datacenter hardware, we also evaluated our approach on EfficientNet [73] and MobileNet [40]. These two neural networks were tailored to run in resource constrained environments such as edge devices. Additionally, we trained the neural networks at batch size 1 and 32. Batch size 1 is commonly used when training a model on devices with limited memory capacity, while batch size 32 is used often when running in datacenters.

To be representative of the evolution of DNN designs over time, we made sure our models cover almost a decade of machine learning research, starting with AlexNet [47] which was published back in 2012 and ending with VIT [23] which was released in 2020. We also tested our approach on MNASNet [72], a model designed by a computer using an automated process called neural architecture search [25].

To validate the scalability of our solution, we tested it on neural networks as small as Alexnet [47] (118 operators) and as large as XLM-R [16] (2007 operators).

5.3. Memory Reduction Resulting from Node Reordering

To evaluate the impact of our tensor lifetime optimization, we compared the peak memory necessary to run various neural networks when using the PyTorch node ordering and the node ordering determined by algorithm 14. In our measurements, we eliminated the impact of memory fragmentation by recording the peak memory PyTorch operators need to request to run these models under both node orderings instead of the actual memory usage.

We find that OLLA reduces peak memory usage by up to 38% compared to PyTorch (Figure 7). On average, our solution

```plaintext
Function 5 PreAllocateAddresses(G)
▷ Find memory locations for a subset of the tensors.
    min_start ← 0
    max_end ← ∞
    base_address ← 0
    processed ← set()
    while max_end > min_start do
        max_duration ← 0
        next_step ← none
        for e in E do
            first_use ← ASAP(src(e))
            last_use ← max_{s∈snks(e)} ALAP(s)
            if first_use < min_start then
                continue
            end if
            if last_use > max_end then
                continue
            end if
            if tensor in processed then
                continue
            end if
            duration ← last_use - first_use
            if duration > max_duration then
                max_duration ← duration
                next_step ← tensor
            end if
            end for
            if not next_step then
                break
            end if
            A_{next_step} ← base_address
            base_address ← base_address + S_{next_step}
            min_start ← first_use
            max_end ← last_use
            add next_step to processed
        end while
```

Figure 7: Peak memory reduction (in %) compared to PyTorch as a result of our node reordering.
achieves a reduction of 22.5% at batch size 1 and 10.1% at batch size 32.

The activations generated during the forward pass are preserved in memory for the backward pass of the training. As a result, OLLA has little to no ability to decrease the memory usage of the forward pass. On the other hand, the order of the computation and application of the gradients with respect to the weights offers a great deal of flexibility, which OLLA leverages to decrease the memory usage of the backward pass. However, the gradients are are roughly smaller than the activations by a factor of batch size. Therefore, at larger batch sizes, most of the memory is used to store activations, while at smaller batch size gradients represent a larger fraction of the total. This explains why our approach is more effective at small batch sizes.

5.4. Memory Savings Coming from Address Generation

We define the fragmentation of a memory allocator as the difference between the memory the allocator needs to reserve from the hardware $MR$ and the size of the resident set $RS$. We measure it when $MR$ reaches its peak value using the ratio $(MR - RS)/MR$.

In all scenarios our address generator can completely eliminate memory fragmentation. By contrast, PyTorch suffered from an average fragmentation of 7.9% at batch size 1, and 26.1% at batch size 32 (Figure 8). The PyTorch memory allocator uses a different strategy for small and large objects, which could explain why fragmentation is significantly worse for the larger batch size. However it is unclear whether it could be modified to better handle large tensors without introducing other drawbacks.

5.5. Node Ordering Time

Solving for equation 14 to optimize node orderings takes a median of $1.4 \pm 0.2$ seconds. Excluding the outlier EfficientNet, the worst case optimization time is 5.2 seconds, and the best case is 100 milliseconds (Figure 9). For EfficientNet, OLLA needs 2 minutes to find the optimal node ordering at batch size 1 and 5 minutes to find a solution that is within 1% of optimal at batch size 32 (Figure 10).

OLLA only needs a small fraction of the time it takes to train a neural network to optimize the lifetime of tensors and significantly reduce the peak memory usage.

5.6. Address Generation Time

Leveraging equation 15, OLLA eliminates fragmentation in a median time of $5.7 \pm 0.6$ seconds (Figure 11). While it takes significant effort to find optimal solutions for GoogleNet and EfficientNet, OLLA reduced fragmentation to less than 1% in 5 minutes or less for these two models. We plot the evolution of the memory fragmentation over time in these two cases in Figure 12.

5.7. Practical Use

Since our optimizer runs ahead of time, it’s important that it completes its task in a short amount of time to avoid negatively impacting the user friendliness of the overall system. We achieved a balance between memory savings and usability.
by enforcing a 5 minute time limit on both the lifetime and location optimizations. Figure 13 shows the overall reduction in peak memory usage achieved within these time limits. OLLA achieves an average improvement of 30.4% at batch size 1, and 36.1% at batch size 32.

PyTorch relies on dynamic memory allocation, which introduces some runtime overhead with each tensor allocation and deallocation. We compared the initial runtime penalty of our approach against the time the PyTorch allocator takes to manage memory while training neural networks at batch size 32. We assume that 1,000,000 iterations through the training loop are required to train a neural network, which is equivalent to processing the entire ImageNet [20] dataset 25 times, and corresponds to 8 training epochs on the IWSLT2017 dataset [10]. Our approach proved to be slightly more runtime efficient overall, saving an average of 5 minutes (Figure 14).

Note that we didn’t directly measure the total training time under both memory management schemes to reduce the noise in the measurements. Additionally, we didn’t report our estimated runtime savings at batch size 1 since the premises of this use case, typically encountered on-device, are very different: while each user would only perform a few training iterations, our optimizations would be applied before shipping the application.

6. Related Work

Various approaches, complementary to ours, have been proposed to break the “memory wall” and train larger networks. The first technique distributes the computation for a single forward-backward iteration over several hardware devices, thus making more memory available overall. However, this approach, known as model parallelism [46], significantly increases the financial cost of training deep neural networks since it requires access to additional expensive compute accelerators and fast networks. Furthermore, partitioning a deep neural network efficiently to balance communication and computation remains an open problem still actively researched [31, 44, 55].

In parallel, the research community has developed numerous solutions to reduce the memory footprint of deep neural networks:
• Novel neural network architectures reduce the number of parameters needed to achieve a given level of accuracy [41, 73]. Furthermore, automated search techniques known as neural architecture search [72] have been proposed to automatically design memory efficient models. The main drawbacks of these methods are that they are time consuming to deploy, and fail to match the result quality of state of the art DNNs.

• Model compression methods [6] prune [53, 29, 56, 24, 37] or share [19] weights to improve the efficiency of the model parameterization. However, the majority of these techniques require training the unpruned neural network first, and are therefore most useful for inference.

• Training using reduced precision arithmetic on 16-bit floating point or even quantized representations [76, 78, 45] significantly reduces memory [27, 50]. However, these techniques can compromise the accuracy of the neural networks, make training unstable, and require careful implementation to be deployed successfully [59, 51].

Several efforts have looked at the problem from a systems perspective, and presented solutions to reduce pressure on the memory subsystem. These techniques encompass:

• In-memory tensor compression, which can result in minimal accuracy loss in many DNN applications [11, 42]. However, this comes with a runtime penalty, since the data must be compressed and uncompressed on the fly.

• Rematerialization, also known as checkpointing, discards activations in the forward pass to save memory, and recomputes those values as needed when computing the gradients. Numerous strategies to identify which activations to discard have been proposed [43, 77, 13, 33, 67]. While effective at reducing memory usage, these techniques add extra computations, which increases the training time.

• Paging, aka spilling, consists of moving data between a small but high bandwidth and low latency memory pool, and a large but slow external memory. This has been demonstrated to effectively offload the data stored on a GPU device onto the host memory [64, 38, 54], but again increases training time due to extra memory transfers.

• More recently, combining several of these techniques has been proposed to increase their effectiveness and mitigate their drawbacks [4, 62] without fully eliminating them.

Additionally, some techniques developed primarily to increase execution speed are also beneficial for memory:

• Operator fusion can reduce memory footprint by avoiding the need to materialize large intermediate buffers and keep them around for backpropagation [58].

• Machine learning frameworks such as PyTorch [61] and TensorFlow [1] allow some of their operators to store the data they generate in one of their input tensors, thus avoiding the need to allocate an output tensor. This is known as in-place update, and saves memory. However, users must manually modify their neural networks to leverage this capability, and it can lead to correctness issues if used indiscriminately [60].

Optimizing the location of tensors in memory to reduce fragmentation, also known as the dynamic storage allocation problem, is NP-hard [30]. This problem has been studied in the context of deep learning by other researchers [65] who proposed an exact formulation to minimize the memory fragmentation of deep neural networks. However, their approach scaled poorly and only succeeded in optimizing two small neural networks in inference mode. As a result, they ultimately advocated for a heuristics based approach.

Improving the lifetime of tensors has also been studied before. Liberis et al. [48] and Serenity [2] looked for a memory-optimal execution schedule by enumerating the topological orders of the DNN graph and calculating their peak memory usage. To speed things up, they both proposed dynamic programming based optimizations to prune the number of orderings they needed to consider. However, the complexity of their algorithms remains prohibitive at $O(|V| \cdot 2^{V})$ in both cases, and they only managed to make them work for inference on tiny graphs. Lin et al. [52] also mentioned reordering computations as a way to enable operator fusion and reduce the peak memory footprint while training. Unfortunately, they didn’t describe the algorithm they used to find a suitable node ordering.

7. Conclusion

The limited memory capacity of the hardware used by deep learning practitioners is one of the main challenges to train state-of-the art neural networks. This "memory wall" limits the size of the neural networks that can be trained, and ultimately impacts the quality of their predictions. Furthermore, as memory needs increase much faster than memory capacity, we expect this memory bottleneck to worsen over time.

To alleviate memory scarcity, we proposed to optimize both the lifetime and location of tensors in memory. We presented an ILP formulation of the problem, and extended it with ad-hoc simplifications to ensure that our approach scales to large neural networks.

We tested our solution, OLLA, on a wide variety of neural networks. We demonstrated experimentally that it can locate tensors optimally in memory, thus eliminating the problem of memory fragmentation. Furthermore, we showed that it further decreases the peak memory usage of deep neural networks by optimizing the lifetime of the tensors, and, by combining these 2 techniques, OLLA reduced peak memory usage by more than 30% on average.

We also emphasized the practicality of OLLA. We established empirically that it scales well and can handle large DNNs. We showed that it finds memory plans that are within 1% of optimal in less than 10 minutes (and often in mere seconds), and measured that OLLA’s optimization time is more than compensated for by eliminating the runtime overhead of dynamic allocation during training.
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