Electronic-photonic circuit crossings

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Electrical control of light in integrated photonics is central to a wide range of research and applications. It is conventionally achieved with thermo-optic tuning, but this suffers from high energy consumption and crosstalk. These challenges could be resolved with nanoelectromechanical photonics but scalable platforms were so far not demonstrated because of incompatibility with conventional multilayer metal architectures and because conventional approaches do not allow crossings of electrical wires and photonic waveguides. Here we use topology optimization to devise a single-layer electronic-photonic circuit crossing with up to 99.8% optical transmission across an isolation trench with excellent electrical isolation. We use the crossing to demonstrate a monolithic silicon nano-electro-mechanical add-drop switch in which the flow of photons, electrons, and mechanical motions are fully integrated within the same layer. Our work enables hitherto impossible opto-electro-mechanical topologies and may lead to new functionalities in nano-opto-electro-mechanical systems, optomechanics, and integrated quantum photonics.

Information technologies rely on controlling two fundamentally different particles: electrons are strongly interacting massive charged fermions while photons are massless and charge-neutral bosons that do not interact. These differences underpin the development of optical communication systems based on low losses and high coherence as well as electronic computing relying on strong interactions. For many reasons, however, integrating electronics and photonics is becoming an increasingly important research frontier: First, a sizeable fraction of the energy consumption in modern computing is spent on routing information through lossy electrical leads, which may be significantly reduced by chip-level optical interconnects [1, 2]. Second, the developments in hybrid quantum technologies call for high-fidelity interfaces between stationary and flying qubits [3, 4], which require unprecedented control and integration of electronics and photonics. Third, the integration of photonics and electronics is at the heart of a wide range of new technologies that rely on advanced nanofabrication for new applications beyond electronics [5], ranging from smart sensors [6] over ultrahigh-bandwidth optical networks [7] to chip-scale particle accelerators [8], and nano-opto-electro-mechanical systems (NOEMS) [9, 10].

Simultaneously controlling the flow of electrons and photons inside the same microchip is challenging because of the conflicting requirements for electronics and photonics: Electronic wires rely on conduction by free electrons but they in turn lead to significant optical losses. Therefore, both research and technology has so far resorted to various multi-layer chip architectures aiming to avoid crossings between wires and waveguides. Existing solutions include optical layers embedded in transparent insulators with metallic surface electrode layers or numerous patterned conducting layers buried below the optical layers and contacted by deep vias in order to route the electrical signals without impeding the optical performance. Common to existing solutions is the need to add more layers or processes as the circuits grow. In other words, the circuit complexity scales superlinearly with the number of (avoided) electronic-photonic crossings. While these solutions can be employed to integrate photonic circuits with CMOS chips [11–13], they are now a limitation for a wide range of research including routing of single photons from quantum dots [14], chip-scale LiDAR solutions [6, 15], photonic interconnects for 5G networks [16], compact sensors [17], electro-optic and thermo-optic devices [18, 19], and nano-electro-mechanical photonic switches [20]. The solution proposed in this work overcomes the system-level complexity in routing electrons and photons inside the chip by introducing a carefully engineered and inversely designed monolithic device. It allows crossing electronic connections and photonic waveguides using the same device layer without introducing significant electrical resistance or optical losses. We focus our effort on silicon membranes fabricated on the silicon on insulator (SOI) platform but the concepts can be readily applied to all other semiconductor platforms.

Figure 1a illustrates a generic circuit topology for routing electrons and photons where photons are guided through the optical links, i.e., photonic waveguides. The optical ports are oriented east-west (EW) while the electrical contacts are oriented north-south (NS). Except for the most primitive integrated electronic-photonic circuits,

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it is impossible to build such architectures without introducing either multilayer technologies or resorting to circuit topologies that involve crossings of photonic waveguides and electronic wires. The immediately apparent challenge of designing an electronic-photonic circuit crossing (EPCC) is to achieve high optical transmission and low reflection in the EW direction as well as low electrical resistance in the NS direction. Furthermore, an important additional requirement for generic multiport devices is that the electrical resistance must be very high in the EW direction to avoid short circuits between the electrical leads. A simple solution would be to introduce an isolation trench through the waveguide to provide electrical isolation but this is clearly a sub-optimal solution as it significantly reduces the optical transmission. For example, introducing a gap of 100 nm in a suspended waveguide results in a transmission of less than 34% and a reflection above 22% over a 100 nm bandwidth centered at 1550 nm (fig. S1). Alternative approaches relying on parameter-optimized tapering (fig. S2) is also resulting in so poor performance that is detrimental to devices with even a minimum of system-level complexity.

An EPCC solution must ensure proper mode matching across the isolation trench. Due to the coherent nature of the photon scattering and interference, designing such a subwavelength mode-matching EPCC is a complicated and non-intuitive problem. We therefore employ inverse design by topology optimization [21, 22] to develop a compact and scalable device that transmits photons efficiently across the electrical isolation trench. The trench must be wide enough to avoid electric breakdown due to Townsend avalanches and field emission. For our experiments, we consider 100 nm trenches that provide electrical isolation for a voltage of at least 25 V [23], suitable for high-voltage applications including NOEMS. As we are interested in maximizing the transmission across a 100 nm isolation trench, while at the same time minimizing reflections, we seek to maximize the figure of merit, \( \Phi = T / (R + \alpha) \), where \( T \) denotes transmission across the isolation trench and \( R \) the reflection, over a spatial region of \( 1.5 \mu m \times 1.0 \mu m \) that corresponds to the length and width of the design domain. The parameter \( \alpha = 1 \)
is added to the denominator to avoid numerical issues as $R \to 0$ caused by the singularity at $R = 0$ as well as to balance the priority to $T$ vs $R$ such that the optimization algorithm will not sacrifice $T$ when $R << 1$. The EPCC is optimized at the wavelengths corresponding to the beginning and the end of the targeted bandwidth, i.e., 1500 nm and 1600 nm, in order to ensure the efficient performance across a 100 nm bandwidth centered at 1550 nm.

Figure 1b illustrates our solution to the EPCC problem. The photonic waveguide is suspended by silicon bridges designed to provide mechanical support without disturbing the propagating optical mode, while at the same time serving as electrical links in the NS-direction. The central part is shown in Fig. 1c and is generated by topology optimization, which results in excellent transmission. This is evident from the lack of resonances in the electric field (Fig. 1d) and time-averaged power flow (Fig. 1e) of the transverse-electric mode. The calculated transmission and reflection spectra are shown in Fig. 1f and feature a transmission of $T > 90.7\%$ and a reflection of $R < 1.35\%$ over a 100 nm bandwidth as well as a peak transmission of $T = 94.2\%$, which is a dramatic improvement compared to the solutions before topology optimization (figs. S1 and S2).

In order to experimentally verify these findings, we fabricate a set of photonic circuits with 0 to 6 EPCCs in series using electron-beam lithography and cryogenic deep reactive ion etching applied to SOI wafers. This enables direct measurement of the insertion loss of a single EPCC using the cut-back method, which separates the coupling losses from propagation losses. Figure 2a shows a dark-field microscope image of such a circuit comprised of 6 EPCCs embedded in a single-mode waveguide, 20 silicon bridges, and two cross-polarized input/output couplers. The position and number of silicon bridges are chosen to provide mechanical stability for maintaining the photonic circuit suspended. Six different sets of each photonic circuit are fabricated on the same chip, which allows us to do ensemble measurements and carefully estimate the standard deviation. Figure 2b compares the experimental transmission spectrum with the numerical calculations and shows excellent agreement.

To illustrate the application of the EPCC, we consider a new type of monolithic electro-mechanical photonic add-drop network that integrates EPCCs with nano-electro-mechanical photonic switches in a single lithographic step. Figure 3a shows a dark-field microscope image of the $2 \times 2$ switch network. The network is built on four reconfigurable directional couplers controlled by electrostatic comb-drive actuators (Fig. 3b), which can induce nanoscale displacements [24] to the mechanically compliant waveguides and thereby change the configuration of the switching network. The light coupled to the input $I_1$ ($I_2$) can be transmitted to the corresponding through port $T_1$ ($T_2$) or directed to any of the drop ports $D_1$ and $D_2$ depending on the driving voltage of the activated comb-drive actuator. Figure 3b shows a scanning electron micrograph of one of the switching elements and illustrates how isolation trenches along with the EPCCs are introduced to the device layer of the SOI wafer to route the electrical signals to the comb-drive actuator. The through- and drop-port transmission at 1550 nm is plotted in Fig. 3c-f and show a clear switching behavior for all voltages. This demonstrates central building blocks for programmable [25, 26] or quantum

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Fig. 2. Experimental realization of the electronic-photonic circuit crossing. (a) Dark-field microscope image of a photonic circuit including 6 EPCCs fabricated on an SOI wafer. The red inset at the center shows a scanning electron micrograph (30° tilted) of a single EPCC. The yellow inset shows the center of the EPCC. (b) Measured optical transmission (green) of the optimized EPCC obtained by a cut-back method showing excellent agreement with theory (black). The green shaded area represents the standard deviation from the mean of six nominally identical sets of devices.
Fig. 3. Demonstration of a single-layer 2 × 2 add-drop switching network combining electronic, photonic, and mechanical degrees of freedom. (a) Dark-field microscope image of the fabricated 2 × 2 add-drop switch made of four electrostatically actuated directional couplers. (b) 45°-tilted scanning electron micrograph of one switching element acquired at a low accelerating voltage of 5 kV in order to illustrate the charging effect, showing that excellent electrical isolation is obtained between the actuator electrodes via multiple EPCCs and isolation trenches. The inset in (b) shows a zoomed top view scanning electron micrograph of one of the EPCCs employed to route the actuation signal to the electrostatic actuators. (c-f) Measured normalized transmission to through ports (red) and drop ports (blue) at 1550 nm over actuation voltages. The incident light is coupled to $I_1$ in (c) and (d) and to $I_2$ in (e) and (f). The driving voltage is applied to the actuators at the top-left (c), the bottom-left (d), the top-right (e), and the bottom-right (f).

Photonic circuits [18] where the full benefit of the EPCC is ultimately harvested in larger networks: Regardless of topology and complexity, advanced electronic-photonic circuits can be fabricated in the same device layer and in a single lithography step.

For larger networks, the optical transmission becomes a limiting factor and we therefore design additional EPCCs while relaxing the bandwidth requirement and allowing for smaller but still feasible gaps [27]. Figure 4 shows EPCCs for (a) 100 nm, (b) 60 nm, and (c) 20 nm isolation gaps topology-optimized for maximum transmission at 1550 nm. The transmission increases with decreasing gap size and for a gap of 20 nm, the peak power transmission reaches a remarkably high value of $T = 99.8\%$. Furthermore, it remains above 99% across a 35 nm bandwidth (fig. S6). Because the overall transmission of circuits with $N$ crossings scales as $T^N$, a power transmission of $T = 99.8\%$ implies that hundreds of EPCCs in series would result in insertion losses below 3 dB. This shows that highly complex hybrids of nanoelectronics, nanophotonics, and nanomechanics can be integrated with negligible losses. Our results indicate that even higher transmission is attainable for smaller gaps.

The EPCC opens perspectives for a wide range of new research and technology. For example, isolation trenches are not only efficient electrical isolators, they are also ideal for thermal isolation in nanophotonic devices [19] or mechanical isolation for quantum optomechanics [28], and we envision our technology enabling, e.g., phonon-photon crossings. In addition, our concepts apply directly to other semiconductor platforms such as gallium arsenide or indium phosphide, where they enable independent electrical control of quantum emitters in integrated photonic circuits [14], thus solving a major scaling problem in integrated quantum photonics and enabling unprecedented circuit topologies in integrated photonics. Our experiment probes parameters ideal for low transmission losses and high operating voltages to actuate stiff springs in quasistatic nano-electro-mechanical switching scenarios but EPCCs can be applied immediately to other regimes. For example, local doping of the
Fig. 4. Topology-optimized EPCCs with near-unity transmission. The calculated time-averaged power flow is shown for designs obtained with single-wavelength topology-optimization with gaps of (a) 100 nm, (b) 60 nm, and (c) 20 nm. The power transmission at 1550 nm for each design is indicated in the figure and reaches 99.8% for a gap of 20 nm.

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ACKNOWLEDGMENTS

Funding: We gratefully acknowledge financial support from the Villum Foundation Young Investigator Program (Grant No. 13170), the Danish National Research Foundation (Grant No. DNRF147 - NanoPhoton), Innovation Fund Denmark (Grant No. 0175-00022 - NEXUS), and Independent Research Fund Denmark (Grant No. 0135-00315 - VAFL). Author contributions: B.V.L., M.A., and S.S. conceived the concepts. S.S. supervised the project. R.E.C., B.V.L., and C.A.R. designed the electronic-photonic circuit crossings and performed the numerical calculations. B.V.L., M.A., M.T.S., and S.S. designed the chips. M.A. and C.A.R. fabricated the samples. B.V.L. and M.A. carried out the experiments. B.V.L., M.A., C.A.R., K.T., and S.S. contributed to theory and data analysis. B.V.L. and S.S. wrote the manuscript with contributions and input from all authors. Competing interests: Part of the work is subject to a patent application by M.A., B.V.L., S.S., and R.E.C. The remaining authors declare no competing interests. Data and materials availability: All data are available in the manuscript or the supplementary materials.
Supplementary information for
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Electronic-photonic circuit crossings without topology optimization

Figure S1 illustrates a naive approach to an electronic-photonic circuit crossing (EPCC) made by introducing an isolation air gap in a photonic waveguide. While this approach can provide sufficient electrical isolation, it suffers from poor optical transmission as well as a high reflection. The transmission is below 34% across the full 100 nm bandwidth that we consider in our study, which renders the naive approach practically useless. For example, 20 of such EPCCs in series would lead to a loss of > 94 dB. To improve the performance of the crossing, one may expand the 400 nm suspended single-mode waveguide to a 1 µm wide silicon region through a parameter-optimized tapering section (Fig S2) which results in a noticeable improvement compared to the naive approach. However, Fig S2 shows that a mode expanding region alone cannot diminish the reflection to sufficiently low values for practical applications. In addition, the 81.4% peak power transmission is detrimental to circuits with a few EPCCs. For this simple tapered structure, 20 EPCCs in series would lead to a loss of 18 dB.

Inverse design of EPCCs by topology optimization

Topology optimization [1] is an inverse design method, applicable across many areas of physics and engineering [2–7]. When applying topology optimization to solve a structural design problem, the problem is recast as a continuous constrained optimization problem, where the quality of the structure under design is measured using a figure of merit, $\Phi$, which is optimized by changing the structural geometry iteratively and systematically. The structure is represented by a continuous design field, used to interpolate between the material(s) constituting it and its surroundings. The continuity of the design field and all operations applied to it enable the use of computationally efficient adjoint sensitivity analysis [8] to compute gradients of $\Phi$ with
Figure S1: Electronic-photonic circuit crossing without optimization. (a) Normalized transverse electric (TE) field ($E_y$) distribution across a 100 nm isolation gap introduced through a single mode suspended waveguide at 1550 nm. (b) Time-averaged power flow along the optical propagation direction ($P_x$) crossing the isolation gap at 1550 nm. (c) Calculated transmission (red) and reflection (blue) showing a transmission (below 34 %) and reflection (above 22 %) across the full spectral range.
Figure S2: Tapered electronic-photonic circuit crossing without optimization. (a) Normalized transverse electric (TE) field ($E_y$) distribution across a 100 nm isolation gap introduced in a tapered single-mode suspended waveguide at 1550 nm. (b) Time-averaged power flow along the optical propagation direction ($P_x$) crossing the isolation gap at 1550 nm. (c) Calculated transmission (red) and reflection (blue) showing a transmission (below 81.4%) and reflection (above 3.5%) across the full spectral range.
Figure S3: Geometry and domain for topology optimization. (a) Sketch of the EPCC design problem comprised of two identical design domains $\Omega_D$ (dark gray) separated by an air gap, an input waveguide to excite the design domain, and an output waveguide to collect the transmitted light. (b) One-fourth of the model and corresponding boundary conditions exploited to mimic the symmetric nature of the problem. (c) Symmetry along $y$-$z$ plane applied to the design domain and thus reducing the design region (red) to one-eighth. (d) Discretized design region employed to solve the EPCC design problem.

With respect to the design field, making it possible to use gradient-based optimization algorithms [9] to solve the optimization problem. Gradient-based methods are orders of magnitude more efficient than non-gradient-based methods, such as genetic algorithms [10]. Reference[11] provides a comparison of a gradient- and non-gradient-based method, as well as an introduction to gradient-based topology optimization. Furthermore, topology optimization allows designing and optimizing nanophotonic geometries with no restrictions except user-defined constraints to ensure, e.g., mechanical integrity and feasibility of fabrication [12–15].

We use topology optimization to design EPCC-structures as described in the following. The physics is modelled in the domain, $\Omega \subset \mathbb{R}^3$, containing a silicon membrane structure suspended
in an air background (see Fig. S3a). The structure consists of an input and an output rectangular waveguide (light gray in Fig. S3a) connected to a region to be designed, $\Omega_D \subset \Omega$ (dark gray in Fig. S3a), with an air gap situated at its center. We model the physics using Maxwell’s equations in the frequency domain by assuming time-harmonic field behaviour and consider a single-mode excitation of the input waveguide. The model domain is truncated using first-order absorbing boundary conditions on all exterior boundaries and input (output) port conditions on the input (output) waveguide. The model symmetries along the $x$-$z$ and $x$-$y$ planes are exploited to reduce the model size (Fig. S3b). Further, mirror symmetry is enforced on the design geometry around the center point in the air gap along the $y$-$z$ plane (Fig. S3c). The region to be designed is marked with red in Fig. S3, b and c. Finally, the design is discretized into piecewise constant elements and restricted to in-plane variations to conform to the fabrication process (Fig. S3d). The model problem is discretized and solved using the finite-element method [16] in COMSOL Multiphysics [17].

As we are interested in maximizing the transmittance, $T$, across the air gap, while minimizing the reflectance, $R$, back into the input waveguide, we consider the following figure of merit,

$$\Phi = \frac{T}{R + 1},$$

where $T$ denotes the transmittance across the EPCC and $R$ denotes the reflectance from the EPCC back into the input waveguide. To avoid numerical modelling issues and ensure a final binary design, we use a standard density filter, cf. Eq. (6) with filter radius $r_f$ and a smoothed threshold operation (Eq. (5)), with threshold sharpness, $\beta$, and threshold level, $\eta$ [18, 19]. We apply a continuation scheme for $\beta$ starting from the initial value $\beta_{\text{ini}}$ and increase this value by the growth factor $\beta_g$ at every iteration until a maximum value of $\beta_{\text{max}}$ is reached.

In order to enable the design of an EPCC operating across specific bandwidths, e.g., $\lambda \in [1500 \text{ nm}, 1600 \text{ nm}]$, we formulate a continuous constrained optimization problem, solved to
maximize the minimum of $\Phi$ over a set of $N$ targeted wavelengths. This problem can be written as

$$\max_{\xi(r)} \min_{\lambda_i} \Phi(E(\lambda_i, \tilde{\xi}))$$  \hspace{1cm} (2)

subject to

$$L_{EM}(n(\tilde{\xi}(r)), E(\lambda_i)) = f_i, \quad \forall \ i \in \{1, 2, ..., N\}$$  \hspace{1cm} (3)

$$n(\tilde{\xi}) = n_{Air} + \tilde{\xi}(n_{Si} - n_{Air}),$$  \hspace{1cm} (4)

$$\tilde{\xi} = \frac{\tanh(\beta \cdot \eta) + \tanh(\beta \cdot (\tilde{\xi} - \eta))}{\tanh(\beta \cdot \eta) + \tanh(\beta \cdot (1 - \eta))},$$  \hspace{1cm} (5)

$$-\left(\frac{r_f}{2\sqrt{3}}\right)^2 \nabla \tilde{\xi}(r) + \tilde{\xi}(r) = \xi(r),$$  \hspace{1cm} (6)

$$0 \leq \xi(r) \leq 1.$$  \hspace{1cm} (7)

Here, $r$ denotes the spatial coordinates, $\xi$ the design field, $L_{EM}(\varepsilon_r(\tilde{\xi}(r)), E) = f$ the Maxwell equations, $n$ the refractive index, and $E$ the electric field. The optimization problem is solved using the globally convergent method of moving asymptotes [9]. The final binary pixel-by-pixel design, obtained by solving the optimization problem, is converted to a set of closed curves, describing the interfaces between silicon and air. The post-processed design is used to compute the numerical performance of the device (see Fig. S4) and serves as the blueprint for the fabricated devices. Table S1 lists the parameters of materials, geometry, finite-element-discretization, and optimization model used to solve the EPCC optimization design problem.

We design an EPCC optimized for operating at $\lambda_1 = 1500$ nm and $\lambda_2 = 1600$ nm, i.e. targeting the bandwidth $\lambda \in [1500 \text{ nm}, 1600 \text{ nm}]$, by solving the optimization problem detailed above. The post-processed design, converted to a set of closed curves, is shown in Fig. S4. Figure S4a and b, illustrate the max-normalized TE-field ($E_y$) distribution and the time-averaged power flow along the optical propagation direction ($P_x$), across a 100 nm isolation gap at 1550 nm, respectively. Figure S4c shows the calculated transmission and reflection spectra of the topology-optimized device showing a transmission above 89.7% with reflection smaller than 1.2% over the 100 nm wavelength bandwidth centered at 1550 nm. The topology optimiza-
Figure S4: Curve-fitted topology-optimized EPCC design. (a) Normalized transverse electric (TE) field ($E_y$) distribution across the EPCC. (b) Time-averaged power flow along the optical propagation direction ($P_x$) for an EPCC constrained to a 100 nm isolation gap. (c) Calculated transmission (red) and reflection (blue) of the curve-fitted topology-optimized EPCC over 100 nm wavelength span centered at 1550 nm.
Table S1: Parameters used in the topology optimization of the EPCC.

| Parameter                          | Variable | Value    |
|------------------------------------|----------|----------|
| Targeted wavelength 1              | $\lambda_1$ | 1500 nm  |
| Targeted wavelength 2              | $\lambda_2$ | 1600 nm  |
| Refractive index of silicon        | $n_{Si}$  | 3.48     |
| Refractive index of air            | $n_{Air}$ | 1.0      |
| Model domain width                 | $\Delta w_\Omega$ | 1600 nm  |
| Model domain height                | $\Delta h_\Omega$ | 1200 nm  |
| Model domain length                | $\Delta l_\Omega$ | 6000 nm  |
| Waveguide width                    | $\Delta w_{WG}$ | 400 nm   |
| Waveguide height                   | $\Delta h_{WG}$ | 250 nm   |
| Waveguide length                   | $\Delta l_{WG}$ | 1450 nm  |
| Design domain width                | $\Delta w_{\Omega D}$ | 500 nm   |
| Design domain height               | $\Delta h_{\Omega D}$ | 250 nm   |
| Design domain length               | $\Delta l_{\Omega D}$ | 1500 nm  |
| Gap width                          | $\Delta gap$ | 100 nm   |
| Design domain brick element width  | $\Delta w_{FE,\Omega D}$ | 30 nm    |
| Design domain brick element height | $\Delta h_{FE,\Omega D}$ | 50 nm    |
| Design domain brick element length | $\Delta l_{FE,\Omega D}$ | 30 nm    |
| Initial guess for the design field | $\xi_{ini}$ | 0.1      |
| Filter radius                      | $r_f$    | 60 nm    |
| Thresholding level                 | $\eta$   | 0.5      |
| Initial thresholding sharpness     | $\beta_{ini}$ | 1.0      |
| Maximum thresholding sharpness     | $\beta_{max}$ | 64.0     |
| Increment factor                   | $\beta_g$ | 2.0      |
| Number of design iterations between each $\beta$-increase | $itr$ | 50       |

Note: The calculation is performed for the nominal device-layer thickness of 250 nm for the silicon-on-insulator (SOI) wafers. However, we measured the thickness of the device layer using variable-angle spectroscopy ellipsometry after fabrication and found a thickness of 240 nm. To better approximate the fabricated device the calculations presented in Fig. S4 (and in Figs. 1d-f and 2b in the main text) is carried out for a device-layer thickness of 240 nm. We attribute the excellent performance obtained for the slightly different device-layer thickness to an inherent robustness of our design, which is likely due to the broadband optimization procedure.
Figure S5: Comparison of curve-fitted and tapered topology-optimized EPCCs. Calculated optical transmission and reflection of (a) curve-fitted and (b) tapered topology-optimized design for 250 nm and 240 nm device thicknesses, corresponding to the nominal and measured device layer thickness, respectively.
By analyzing and simulating the topology-optimized design, we identify that some of the designed features are responsible for expanding the optical mode. Thus, as the final design step in order to simplify the design geometry, we replace these features with a parameter-optimized tapering section as shown in Fig. 1. In order to compare the performance of the tapered design with the curve-fitted topology-optimized design, we define a broadband figure of merit ($\Phi_b$) as,

$$\Phi_b = \frac{1}{N} \sum_{i=1}^{N} \frac{T(\lambda_i)}{R(\lambda_i) + 1}$$

(8)

Where, $N$ denotes the number of wavelengths at which the spectra are calculated, i.e., 11 (from 1500 to 1600 nm with a 10 nm interval) in Figs. 1f and S4c. Figure S5, a and b, shows the transmission and reflection spectra along with the corresponding broadband figure of merit ($\Phi_b$) of the curve-fitted and tapered topology-optimized design calculated for two different device thicknesses: (i) 250 nm corresponding to the original thickness of the device layer of the SOI wafer, and (ii) 240 nm corresponding to the thickness of the fabricated device. Here, two main observations can be made: (i) the 10 nm thinner device layer does not have a significant influence on the performance of the device and only leads to a small blue-shift in the transmission and reflection spectra showing the robustness of the designed EPCC to small variations in device thickness, and (ii) replacing the mode-expanding features with a tapering section results in an overall better performance, when averaged across the full 100 nm bandwidth. When comparing the performance at the two wavelengths for which the EPCC was initially designed, i.e. 1500 nm and 1600 nm (at 250 nm thickness) the curve-fitted design performs best.

In addition to the original design presented above and explored experimentally, we design a set of EPCCs for a few different isolation gaps including a very small, yet feasible, gap of 20 nm in order to illustrate the generality of our approach for routing optical and electrical signals in large-scale circuits. Encouraged by the already high transmission obtained for the 100 nm designs, we aim for reaching transmissions close to unity. Since the reflection is bound
Figure S6: Topology-optimized EPCCs with near-unity transmission. Calculated transmission (solid) and reflection (dashed) of the curve-fitted topology-optimized EPCCs for crossings with 20 nm (yellow), 60 nm (green), and 100 nm (purple) isolation gaps optimized for maximum transmission at 1550 nm corresponding to the designs shown in Fig. 4 in the main text.

by $T + R = 1$, we disregard the reflection in the figure of merit and simply define it as $\Phi = T$, where $T$ is power transmission across the isolation trench only at $\lambda = 1550$ nm. The curve-fitted topology-optimized design of these EPCCs are presented in Fig. 4 in the main text, and the calculated transmission and reflection are shown in Fig S6.

Fabrication of EPCC and nano-electro-mechanical switch

The samples are fabricated from undoped (100) SOI wafers (SOITEC) with a 3 $\mu$m buried oxide. The nominally undoped silicon device layer has a resistivity of $\sim$ 10 $\Omega$ cm, which is sufficiently low for making electrical contacts while imposing minimal optical absorption losses. The devices are patterned in positive-tone 180 nm chemically semi-amplified resist (Allresist CSAR 62) using 100 keV electron-beam lithography (Jeol 9500FSZ). A 20 nm aluminum decharging layer is deposited by thermal evaporation before the e-beam exposure and removed (60 s 2.38%
Figure S7: Fabricated curve-fitted topology-optimized EPCC. A scanning electron micrograph (30° tilted view) of the curve-fitted topology-optimized EPCC.

TMAH) prior to development (60 s amyl acetate, AR-600-546, 20 °C).

The patterns are transferred into the device layer using a continuous cryogenic (−19 °C) deep reactive ion etching (DRIE). The remaining resist is removed with a solvent (Microposit Remover 1165) and the sample surface is cleaned with a plasma descum. Figure S7 shows a scanning electron micrograph of the fabricated device. For the switch chip, an additional metalization is performed with a negative mask (2 μm nLOF) defined using maskless UV lithography (Heidelberg MLA150). The native oxide is removed with argon-ion sputtering, and, under the same vacuum, a 5 nm chromium adhesion layer and a 200 nm gold contact layer are deposited using e-beam evaporation, finally followed by lift-off (Microposit Remover 1165).

All devices are released with temperature- and pressure-controlled anhydrous (ethanol-assisted) vapor-phase hydrofluoric acid in two steps and with multiple chamber purges to avoid stiction in an SPTS Primaxx uEtch chamber. The first step, the release step, etches 530 nm over
3 cycles, which releases the waveguides. The second step, the deep etch, etches 4.2 µm over 2 cycles. The samples are placed on a 250 °C hotplate for 2 min prior to the etch, which is found to avoid residues from the etch.

**Experimental procedure**

Loss measurements of each device can be accurately performed by the cutback method, where the device loss is extracted by comparing the optical transmission through a varying number of devices, in this case $N = \{0, 1, 2, 3, 4, 5, 6\}$ in an optical transmission-line circuit as shown in Fig. 2a in the main text. A free-space optical setup is used to carry out transmission measurements on each circuit. A linearly polarized tunable laser (Santec TSL-710) is coupled to the chip via an input grating coupler while swept from 1500 to 1600 nm with a step of 0.5 nm. A grating coupler with 90-degree rotation, and hence orthogonal polarization, is used to couple the output light to a single-mode optical fiber, where the collected light is delivered to an optical spectrum analyzer (Yokogawa AQ6370D) for the spectral measurements. The orthogonal in- and output grating couplers eliminate the direct laser light reflection from the chip so that only light transmitted through the device is recorded.

Figure S8 shows raw transmission data of six nominally identical sets of photonic circuits in which each set is comprised of 7 transmission lines with 0 to 6 curve-fitted topology-optimized devices. Because of reflection at the location of the grating couplers, a Fabry-Perot cavity is created at each circuit that results in fringes in the transmission spectra. The effect of the Fabry-Perot cavity can be discarded by considering the upper peak envelope of the transmission spectra (bold lines in Fig S8, a-f), which is obtained by calculating the local maxima through a moving window of 5 data points (2 nm spectral window) followed by a moving average of the same window size.

In order to evaluate the experimental transmission of the curve-fitted topology-optimized
Figure S8: Characterization of curve-fitted topology-optimized EPCC. (a-f) Raw data and envelopes (bold lines) for 6 identical sets of photonic circuits each comprised of 7 transmission lines with 0 to 6 curve-fitted topology-optimized EPCCs.
Figure S9: Assessment of transmission efficiency of curved-fitted topology-optimized EPCC through the cut-back method. (a-f) Transmission of each set of circuits vs number of EPCCs at 1550 nm. The slope of the linear fit (black line) gives the propagation loss and thus the transmission efficiency.
Figure S10: Measured optical transmission of curve-fitted topology-optimized EPCC obtained through the cut-back method vs theory. The transmission spectrum is extracted by evaluating the transmission efficiency through the method shown in Fig. S9 at each data points corresponding to wavelengths of the tunable monochromatic light source used to conduct the experiment. The green shaded area represents the standard deviation from the mean transmission of the six replicas. Numerical calculations were performed for the measured device-layer thickness of 240 nm.

device, a linear fit is applied to each set of data associated with each nominally identical set of photonic circuit at each collected data point, i.e, each wavelength of the obtained transmission. The transmission loss, $L$, can thereby be determined by directly measuring the gradient of the fit, and thus the transmission efficiency of the device measured by $T = 10^{-\frac{L}{10}}$.

Figure S9, a-f, shows this process at $\lambda =1550$ nm. Similarly, the transmission spectrum of the device can be extracted from 1500 to 1600 nm for each set of photonic circuits that in total provides 6 transmission spectra extracted from 6 sets of nominally identical photonic circuits. Figure S10 illustrates the mean transmission (green curve) and the standard deviation from the
Figure S11: Characterization of tapered topology-optimized EPCC. (a-f) Raw data and envelopes (bold lines) for 6 identical sets of photonic circuits each comprised of 7 transmission lines with 0 to 6 tapered topology-optimized EPCCs.
Figure S12: Assessment of transmission efficiency of tapered topology-optimized EPCC through the cut-back method. (a-f) Transmission of each set of circuits vs number of EPCCs at 1550 nm. The slope of the linear fit (black line) gives the propagation loss and thus the transmission efficiency.
mean (green shaded area), obtained through conducting transmission measurements on in total 42 transmission line circuits, and compares it with the theoretical calculations for curve-fitted topology-optimized design. A similar approach, as shown in Figs. S11 and S12, is used to extract the transmission spectra of the tapered topology-optimized EPCC presented in Fig. 2b of the main text.

**In-plane nano-electro-mechanical add-drop switch using electronic-photonic circuit crossings**

Figure S13a shows an optical microscope image of the fabricated 2x2 add-drop switch. The chip layout includes a ground contact as well as four drive contacts for actuating the switching elements. The drive contacts are electrically connected to the switching elements and isolated from each other by the isolation trenches, the EPCCs, and the supporting buried-oxide layer, as shown in Fig. S13b. Each switching element is comprised of a directional coupler driven by two electrostatic comb-drive actuators [20] (see Fig. S14). The directional couplers comprise two suspended waveguides in which the coupling between them and thus the flow of photons is controlled by an adjustable gap separating the waveguides. The length and the initial gap of the directional coupler are chosen such that at zero bias voltage the input light is coupled to output 1 (Fig. S15a). By driving the comb-drive actuators, the gap and thus the coupling strength is adjusted such that the input light is coupled to output 2 (Fig. S15b). The switch network is characterized by sequentially applying voltages to the drive contacts. We use a revised version of the silicon bridge in the add-drop switch to provide higher optical transmission [21].

We characterize the electrical crosstalk between different nano-electro-mechanical actuators by routing light through parts of the switch network while applying a voltage to another actuator outside the optical path and measuring any spurious influence on the transmission. In detail, the driving signal is applied first to the bottom-right actuator (labeled as 1 in Fig. S13) and then
Figure S13: 2x2 micro-electro-mechanical add-drop switch chip. (a) Optical microscopy image of the 2x2 add-drop switch chip. Electrical pads are placed surrounding the photonic network and the voltages routed towards four nano-electro-mechanical directional couplers through multiple EPCCs. (b) 45° tilted scanning electron micrograph of the four switching elements taken at a low accelerating voltage of 5 kV. The charging effect in the SEM clearly shows how the EPCCs route the voltages from the contact pads to their corresponding nano-electro-mechanical directional coupler along mutually isolated electrical domains.
Figure S14: Fabricated nano-electro-mechanical directional coupler. (a) 45° tilted scanning electron micrograph of one switching element comprised of an adjustable directional coupler driven via two comb-drive actuators. (b) A zoomed-in scanning electron micrograph of the directional coupler.
Figure S15: Electric field plot of a non-actuated (a) and actuated (b) directional coupler.

Figure S16: Characterization of cross-talk and hysteresis in nano-electro-mechanical switch network based on EPCCs. (a) Measured transmission from $I_2$ to $T_2$ as a function of actuation voltage for two actuated comb drives showing no significant electrical crosstalk between the electrostatic actuators. (b) Measured transmission from $I_2$ to $T_2$ when sweeping the voltage in opposite directions, exhibiting no significant hysteresis.
to the top-left actuator (labeled as 3 in Fig. S13), while the input light is coupled to \( I_2 \) and the output light is collected from \( T_2 \). Figure S16a shows the switching operation for this experiment. When actuator 1 is driven, the input light is routed from \( T_2 \) to \( D_2 \) (see Fig. 3f of the main text), so \( T_2 \) depends on the actuation voltage. When actuator 3 is driven, \( T_2 \) does not depend on the actuation voltage showing that there is no significant crosstalk from actuator 3 to actuators controlling \( T_2 \), i.e., actuators 1 and 4. Note that in our particular experimental setup, only one actuator (in this case actuator 3) is driven and the other actuators are at floating potentials, which explains the small deviation in \( T_2 \) at high voltages shown in Fig. S16a.

Nano-electro-mechanical actuation allows in principle hysteresis-free actuation and we corroborate that by measuring the transmission in our switch while sweeping the driving voltage in opposite directions. The result is shown in Fig. S16b and no significant hysteresis is observed.

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