A 90 nm based CMOS biquad Low pass filter for 3 KHz wireless applications with 23.6 dB gain and low power

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Abstract. This paper proposes analog low pass filter based on CMOS biquad structure. The inverter based 6th order designed filter achieves the frequency bandwidth of 3 KHZ. The W and L ratio of PMOS transistor provides better gain of 23.6 dB. This proposed structure has been designed based on 90 nm technology with better IIP3. The filter structure is supplied by 1.8 v while consuming 72.3uW and the obtained noise value is maximum of 7.6 mV/sqrt(Hz) with low total harmonic distortion (THD) of 15.62 % comparatively good than the existing work.

1. Introduction

Analog filters are most suitable and broadly recommended in different wireless applications. The operational amplifier based filter design secures better linearity but may limit the loop gain. The CMOS based structure involves in the filter implementation with improved gain. The Transconductance – Capacitor (Gm-C), the Source follower based filter design and Inverter based design approaches are more popular in designing biquad filter [1], [2]. Developing a small MOS transistor as an active element not consider linearization & fitting it into a single branch [3] is certainly a compact and low power solutions. A single branch low pass filter considered to attain a wide range of tuning (KHz to GHz) is described in detail [4]. The added differences further established with the help of source follower [5], [6]. However based on the constraints the suitable approach is chosen for better performance of the filter. The Continuous time low pass filters are majorly used in bio-medical applications ranging from low to 10 KHz [7], [8] and for large frequency applications can be found in [9], [10] &[11]. The low pass filter is has been designed by cascading biquad structure, comprises complementary devices. The recent biquad structure is implemented using flipped voltage follower which utilizes less power [12]. In this brief we proposed a high gain wide range 6th order CMOS based biquad active filter utilizes MOS transistors designed by 90 nm technology achieves gain of 23.6 dB with lower power consumption. The rest of this paper is organizes as follows. Related works are discussed in section II, Section III describes the suggested biquad filter circuit implementation. The obtained results are discussed in section IV and Section V concludes with summary.

2. Related work

The conventional source follower and flipped source follower approach based designed filters were compared with wideband subthreshold source follower and implemented in [5]. The structure designed based on common gate(CG) makes to improve gain of the structure with tunable frequency of 50-450
MHz, 15 dB noise figure and IIIP3 is 12 dB. Second order butterworth tunable low pass filter is implemented based on Subthreshold source follower [2] achieves 4-100 Hz for bio signal applications. The implemented filter is fabricated in 180 nm technology & consumes 25.9 nW with gain of -3.25 dB. The major sources of noise are analysed and various capacitor values were utilised to tune the frequency. A nano power 4th order based band pass filter response is obtained for a 0.5 v supply with frequency ranges from 125 Hz to 16 KHz is implemented [3]. The filter circuit comprising of three MOS transistors and two capacitors. The filter is fabricated in 180nm technology with 2 nW power consumption. A composite source follower based 4th order continuous time filter was implemented in 180 nm technology for WLAN application supplied by 1.8 v. This topology achieves 17.5 dB IIIP3 and 79 dB of DR. The DC gain of -3.5 dB is achieved and consumes 2.25 mA [6]. A 4th order low pass analog filter is implemented with biquadratic cells, realized using the Super Source Follower topology. This circuit comprise of four MOS transistors and two capacitors. Two MOS transistors are used for signal processing and other two transistors for biasing purpose. The filter prototype is integrated in 180 nm CMOS technology. For a 33 MHz cut-off frequency, the circuit performs 18 dBm IIP3 at 2 MHz & 3 MHz, with current 770 µA for a single 1.8 v supply voltage [11]. The inductor less based biquad design with cross coupled NMOS transistor based design are suitable for high frequency bandpass multiband/multi-mode SDR applications [13]. This design utilizes 1.2 v with Q factor between 2 to 8. The simulated results shows the frequency of 2 GHz to 5 GHz and the power is 4.8mW. The fourth order filter uses the gain boosted Opamp secures the frequency range of 20 KHz-16 MHz while consuming power 19 mW [14].

3. Proposed filter design

The proposed sixth order low pass CMOS based filter implementation is shown in Figure 1. Three inverter based biquads are cascaded. Each section consists of second order design and each structure is increasing its order of the filter the overall efficiency is decreased. So designer should consider while designing the filter not exceeding the second order structure in each section. The inverter based structure is utilized in this filter implementation which consumes the supply voltage of 1.8 v. The PMOS1-PMOS6 and NMOS1-NMOS6 transistors are more suitable to achieve the expected gain and bandwidth with tunable capacitors C1, C2 and C3 ranges from 6 pf to 60 pf for low frequency applications. The condition of bias is to be varied over a frequency range and improved gain is established at minimum input signals. The transistors are biased in strong inversion region and saturation mode for higher performance in terms of speed.

| Transistor | W(nm) | L(nm) |
|------------|-------|-------|
| PM1        | 350   | 100   |
| PM2        | 350   | 100   |
| PM3        | 570   | 100   |
| PM4        | 570   | 100   |
| PM5        | 380   | 100   |
| PM6        | 380   | 100   |
| NM1-NM6    | 120   | 100   |

2
4. Results and discussion
The proposed structure is implemented in cadence virtuoso 90 nm technology with 1.8 v. The measured frequency and gain is discussed in this section. The capacitors C1, C2 and C3 are involving in frequency analysis to secure exact bandwidth of this proposed 6th order filter. The proposed filter is achieving the gain of 23.6 dB for the frequency around 2 KHz shown in the Figure 2, comparatively better than [2] and [3]. The bandwidth of the filter is achieved about 3.4 KHz with gain of 20.7 dB shown in Figure 3. If number of order of biquad is cascaded increases the performance and gain. The Figure 4. shows the gain of the filter comparing different order (second, four and six) or the cascaded stages and indicates the maximum gain at 6th order inverter based implementation.
Figure 2. Gain of the proposed filter

The PMOS and cross coupled NMOS transistor based structure improves the overall gain of the filter and achieves maximum gain. The width (W) and length (L) of the utilized transistors are tabulated in Table 1. The width of the PMOS transistor improves the gain through the value of transconductance. The capacitors are combining with the resistive elements by transistors and achieving expected frequency band.

Figure 3. Bandwidth of the proposed filter
Figure 4. Gain of the filter for different order

The overall gain can be improved by cascading the biquads, the order of the each sector is two and three stages are cascaded to achieve maximum gain. The second order achieves gain around 21 dB, fourth order design achieves the gain 22.5 dB and the 6th order achieves 23.6 dB as shown in Fig 4. The Gm-C (Transconductance-Capacitor) method is giving better performance and opamp VTA based approaches are giving better linearity than other designs. The gain and Phase responses are plotted in Figure 5, which shows the better linearity. The phase value is plotted and achieves -100 degree upto 3 KHz.

Figure 5. Response of the Gain and Phase
Figure 6. Noise of the filter

The noise and consumed power of the filter is shown in Figure 6 and Figure 7. The noise of the filter is suppressed due to proposed topology. The maximum noise of the filter is about 7.6 mV/sqrt(Hz) and the maximum power consumption of the filter is 72.3 uW satisfies the specifications compare than [5], [14].

Figure 7. Power consumption of the filter

The IIP3 of the filter is giving the positive values in dB shown in Figure 8, and gives the low THD (total Harmonic Distortion) is about 15.62 percent shown in Figure 9.
Figure 8. IIP3 of the filter

Figure 9. THD of the proposed filter
Table 2. Performance comparison of previous work with proposed work

| References | Proposed work | [2] | [3] | [5] | [13] | [14] |
|------------|---------------|-----|-----|-----|------|------|
| Technology (nm) | 90 | 180 | 180 | 180 | 65 | 65 |
| V_{dd}(v) | 1.8 | 1.8 | 0.5 | 1.8 | 1.2 | 1.8 |
| Order | 6 | 2 | 4 | 2 | 4 | 4 |
| Gain(dB) | 23.6 | -3.25 | -2.55 | 0 | -6.7 | 61 |
| IIP3(dB) | 83.81 | - | - | 26-31.5 | - | 22.1 |
| Bandwidth | 3 KHz | 100 | 3.2KHz-19.7KHz | 50-450MHz | 250-2500MHz | 0.02-16MHz |
| Noise | 7.6mV/sqrt(Hz) | 8.985 uVrms | 90uVrms | <15 | 14.2 V/sqrt(Hz) | 44.6 uVrms |
| Power | 72.3μW | 25.9nW | 2nW | 25mW | 4.8mW | 19mW |

5. Conclusion
This paper proposes the inverter based 6th order biquad low pass filter topology implemented in 90 nm technology. The proposed filter secures the gain of 23.6 dB for 3 KHz and achieves better IIP3 with output noise of 7.6mV/sqrt(Hz) while consumes 1.8 v. The filter consumes the power maximum of 72.3 uW. The designed low pass filter gives the better performance with THD of 15.62 % and suitable for different low voltage wireless applications.

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