T-count Optimized Design of Quantum Integer Multiplication

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Abstract—Quantum circuits of many qubits are extremely difficult to realize; thus, the number of qubits is an important metric in a quantum circuit design. Further, scalable and reliable quantum circuits are based on Clifford + T gates. An efficient quantum circuit saves quantum hardware resources by reducing the number of T gates without substantially increasing the number of qubits. Recently, the design of a quantum multiplier is presented by Babu [1] which improves the existing works in terms of number of quantum gates, number of qubits, and delay. However, the recent design is not based on fault-tolerant Clifford + T gates. Also, it has large number of qubits and garbage outputs. Therefore, this work presents a T-count optimized quantum circuit for integer multiplication with only $4 \cdot n + 1$ qubits and no garbage outputs. The proposed quantum multiplier design saves the T-count by using a novel quantum conditional adder circuit. Also, where one operand to the controlled adder is zero, the conditional adder is replaced with a Toffoli gate array to further save the T gates. To have fair comparison with the recent design by Babu and get an actual estimate of the T-count, it is made garbageless by using Bennett’s garbage removal scheme. The proposed design achieves an average T-count savings of 47.55% compared to the recent work by Babu. Further, comparison is also performed with other recent works by Lin et. al. [2], and Jayashree et. al. [3]. Average T-count savings of 62.71% and 26.30% are achieved compared to the recent works by Lin et. al., and Jayashree et. al., respectively.

I. INTRODUCTION

Among the emerging computing paradigms, quantum computing appears to be promising due to its applications in number theory, encryption, search and scientific computation [4] [5] [6] [7] [8] [9]. Quantum circuits for integer arithmetic operations such as addition, subtraction and multiplication are required in the quantum circuit implementations of many quantum algorithms in these areas. Thus, researchers have included dedicated libraries of basic quantum integer arithmetic functions for use in quantum programming languages such as Quipper and LIQUi and in quantum computing design tools such as those proposed in [10] [11] [12] and [13].

Quantum circuits do not lose information during computation and quantum computation can only be performed when the system consists of quantum gates. Thus, in any Quantum circuit there is a one-to-one mapping between the input and output vectors. Any constant inputs in the quantum circuit are called ancillae. Garbage output refers to any output which exists in the quantum circuit to preserve one-to-one mapping but is not one of the primary inputs nor a useful output. The inputs regenerated at the outputs are not considered garbage outputs [14]. Ancillae and garbage outputs are circuit overhead that need to be minimized.

The fault tolerant implementation of quantum circuits is gaining the attention of researchers because physical quantum computers are prone to noise errors [15] [16] [17] [18]. Fault tolerant implementations of quantum gates and quantum error correcting codes can be used to overcome the limits imposed by noise errors in implementing quantum computing [16] [19]. Recently, researchers have implemented quantum logic gates such as the controlled phase gate, controlled square-root-of-not gate, Toffoli gate, Fredkin gate and quantum full adder with the fault tolerant Clifford + T gate set due to its demonstrated tolerance to noise errors [20] [21]. However, the increased tolerance to noise errors comes with the increased implementation overhead associated with the quantum T gate [19] [21]. Because of the increased cost to realize the T gate, T-count has become an important performance measure for fault tolerant quantum circuit design [19] [22].

The design of quantum integer multiplication circuits has received notable attention in the literature. Garbage-less designs such as those in [23], [2] have significant T gate costs. Other works such as the recent design in [1] present T gate efficient designs but do not include the additional ancillae and T gate costs from eliminating garbage outputs in the cost calculations. As a result, the total quantum circuit may end up requiring $n$ extra qubits and the actual T gate cost may end up being doubled. While the integer multiplication circuits presented in existing works such as [2] and [1] are interesting designs, these integer multipliers have a significant gate overhead in terms of T-count. In this work, we present the design of a quantum integer multiplication circuit that is garbageless, requires $4 \cdot n + 1$ qubits and is optimized for T-count. The quantum integer multiplication circuit is based on a proposed quantum conditional addition circuit with no input carry that is garbageless and optimized for T-count. The proposed quantum integer multiplication circuit based on our proposed design is compared and is shown to be better than existing designs of quantum integer multiplication circuit in terms of T-count.

This paper is organized as follows. Section II presents background information on the Clifford + T fault tolerant quantum gate family, defines the T-count fault tolerant quantum gate family, defines the T-count performance measure, presents the algorithm that that the proposed quantum integer multiplication circuit is based on and describes the Bennett’s garbage removal scheme. In section III the design of the proposed quantum conditional addition circuit with no input carry is discussed. The design of the proposed quantum
integer multiplication circuit is presented in section IV.

II. BACKGROUND

| Type of Gate                  | Symbol | Matrix          |
|------------------------------|--------|-----------------|
| Not gate                     | N      | \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} |
| Hadamard gate                | H      | \begin{bmatrix} 1 & 1 \\ \sqrt{2} & -1 \end{bmatrix} |
| T gate                       | T      | \begin{bmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{bmatrix} |
| T gate Hermitian transpose   | T^†    | \begin{bmatrix} 1 & 0 \\ 0 & e^{-i\pi/4} \end{bmatrix} |
| Phase gate                   | S      | \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} |
| Phase gate Hermitian transpose| S^†   | \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} |
| Feynman gate                 | C      | \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} |

**TABLE I: The Clifford + T gate set**

![Fig. 1: The Toffoli gate and its fault tolerant Clifford + T gate implementation [21]. This fault tolerant Clifford + T gate implementation of the Toffoli gate has a T-count of 7.](image)

A. Quantum Gates

Fault tolerant implementation of quantum circuits is gaining the attention of researchers because physical quantum computers are prone to noise errors [15] [16] [18]. Recently, researchers have implemented quantum logic gates and circuits with the fault tolerant Clifford + T gate set due to its demonstrated tolerance to noise errors [20] [21]. The quantum integer multiplication circuit proposed in this work is comprised of Not, Feynman and Toffoli gates exclusively. Table I illustrates that the Feynman gate and the Not gate are in the set of gates that make up the Clifford + T gate family. The Toffoli gate is a 3 input, 3 output logic gate and has the mapping A, B, C to \( A \cdot B \oplus C \). In this work, we use the fault tolerant implementation of the Toffoli gate designed in [21] shown in figure 1.

B. Evaluation of Quantum Circuit Performance

Evaluating fault tolerant quantum circuit performance in terms of T-count is of interest to researchers because the fault tolerant implementation costs of the T gate is significantly greater than the fault tolerant implementation costs of the other Clifford + T gates [19] [22]. T-count is the total number of T gates or Hermitian transposes of the T gate in a quantum circuit. The Clifford + T implementation of the Toffoli gate illustrated in figure 1 has a T-count of 7.

C. Shift and Add Multiplication Algorithm

Algorithms for the multiplication of integers in hardware have drawn the interest of researchers. Researchers have developed many multiplication algorithms such as shift and add, Booth's algorithm and Karatsuba's algorithm. In this work, we present a quantum implementation of the shift and add multiplication algorithm optimized for T-count.

Consider the multiplication of two \( n \) bit numbers \( a \) and \( b \). At the end of computation, the shift and add multiplication algorithm returns the product \( p \) of the multiplication of the two numbers \( a \) and \( b \). The steps of the shift and add multiplication algorithm are illustrated for the multiplication of the number \( a \) by the number \( b \).

- Step 1: Assign the value 0 to the product \( p \).
- Step 2: For \( i = 0 : 1 : n - 1 \):
  - Calculate \( p = p + (a \land b_i) \cdot 2^i \).
- Step 3: Return product \( p \).

D. Related Work

The design of quantum integer multiplication circuits has received notable attention in the literature. However, most works target reversible computing and suffer from high garbage output costs [24] [25] [26]. The works proposed in [23], [27], [2] and [3] are appropriate for quantum computation. Papers [23] and [27] present quantum multiplication circuits in the quantum Fourier transform (QFT) domain. While garbage-less in nature, these circuits have significant Clifford + T gate costs [28]. The quantum integer multiplication circuits presented in papers [2] and [3] require significantly fewer quantum gates to realize and are garbage-less. The existing quantum integer multiplication circuits are made using Not, Square Root of Not, Feynman and Toffoli gates [2] [3] [1]. The Not and Feynman gates are members of the Clifford + T gate family [20]. The Square Root of Not and Toffoli gates can be realized with 7 and 15 Clifford + T gates respectively [21]. Further, in a recent work, a quantum integer multiplication circuit design is proposed [1]. The design presented in [1] consists of a new quantum AND circuit and quantum full adder circuit. The quantum AND circuit and quantum full adder are created with Feynman gates and square root of not gates. The multiplication circuit itself is based on a two step algorithm: (i) create all partial products with the quantum AND circuit and (ii) combine all partial products with the quantum full adder. To reduce circuit depth, the partial products are realized in parallel. Further, to reduce the depth of the partial product addition, a design methodology based on a partial product addition tree is used. While the design in [1] is optimized in terms of depth, this design suffers from significant ancillae and garbage output costs. While the integer multiplication circuits presented in papers [2], [3] and [1] are interesting designs, these integer multipliers have significant gate overhead in terms of T-count.

E. Methodology to Remove Garbage Outputs from Quantum Integer Multiplication Circuit Designs

In section II-D we presented existing quantum integer multiplication circuits that are garbageless in nature. However,
other recent works (such as the design in by Babu ([1])) that show promise in the terms of T-count suffer from significant ancillae and garbage output overhead. In order to be usable in quantum computing, these designs must be made garbageless in nature. We can apply the Bennett’s garbage removal scheme to make such designs garbageless [29].

Consider the multiplication of two bits numbers $a$ and $b$ stored in quantum registers $|A\rangle$ and $|B\rangle$ by a design such as the one in [1]. At the end of computation, the quantum registers $|A\rangle$ and $|B\rangle$ will keep the values $a$ and $b$ respectively. The product of $a$ and $b$ will appear on a quantum register $|P\rangle$ that is initialized with $|P_i\rangle = 0$ for $0 \leq i \leq 2 \cdot n - 1$. Further, there will be an additional quantum register $|G\rangle$ that is initialized to 0. The quantum register $|G\rangle$, at the end of computation, will hold the garbage outputs.

The Bennett’s garbage removal scheme removes the garbage outputs by applying the logical reverse of the original design to the quantum registers $|A\rangle$, $|B\rangle$, $|P\rangle$ and $|G\rangle$. To preserve the product of $a$ and $b$, the contents of quantum register $|P\rangle$ is copied to another quantum register $|Y\rangle$ that is initialized with $|Y_i\rangle = 0$ for $0 \leq i \leq 2 \cdot n - 1$. Therefore, at the end of computation, the quantum registers $|A\rangle$ and $|B\rangle$ will keep the values $a$ and $b$ respectively. At the end of computation, the quantum register $|P\rangle$ that originally stored the product will be restored to the value 0. Finally, the quantum register $|G\rangle$ that originally stored the garbage outputs will be restored to the value 0 at the end of computation.

The steps of the Bennett’s garbage removal scheme are explained below. The methodology is generic and can be used on any quantum integer multiplication circuit that has garbage outputs. An illustrative example of the methodology for a generic multiplication circuits with garbage outputs is also shown. Figure 2 illustrates steps 1 through 3.

**Figure 2:** Generation of garbageless quantum multiplication circuit: steps 1-3.

- **Step 1:** At quantum registers $|A\rangle$, $|B\rangle$, $|P\rangle$ and $|G\rangle$ apply the quantum multiplication circuit such that the registers $|A\rangle$ and $|B\rangle$ will maintain the same value, location $|P\rangle$ will hold the product and location $|G\rangle$ will contain the garbage outputs.

- **Step 2:** For $i = 0 : 1 : 2 \cdot n - 1$
  At locations $|P_i\rangle$ and $|Y_i\rangle$ apply a Feynman gate such that the location $|P_i\rangle$ will maintain the same value while location $|Y_i\rangle$ is transformed to the value in location $|P_i\rangle$.

- **Step 3:** At quantum registers $|A\rangle$, $|B\rangle$, $|P\rangle$ and $|G\rangle$ apply the logical reverse quantum the multiplication circuit such that the registers $|A\rangle$ and $|B\rangle$ will maintain the same value, location $|P\rangle$ will be restored to the value 0 and location $|G\rangle$ will be restored to the value 0.

This methodology, while able to remove garbage outputs from a quantum multiplication designs such as the one in [1], does add additional quantum gates and qubit costs. The methodology will add $2 \cdot n + 1$ ancillae to the design and increase the T-count by a factor of at least two.

**III. DESIGN METHODOLOGY OF PROPOSED QUANTUM CONDITIONAL ADDITION CIRCUIT WITH NO INPUT CARRY**

We present the design of the proposed quantum conditional addition (Ctrl-Add) circuit with no input carry. The design has no garbage outputs. The proposed method improves the T-count of the quantum Ctrl-Add circuit compared to existing design approaches which have no garbage outputs. Consider the conditional addition of two $n$-bit numbers $a_i$ and $b_i$ stored at quantum registers $|A_i\rangle$ and $|B_i\rangle$ respectively (where $0 \leq i \leq n - 1$). The addition of $a_i$ and $b_i$ is conditioned on the value of the 1 bit number $ctrl$ stored at quantum register $|Ctrl\rangle$. Further, consider that quantum register locations $|A_0\rangle$ and $|A_{n+1}\rangle$ are initialized with $z \in 0, 1$. At the end of the computation, the quantum register $|B_i\rangle$ will have the value $s_i$ while the quantum register $|A_i\rangle$ keeps the value $a_i$. The additional quantum register locations $|A_{n}\rangle$ that initially stored the value $z$ will have the value $s_n$ at the end of computation. Thus, $|A_{n}\rangle$ will have the value $s_n$ when $z = 0$. Further, the additional quantum register location $|A_{n+1}\rangle$ that initially stored the value $z$ will have the value $z$ at the end of computation. Here $s_i$ is the sum bit and is defined as:

$$s_i = \begin{cases} a_i \oplus b_i \oplus c_i & \text{if } 0 \leq i \leq n - 1 \text{ and } ctrl = 1 \\ c_n & \text{if } i = n \text{ and } ctrl = 1 \\ b_i & \text{if } 0 \leq i \leq n - 1 \text{ and } ctrl = 0 \\ z & \text{if } i = n \text{ and } ctrl = 0 \end{cases}$$

where $c_i$ is the carry bit and is defined as:

$$c_i = \begin{cases} 0 & \text{if } i = 0 \\ a_{i-1} \cdot b_{i-1} \oplus b_{i-1} \cdot c_{i-1} \oplus a_{i-1} \cdot c_{i-1} & \text{if } 1 \leq i \leq n \end{cases}$$

The proposed design methodology of generating the quantum Ctrl-Add circuit with no input carry minimizes the garbage outputs by using the strategy first reported in [30]. When $ctrl = 1$, the carry bits $c_i$ are produced based on the inputs $a_{i-1}, b_{i-1}$ and the carry bit $c_{i-1}$ from the previous stage. All of the generated carry bits $c_i$ are stored on the
quantum register $|A_i\rangle$ which initially was used to store $a_i$ for $0 \leq i \leq n - 1$. After the generated carry bits are used in further computation, the quantum register $|A_i\rangle$ is restored to the value $a_i$ while the quantum register $|B_i\rangle$ stores the sum bit $s_i$ for $0 \leq i \leq n - 1$.

The proposed design methodology of generating the quantum Ctrl-Add circuit with no input carry is explained below. The proposed methodology is generic and can design a quantum Ctrl-Add circuit with no input carry of any size. The steps involved in the proposed methodology are shown in figure 3. Steps 5 through 7 of the methodology are shown in figure 4.

A. Steps of Design Methodology

- **Step 1:** For $i = 1 : 1 : n - 1$
  At each pair of quantum register locations $|A_i\rangle$ and $|B_i\rangle$ apply a Feynman gate such that the location $|A_i\rangle$ will maintain the same value, while location $|B_i\rangle$ is transformed to $|A_i \oplus B_i\rangle$.

- **Step 2:** Step 2 has the following two sub-steps:
  - **Step 1:** At quantum register locations $|Ctrl\rangle, |A_{n-1}\rangle$ and $|A_n\rangle$ apply a Toffoli gate such that the locations $|Ctrl\rangle, |A_{n-1}\rangle$ and $|A_n\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.
  - **Step 2:** For $i = n - 2 : -1 : 1$
    At each pair of quantum register locations $|A_i\rangle$ and $|A_{i+1}\rangle$ apply a Feynman gate such that the location $|A_i\rangle$ will maintain the same value while the location $|A_{i+1}\rangle$ is transformed to $|A_i \oplus A_{i+1}\rangle$.

- **Step 3:** For $i = 0 : 1 : n - 2$
  At quantum register locations $|B_i\rangle, |A_i\rangle$ and $|A_{i+1}\rangle$ apply a Toffoli gate such that $|B_i\rangle$ and $|A_i\rangle$ and $|A_{i+1}\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.

- **Step 4:** Step 4 has the following four sub-steps:
  - **Step 1:** At quantum register locations $|B_{n-1}\rangle, |A_{n-1}\rangle$ and $|A_{n+1}\rangle$ apply a Toffoli gate such that the locations $|B_{n-1}\rangle, |A_{n-1}\rangle$ and $|A_{n+1}\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.
  - **Step 2:** At quantum register locations $|Ctrl\rangle, |A_{n+1}\rangle$ and $|A_n\rangle$ apply a Toffoli gate such that the locations $|Ctrl\rangle, |A_{n+1}\rangle$ and $|A_n\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.
  - **Step 3:** At quantum register locations $|B_{n-1}\rangle, |A_{n-1}\rangle$ and $|A_{n+1}\rangle$ apply a Toffoli gate such that the locations $|B_{n-1}\rangle, |A_{n-1}\rangle$ and $|A_{n+1}\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.
  - **Step 4:** At quantum register locations $|Ctrl\rangle, |A_{n+1}\rangle$ and $|B_{n-1}\rangle$ apply a Toffoli gate such that the locations $|Ctrl\rangle, |A_{n+1}\rangle$ and $|B_{n-1}\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.

- **Step 5:** For $i = n - 2 : -1 : 0$. Step 5 has the following two sub-steps:
  - **Step 1:** At quantum register locations $|B_i\rangle, |A_i\rangle$ and $|A_{i+1}\rangle$ apply a Toffoli gate such that the locations $|B_i\rangle, |A_i\rangle$ and $|A_{i+1}\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.
  - **Step 2:** At quantum register locations $|Ctrl\rangle, |A_i\rangle$ and $|B_i\rangle$ apply a Toffoli gate such that the locations $|Ctrl\rangle, |A_i\rangle$ and $|B_i\rangle$ are passed to the inputs $A, B, C$ respectively, of the Toffoli gate.

- **Step 6:** For $i = 1 : 1 : n - 2$
  At each pair of quantum register locations $|A_i\rangle$ and $|A_{i+1}\rangle$ apply a Feynman gate such that the location $|A_i\rangle$ will maintain the same value while the location $|A_{i+1}\rangle$ is transformed to $|A_i \oplus A_{i+1}\rangle$.

- **Step 7:** For $i = 1 : 1 : n - 1$
  At each pair of quantum register locations $|A_i\rangle$ and $|B_i\rangle$ apply a Feynman gate such that the location $|A_i\rangle$ will maintain the same value, while location $|B_i\rangle$ is transformed to $|A_i \oplus B_i\rangle$.

Fig. 3: Generation of a 4-qubit quantum Ctrl-Add circuit with no input carry: steps 1-4.
Theorem: Let a and b be two n bit binary numbers represented as $a_i$ and $b_i$, $ctrl \in 0, 1$ be a 1-bit input and $z \in 0, 1$ is another 1-bit input, where $0 \leq i \leq n - 1$, then the proposed design methodology results in a quantum Ctrl-Add circuit with no input carry that functions correctly. The proposed design methodology designs a n-bit Ctrl-Add circuit that produces the sum output $s_i$ at the quantum register where $b_i$ is stored, while it restores the quantum register where $a_i$ is initially stored to the value $a_i$ for $0 \leq i \leq n - 1$. Further, the additional quantum register locations $|A_n\rangle$ and $|A_{n+1}\rangle$ where $z$ is initially stored will have the values $z \oplus s_n$ and $z$ respectively.

Proof: The proposed design methodology will make the following changes to the inputs. An example of the transformation of the inputs states after Steps 1 through 4 is illustrated for a 4-bit quantum Ctrl-Add circuit with no input carry in figure 3. An example of the transformation of the inputs states after Steps 5 through 7 is illustrated for a 4-bit quantum Ctrl-Add circuit with no input carry in figure 4.

- Step 1: Step 1 of the proposed design methodology transforms the input states $|a_i\rangle$ and $|b_i\rangle$ for $0 \leq i \leq n - 1$ to:

$$|b_0\rangle|a_0\rangle \left( \bigoplus_{i=1}^{n-1} |b_i \oplus a_i\rangle|a_i\rangle \right) |z\rangle|z\rangle$$  \hspace{1cm} (3)

- Step 2: Step 2 of the proposed design methodology transforms the input states $|a_i\rangle$ and $|b_i\rangle$ for $0 \leq i \leq n - 1$ to:

$$|b_0\rangle|a_1\rangle \left( \bigoplus_{j=2}^{n-1} |b_i \oplus a_i\rangle|a_i \oplus a_{i-1}\rangle \right)$$  \hspace{1cm} (4)

Step 2 of the proposed design methodology transforms the remaining input states $|a_n\rangle, |a_{n+1}\rangle$ to:

$$|z \oplus a_{n-1} \cdot ctrl\rangle|z\rangle$$  \hspace{1cm} (5)

- Step 3: Step 3 has $n - 1$ Toffoli gates. The first Toffoli gate takes $b_0$, $a_0$ and $a_\bar{1}$ as inputs and produces the output as $b_0$, $a_0$ and $a_1 \oplus c_1$ where $c_1$ represents the generated output carry after the addition of $b_0$ and $a_0$. The remaining $n - 2$ Toffoli gates take $a_i \oplus b_i$, $a_i \oplus c_i$ and $a_i \oplus a_{i+1}$ as inputs and produces the outputs as $a_i \oplus b_i$, $a_i \oplus c_i$ and $a_{i+1} \oplus c_{i+1}$. Thus, after Step 3, input states are transformed to:

$$|b_0\rangle|a_0\rangle \left( \bigoplus_{i=1}^{n-1} |b_i \oplus a_i\rangle|a_i \oplus c_i\rangle \right) |z \oplus a_{n-1} \cdot ctrl\rangle|z\rangle$$  \hspace{1cm} (6)

- Step 4: Step 4 has four Toffoli gates. The first Toffoli gate takes $a_{n-1} \oplus b_{n-1}$, $c_{n-1} \oplus a_{n-1}$ and $z$ as inputs to produce the outputs as $a_{n-1} \oplus b_{n-1}$, $c_{n-1} \oplus a_{n-1}$ and $z \oplus (\bar{a}bc + abc)$ where $a, b$ and $c$ are the compliments of $a, b$ and $c$. The third output of the Toffoli gate is $z \oplus (\bar{a}bc + abc)$ because the gate realizes $A \cdot B \oplus C$ where $A, B$ and $C$ are inputs to the Toffoli gate. Thus, the Toffoli gate will have the third input as $z \oplus (a_{n-1} \oplus b_{n-1}) \cdot (c_{n-1} \oplus a_{n-1}) = z \oplus (\bar{a}bc + abc)$. The second Toffoli gate takes $ctrl, z \oplus (\bar{a}bc + abc)$ and $z \oplus a_{n-1} \cdot ctrl$ is inputs to produce the outputs as $ctrl, z \oplus (\bar{a}bc + abc)$ and $z \oplus c_n \cdot ctrl$. Note that $z \oplus c_n \cdot ctrl = z \oplus s_n$. The third Toffoli gate takes $a_{n-1} \oplus b_{n-1}$, $c_{n-1} \oplus a_{n-1}$ and $z \oplus (\bar{a}bc + abc)$ as inputs to produce the outputs as $a_{n-1} \oplus b_{n-1}$, $c_{n-1} \oplus a_{n-1}$ and $z$. The fourth Toffoli gates takes the inputs $ctrl, a_{n-1} \oplus c_{n-1}$ and $a_{n-1} \oplus b_{n-1}$ to produce the outputs as $ctrl, a_{n-1} \oplus c_{n-1}$ and $b_{n-1} \oplus c_{n-1} \cdot ctrl$. Thus, Step 4 transforms the input states $|a_i\rangle$ and $|b_i\rangle$ for $0 \leq i \leq n - 2$ to:

$$|s_0\rangle|a_0\rangle \left( \bigoplus_{i=1}^{n-2} |b_i \oplus a_i\rangle|a_i \oplus c_i\rangle \right)$$  \hspace{1cm} (7)

Step 4 transforms the remaining input states $|a_{n-1}\rangle, |b_{n-1}\rangle, |a_n\rangle, |a_{n+1}\rangle$ to:

$$|b_{n-1} \oplus c_{n-1} \cdot ctrl\rangle|a_{n-1} \oplus c_{n-1} \cdot ctrl\rangle|z \oplus s_n\rangle|z\rangle$$  \hspace{1cm} (8)
Step 5:
Step 5 has $2 \cdot n - 2$ Toffoli gates. The transformations performed by the first $2 \cdot n - 4$ Toffoli gates are illustrated below:

For $i = n - 1 : 1 : 2$: Toffoli gate $2 \cdot i$ takes $b_{i-1} \oplus a_{i-1}$, $c_{i-1} \oplus a_i$ as inputs to produce the outputs as $b_{i-1} \oplus a_{i-1}$, $c_{i-1} \oplus a_i$ and $a_{i-1} \oplus a_i$. Toffoli gate $2 \cdot i - 1$ takes $\text{ctrl}$, $c_i \oplus a_{i-1}$ and $b_{i-1} \oplus a_{i-1}$ as inputs to produce the outputs as $\text{ctrl}$, $c_i \oplus a_{i-1}$ and $b_{i-1} \oplus c_{i-1} \cdot \text{ctrl}$.

Toffoli gate $2 \cdot n - 3$ takes $b_0$, $a_0$ and $c_1 \oplus a_1$ as inputs to produce the outputs as $b_0$, $a_0$ and $a_1$. Toffoli gate $2 \cdot n - 2$ takes $\text{ctrl}$, $a_0$ and $b_0$ as inputs to produce the outputs as $\text{ctrl}$, $a_0$ and $s_0$. Thus, Step 5 transforms the input states $|a_i\rangle$ and $|b_i\rangle$ for $i = 0$ and $i = 1$ to:

$$|s_0\rangle|a_0\rangle|b_1 \oplus c_1 \cdot \text{ctrl}|a_1\rangle$$

(9)

Step 5 transforms the input states $|a_j\rangle$ and $|b_i\rangle$ for $2 \leq j \leq n + 1$ and $2 \leq i \leq n - 1$ to:

$$\left(\bigoplus_{i=2}^{n-1} |b_i \oplus c_i \cdot \text{ctrl}|a_i \oplus a_{i-1}\rangle\right) |z \oplus s_n\rangle|z\rangle$$

(10)

Step 6:
Step 6 of the proposed design methodology transforms the input states to:

$$|s_0\rangle|a_0\rangle \left(\bigoplus_{i=1}^{n-1} |b_i \oplus c_i \cdot \text{ctrl}|a_i\rangle\right) |z \oplus s_n\rangle|z\rangle$$

(11)

Step 7:
Step 7 of the proposed design methodology transforms the input states to:

$$\left(\bigoplus_{i=0}^{n-1} |s_i\rangle|a_i\rangle\right) |z \oplus s_n\rangle|z\rangle$$

(12)

Thus, the proposed design methodology transforms the quantum register where $b_i$ is initially stored to the sum $s_i$, while the quantum register where $a_i$ is originally stored will be restored to the value $a_i$. The additional quantum register locations $|A_n\rangle$ and $|A_{n+1}\rangle$ where $z$ is initially stored will have $z \oplus s_n$ and $z$ respectively. Hence, the proposed design methodology generates a quantum Ctrl-Add circuit with no input carry that is functionally correct.

B. Cost Analysis

TABLE II: Comparison of quantum Ctrl-Add circuits

| qubits | 1     | 2     | Proposed |
|--------|-------|-------|----------|
| T-count | $56 \cdot n$ | $28 \cdot n + 7$ | $21 \cdot n + 14$ |
| ancillae | $2 \cdot n + 1$ | $2 \cdot n + 1$ | $2 \cdot n + 1$ |

The T-count of the proposed quantum Ctrl-Add circuit with no input carry is illustrated shortly for each step of the proposed design methodology. We calculate total T-count for the proposed quantum Ctrl-Add circuit with no input carry by summing the T-count for each step of the proposed design methodology.

Step 1:
- The T-count for this Step is 0.

Step 2:
- The T-count for this step is 7.

Step 3:
- The T-count for this Step is $7 \cdot (n - 1)$.

Step 4:
- The T-count for this Step is 28.

Step 5:
- The T-count for this Step is $14 \cdot (n - 1)$.

Step 6:
- The T-count for this Step is 0.

Step 7:
- The T-count for this Step is 0.

Thus, the total T-count of an $n$ bit proposed quantum Ctrl-Add circuit with no input carry is given as:

$$7 + 7 \cdot (n - 1) + 28 + 14 \cdot (n - 1) = 21 \cdot n + 14$$

A comparison of the proposed quantum Ctrl-Add circuit with no input carry with existing designs is illustrated in table II which shows that the proposed design has a lower T-count compared to existing designs. Table II illustrates that the order of growth of the T-count for the proposed quantum Ctrl-Add circuit with no input carry is linear. Thus, the T-count is $O(n)$. Further, table II shows that the savings in the T-count of the proposed design does not come at the cost of additional qubits. Also, table II illustrates that the order of growth of the qubit cost for the proposed quantum Ctrl-Add circuit with no input carry is linear. Thus, the qubit cost is $O(n)$.

Table III shows the comparison in terms of the T-count and shows that the proposed quantum Ctrl-Add circuit with no input carry achieves improvement ratios ranging from

| qubits | 1     | 2     | Proposed |
|--------|-------|-------|----------|
| T-count | $56 \cdot n$ | $28 \cdot n + 7$ | $21 \cdot n + 14$ |
| ancillae | $2 \cdot n + 1$ | $2 \cdot n + 1$ | $2 \cdot n + 1$ |

1 is the design by Lin et. al. [2]
2 is the design by Jayashree et. al. [3]
56.25% to 62.30% and 17.65% to 24.76% compared to the designs presented in Lin et al. ([2]) and Jayashree et al. ([3]) respectively.

**IV. DESIGN OF PROPOSED QUANTUM INTEGER MULTIPLICATION CIRCUIT**

![Graphical representation of components used in the proposed quantum integer multiplication circuit.](image)

The proposed quantum integer multiplication circuit is designed without garbage outputs and with a lower T-count compared to the existing design approaches which have no garbage outputs. The quantum integer multiplication circuit is based on the proposed quantum Ctrl-Add circuit with no input carry and the Toffoli gate array. Figure 5 shows the graphical representation of components used in the quantum integer multiplication circuit.

Consider the multiplication of two bit numbers \(a\) and \(b\) stored in quantum registers \(|A\rangle\) and \(|B\rangle\) respectively. Further, consider a quantum register \(|P_i\rangle\) where each qubit \(|P_i\rangle\) where \(0 \leq i \leq 2 \cdot n\) is initialized with \(z = 0\). At the end of the computation, the quantum registers \(|A\rangle\) and \(|B\rangle\) keep the values respectively. Further, at the end of computation, the quantum register \(|P_1\rangle\) that initially stored instances of the value \(z\) will have the value \(p_i\) for \(0 \leq i \leq 2 \cdot n - 1\). Here, \(p_i\) is the \(i\)th bit of the product of \(a\) and \(b\). The quantum register location \(|P_2\rangle\) is restored to the value 0 at the end of computation.

The proposed design methodology reduces the T-count by using the proposed quantum Ctrl-Add circuit with no input carry designed in section III. Further, the proposed design methodology selectively replaces instances of the quantum Ctrl-Add circuit with no input carry with a Toffoli gate array at the appropriate places.

The proposed design methodology of generating the quantum integer multiplication circuit is explained below. The proposed methodology is generic and can design a quantum integer multiplication circuit of any size. The steps involved in the proposed methodology are presented for the conditional addition of two \(n\) bit numbers \(a_i\) and \(b_i\), where \(0 \leq i \leq n - 1\). An illustrative example of the generation of a quantum integer multiplication circuit that can perform the multiplication of two 4 bit numbers \(a = a_0 \cdots a_3\) and \(b = b_0 \cdots b_3\) is shown in figure 6. The quantum circuit after each Step of the methodology is shown in figure 6.

**A. Steps of Design Methodology**

- **Step 1:** For \(i = 0 : 1 : n - 1\) At locations \(|B_0\rangle, |A_i\rangle\) and \(|P_i\rangle\) apply a Toffoli gate such that the locations \(|B_0\rangle\) and \(|A_i\rangle\) will maintain the same value while location \(|P_i\rangle\) transforms to the value \(b_0 \cdot a_i\).

- **Step 2:** Step 2 has the following three sub-steps
  - **Step 1:** For \(i = 1 : 1 : n\) Apply the pair of locations \(|A_{i-1}\rangle\) and \(|P_i\rangle\) to a quantum Ctrl-Add circuit with no input carry such that the location \(|A_{i-1}\rangle\) will maintain the same value while location \(|P_i\rangle\) transforms to the sum bit \(s_{i-1}\).
  - **Step 2:** Apply location \(|B_1\rangle\) to the quantum Ctrl-Add circuit such that the operation of the Ctrl-Add circuit will be conditioned on the value of \(|B_1\rangle\).
  - **Step 3:** Apply locations \(|P_{n+1}\rangle\) and \(|P_{n+2}\rangle\) to the quantum Ctrl-Add circuit such that location \(|P_{n+1}\rangle\) transforms to the sum bit \(s_n\) and location \(|P_{n+2}\rangle\) will maintain the same value at the end of computation.

- **Step 3:** Step 3 is repeated \(n - 2\) times. For \(j = 2 : 1 : n - 1\) This Step has the following three sub-steps
  - **Step 1:** For \(i = 0 : 1 : n - 1\) Apply the pair of locations \(|A_i\rangle\) and \(|P_{i+j}\rangle\) to a quantum Ctrl-Add circuit with no input carry such that the location \(|A_i\rangle\) will maintain the same value while location \(|P_{i+j}\rangle\) transforms to the sum bit \(s_i\).
  - **Step 2:** Apply location \(|B_j\rangle\) to the quantum Ctrl-Add circuit such that the operation of the Ctrl-Add circuit will be conditioned on the value of \(|B_j\rangle\).
  - **Step 3:** Apply locations \(|P_{n+j}\rangle\) and \(|P_{n+j+1}\rangle\) to the quantum Ctrl-Add circuit such that location \(|P_{n+j}\rangle\) transforms to the sum bit \(s_n\) and location \(|P_{n+j+1}\rangle\) will maintain the same value at the end of computation.

**Theorem:** Let \(a\) and \(b\) be two \(n\) bit binary numbers represented as \(a_i\) and \(b_i\) and \(p\) is another \(2 \cdot n\) bit binary number represented as \(p_i\) and \(p_i = 0\), then the proposed design methodology results in a quantum integer multiplication circuit that functions correctly. The proposed design methodology designs an \(n\) bit multiplication circuit that gets the product output at the quantum register where \(p_i\) is initially stored while the locations where \(a\) and \(b\) are initially stored are restored to the values \(a\) and \(b\) respectively.

**Proof:** The proposed design methodology will make the following changes on the inputs. For illustrative purposes, the transformation of the input states for a four bit quantum integer multiplication circuit after each Step is shown in figure 6.:

- **Step 1:** Step 1 of the proposed methodology transforms the input states to:

\[
\begin{bmatrix}
|A_{i-1}\rangle \\
|B_i\rangle \\
|B_0 \cdot A_i\rangle \\
|0\rangle
\end{bmatrix}
\]

- **Step 2:** Step 2 has a Ctrl-Add circuit with no input carry which takes the inputs \(a_i\) and \(p_{i+1}\) for \(0 \leq i \leq n - 1\) and the input \(b_1\). At the end of computation the locations \(p_{i+1}\) will have the value \(s_i\) for \(0 \leq i \leq n - 1\). Further,
at the end of computation the locations which originally stored \( b_1 \) and \( a_i \) are restored to the values \( b_1 \) and \( a_i \), respectively where \( 0 \leq i \leq n - 1 \). Thus, after Step 2 the input states are transformed to:

\[
\left( \bigotimes_{i=0}^{n-1} |A_i\rangle \right) \left( \bigotimes_{i=0}^{n-1} |B_i\rangle \right) |p_0\rangle|p_1\rangle \left( \bigotimes_{i=2}^{n+2} |s_{i-2}\rangle \right) \left( \bigotimes_{i=n+3}^{2n} |0\rangle \right)
\]

(15)

- **Step 3:** Step 3 is repeated a total of \( n - 2 \) times.
  - For Iteration one of Step 3, a quantum Ctrl-Add circuit with no input carry takes the inputs as \( a_i \) and \( p_{i+2} \) for \( 0 \leq i \leq n - 1 \) and the input \( b_2 \). At the end of computation the locations \( p_{i+2} \) will have the value \( s_i \) for \( 0 \leq i \leq n - 1 \). Further, at the end of computation the locations which originally stored \( b_2 \) and \( a_i \) are restored to the values \( b_2 \) and \( a_i \), respectively where \( 0 \leq i \leq n - 1 \). Thus, after Iteration one of Step 3 the input states are transformed to:

\[
\left( \bigotimes_{i=0}^{n-1} |A_i\rangle \right) \left( \bigotimes_{i=0}^{n-1} |B_i\rangle \right) |p_0\rangle|p_1\rangle |p_{i+2}\rangle \left( \bigotimes_{i=2}^{n+2} |s_{i-2}\rangle \right) \left( \bigotimes_{i=n+3}^{2n} |0\rangle \right)
\]

(16)

- For Iteration \( j \) of Step 3 where \( 2 \leq j \leq n - 3 \), a quantum Ctrl-Add circuit with no input carry takes the inputs as \( a_i \) and \( p_{i+1+j} \) for \( 0 \leq i \leq n - 1 \) and the input \( b_1+j \). At the end of computation the locations \( p_{i+1+j} \) will have the value \( s_i \) for \( 0 \leq i \leq n - 1 \). Further, at the end of computation the locations which originally stored \( b_1+j \) and \( a_i \) are restored to the values \( b_1+j \) and \( a_i \), respectively, where \( 0 \leq i \leq n - 1 \). Thus, after Iteration \( j \) of Step 3 the input states \( |A_i\rangle \) and \( |B_i\rangle \) for \( 0 \leq i \leq n - 1 \) are transformed to:

\[
\left( \bigotimes_{i=0}^{n-1} |A_i\rangle \right) \left( \bigotimes_{i=0}^{n-1} |B_i\rangle \right)
\]

(17)

After Iteration \( j \) of Step 3 the input states \( |P_i\rangle \) for \( 0 \leq i \leq 2 \cdot n \) is transformed to:

\[
\left( \bigotimes_{i=0}^{j} |P_i\rangle \right) \left( \bigotimes_{i=j+1}^{j+1+n} |s_{i-j-1}\rangle \right) \left( \bigotimes_{i=j+n+2}^{2n} |0\rangle \right)
\]

(18)

- For Iteration \( n - 2 \) of Step 3, a quantum Ctrl-Add circuit with no input carry takes the inputs as \( a_i \) and \( p_{i+(n-2)} \) for \( 0 \leq i \leq n - 1 \) and the input \( b_{n-1} \). At the end of computation the locations \( p_{i+(n-2)} \) will have the value \( s_i \) for \( 0 \leq i \leq n - 1 \). Further, at the end of computation the locations which originally stored \( b_{n-1} \) and \( a_i \) are restored to the values \( b_{n-1} \) and \( a_i \), respectively, where \( 0 \leq i \leq n - 1 \).

\[
\left( \bigotimes_{i=0}^{n-1} |A_i\rangle \right) \left( \bigotimes_{i=0}^{n-1} |B_i\rangle \right) \left( \bigotimes_{i=0}^{2n-1} |P_i\rangle \right) |0\rangle
\]

(19)

Thus, the proposed design methodology transforms the quantum register \( |P_i\rangle \) that originally stored 0 to the product of \( a \) and \( b \) for \( 0 \leq i \leq 2 \cdot n - 1 \) while the quantum registers \( |A\rangle \) and \( |B\rangle \) where \( a \) and \( b \) are initially stored, respectively, will be restored to the values \( a \) and \( b \), respectively. Further, the quantum register location \( |P_{2n}\rangle \) where 0 was stored initially is restored to the value 0. This proves to the correctness of the proposed methodology to design a quantum integer multiplication circuit.

### B. T-count Analysis

The T-count of the proposed quantum integer multiplication circuit is illustrated shortly for each step of the proposed design methodology. We calculate total T-count for the proposed quantum integer multiplication circuit by summing the T-count for each step of the proposed design methodology.
The order of growth of the T-count for the proposed quantum integer multiplication circuit is linear. Thus, the qubit cost is $O(n)$.

**TABLE VI: Comparison between the design by Babu [1] and the proposed work in terms of ancillae**

| qubits | 1 | Proposed | % Impr. w.r.t. 1 |
|--------|---|----------|-----------------|
| 4      | 18 | 9        | 50.00           |
| 8      | 57 | 17       | 70.18           |
| 16     | 178 | 33      | 81.46           |
| 32     | 608 | 65      | 89.31           |
| 64     | 2210 | 129   | 94.16           |
| 128    | 8368 | 257   | 96.93           |

Average: 80.34

1 is the design by Babu [1] modified to remove garbage output. The designs by Lin et. al. and Jayashree et. al. are not compared because the ancillae for these designs is nearly the same as the proposed work.

Table V shows the comparison in terms of T-count which shows that the proposed design methodology achieves improvement ratios ranging from 39.02% to 49.56%, 62.50% to 64.06% and 25.15% to 32.35% compared to the designs presented by Babu ([1]), Lin et. al. ([2]) and Jayashree et. al.([3]). Table VI shows the comparison in terms of ancillae which shows that the proposed design methodology achieves improvement ratios ranging from 50.00% to 96.93% compared to the recently proposed design by Babu ([1]). Table VII shows the comparison in terms of total qubits and shows that the proposed design methodology achieves improvement ratios ranging from 59.52% to 94.22% compared to the recently proposed design by Babu ([1]). We calculated total qubits by

**Step 1:**
- The T-count for this Step is $7 \cdot n$.

**Step 2:**
- The T-count for this Step is $28 \cdot n + 14$.

**Step 3:** Step 3 is repeated $n−2$ times. For $i = 0 : 1 : n−2$:
- The T-count for the $i$th iteration of this Step is $28 \cdot n + 14$.

Therefore, the total T-count of the proposed quantum integer multiplication circuit is $21 \cdot n^2 − 14$.

A comparison of the proposed quantum integer multiplication circuit with existing designs is illustrated in table IV which shows that the proposed design has a lower T-count compared to existing designs. To compare the proposed work against the recent quantum integer multiplication circuit design presented by Babu [1], we implemented the design using the fault tolerant Clifford + T gate family. We used the Clifford + T implementation of the square root of not gate presented in [21] in the implementation of the design by Babu. The implementation in [21] requires three T gates and four Clifford gates. We also made the quantum integer multiplication circuit designed by Babu garbageless by applying the Bennett’s garbage removal scheme described in section II-D. Consequently, the garbageless form of the quantum circuit by Babu requires $2 \cdot n + 1$ additional qubits and sees an increase in the T-count by a factor of 2x.

Table IV illustrates that the order of growth of the T-count for the proposed quantum integer multiplication circuit is quadratic. Thus, the T-count is $O(n^2)$. Table IV shows that the proposed design has a lower overall qubit cost. Table IV illustrates that the order of growth of the qubits for the proposed quantum integer multiplication circuit is linear. Thus, the qubit cost is $O(n)$.

**TABLE IV: Comparison of quantum integer multiplication circuits**

|       | 1  | 2  | 3  | Proposed |
|-------|----|----|----|----------|
| T-count | $56 \cdot n^2$ | $28 \cdot n^2 + 7 \cdot n$ | $42 \cdot n^2 − 42 \cdot n + 48$ | $21 \cdot n^2 − 14$ |
| qubits | $5 \cdot n + 1$ | $4 \cdot n + 1$ | NA | $4 \cdot n + 1$ |
| ancillae | $3 \cdot n + 1$ | $2 \cdot n + 1$ | NA | $2 \cdot n + 1$ |

1 is the design by Lin et. al. [2]
2 is the design by Jayashree et. al. [3]
3 is the design by Babu [1] modified to remove garbage output.

Table entries are marked NA where a closed-form expression is not available for the design by Babu [1].

**TABLE V: T-count comparison of quantum integer multiplication circuits**

| qubits | 1 | 2 | 3 | Proposed | % Impr. w.r.t. 1 | % Impr. w.r.t. 2 | % Impr. w.r.t. 3 |
|--------|---|---|---|----------|-----------------|-----------------|-----------------|
| 4      | 896 | 476 | 528 | 322    | 64.06           | 32.35           | 39.02           |
| 8      | 3584 | 1848 | 2352 | 1330  | 62.89           | 28.03           | 43.45           |
| 16     | 14336 | 7280 | 10032 | 5362  | 62.60           | 26.35           | 46.55           |
| 32     | 57344 | 28896 | 41520 | 21490 | 62.52           | 25.63           | 48.24           |
| 64     | 229376 | 115136 | 169008 | 86002 | 62.51           | 25.30           | 49.78           |
| 128    | 917504 | 459648 | 682032 | 1376242 | 62.50         | 25.07           | 49.94           |
| 256    | 3670016 | 1836800 | 2740272 | 1376242 | 62.50         | 25.07           | 49.78           |
| 512    | 14680064 | 7343616 | 10985520 | 5505010 | 62.50         | 25.04           | 49.89           |
| 1024   | 58720256 | 29367296 | 43991088 | 22020082 | 62.50         | 25.02           | 49.94           |
| 2048   | 234881024 | 117454848 | 176062512 | 88080370 | 62.50         | 25.01           | 49.97           |

Average: 62.71, 26.30, 47.55

1 is the design by Lin et. al. [2]
2 is the design by Jayashree et. al. [3]
3 is the design by Babu [1] modified to remove garbage output.
summing the garbage outputs, qubits holding the product and qubits of the inputs.

**TABLE VII: Comparison between the design by Babu [1] and the proposed work in terms of total qubits**

| Total qubits | Babu [1] | Proposed | % Impr. w.r.t. Babu |
|--------------|----------|----------|---------------------|
| 4            | 42       | 17       | 59.52               |
| 8            | 90       | 33       | 63.33               |
| 16           | 243      | 65       | 73.25               |
| 32           | 737      | 129      | 82.50               |
| 64           | 2467     | 257      | 89.58               |
| 128          | 8881     | 513      | 94.22               |

Average: 77.07

1 is the design by Babu [1] modified to remove garbage output total qubits is the sum of the garbage outputs, qubits for the product and the qubits of the inputs The designs by Lin et al. and Jayashree et. al. are not compared because the total qubits for these designs is nearly the same as the proposed work.

**V. CONCLUSIONS**

In this work, we have presented the design of a quantum integer multiplication circuit optimized in terms of T-count with \(4 \cdot n + 1\) qubits. Further, the proposed quantum integer multiplication circuit does not produce garbage outputs. The design of subcomponents used in the proposed quantum integer multiplication circuit such as the proposed quantum conditional addition circuit with no input carry are also illustrated. The proposed quantum integer multiplication circuit is shown to be superior to the existing designs in terms of T-count. All of the proposed designs in this work are functionally verified by formal proof and Verilog simulation. We conclude that the proposed quantum integer multiplication circuit will find applications in quantum computing that requires integer multiplication where T-count is of primary concern.

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