An enhanced time-to-digital conversion solution for pre-bond TSV dual faults testing

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Abstract: Pre-bond TSV test plays a vital role in improving the yield and reducing the cost of 3D ICs. In this paper, a non-invasive solution for pre-bond TSV test based on pulse shrinking is proposed. This method makes use of the fact that defects in TSV lead to variation in the propagation delay - the rise and fall times are first transformed into pulse width, and the pulse shrinking technique is used to digitize the pulse width into a digital code which is then compared with an expected value for a fault-free TSV. Experiments on TSV defect detection are carried out using HSPICE simulations with realistic models for 45 nm CMOS technology. Experimental results show that the proposed method can detect not only open (leakage) fault but also dual faults with high resolution.

Keywords: 3D ICs, TSV, pre-bond test

Classification: Integrated circuits

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1 Introduction

Three-dimensional integrated circuits (3D ICs) are invented to address the scaling challenge by stacking multiple 2D dies together and connecting them through silicon vias (TSVs). However, the yield of TSV-based 3D integrated circuits (ICs) is unsatisfactory in the semiconductor industry [1]. TSVs are vulnerable in the manufacturing process and many physical defects, such as micro-voids and pin-holes, frequently occur. Typically, several TSV defects can be modeled by two common types of TSV faults, namely resistive open and leakage faults. Testing for manufacturing defects is inherently important to ensure the required product quality since one single defect in a TSV may damage the entire 3D IC. Hence, TSVs need to be thoroughly tested to enhance their yield and reliability [2, 3, 4, 5, 6]. Pre-bond TSV testing is always one of the main challenges in 3D-IC test flow due to the limited TSV accessibility.

Many pre-bond TSV testing methods have been presented in the recent literature [7, 8, 9]. In [7], an approach called CAF-WAS (Charge-and-Float, Wait-and-Sample) with phase-locked loops was proposed for TSV leakage fault detection. However, this method just detect the TSV leakage faults, and the wait time-generating circuit needs to be designed carefully as it is sensitive to the threshold of targeted fault. Furthermore, there is little flexibility as it is difficult to fix an exact wait time for various TSVs of different sizes. Huang et al. [8] proposed a ring oscillator-based solution to detect micro-voids and pin-holes in pre-bond TSV. In this method, TSV is used as the load to be connected to the ring oscillator, and the oscillation period is captured by extra binary counters that use the oscillating signal as a clock. As TSV manufacturing defects change the propagation delay of the ring oscillator nets, TSV parameter deviations are detected through the deviation from the expected rings oscillation periods. Deutsch et al. [9, 10] presented a TSV test method using duty-cycle detectors in pre-bond TSV. This method improves the measurement resolution and realizes the fault diagnosis of the weak leakage defects. However, there are several shortcomings in this method.
Firstly, the oscillation period lies on the nanosecond level while the propagation delay caused by TSV RC parameter deviations spreads over the picosecond level. As a result, some subtle variations in TSV may be masked by the DFT circuitry. Secondly, it is difficult to guarantee the stability of the circuit for testing duty cycle.

In [6], we have illustrated a pulse shrinkage method for pre-bond TSV testing, it can detect TSV faults with high resolution. However, when the resistive open fault occurs, the change of pulse width caused by open circuit fault is very small or even negligible. In fact, the change of rise time and fall time is greater than that of pulse width, which means that rise time and fall time are easier to measure separately. To tackle the problem that rise time along with fall time will offset each other, in this paper, an enhanced test method for pre-bond TSV using a technique named pulse shrinking test (or PS test for short) is presented. For a given TSV under test, the PS test supplies a test signal (rising edge or falling edge) at the driving end. Due to the loading effect of the TSV, the signal arriving at the receiving end tends to have a constant rise/fall time, which is converted to a pulse width. Finally, the pulse shrinking technique is used to measure the pulse width. If the TSV is faulty with excessive resistances or larger equivalent capacitance, the voltage waveform will be distorted and will thus lead to a different rise/fall time. As a result, the fluctuation in rise/fall time is converted to the corresponding pulse width, and the measurement results are presented in the form of digital codes and compared with the standard values for fault-free TSVs.

2 The proposed pre-bond TSV test structure and solution

2.1 Circuit converting TSV delay to pulse width

To address the issue described above in [6], a new solution based on the pulse shrinking is proposed to measure the delay change in a rising transition and a falling transition separately. As shown in Fig. 1, the new circuit is used to convert the rise time and fall time to two separate pulses, each having a characteristic pulse width. A rising transition arriving at the input of the driving gate will propagate to the XOR gate along two different paths. One path directly connects \( V_{in} \) to an input pin of the XOR gate, while the other connects \( V_{in} \) to another input pin of the XOR gate through the circuit consisting of a driving gate, a TSV and a receiving gate. The two-path signals will generate a pulse whose width is dependent on the TSV delay through the XOR gate. Similarly, a falling transition from \( V_{in} \) can also be converted to a pulse with a characteristic width.

In order to prove that this method is better than the preliminary scheme in [6] that directly uses an input pulse through TSV, HSPICE simulation is carried out and the results are presented below. It should be noted that the proposed method is able
to detect defective TSVs with a diameter of 5 μm and a depth of 50 μm, and the Nangate 45 nm open cell library is used and $C_{TSV}$ is fixed at typical 59 fF in our simulations. The proposed scheme measures the delay induced by the TSV capacitance in order to reflect whether there exists any TSV fault and the characteristics of the faults existing. The measured delay can exactly reflect the magnitude of the equivalent TSV capacitance of the TSV fault.

In Fig. 2, the deviation of pulse width/rise time/fall time from their reference values (vertical axis) are respectively plotted against the open resistance $R_O$ (horizontal axis). The curve obtained using the previous method in [6] shows that the pulse width deviates from the reference value by less than 10 ps when the open resistance is less than 5 kΩ. Yet the curves obtained from measuring the rise and fall time separately show a deviation of more than 10 ps when the open resistance is only 0.9 kΩ. That is to say, if the test resolution is 10 ps, the previous method can only diagnose 5 kΩ open fault but the new solution can diagnose an open fault as weak as 0.9 kΩ. Therefore, this new method is better than the previous one in diagnosing weak TSV open fault.

![Fig. 2. Comparison of the rise or fall time with pulse width in the presence of a resistive open fault.](image)

### 2.2 Pulse shrinking circuit

The purpose of our approach is to detect TSV faults by varying the path delay parameters of circuits with TSV. These variations will be converted to pulses with characteristic pulse widths and the pulse widths are then measured using a pulse shrinking circuit with a time-to-digital converter (TDC). The overall test architecture is composed of a pulse-generating circuit and a pulse-shrinking circuit, as shown in Fig. 3.

The circuit for pulse generation contains $n$ TSVs under the test, where $n$ can be selected according to the actual placement of the adjacent TSVs. In order to select a TSV to test, multiplexers are used in the front of the driving buffers and at the back of the receiving buffers.

The multiplexers enable signals $S_1...S_n$ to do selection between the operation signal coming from the internal logic and the rise (or fall) edge of the test transition signal $V_i$. If $S_1 = S_2 = ... = S_n = 1$, all the multiplexers select the operation signal and the circuit is in the normal operation mode. If $S_1 = 0, S_2 = ... =
Sn = 1, the circuit is configured into the TSV test mode, with the test object being TSV1. The signals Select \([m]\), where \(m = \lfloor \log_2 n \rfloor\), control the \(n:1\) multiplexer to select output of a receiving buffer and connect it to an input of the XOR gate. Finally, the rising (falling) edge is converted to a pulse with a characteristic width by the XOR gate. The pulse signal is inverted and transmitted to the next measuring module.

The two NAND gates in the delay chain of the pulse shrinking modules are implemented to be inhomogeneous gates as well as the coupling circuit. The purpose is to keep the pulse width when the pulse passes through them. The cyclic delay chain is composed of a lot of pulse shrinking elements, each including two inverters with inhomogeneous dimensions. The amount of shrinkage in pulse width after a pulse passes through one shrinking element is equal to the test resolution. The output of each shrinking element is used as a clock for the corresponding DFF and the data input to the DFF is constantly tied to 1. Therefore, a DFF will output 1 if a transition occurs at its clock terminal. The DFF will be reset when the pulse is transmitted to the next element, implying that only one DFF is set to 1 before the pulse disappears. The counter is used to record the number of loops that the pulse has undergone in the delay chain. Finally, the state of the counter and the DFF is decoded into a digital code.

Equation (1) can be used to calculate the actual time, where offset is the measurement offset related to the setup and hold time of the DFF.

\[
\text{Delay} = \text{Digital code} \times \text{resolution} + \text{offset}
\]

### 3 Simulation results

To evaluate the performance of the proposed pulse shrinking method, a simulation is executed using HSPICE tool with a 45 nm predictive technology model (PTM) CMOS process [6]. The cyclic delay chain consists of 25 pulse shrinking elements with the resolution of 7 ps. Each of the pulse shrinking elements is composed of two heterogeneous inverters. The W/L value of the first inverter is 4/1(200 nm/
50 nm) for PMOS and 1/1(50 nm/50 nm) for NMOS, and that of the second inverter is designed to be 2/1(100 nm/50 nm) for PMOS and 1/1(50 nm/50 nm) for NMOS. The buffer cell BUF.X4 in Nangate 45 nm Open Cell Library is selected as the TSV driving buffer, and the X1 version of the cells are used for other gates.

3.1 Open fault test

A resistive open fault at the half of the TSV with a typical value of 59 fF is simulated. The input test signal is the rising/falling edge of $V_{in}$ and $R_O$ varies from 0 kΩ (no fault) to 20 kΩ (serious resistive open fault) at the typical supply voltage $V_{DD} = 1.1$ V.

With the circuit model shown in Fig. 3, the signal transition is analyzed and recorded by the digital code. Fig. 4 shows the digital code obtained from rising and falling transition tests in the case of a resistive open fault. As expected, an increase in the resistance $R_O$ will lead to a decrease in digital code from 22 to 11, indicating that the resistive open fault of a sufficient size can be detected by reading the digital code directly. When the resistance $R_O$ increases from 14 kΩ to 20 kΩ, the digital code does not change but stays constant at 11, which implies that the TSV is completely damaged at the half position. As the resistance $R_O$ decreases from 0.4 kΩ to 0 kΩ, the digital code stays constant at 21, which means that only open
resistances greater than 0.4 \( \Omega \) can be detected accurately by the proposed scheme and it is considered to be no resistive open fault if \( R_O \) is less than 0.4 \( \Omega \).

In order to verify the accuracy of the proposed method in this paper, Equation (1) is used to calculate digital code from the measured result, which is then compared with the real delay of TSV. The simulation results are shown in Fig. 5. It can be observed that the difference between the measured result and the actual value is very small and almost negligible no matter the rising or the falling edge is tested. Fig. 5 also shows that there is a strong correlation between the measured value and the actual TSV delay. The average difference between the test result and the samples is 1.2\%, while the maximum difference is 3.1\%.

3.2 Leakage fault test

A different behavior from that in the case of resistive open faults is observed when TSV leakage faults are detected. To demonstrate this different behavior, the same simulation approach as described above is used. Fig. 6 shows the dependence of the digital code on the leakage resistance \( R_L \).

Firstly, it is observed that the digital code obtained from the rising edge test decreases from 58 to 21 as the leakage resistance increases, a remarkably different behavior from the cases of fault-free TSV and TSV with resistive open faults. Secondly, the digital code of falling edge test increases from 6 to 20 as the leakage
resistance increases. Thirdly, if the node voltage of the TSV is too low and the $R_L$ is less than 3 kΩ, the recorded digital code will stay unchanged. When the leakage resistance $R_L$ is more than 100 kΩ, the digital code remains stable at 22, which indicates that the leakage current is too small to be detected. Hence the weakest leakage resistance that can be identified by this proposed scheme is about 100 kΩ.

Similarly, Equation (1) can also be used to calculate the measured result which can then be compared with the actual TSV delay. As shown in Fig. 7, the difference between the measured result and the actual value is very small and negligible, no matter the rising or the falling edge is tested. It is also observed that the measured value is strongly dependent on the actual TSV delay. The difference is 1.4% on average between the value captured by the test and that by actual sampling, while the maximum difference is 3.3%.

### 3.3 Jointly open and leakage faults test

Open and leakage defects may occur simultaneously in a TSV, and the analysis under such a situation is very complicated because of the different effects of the two defects. From the analysis before, both the open fault and leakage fault in a TSV will lead to a decrease in the falling transition time, implying that the effect of the two types of faults on the falling edge test is the same. The existing methods may not be able to differentiate a TSV having the two faults simultaneously from a fault-free TSV. This problem is also studied in this paper, and a TSV with both open and leakage faults can be detected by means of the idea that the rising time and falling time are measured individually.

Two models, called Model 1 and Model 2, are studied when a TSV is affected by a resistive-open fault and a resistive leakage fault at the same time, as shown in Fig. 8. In Model 1, the open fault occurs above the leakage fault, and in Model 2, the open fault is closer to the floating end of the TSV than the leakage fault. Using the two models, simulations are carried out for the pulse width (delay) created by the input rising edge and falling edge under different TSV leakage resistance $R_L$ and open resistance $R_O$. Using Model 1, the relationship between $R_O$ and the delay in the rising edge test under different $R_L$ is shown in Fig. 9(a), and that in the falling edge test is shown in Fig. 9(b). Similarly, Fig. 10 shows the results of the same simulations using Model 2. It is observed that no matter which model is used, the results of the simulations are essentially consistent with those calculated using
Equation (1). It is also noticed that the delay value indicating fault free is only used as a delay reference, which does not change as $R_O$.

Fig. 9. TSV delay due to the two types of coexisting faults using Model 1. (a) Rise time, (b) Fall time.

Fig. 10. TSV delay due to the two types of coexisting faults using Model 2. (a) Rise time, (b) Fall time.
From Fig. 9(a) and Fig. 10(a), it is can be found that the open fault and leakage fault may mask each other, leading to the result that the TSV delay obtained when the two defects occur simultaneously in a TSV is the same as that in a fault-free case. However, the measured result is always smaller than the fault-free reference value, as shown in Fig. 9(b) and Fig. 10(b). That is to say, in a falling edge-based TSV delay test on a TSV with both open and leakage faults existed, the fall time is always shorter than that of the TSV with fault-free, which is used to test a TSV with the two types of faults simultaneously.

4 Conclusion

In this paper, a new pulse shrinking-based test method is proposed to detect TSV faults at an early stage of the manufacturing process of 3D ICs, thereby ensuring the yield of integrated circuits. The experimental results show that the proposed method not only can be used to accurately detect open fault and leakage fault in TSVs when only one type of fault is present though they are weak, but also can be used to detect both types of faults when they coexist to a certain extent. It is the first time to present such a test method in which the input rising and falling edge transitions are separately converted to pulses with characteristic widths, which are then used to detect TSV faults. Unlike the methods that obtain results by simultaneously adopting the two types of edges, it overcomes the problem caused by the mutual masking effect of the open and leakage faults on the measured delay time.

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