Study on differential mode conducted interference of trigger circuit of high-power thyristors in pulsed power supply

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Abstract. The trigger circuits of high-power thyristors in pulsed power supply (PPS) contain a large number of pulse transformers, switching MOSFETs (SMFETs) and other passive devices. Fast on-off of SMFETs and pulse transformers often lead to differential mode conducted interference (DMCI) problems in trigger circuits of high-power thyristors. This paper mainly discusses DMCI problems in trigger circuits of high-power thyristors in the following aspects: initially, circuit models of high-frequency parasitic parameters of pulse transformer and SMFET are established; next, principles of DMCI in trigger circuits of high-power thyristors are investigated; furthermore, DMCI suppression methods are also analyzed; ultimately, experiments have been carried out to verify the theoretical analysis.

1. Introduction
High-power thyristor is widely adopted as a power switching device in a PPS [1-3]. Compared with other similar switching devices, high-power thyristors have a relatively lower-cost in applications of high voltage and current. It is significant that the trigger pulse of high-power thyristors must be with high accuracy in PPS because it directly affects the performance of a PPS.

Trigger pulse of high-power thyristors is one of the key factors affecting the reliability of a PPS. If trigger pulse of high-power thyristors is abnormal, PPS will also be abnormal. Trigger pulse of high-power thyristors can affect the accuracy of trigger pulse that is closely related to triggering consistency of high-power thyristors and the accuracy of the high-power output pulse of a PPS.

Plenty of pulse transformers and SMFETs applied in trigger circuit of high-power thyristors generate numerous change rates of voltage $du/dt$ and current $di/dt$, which can result in electromagnetic conducted interference (EMCI) problems [4-6]. Generally, trigger pulses are sensitive to EMCI in trigger circuit of high-power thyristors.

EMCI is usually divided into common-mode conducted interference (CMCI) and differential-mode conducted interference (DMCI). In order to improve the reliability of a PPS, this paper aims to discuss DMCI in a trigger circuit of high-power thyristors and find some effective methods to suppress it. In the experiments of DMCI in trigger circuits of high-power thyristors, the peak (PK) spectrums of DMCI are measured in the frequency range of 10kHz-10MHz.
2. Principle of DMCI in trigger circuits of high-power thyristors

2.1. Principle of trigger circuits of high-power thyristors

The principle of trigger circuits of high-power thyristors is shown in figure 1. Figure 1(a) is the schematic diagram of trigger circuits of high-power thyristors and figure 1(b) is the circuit principle of a one-stage trigger circuit of high-power thyristors. According to figure 1(a) and figure 1(b), the trigger circuits of high-power thyristors are mainly composed of powerful trigger units, MCU control units, and remote control computer units.

The powerful trigger units are mainly composed of a DC power source module and several powerful trigger pulse forming modules (PFMs). The powerful trigger units can generate trigger pulses with certain time sequences according to received instructions.

The DC power source module usually applies the principle of switching power supply (SPS) to convert the AC power source from an uninterruptible power supply (UPS) into a DC power source.

A powerful trigger PFM mainly consists of a SMFET and a pulse transformer. The SMFET can convert the DC power source into powerful trigger pulses according to time sequences. The powerful trigger pulses are transmitted to the gates of high-power thyristors by the pulse transformer. The trigger circuit of high-power thyristors can be divided into one-stage trigger circuit of high-power thyristors, two-stage trigger circuit of high-power thyristors,..., and N-stage trigger circuit of high-power thyristors according to the number of powerful trigger units.

MCU control units can communicate with remote control computers through serial communication modules. Due to a long distance between MCU control units and remote control computers, all signals between them are transmitted through optical fibers. The conversion mode of the signals is electric-optical-electric, which can effectively guarantee high qualities of signals in long-distance transmission. MCU control units, on the one hand, directly generate time sequences of trigger pulses according to the instructions from remote control computers; on the other hand, it also returns feedback information of trigger pulses to remote control computers. Remote control computers can automatically check the feedback information from MCU control units. If there is an abnormality, it can provide operators with possible causes of the abnormality, which is convenient for them to quickly lock sources of the problem.

![Schematic diagram of trigger circuits of high-power thyristors.](image1)

**Figure 1.** Principle of trigger circuits of high-power thyristors.

2.2. High-frequency parasitic parameters of key components

2.2.1. High-frequency parasitic parameters of a pulse transformer: In a powerful trigger unit, the high-frequency parasitic parameter of a pulse transformer is closely related to DMCI [7-10]. The distributed parasitic capacitance model of a pulse transformer is shown in figure 2(a). $C_{SCIN}$ and $C_{SC2N}$ are distributed capacitances between the secondary winding and the core, $C_{SP1N}$ and $C_{SP2N}$ are distributed
capacitances between the primary winding and the secondary winding, \( C_{PC1N} \) and \( C_{PC2N} \) are distributed capacitances between the primary winding and the core, \( C_{SS1N} \) and \( C_{SS2N} \) are distributed capacitances between turns of the secondary winding, \( C_{PP1N} \) and \( C_{PP2N} \) are distributed capacitances between turns of the primary winding. There are many distributed capacitances in this model, which are not conducive to actual extractions. The lumped parasitic parameter model of a pulse transformer is shown in figure 2(b). \( C_{PP} \) is an equivalent parasitic capacitance between turns of the primary winding, \( C_{SS} \) is an equivalent parasitic capacitance between turns of the secondary winding, \( L_P \) is an equivalent leakage inductance of the primary winding, \( L_S \) is an equivalent leakage inductance of the secondary winding, \( R_P \) is an equivalent resistance of the primary winding, \( R_S \) is an equivalent resistance of the secondary winding, \( C_{SP1} \) and \( C_{SP2} \) are equivalent parasitic capacitances between the primary winding and the secondary winding, \( C_{P1} \) and \( C_{P2} \) are equivalent parasitic capacitances between the primary winding and the magnetic core, \( C_{SC1} \) and \( C_{SC2} \) are equivalent parasitic capacitances between the primary winding and the core. The parasitic parameters in the lumped parameter model can be extracted by practical methods, which can be applied in EMCI predictions of circuits. The specific extraction methods are shown in references [11]-[12]. The existence of the equivalent leakage inductance \( L_P \) and the equivalent parasitic capacitance \( C_{PP} \) of the primary winding are usually considered as the factors deteriorating DMCI in trigger circuits of high-power thyristors.

![Distributed parasitic capacitance model of a pulse transformer.](image1)

![Lumped parasitic parameter model of a pulse transformer.](image2)

**Figure 2.** High-frequency parasitic parameter models of a pulse transformer.

Based on figure 2(a) and figure 2(b), the relationship between distributed parameters and lumped parameters of the pulse transformer can be expressed as equations (1)-(5).

\[
C_{SP1} + C_{SP2} = \sum_{N=1}^{N=N_{MAX}} (C_{SP1N} + C_{SP2N})
\]  

(1)
2.2.2. High-frequency parasitic parameters of a SMFET  A SMFET usually has three pins: drain, source, and gate. There is a parasitic capacitance at the PN junction of every two pins. Figure 3 shows the equivalent parasitic parameter model of a SMFET. $L_D$ is a high-frequency parasitic inductance at the drain, $L_S$ is a high-frequency parasitic inductance at the source, $R_G$ is an equivalent resistance of the gate, $C_{DG}$ is a high-frequency parasitic capacitance between the drain and the source, $C_{GS}$ is a high-frequency parasitic capacitance between the gate and the source, and $C_{DS}$ is a high-frequency parasitic capacitance between the drain and the source [13-14]. In a trigger circuit of high-power thyristors, there is continuous on-off of SMFET, leading to a continuous voltage change rate $du/dt$ or a current change rate $di/dt$, which result in the generation of DMCI. The existence of high-frequency parasitic parameters, on the one hand, provides a coupling pathway for DMCI; on the other hand, it can cause damping oscillation of the voltage or current between the drain and the source, which aggravates DMCI.

\[
C_{PC1} + C_{PC2} = \sum_{n=1}^{N} (C_{PC1n} + C_{PC2n})
\]

(2)

\[
C_{SC1} + C_{SC2} = \sum_{n=1}^{N} (C_{SC1n} + C_{SC2n})
\]

(3)

\[
\frac{1}{C_{PP}} = \sum_{n=1}^{N} \left( \frac{1}{C_{PP1n} + C_{PP2n}} \right)
\]

(4)

\[
\frac{1}{C_{SS}} = \sum_{n=1}^{N} \left( \frac{1}{C_{SS1n} + C_{SS2n}} \right)
\]

(5)

**Figure 3.** Equivalent circuit model of high-frequency parasitic parameter of a SMFET.

2.3. Principle of the DMCI in trigger circuits of high-power thyristors

To meet the requirements of volume limitation, several trigger circuit units usually share a DC power source forming a multi-stage trigger circuit of high-power thyristors, which can inevitably lead to the aggravation of DMCI. Based on the parasitic parameter models of pulse transformer and SMFET, figure 4 shows the principle of DMCI in a three-stage trigger circuit of high-power thyristors. Figure 4(a) shows the coupling principle of DMCI in the circuit. It can be seen from figure 4(a) that the DMCI in each trigger circuit unit superposes at the power input port and then enters other trigger circuit units.

Figure 4(b) is a simplified circuit model of DMCI in the circuit of figure 4(a). $Z_{dnn}$ (n=1,2,3) is an equivalent DMCI impedance in the $n$th trigger circuit unit, $V_{dnn}(t)(n=1,2,3)$ is an equivalent DMCI voltage in the $n$th trigger circuit unit, $i_{dnn}(t)(n=1,2,3)$ is an equivalent DMCI current in the $n$th trigger...
circuit unit, and \( i_{dm}(t) \) is a total DMCI current at the power input port of the trigger circuit units. Assuming that \( V_{dm1}(t) = V_{dm2}(t) = V_{dm3}(t) \) and \( Z_{dm1} = Z_{dm2} = Z_{dm3} \), then:

\[
\begin{align*}
    i_{dm}(t) &= \frac{V_{dm}(t)}{2R_{dm1} + Z_{dm1} / 3} \\
    V_{dm}(t) &= 2R_{dm1}i_{dm}(t)
\end{align*}
\]

Figure 4(c) is the extended circuit model of DMCI in an \( N \)-stage trigger circuit of high-power thyristors based on figure 4(b). Assuming that \( V_{dm1}(t) = V_{dm2}(t) = \cdots = V_{dmn}(t) \) \( (n=1, 2, \cdots, N) \) and \( Z_{dm1} = Z_{dm2} = \cdots = Z_{dmn} \) \( (n=1, 2, \cdots, N) \), then:

\[
\begin{align*}
    i_{dm}(t) &= \frac{V_{dm}(t)}{2R_{dm} + Z_{dm}/n} \\
    V_{dm}(t) &= 2R_{dm}i_{dm}(t)
\end{align*}
\]

It can be seen from equation (8) that with the increase of the trigger circuit stage of high-power thyristors, the total DMCI current \( i_{dm}(t) \) increases, resulting in the aggravation of DMCI.

(a) Coupling principle of DMCI in three-stage trigger circuit of high-power thyristors.
2.4. Suppressive methods of DMCI in trigger circuits of high-power thyristors

Generally, implanting an EMI filter at the power input port of a trigger circuit of high-power thyristors can effectively suppress DMCI. Figure 5(a) shows a circuit model of a one-stage EMI filter, which is mainly composed of differential-mode (DM) capacitors $C_{dm1}$ and $C_{dm2}$, common-mode (CM) capacitor $C_{cm}$. Figure 5(b) is the equivalent DM circuit model of figure 5(a). Due to the volume limitation of an EMI filter in the trigger circuit of high-power thyristors, leakage inductance $L_{cm}$ of CM choke $L$ is used to suppress the DMCI. In fact, both DM/CM capacitors and CM choke have high-frequency parasitic parameters, so it is necessary to consider the influence of these factors on the performance of an EMI filter. The extraction methods of high-frequency parasitic parameters of an EMI filter proposed in references [15-17].

3. Experimental results and analysis

3.1. DMCI test layout

Figure 6 shows the DMCI test layout. Main equipments include an automatic test computer, an EMI receiver, a line impedance stabilization network (LISN) and a DC power source. The LISN can provide a standard 50Ω impedance to match with EMI receiver and filter out interference from DC power source, which makes measured results more accurate. The simplified circuit model of a LISN is shown in figure 7. Generally, the inductance $L_1 = L_2 = 50 \mu \text{H}$, the capacitance $C_{dm} = 0.1 \mu \text{H}$, the resistance $R_{dm} = 50 \Omega$ [18]. The measured time-domain signal of DMCI $V_{dm}(t)$ can be expressed as equation (9):

$$V_{dm}(t) = \frac{V_{+}(t) - V_{-}(t)}{2}$$

Where, $V_{+}(t)$ is mixed time-domain signals of DMCI and CMCI in $V_{IN+}$ of the power input port. $V_{-}(t)$ is mixed time-domain signals of DMCI and CMCI in $V_{IN-}$ of the power input port.
EMI receiver can easily separate DMCI and CMCI by an integrated separate module of DMCI and CMCI. The main function of an EMI receiver is to convert the time-domain signals of EMCI obtained from the LISN into the frequency-domain signals of EMCI by FFT calculations. The automatic test computer reads EMCI spectrums obtained from EMI receiver and presents it to researchers for analysis.

3.2. Experimental results

3.2.1. Influence of trigger frequency on DMCI Generally, trigger frequency \( f_t \) is set according to requirements and lower than 200kHz. Different trigger frequencies lead to different DMCI. Three different trigger frequencies are set during the test of DMCI. Figure 8 shows the measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors (\( f_t=50\)KHz, 100kHz, and 150kHz, respectively; load resistance \( R_{load}=1k\Omega \)).

It can be seen from figure 8 that in the frequency range of 10kHz-10MHz, with the increase of trigger frequency, PK values of the DMCI spectrums also increase, indicating that the DMCI becomes heavier with the increase of trigger frequency.
3.2.2. Suppressive methods of DMCI for the DMCI. In a trigger circuit of high-power thyristors exceeds standard, EMI filtering components are usually implanted at the power input port to suppress it. Figure 9 shows the measured PK spectrums of DMCI in trigger circuits of high-power thyristors when several different EMI filtering components are implanted at the power input port, respectively.

It can be seen from Figure 9(a) that the CM choke (L=3.1mH) has an obvious suppression effect on DMCI after the frequency of 0.5MHz; from Figure 9(b), it can be seen that the DM capacitors (C_{dm1}=1μF, C_{dm2}=10 nF) can effectively suppress DMCI in the frequency range of 10kHz-10MHz. Compared with Figure 9(a) and Figure 9(b), the DM capacitors (C_{dm1}=1μF, C_{dm2}=10 nF) have a better suppression effect on DMCI than the CM choke (L=3.1mH). It can be seen from Figure 9(c) that the peak values of DMCI spectrums are almost equal when implanting with a one-stage EMI filter (L=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) at the power input port of a two-stage trigger circuit of high-power thyristors and two DM capacitors (C_{dm1}=1μF, C_{dm2}=100 nF) at the power input port of a one-stage trigger circuit of high-power thyristors. According to equation (8), the larger the circuit stage N, the heavier the DMCI in a trigger circuit of high-power thyristors. Therefore, the EMI filter (L=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) has a better suppression effect on DMCI than the capacitors (C_{dm1}=1μF, C_{dm2}=100 nF). It can be seen from Figure 9(d) that the PK values of DMCI spectrum when one-stage EMI filter (L=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) implanted at the power input port of a two-stage trigger circuit of high-power thyristors are about 5dBμV smaller than that of a three-stage trigger circuit of high-power thyristors in the harmonic frequencies less than or equal to 100kHz; the PK values of DMCI spectrum when one-stage EMI filter (L=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) implanted at the power input port of a two-stage trigger circuit of high-power thyristors are almost equal to that of a three-stage trigger circuit of high-power thyristors in the harmonic frequencies greater than 100kHz.

Figure 8. Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors (f=50kHz, 100kHz, and 150kHz; R_{load}=1kΩ).

(a) Measured PK spectrums of DMCI (f=50kHz and 100kHz; R_{load}=1kΩ).

(b) Measured PK spectrums of DMCI (f=100kHz and 150kHz; R_{load}=1kΩ).

(a) Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors with/without a CM choke (L=3.1mH) at the power input port.

(b) Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors with/without DM capacitors (C_{dm1}=1μF, C_{dm2}=100 nF) at the power input port.
In summary, the leakage inductance of a CM choke can be used to suppress relatively minor DMCI in a trigger circuit of high-power thyristors; DM capacitors or DM inductors can be implanted in an EMI filter to suppress relatively heavier DMCI in a trigger circuit of high-power thyristors.

4. Conclusion
To improve the reliability of a PPS, the DMCI in the trigger circuit of high-power thyristors has been investigated based on the following aspects: high-frequency parasitic parameters of key devices; generation principle of DMCI in the trigger circuits of high-power thyristors; suppression methods of DMCI. According to the theoretical analysis and experimental results, EMI filtering components (DM capacitor/inductor, CM choke, EMI filter and so on) can effectively suppress DMCI. Besides, limiting high-frequency parasitic parameters of key devices is also an effective way to suppress DMCI.

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