PXIe-based multi-channel data acquisition system of soft X-ray camera

Shixing Liu(1), Yajie Song1, Guangzhu Liu1, Hao Ren1, Hongrui Cao2, Qihang Zhou1, Mofei Yang1, Wei Lu1, and Cao Sun1

Abstract Soft X-ray cameras will be widely used in the ITER (International Thermonuclear Experimental Reactor) diagnostic system. To acquire their output data to display the signal changes on a computer, a PXIe (PCI Express xXensions for Instrumentation)-based multi-channel data acquisition system for a soft X-ray camera has been designed and is presented in this paper. The Xilinx FPGA (Field-Programmable Gate Array) chip Kintex7-325T-900-2 is adopted as a controller in this system. The hardware’s composition and the PXIe bus transmission of this system are presented and discussed. The acquisition and transmission of the soft X-ray camera’s multi-channel data has been accomplished with subsequent processing. Currently, this system can collect signals within 1 MHz, and the system’s signal resolution has achieved 0.122 mV.

Keywords: soft X-ray camera, ITER, PXIe, acquisition system, FPGA

Classification: Circuits and modules for electronic instrumentation

1. Introduction

To solve the declining number of energy sources, such as oil, natural gas and coal, the ITER project has built a large Tokmak device with controlled ignition and self-sustaining combustion to achieve nuclear fusion to generate energy [1, 2, 3]. Undoubtedly, during nuclear fusion, a large number of soft X-rays (with an energy range from 0.1 keV to 10 keV) [4] will be generated. The X-rays are particle flows caused by the transition of electrons in atoms between two widely different energy levels. In the field of nuclear radiation measurement, the amplitude of the output signal from a nuclear radiation detector is proportional to the energy of the incident particles. The energy of the incident particles can be obtained by measuring the amplitude of the signals from nuclear radiation. To adequately collect and analyze the soft X-ray, a soft X-ray camera is adopted to obtain soft X-ray radiation signals during nuclear fusion [5]. This camera converts optical signals into electrical signals through photodiode [5, 6, 7]. The intensity of soft X-ray can be calculated by measuring the output signals of the soft X-ray camera. The signals (the amplitude ranges from −10 V to 10 V and the frequency ranges from 0 Hz to 1 MHz) output from the soft X-ray camera need to be effectively acquired and processed.

To adequately collect and analyze the soft X-ray camera’s output signals, a PXIe-based multi-channel data acquisition system for a soft X-ray camera that can convert analog signals into digital signals has been designed and is presented in this paper. FPGA, which is generally not affected by radiation, is adopted to collect the soft X-ray camera’s output signals. Compared to a traditional NIM (Nuclear Instrument Module) chassis of nuclear radiation signals [8], this system has almost no interference among the multiple signals acquisition boards, nor does it have interference between the signal acquisition circuit boards and the host computer during signal transmission.

2. Acquisition system

A block diagram of the soft X-ray camera’s signal acquisition process is presented in Fig. 1. The output signals of soft X-ray camera, which are pulse current signals, are first amplified by the analog signals amplification circuit. Then the ADC (Analog-to-Digital Converter) convert the analog signals into digital signals. Following, the FPGA is adopted to process the digital signals output from the ADC. When the FPGA receives the trigger signal, the processed digital signals are transmitted to the NI (National Instruments) chassis through the PXIe interface, and finally the NI chassis transmit the digital signals to the CODAC (Control, Data Access and Communication) central control system through the ethernet interface. In the following, the hardware together with the firmware and the software of this acquisition system will be clearly presented.

1a) liux@hfut.edu.cn

Fig. 1. Block diagram of the soft X-ray camera’s signal acquisition process.

2.1 Hardware

The data acquisition board has 8 signal input ports and a trigger input port, and the architecture of the PXIe-based multi-channel data acquisition system is presented in Fig. 2. The designed data acquisition circuit boards mainly

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include four aspects: analog signals circuit, ADC circuit, FPGA and PXIe connection circuit, and power supply.

2.1.1 Analog signal circuit

To precisely acquire the soft X-ray camera’s output under different signal voltage ranges, the FPGA is first used to control the signal switching circuit which adopt a relay [9] and a BJT (Bipolar Junction Transistor) to adapt to the two voltage range situations, which include ‘$-10\text{V}$–$10\text{V}$’ and ‘$-2\text{V}$–$2\text{V}$’ in this system. The circuit diagram of signal switching is presented in Fig. 3. If the input signal range is ‘$-10\text{V}$–$10\text{V}$’, the signal will enter the step-down circuit composed of the resistors Ra2, Ra3, and Ra4, and the output signal of the step-down circuit ranges from $-2\text{V}$ to $2\text{V}$. If the input signal voltage range is ‘$-2\text{V}$–$2\text{V}$’, the signal will directly enter the analog signals amplification circuit. Second, a two-stage amplifier connection is used in the analog signals amplification circuit. The circuit diagram of the analog signals amplification is presented in Fig. 4. Additionally, a trigger driver circuit has been designed to trigger FPGA to transmit the digital signals to the PXIe interface, as shown in Fig. 2.

The gain of the circuit in Fig. 4 can be determined by Eq. (1).

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{V_{\text{out}}^P - V_{\text{out}}^N}{V_{\text{in}}} = \frac{R_F + R_G}{R_G}.$$  \hspace{1cm} (1)

According to the Fig. 4, the transfer function of a single channel analog signals circuit can be determined by Eq. (2), Eq. (3), and Eq. (4).

$$H_P(S) = \frac{V_{\text{out}}^P}{V_{\text{in}}} = \frac{1}{sC_1R_1 + 1}.$$  \hspace{1cm} (2)

$$H_N(S) = \frac{V_{\text{out}}^N}{V_{\text{in}}} = -\frac{R_F}{R_G(sC_1R_1 + 1)(sC_2R_F + 1)}.$$  \hspace{1cm} (3)

$$H(S) = H_P(S) - H_N(S) = \frac{sC_2R_F + R_F + R_G}{R_G(sC_1R_1 + 1)(sC_2R_F + 1)}.$$  \hspace{1cm} (4)

Here, the single-ended four-channel operational amplifier ADA4851 [10] is adopted as the preamplifier, which also acts as a voltage follower to buffer, isolate, and improve load capacity and impedance matching; the dual-channel operational amplifier LT1819 [11] is adopted as the main amplifier, which also acts as the driver of the ADC in the single-ended mode to differential mode, as shown in Fig. 4. The gain of the analog signals amplification circuit is 2, so the output signal of it ranges from $-4\text{V}$ to $4\text{V}$.

2.1.2 ADC circuit

The ADC input voltage range has to meet the output voltage range of the analog signals amplification circuit. Additionally, the sampling rate of the ADC has to meet the Nyquist sampling rate, and the ADC has to enable the FPGA to read the digital signals of its output. The commonly used ADC LTC2325 (16 bit) [12], which has four simultaneously sampling serial transmission channels and can achieve a 5 MSPS (Million Samples Per Second) sampling rate, is adopted in this system. To ensure the accuracy of data acquisition and to reduce signal crosstalk, SDR (Single Data Rate) and LVDS (Low-Voltage Differential Signaling) modes are adopted. A circuit diagram of the ADC LTC2325 is presented in Fig. 5. The timing diagram of the LTC2325 presented in [12] is adopted. The sampling and conversion of the LTC2325 are controlled by a CNV (Convert) pin, the rising edge on the CNV will start the sampling process, and the falling edge will start the conversion and readout process. The conversion process is timed by the SCK (Serial Data Clock) provided at [12].

2.1.3 FPGA and PXIe connection circuit

The ADC’s output digital signals can be acquired by the FPGA. In this system, a Xilinx FPGA chip Kintex7-325T-900-2, whose operating time can reach less than 1 ns [13], is adopted. The output of the ADC will be obtained by the FPGA. However, because the FPGA chip being exposed to
radiation will undoubtedly cause the problem of single event upset, the functions performed by the system will be adversely affected. Therefore, to reduce the probability of single event upset in this system, the Verilog HDL (Hardware Description Language) and the design of the peripheral circuit for the FPGA have been continuously modified and optimized. The PXIe connector is used to transmit the FPGA’s output data to the NI chassis with transmission speeds that can reach up to 2.5 Gb/s [1, 3, 14, 15, 16, 17, 18, 19]. The connection circuit diagram of FPGA and PXIe is presented in Fig. 6. The pins’ functions of the PXIe connector are presented in Table I.

| Table I. Pins’ functions of the PXIe connector |
|-----------------------------------------------|
| PXIe DSTARB | PXIe DSTARB is designed for distributing high-speed, high-quality trigger signal from the NI chassis |
| PXI TRIG | PXI TRIG is a bidirectional trigger signal, and it is used to trigger the PXIe connector |
| REFCLK | 100 MHz reference clock |
| PXIe CLK100 | 100 MHz clock signal |
| PERST | Reset signal |
| PET | Signal transmission pin of the PXIe connector |
| PER | Signal reception pin of the PXIe connector |

2.1.4 Power supply
The power supply module is designed as DC/DC (Direct Current to Direct Current) combination with LDO (Low Dropout Regulator) in this system. The DC/DC primarily converts higher voltages into lower voltages. The LDO mainly provides a power supply with low noise for the system’s main chips. A stabilized voltage supply is used to provide 12 V, and the power chips are used to convert the 12 V to the required supply voltages, such as −6 V, −5 V, 1 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V, 5 V, and 12 V. The power supply block diagram is presented in Fig. 7.
2.2.2 Software
To save and analyze the obtained signals from the PXIe connector, the host computer interface has been designed in LabVIEW 2017. The digital signals execution flow chart of LabVIEW-based interface is presented in Fig. 10, the functions of the host computer modules are presented in Table II, and the data processing module from LabVIEW is presented in Fig. 11.

![Digital signals execution flow chart of LabVIEW-based interface.](Image)

**Table II. Functions of the host computer modules**

| Function     | Description                                                                 |
|--------------|-----------------------------------------------------------------------------|
| Initial      | Set port ID, data save path and open the software                           |
| Idle         | Write the output data, initial and generate random array                    |
| Start        | Write the sent array of PXIe                                               |
| DAQ          | Judge, read, and calculate the PXIe data, replace the random array          |
| Data Ready   | Register changes to the write state                                        |
| Exit         | Exit the command                                                           |

![Data processing module from LabVIEW.](Image)

3. Experimental results

3.1 The attenuation curve of the analog signals circuit
The attenuation curve is presented in Fig. 12. The signals collected by the analog signals circuit of this system do not attenuate at frequencies less than 15 MHz.

![Attenuation curve](Image)

3.2 The digital signal acquired by FPGA
Here, a 0.5 MHz sine wave is adopted as an example. The ADC output digital signal acquired by FPGA is displayed by the function of ‘Set Up Debug’ in the software Vivado 2016.3, which is presented in Fig. 13. The ADC chip LTC2325 has an $8\,V_{pp}$ (Peak-Peak) ($-4\,V$–$4\,V$) differential input range and no missing codes at 16 bits. The most significant bit is the sign bit, and the remaining 15 bits are the data bits [12]. Because the gain of the analog signals amplification circuit has been set as 2, the resolution can reach 0.122 mV. The input voltage (mV) of the signal can be calculated by Eq. (5), where $D[i]$ is the i-th bit of the ADC output.

$$V_{in} = \begin{cases} 
0.122 \times 2^0 \times D[i], & D[15] = 0 \\
0.122 \times 2^0 \times (D[i] - 1), & D[15] = 1.
\end{cases}$$

![Digital signal diagram fetched by set up debug.](Image)

(a) 0 V Low level, 2 V High level, 0.5 MHz frequency sine wave.
(b) −1 V Low level, 1 V High level, 0.5 MHz frequency sine wave.
3.3 Input signal echo in the host computer

The waveform echo of the signal in the host computer is presented in Fig. 14 after data processing.

![Signal echo in the host computer](image)

**Fig. 14.** Signal echo in the host computer (−1 V Low level, 1 V High level, 0.5 MHz frequency sine wave).

4. Conclusion

In this paper, a designed PXIe-based multi-channel data acquisition system of soft X-ray camera’s output signals is adopted, multi-channel chips and serial ADCs are adopted. Specially, a differential transmission mode is adopted to reduce the signal crosstalk in this system. Soft X-ray camera signals within 1 MHz have been acquired and processed by this system.

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References

[1] M. Ruiz, et al.: “ITER fast plant system controller prototype based on PXIe platform,” Fusion Eng. Des. 87 (2012) 2030 (DOI: 10.1016/j.fusengdes.2012.05.013).
[2] B. Gonçalves, et al.: “ITER fast plant system controller prototype based on ATCA platform,” Fusion Eng. Des. 87 (2012) 2024 (DOI: 10.1016/j.fusengdes.2012.04.005).
[3] D. Sanz, et al.: “Advanced data acquisition system implementation for the ITER neutron diagnostic use case using EPICS and FlexRIO technology on a PXIe platform,” IEEE Trans. Nucl. Sci. 63 (2016) 1063 (DOI: 10.1109/TNS.2016.2517402).
[4] Y. H. Chung, et al.: “Design of a compact soft X-ray pinhole camera for plasma studies in the Hanbit magnetic mirror device,” NSSMIC 1 (2000) 141 (DOI: 10.1109/NSSMIC.2000.949066).
[5] L. Hu, et al.: “Design and test of irradiation-related components in ITER radial X-ray camera,” IEEE Trans. Nucl. Sci. 65 (2018) 2398 (DOI: 10.1109/TNS.2018.2849410).
[6] L. Hu, et al.: “Outline design of ITER radial X-ray camera diagnostic,” Fus. Sci. Technol. 70 (2016) 112 (DOI: 10.13182/FST15-137).
[7] L. Hu, et al.: “Preliminary design and R&D of ITER diagnostic-radial X-ray camera,” Nucl. Instrum. Methods Phys. Res. Sect. A 870 (2017) 50 (DOI: 10.1016/j.nima.2017.07.021).
[8] G. Nan, et al.: “Design of multi-channel pulse amplitude acquisition card based on NIM system,” Nuclear Electronics & Detection Technology 31 (2011) 1250.
[9] Omron, Inc: G6K.
[10] Analog Devices, Inc: ADA4851-1/ADA4851-2/ADA4851-4.
[11] Analog Devices, Inc: LT1818/LT1819.
[12] Analog Devices, Inc: LTC2325-16.
[13] Xilinx, Inc: Kintex-7 FPGA Data Sheet (DS182), v2.16.1 (2018).
[14] S. Miao, et al.: “Review, comparison and outlook of test bus,” ICEMI (2011) 211 (DOI: 10.1109/ICEMI.2011.6037799).
[15] R. D’Arcy, et al.: “Characterisation of the PXIE Allison-type emittance scanner,” Nucl. Instrum. Methods Phys. Res., Sect. A 815 (2016) 7 (DOI: 10.1016/j.nima.2016.01.039).
[16] D. Sanz, et al.: “IEEE 1588 clock distribution for FlexRIO devices in PXIe platforms,” Fusion Eng. Des. 89 (2014) 652 (DOI: 10.1016/j.fusengdes.2014.02.029).
[17] A. Carpeño, et al.: “Implementing a neutron-diagnostic advanced DAQ system use case on a PXIe platform through a 3D remote laboratory,” Fusion Eng. Des. 123 (2017) 882 (DOI: 10.1016/j.fusengdes.2017.03.100).
[18] H. Xili, et al.: “Measurement for thin film transistor electrical performance based on PXIe bus,” ICEMI (2017) 562 (DOI: 10.1109/ICEMI.2017.8266004).
[19] M. Gou, et al.: “Design of the PXIe bus reconfigurable test instrument,” Process Automation Instrumentation 38 (2017) 68 (DOI: 10.16086/cj.ksn.2010-0380.201711017).
[20] W. Fu, et al.: “A low delay transmission mechanism of multi-channel video based on FPGA,” IOP Conf. Ser.: Mater. Sci. Eng. 322 (2018) 052032 (DOI: 10.1088/1757-899X/322/5/052032).
[21] A. Kulkarni, et al.: “An energy-efficient programmable manycore accelerator for personalized biomedical applications,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 26 (2018) 96 (DOI: 10.1109/TVLSI.2017.2754272).
[22] Q. Ran, et al.: “Design of data acquisition system for dynamic simulation centrifuge test,” ICEMI (2011) 147 (DOI: 10.1109/ICEMI.2011.6037785).
[23] D. Mbakoyannis, et al.: “Energy-performance considerations for data offloading to FPGA-based accelerators per PCIe,” ACM Trans. Archit. Code Optim. 15 (2018) 14 (DOI: 10.1145/3180263).
[24] E. Esquembri, et al.: “Hardware timestamping for an image acquisition system based on FlexRIO and IEEE 1588 v2 standard,” IEEE Trans. Nucl. Sci. 63 (2016) 228 (DOI: 10.1109/TNS.2016.2516640).
[25] S. Saxena and A. I. Hawari: “Investigation of FPGA-based real-time adaptive digital pulse shaping for high-count-rate application,” IEEE Trans. Nucl. Sci. 64 (2017) 1733 (DOI: 10.1109/TNS.2017.2692219).
[26] H. Choe, et al.: “Multichannel FPGA-based data-acquisition system for time-resolved synchrotron radiation experiments,” IEEE Trans. Nucl. Sci. 64 (2017) 1320 (DOI: 10.1109/TNS.2017.2655366).
[27] H. Zeng, et al.: “Wideband signal transceiver module with a Doppler shift function,” Rev. Sci. Instrum. 89 (2018) 125110 (DOI: 10.1063/1.5066322).
[28] R. Herrero, et al.: “FPGA-based solutions for analog data acquisition and processing integrated in area detector using FlexRIO technology,” IEEE Trans. Nucl. Sci. 65 (2018) 781 (DOI: 10.1109/TNS.2017.2782827).
[29] A. Borowicz: “Using a multichannel Wiener filter to remove eyeblink artifacts from EEG data,” Biomed. Signal. Process. 45 (2018) 246 (DOI: 10.1016/j.bsp.2018.05.012).
[30] L. Tan, et al.: “Design and implementation of multi-channel data acquisition system based on FPGA,” Electr. Meas. Technol. 41 (2018) 57 (DOI: 10.19651/j.cki.ent.1701226).
[31] S. Li: “Design of multi-channel data acquisition and analysis system based on LabVIEW,” Telecom Power Technol. 33 (2016) 95 (DOI: 10.19399/j.cki.ipt.2016.03.037).
[32] P. Shi: “Design of FPGA multi-channel data acquisition system based on gigabit Ethernet,” Electronic Sci. & Tech. 28 (2015) 123 (DOI: 10.16180/j.cki.isst.2015.02.033).
[33] S. Zhang, et al.: “Design of high-speed multi-channel data acquisition system based on FPGA and ARM,” Automation & Instrumentation (2015) 110 (DOI: 10.14016/j.cki.1001-9227.2015.08.110).
[34] J. Shi, et al.: “Design of the FPGA-based multichannel data acquisition system,” Electrical Automation 38 (2016) 15 (DOI: 10.3969/j.issn.1000-3886.2016.01.006).

[35] G. Liu, et al.: “A digital method for the discrimination of neutrons and γ rays with organic scintillation detectors using frequency gradient analysis,” IEEE Trans. Nucl. Sci. 57 (2010) 1682 (DOI: 10.1109/TNS.2010.2044246).

[36] J. van Es, et al.: “Accuracy of X-ray with perfusion scan in young patients with suspected pulmonary embolism,” Thromb. Res. 136 (2015) 221 (DOI: 10.1016/j.thromres.2015.05.018).

[37] A. Kumar, et al.: “Design and FPGA synthesis of three stage telecommunication switching in HDL environment,” Proc. Comput. Sci. 48 (2015) 454 (DOI: 10.1016/j.procs.2015.04.119).

[38] N. Hoque: “Real-time DDoS attack detection using FPGA,” Comput. Commun. 110 (2017) 48 (DOI: 10.1016/j.comcom.2017.05.015).

[39] M. Peker: “Hardware implementation of a scale and rotation invariant object detection algorithm on FPGA for real-time applications,” Turk. J. Elec. Eng. & Comp. Sci. 24 (2016) 4368 (DOI: 10.3906/elk-1406-187).

[40] Y. Shan, et al.: “An efficient precision estimation method for a multichannel data acquisition system,” IEICE Electron. Express 10 (2013) 20130393 (DOI: 10.1587/elex.10.20130393).