1. Introduction

Digital integrated circuits are mostly consisting of transistors. In digital market it is observed that physical size of the devices is getting chopped with the enhancement of technology. In year 1971, semiconductor devices were manufactured at 10 um nodes and now at present this technology node has reached to approximately 20 nm and the devices are getting portable. As physical size of device is getting lower means the size of internal components is also reducing. Transistor acts as a backbone in any electrical circuit. In order to achieve a very proficient performance, it is very important for internal components to work at their best. If we look upon the MOS transistor, short channel effects comes into picture when device comes to scaling and therefore there is a need to improve the performance of internal components of the device to achieve performance far better than the threshold. Internal electrical components need to provide a high quality output with lesser losses of power. MOS transistor act as an electrical switch which functions in many circuits like complementary MOS etc. Switching is one of the most significant activities in any circuit.

The conventional MOSFET comprises of source and drain junction. The short channel effects which devastate the performance of any device are involved due to presence of P-N junctions. It has become a need to reduce short channel effects along with the reduction in channel of the device. It has also become a challenge for fabrication industry to fabricate such conventional MOSFET's at smaller scale with very fine and accurate alignment of junctions. A new concept has been enlightened to reduce such complexity in which MOS transistor are made without junctions resulting into reduction of short channel effects known as junction less technology. A junction less device has a uniform doping throughout the distance from source to drain.

Electron densities varying with gate to source voltage for conventional and junction less dual gate MOS is shown in Figure 1 and Figure 2 respectively. In figure 1 we can see the various stages of electron density of conventional MOS at different gate voltages. When gate voltage is at 0V...
there are no carriers in the channel region, as gate voltage starts increasing and reaches at 1V we can see the channel starts forming at upper and lower surface of the substrate due to the presence of dual gate. After gate voltage increased from 1V we can imagine the proper inversion of channel taking place in conventional dual gate MOS. A conventional MOS device works after inversion mode is setup. The channel so created in conventional mode is on the surface of the device called surface conduction and in junction less channel is created in the bulk of the device called as bulk conduction. In dual gate MOSFET, there are two gates which are interconnected to each other and controlling the flow of carriers whether it is conventional or junction less device. The work function of both the gates in junction less device plays an efficient role to switch off or on the device. Junction less devices are always operated at those work functions which are opposite to conventional one. This means the work function for conventional NMOS is same as that for junction less PMOS. In Figure 2, we can see the channel formation in terms of electron density when gate voltages are increased from 0V to 1V.

In this paper the drawing structure and simulations of double gate junction less and conventional P and N-type along with short channel and performance parameters have been measured at different channel lengths. In addition to this the structure and various simulation results of junction less CMOS inverter is also evaluated at various technology nodes. All structures N-type DGJLT, P-type DGJLT, N-type Conventional DGMOS, P-type conventional DGMOS, junction-less CMOS inverter are drawn using TCAD simulator. All simulations are performed at different dimensions, different work function, different channel lengths. This paper is classified as follows. In section 2, the structure of various devices and conditions for simulations will be discussed. In section 3, the simulations results of junction less CMOS and other conventional and junction less DGNMOS and DGPMOS will be discussed at different parameters and in section 4 will conclude all the discussion.

2. Device Structure

The devices used for simulation are drawn using TCAD software. All structures are drawn at different channel lengths. The conventional N-type and P-type double gate MOS are drawn with N-type polysilicon and P-type Polysilicon as gate materials respectively. The N-type and P-type junction less double gate MOS have P-type polysilicon and N-type polysilicon respectively. The structure of junction-less N-type/P-type and conventional N-type/P-type are shown in Figure 3. a and 3. b respectively. The conventional double gate N-type/P-type MOS has different source/drain and channel doping whereas in junction-less N-type/ P-type has an identical doping.
A new type of device made using junction less technology called junction less double gate complementary MOS. A junction less inverter is made by combining both junction less NMOS and PMOS with an oxide separating them. All design parameters are same used for designing JLT PMOS/NMOS. Design parameter values are illustrated in Table A. CMOS inverter is used in almost all digital circuits for switching.

This JLT CMOS made using double gate transistors are easily fabricated as there is no need to form n-well/P-well which is necessary for conventional CMOS. As in this type of inverter we have both junction less transistors giving their best performance parametric values at small dimensions. This type of inverter can be easily fabricated at smaller scale dimensions. There are no junctions present in this CMOS structure which will reduce the devastation of the performance of the inverter. The physics of JLT CMOS inverter is different due to presence of bulk conduction in this technology. CMOS acts as an inverter in which the input is applied onto both the gates of the transistor and output is obtained at the drain ends of both the transistor. The width of JLT PMOS is made double than NMOS so that charging time of output node can become almost same as that of discharging time.

The doping for both junction less double gate NMOS and junction-less double gate PMOS are taken same as 1.5e+19 cm⁻³. This is due to series connection of both PMOS and NMOS. The current flowing has to be same throughout the inverter. JLT CMOS inverter is structured by combining 10, 20, 30, 40nm of JLT-PMOS and NMOS. JLT CMOS structure is shown in Figure 4. Channel formation in JLT CMOS inverter at different gate voltages is also shown in Figure 5. This CMOS structure is closely packed than conventional one. Doping in junction less devices needs to be higher to achieve better on current due to the presence of one type of impurities. All four gates in the JLT CMOS inverter structure are interconnected and input is applied to the common gate. Also both drains of PMOS and NMOS are too interconnected to obtain the output.

As JLT CMOS structure is made by combining both JLT PMOS and NMOS. Therefore it can be observed that channel formation which is used to carry current in the inverter is like one after the other. It can be seen in figure E that net increase in charge is observed first in JLT NMOS and then JLT PMOS. Clearly for JLT NMOS gate voltages will be applied positive as threshold voltage.

| Parameter Name | Conv. DGNMOS | JLT DGNMOS | Conv. DGPMOS | JLT DGPMOS | JLT CMOS |
|----------------|--------------|-------------|--------------|-------------|----------|
| Work function  | 4.2eV        | 5.3eV       | 5.2eV        | 4.2eV       | PMOS     |
|                |              |             |              |             | NMOS     |
|                |              |             |              |             | 4.2eV    |
|                |              |             |              |             | 5.3eV    |
| Channel length | 10-40nm      | 10-40nm     | 10-40nm      | 10-40nm     | 10-40nm for both PMOS and NMOS |
| Type of gate material | N+ polysilicon | P+ polysilicon | P+ polysilicon | N+ polysilicon | PMOS |
|                |              |              |              |              | NMOS |
|                |              |              |              |              | N+ Poly |
|                |              |              |              |              | P+ Poly |
| Oxide thickness | 1nm          | 1nm         | 1nm          | 1nm         | 1nm each for both PMOS and NMOS |
| Doping         | 1)N-type S/D = 1e+20 cm⁻³ 2)P-type Sub = 1e+18 cm⁻³ | N-type S/D/ Sub: 1.5e+19 cm⁻³ | 1)P-type S/ D=1e+20 cm⁻³ 2)N-type Sub- =1e+18 cm⁻³ | P-type S/D/ Sub: 1.5e+19 cm⁻³ | Doping values used for JLT NMOS and JLT PMOS |
Simulation and Characterization of Junction Less CMOS Inverter at Various Technology Nodes

In this paper, Junction less CMOS inverter is made by using double gate MOS as there are two gates which are placed at the top and bottom to control the flow of carriers in both JLT PMOS and JLT NMOS. The presence of two gates in a structure also ensures that no part of the structure is far from the gate which is controlling the gate flow. Using double gate structure, it is possible to achieve better short channel effects. The design and fabrication of junction less CMOS is easier and simpler than conventional one. Doping and work function of both the JLT MOS is responsible for the current flowing in the device and is responsible for carriers to get depleted and hence making the device off.

**Figure 4.** Structure of junction-less CMOS inverter

**Figure 5.** Net charge increase (cm$^{-3}$) in JLT PMOS after JLT NMOS in double gate Junction less CMOS inverter.

### 3. Results and Comparison

The performance of any structure depends upon the performance of individual components. As the CMOS inverter is made using PMOS and NMOS therefore the electrical characteristics of both types of transistor will be responsible for the results of an inverter. Conventional MOS and junction less MOS are compared at various channel lengths. There are different parameters which can define the performance of conventional and JLT namely ON current, OFF current, ON/OFF current ratio, Threshold voltage, subthreshold slope, Drain Induced Barrier Lowering (DIBL) are measured at various conditions mentioned in table. All results of simulations are obtained after considering some conditions. There is no impact ionization effect is taken as due to this effect the carrier concentration will shoot up and will disturb all the analysis related to given parameters, mobility model is taken to be as Lombardi, all are performed at room temperature and at smaller voltages.

#### 3.1 Conventional DGMOS vs Junction Less DGMOS

Conventional MOS are made of different types of doping in the substrate. They are namely P channel MOS or N channel MOS. Due to the presence of junctions it has been observed that short channel effects starts devastating the performance of the device. As technology nodes are reducing to improve the area and speed, it has been seen that leakage current which is an undesired current starts increasing to a large value and hence disturbing all performance parameters.

**Figure 6** shows the leakage current at 10, 20, 30, 40nm channel length of both conventional and junction less MOS. Junction less MOS are free of junctions and short channel effects are very small in comparison to conventional one. Leakage current is the most threatening parameter for any device. This can detrimental the accomplishment of any device.

From figure 6 it can be explained that the junction less transistor has a leakage current of order $10^{-9}$A at L= 10nm and $10^{-15}$A at L=40nm and conventional double gate MOS has a leakage current of order $10^{-7}$A at L=10nm and $10^{-11}$ A at L=40nm. The undesired current is decreasing as the length of the channel is increasing this is due to increase in the area of the device. Leakage current is responsible for the worst output. As technology nodes are decreasing year by year leakage current is increasing and in order to obtain a high class performance of the device along with the scaling, the junction less transistor technology has becoming an assurance to achieve the best performance parameters along with the scaling. The dimensions of the devices are lowered down to achieve the faster speed. But the leakage current as a tradeoff is spoiling the performance of the device. However it can be observed that for same conditions the conventional dual gate MOS is giving worst performance than junction less DGMOS. Also ON current is observed to be approximately of order $10^{-5}$A for both types of technologies. All performance parameters such as ON current, OFF current, ON/OFF current ratio, Threshold voltage, subthreshold slope, Drain Induced Barrier Lowering (DIBL) at channel lengths 10nm, 20nm, 30nm, 40nm have been calculated.

The leakage...
current in conventional double gate MOS is much higher than double gate Junction less transistor. Therefore the performance of any device made of conventional MOS will give worst performance than device made of junction less technology.

3.2 Junctionless CMOS Inverter

Complementary MOS technology is used in many digital circuitries. CMOS uses a combination of P-type and N-type transistor. PMOS and NMOS are connected in series to achieve the same current. It has been observed in previous section that conventional MOS has larger leakage current than junction less. Also fabrication of conventional MOS is somewhere typical than junction less MOS. To achieve best results from the device, it is necessary to use junction less based PMOS and NMOS. CMOS device has a main important characteristics that it has a good noise margin. Figure 7 shows the butterfly curve or voltage transfer characteristic curve of double gate junction less based CMOS inverter at channel lengths 10nm, 20nm, 30nm, 40nm of both PMOS and NMOS each.

![Figure 6. Transfer characteristics of double gate junction less (left) and conventional (right) MOS at Vds=50mV.](image)

![Figure 7. VTC curve of DG-junction less CMOS at various channel lengths.](image)

It can be observed from the above figure that as the channel length is increased of both PMOS and NMOS say from 10nm to 40nm, the VTC curve become more steeper. At 40nm technology due to increase in area of the each device the leakage current is almost negligible and this means when the device is off there will almost no current which is flowing in the device and hence when input voltage becomes higher the output tends to zero immediately resulting into better performance of junction less based CMOS inverter. The below mentioned steps shows the fabrication of conventional CMOS inverter, it can be seen that total of 20 steps have to be followed for fabricating conventional CMOS

- Take a Substrate
- Grow an oxide layer over the substrate
- Grow a photoresist layer either positive or negative
- Do masking over it
- Remove the photoresist layer
- Remove the oxide layer deposited
- Again remove the photoresist layer depending upon where window has to be etched
- Using Ion- implementation, make N-well regions
- Remove Silicon dioxide from selected areas
- Deposit the polysilicon layer on both the gates
- Remove unnecessary layers from the surface
- Grow the oxide layer again
- Do masking and diffuse N-type material to make Source and drain for NMOS
- Oxide layer which are deposited needs to be stripped
- Diffuse P-type material to form PMOS
- Again grow thick field oxide
- Do the metallization, using aluminium to form metal contacts
- Remove all the excess material from the surface
- Make the terminals
- Finally assigned all the names of the terminals

In junction less transistor, there is no need to form any junctions in the entire device. Therefore no need to form N-well and p-well regions mentioned in step no 8. Along with this step, the other steps used to implement this region will also be reduced. So junction less based CMOS inverter will have lesser fabrication steps.

Noise margin is defined as the amount of noise that CMOS circuit can handle without affecting the performance of the device. The VTC curve at channel length 40nm is more stepper and better than any other channel length therefore noise margin is expected to achieve higher value. The value of noise margin is mentioned in Table B.
Table B. Noise margin of junction less based CMOS inverter high voltage 1V

| Channel length | High Noise Margin (NM_H) | Low Noise Margin (NM_L) |
|----------------|--------------------------|-------------------------|
| 10nm           | 0.28                     | 0.32                    |
| 40nm           | 0.43                     | 0.52                    |

The transient response of junction less CMOS inverter is shown in Figure 8. Junction less technology can also show the same transient response than that of conventional in an improved version and with an easy fabrication. The transient response is an evidence which shows that junction less PMOS and NMOS are worth to make an important building block of electrical circuit.

The transient response of junction less CMOS inverter is shown in Figure 8. Junction less technology can also show the same transient response than that of conventional in an improved version and with an easy fabrication. The transient response is an evidence which shows that junction less PMOS and NMOS are worth to make an important building block of electrical circuit.

Figure 8. Transient behavior of double gate junction less CMOS inverter at channel lengths 20 nm and 40 nm of each JLT PMOS and JLT NMOS.

It can be illustrated from the figure that when channel lengths of both P-type and N-type JLT’s is 20 nm output response is taking lesser time than at channel lengths 40 nm. This means that speed of operation at 20 nm is greater than 40 nm. The blue line is reaching low or high potential first than the black line representing channel length 40 nm. A better and an accurate transient curve of CMOS inverter can be obtained due to better performance parameters of Junction less transistors.

4. Conclusion

The double gate junction less transistor has proved to be better than conventional one in terms of performance parameters. The channel formation and the importance of both junction less and conventional transistors have been explained. Double gate junction less transistor based CMOS inverter is also structured and analysis for the same has been done at different technology nodes. It has been concluded that for scaled and smaller devices the junction less technology has proved to be capable of providing good performance of the devices with lesser flaws. The noise margin and speed of junction less CMOS inverter at various nodes have been discussed. Junction less based CMOS inverter resulted into sharp VTC pattern and can promise lesser fabrication steps than conventional inverter. Therefore at lower voltages, to overcome short channel effects, junction less based devices are best proven candidature for upcoming technology nodes. The device namely CMOS inverter made using junction less technology in this paper has proved that all characteristics of CMOS inverter is same that of conventional with little improvement, however in terms of fabrication point of view, for a fabrication engineer to make such devices with lower channel lengths is somewhere easier than conventional one.

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