Thermal management of coaxial through-silicon-via (C-TSV)-based three-dimensional integrated circuit (3D IC)

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Abstract: The analytical temperature model of coaxial through-silicon-via (C-TSV)-based three-dimensional integrated circuit (3D IC) is developed based on the Fourier’ law of heat transfer and energy conservation, and is verified by employing ANSYS. Based on the theoretical model, several design guidelines are concluded. From the point of thermal management, 1) TSV should be inserted with high density; 2) Cu is a better material than Al and W; 3) the 3D IC layer should be as few as possible; 4) the silicon substrate thickness should be as thin as possible; 5) the temperature-sensitive modules should be placed near TSV and heat sink.

Keywords: thermal management, three-dimensional integrated circuit (3D IC), coaxial through-silicon-via (C-TSV), temperature

Classification: Integrated circuits

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1 Introduction

The three-dimensional integrated circuit (3D IC) has attracted tremendous interest in semiconductor industry consists of multiple dies stacked into a single chip [1]. The key enabling technology for 3D IC is through-silicon-via (TSV) [2], which allows for implementing vertical electrical connections between active layers and thus a reduction of global interconnects and total wire-length. Therefore, TSV-based 3D IC can provide higher timing performance, lower power consumption, and smaller chip footprint area [3].

The coaxial TSV (C-TSV) offers superior electrical performance in high frequency applications than ordinary cylindrical and annular TSVs [4], and consequently has drawn more and more attentions of researchers. By now, the electrical and thermo-mechanical performances of C-TSV-based 3D IC have been studied sufficiently [5, 6, 7, 8]. However, there is hardly research focusing on the temperature performance and thermal management.

In this letter, the analytical model of the temperature of C-TSV-based 3D IC is developed and verified, based on which the temperature performance is investigated and several design guidelines are given.

2 Analytical model

The schematic of a C-TSV-based n-layer 3D IC is shown in Fig. 1(a). Every die is comprised by silicon substrate layer and back end of line (BEOL) metal-dielectric layer, and connected to neighboring dies through a bonding layer. The package and heat sink is at the top and bottom, respectively [8]. On the right side of Fig. 1(a), the drawing of partial enlargement of the cross-sectional view of C-TSV is also given, which is composed of the metallic core, surrounding silicon dioxide and metallic annuluses, and outer oxide liner to separate metal from silicon substrate [9].

In general, one-dimensional approximation is always assumed to evaluate the thermal behavior of TSV-based 3D IC [10]. That is to say, uniform heat flows to the ambient through the heat sink and package, neglecting horizontal heat spreading. Fig. 1(b) shows the equivalent thermal resistance network, where $T_{\text{amb}}$ is the ambient temperature; $R_{\text{BEOL}}$, $R_{\text{Si}}$, $R_{\text{bond}}$, $R_{\text{C-TSV}}$, $R_{\text{hs}}$, and $R_{\text{pk}}$ represent the thermal resistances of BEOL, silicon substrate, bonding layer, C-TSV, heat sink, and package, respectively; $j = 1, 2, \ldots, n$, is the $j$th layer of 3D IC; $R_j$ is the total thermal resistance of the $j$th layer; $T_j$ is the temperature at the top of the $j$th layer; $Q_j$ is the heat generation of the $j$th layer, including the device power on the top of each substrate surface and interconnects power in each BEOL layer; $q_j$ is the heat flow from the $j$th to the $(j - 1)$th layer.
According to the Fourier’s law of heat transfer and energy conservation, the analytical expression for temperature of the top of the $i$th layer of an $n$-layer 3D IC can be described as [10]

$$
T_i = \frac{R_{hs}}{1 - F_j} \left( 1 + \sum_{j=1}^{i} \frac{R_j}{R_{hs}} \right) + \frac{R_{hs}}{1 - F_j} \left( 1 + \sum_{j=1}^{i-1} \frac{R_j}{R_{hs}} - F_j \sum_{j=i+1}^{i} \frac{R_j}{R_{hs}} \right) + T_{amb}
$$

where

$$
F_j = \frac{1 + \sum_{l=1}^{j} \frac{R_l}{R_{hs}}}{1 + \frac{R_{pk} + \sum_{l=1}^{n} \frac{R_l}{R_{hs}}}{R_{hs}}}
$$

We define C-TSV insertion density $\rho$ as a ratio of C-TSV-occupied area and the total die area $S$. According to Ohm’s Law, the total thermal resistance of the first layer $R_1$ and the $j$th ($j = 2, 3, \ldots, n$) layer $R_j$ can be expressed as

$$
R_1 = \frac{t_{Si}}{k_{Si}S} + \frac{t_{BEOL}}{k_{BEOL}S}
$$

$$
R_j = \frac{1}{(1 - \rho)S} \left( \frac{t_{Si}}{k_{Si}} + \frac{t_{bond}}{k_{bond}} + \frac{t_{BEOL}}{k_{BEOL}} \right) || R_{C-TSV} \quad (j = 2, 3 \ldots, n)
$$

$$
R_{C-TSV} = \frac{t_{TSV}}{\rho k_{TSV}S \left( 1 - \frac{r_{m}^2 + 2(t_{m} + r_{m})}{r_{m} + t_{d} + t_{m}} \right)}
$$

where $k_{BEOL}$, $k_{Si}$, and $k_{bond}$ are the thermal conductivities and $t_{BEOL}$, $t_{Si}$, and $t_{bond}$, are the thicknesses of BEOL, silicon substrate, and bonding layer, respectively; $k_{TSV}$ is the thermal conductivity of TSV metal; $t_{TSV}$ is the height of C-TSV; $r_{m}$, $t_{m}$, and $t_{d}$ are the inner metal radius, outer metal thickness, and dielectric thickness of C-TSV, respectively.

By substituting Eqs. (2)–(5), we can obtain the analytical expression for temperature of C-TSV-based 3D IC.
3 Model verification

Finite element method (FEM) simulation is performed using ANSYS [11] to verify the analytical model for the temperature of C-TSV-based 3D IC, taking a ten-layer 3D IC for instance. In the FEM simulation, the internal heat generation is selected for the top surface of substrate and the body of BEOL, the perfectly insulated boundary condition is applied to the four side surfaces; and the ambient temperature of 27°C is fixed to the top surface of package and the bottom surface of heat sink. The structure and physical parameters used for the FEM simulation and analytical model are listed in Tables I and II, respectively.

| Table I. Values of the structure parameters |
|---------------------------------------------|
| Parameter                          | Value       |
| C-TSV height of every layer         | 80 µm       |
| Dielectric thickness of C-TSV       | 2 µm        |
| Inner metal radius of C-TSV         | 3 µm        |
| Outer metal thickness of C-TSV      | 2 µm        |
| Oxide liner thickness of C-TSV      | 0.1 µm      |
| Thickness of silicon substrate      | 50 µm       |
| Thickness of bonding layer          | 10 µm       |
| Thickness of BEOL                   | 20 µm       |
| 3D IC layer number                  | 10          |
| Die area                           | 10 × 10 mm² |

| Table II. Values of the physical parameters |
|---------------------------------------------|
| Parameter                          | Value       |
| Thermal conductivity of BEOL          | 1.4 W/(m·K) |
| Thermal conductivity of silicon substrate | 150 W/(m·K) |
| Thermal conductivity of bonding layer | 0.15 W/(m·K) |
| Thermal conductivity of TSV metal     | 390 W/(m·K) |
| Power density of device layer         | 12.5 W/cm²  |
| Power density of BEOL layer           | 1.25 W/mm³  |
| Thermal resistance of heat sink       | 2 K/W       |
| Thermal resistance of package         | 20 K/W      |

Fig. 2. Temperature distribution of a ten-layer C-TSV-based 3D IC.
Fig. 2 compares the temperature results obtained from the analytical model and FEM simulation for a ten-layer 3D IC. It is shown that, the results of analytical model matches well with the FEM simulation data, which proves the accuracy of the analytical model. In addition, the temperature of the layer close to the heat sink is much lower than that of the layers far from heat sink, due to the high transmission efficiency of heat sink. The top two layers have the similar temperature, since the package can dissipate some heat of the top layer.

4 Design guidelines

In this section, according to the analytical model, the impacts of several crucial parameters of C-TSV-based 3D IC on the temperature are analyzed, based on which the design guidelines are given for the thermal management of C-TSV-based 3D IC.

Fig. 3(a), (b), (c), and (d) show the temperature variation of C-TSV-based 3D IC with TSV insertion density, TSV metal material, 3D IC layer, and silicon substrate thickness, respectively. It is shown that, firstly, as the C-TSV insertion density increases, the temperature of 3D IC except the first layer decreases obviously, especially when the C-TSV insertion density is low. For the first layer of a ten-layer 3D IC, the temperature increases as the C-TSV insertion density increases. The reason is that, the first layer is the heat diffusion path of other layers. As the heat diffuses faster, the more the heat is gathered in the first layer and the higher the temperature. Secondly, although it induces thermal stress during the
fabrication process [4], Cu is the best choice from the point of thermal management, due to the larger thermal conductivity than Al and W. Thirdly, the temperature of each layer of C-TSV-based 3D IC decreases almost linearly as the 3D IC layer or the silicon substrate thickness decreases. Finally, the layers near heat sink possess lower temperature than those near package, since the heat sink has a larger thermal conductivity than package.

On the basis of the analysis above, it can be concluded some design guidelines as follows. From the point of thermal management, 1) TSV should be inserted with high density especially near the temperature-sensitive modules, and dummy TSV should be inserted as much as possible for heat transfer; 2) Cu is a better material than Al and W; 3) the layer of 3D IC should be as few as possible; 4) the silicon substrate thickness should be as thin as possible; 5) the temperature-sensitive modules should be placed near TSV and heat sink.

5 Conclusion

In this letter, the analytical model of the temperature of C-TSV-based 3D IC is developed according to the Fourier’ law of heat transfer and energy conservation. And then, the analytical model is verified by employing ANSYS software, taking a ten-layer 3D IC for instance. It is shown that the results of analytical model consistent well with the FEM simulation data. Using the analytical model, the impacts of several variables on the temperature are investigated, based on which the design guidelines are given for the thermal management of C-TSV-based 3D IC.

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