High Performance and Scalable AWG for Superconducting Quantum Computer

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Abstract—Superconducting quantum computer is manufactured based on semiconductor process which makes qubits integration possible. At the same time, this kind of qubit exhibits high performance fidelity, de-coherence time, scalability and requires a programmable arbitrary waveform generator (AWG). This paper presents implementation of an AWG which composed of two gigabit samples per second (GSPS) sampling rate, 16 bit vertical resolution digital to analog converters (DACs). The AWG integrated with separate microwave devices onto a metal plate for the scale-up consideration. A special waveform sequence output controller is designed to realize seamless waveform switching and arbitrary waveform generator. The jitter in multiple AWG channels is around 10ps, Integral nonlinearity (INL) as well as differential nonlinearity (DNL) is about 2 LSB, and the qubit performance of the de-coherence time ($T_2^*$) achieved 33% promotion over that of a commercial 1 GSPS, 14 bit AWG.

I. INTRODUCTION

Superconducting qubit represents one of the most possible quantum computing schemes, which exhibits excellent performance in fidelity, de-coherence time and integration. Qubit controlling and reading can be achieved by commercial 1 GSPS DAC and ADC by use of IQ mixer in microwave modulation for up/down conversion [1], [2].

As shown in Fig. 1, superconducting quantum computing control system is composed of multiple independent parts, including switching network, clock & synchronization, qubit control, qubit read, bias and host. Each control unit is formed by AWGs, filters, differential amplifiers, power splitter and high precision DC sources. These parts can be used flexibly in accordance with the needs of system control requirement. Readout modules include a data acquisition (DAQ) and other parts that included in control unit. The clock and trigger system consists of a phase locked loop (PLL) and multiple signal fan-out units that supports the function of fanning out one input to multiple outputs, providing the clock and trigger signals that required for system synchronization.

To perform a qubit measurement, the control module prepares the qubits to a known state, and then, the readout module reads out the information of the qubits in a nondestructive measurement mode. Next, according to the qubit’s state information, the control module carries out the feedback control on AWGs’ output.

In general, a quantum chip is manufactured with each qubit exhibits different characteristic frequencies. As a result, one may concurrently read multiple qubits by frequency superposition in one read out module. Typically, ratio between the channel number of qubit control and qubit readout is around 4 to 10. This means the proportion between the channel number of AWG and DAQ is about 10 to 1. Hence, high-speed, high-precision AWG and its synchronization control represent the demand and challenges in such a system. The required synchronization accuracy between the channels of superconducting qubits is in the order of picoseconds.

The design of superconducting quantum bit chip is constantly exploring, and its new control requirements are springing up. For example, rapid calibration of modulation waveform, realization of specific rapid demodulation algorithm, and rapid feedback control required by the fault-tolerant quantum computing etc. Such a control device represents a highly customized system.

Over the past few years, several groups, e.g. in UCSB, IBM, ETH Zurich, Yale and BBN technologies, have implemented superconducting quantum computing control platforms [3], [4], [5]. Moreover, control systems have been realized in ultralow temperature environments [6], [7]. However, commer-
cially available devices cannot satisfy all the requirements, especially for programmable and compact demands. Therefore, to realize a large scale quantum computer, it is desirable to develop a high performance programmable, compact and extensible arbitrary waveform generator (AWG). This paper presents an AWG framework and waveform output sequence controller with extensible consideration. To validate the self-made AWG, we compare the qubit de-coherence time $T_2^*$ measurement results of our AWG with those of the commercial 1 GSPS 14 bit AWG.

II. AWG IMPLEMENTATION

A. HARDWARE

The AWG unit is composed by a Xilinx Field-Programmable Gate Array (FPGA) and two high performance Digital-to-Analog Converter (DAC) chips. Such an AWG is capable of providing four arbitrary waveform output channels, each of which operating at 2 GSPS and provide outputs with 16 bit resolution. We use the JESD204B protocol to achieve transmission of the high speed digital data rate of about 160 Gbps. Bipolar signals are achieved by passing the outputs through low pass filters and differential amplifiers. As shown in Fig. 3, a reliable communication is ensured by the information exchange via a gigabit Ethernet running on TCP/IP protocol. An external input clock that enables multiboards to operate under a synchronous source is fanned out and distributed equally to the FPGA and DACs. Another external input trigger which is synchronized to the same clock source can provide accurate output control. An extensible AWG array may be easily achieved by integration of multiple AWGs with a dedicated synchronize control module.

To reduce the size of the system, we integrate the AWG with individual IQ mixers and power splitters onto one metal plate, and constraint the height to 1U of the standard server rack. As shown in Fig. 3, two channels are used from the same chip as I/Q signals and are wired to the IQ mixers corresponding inputs. A common microwave source is connected to the power splitter and four outputs are separately fanned out to 4 IQ mixers LO input. Every compensative channel exiting from the differential amplifier will be used for monitoring or fast bias controlling.

B. FPGA IMPLEMENTATION

Figure 2 shows the block diagram of the signal flow in the FPGA. A Xilinx MicroBlaze processor generated by the Vivado software is embedded in the FPGA and communicates with all peripherals through the Advanced eXtensible Interface (AXI) bus. The software running on the processor implements a reliable communication with the host computer through lightweight TCP/IP stack. It also configures the operating parameters through the SPI/GPIO IPs on the AXI bus to the peripheral chips and function modules. Meanwhile, the working state of the AWG is periodically sent to local area network (LAN) through UDP broadcast packets, so that the system states may be monitored by any host in the same network.
LAN. The key waveform output control data is also transmitted through the network and sent to the waveform output control module.

The waveform output control module operates under the 250MHz clock which coming from the external clock interface. The same clock input makes multiple AWG modules operating in one clock source. The module interface with the DAC chip is completed by the JESD204B IP core which is operating in 10Gbps rate. The JESD204B protocol supports deterministic delay control, and realizes computable time delay of the waveform data from the JESD204B IP core input to the DAC output.

### C. AWG CONTROL

We implement a waveform output sequence controller for each channel. The controller is composed of three parts, i.e., a waveform data memory (WDM), a sequence data memory (SDM) and a finite state machine (FSM) for reading and controlling. As shown in Fig. 4 the memory data may be set by the host-computer and provides direct arbitrary waveform output. According to the flag bits of the sequence data, the FSM reads the sequence data from the WDM and determines the output mode of the waveform data. Output control mode includes the start address, length, trigger source, counter value, etc. In general, the programmable arbitrary waveform generate function is achieved by the FSM together with the WDM and SDM.

When running an arbitrary waveform output, at the beginning, the resources are ready for the first sequence data to execute. When a sequence data is running, the FSM prefetching the next sequence data to determine and prepare the resources required for its running. Hence, the resources are ready for every sequence data to be executed, and we may seamlessly switch to the next instruction without delay and splicing multiple waveform data. However, there is a constraint, where the output length of each waveform area cannot be less than 4. The purpose of doing this is to ensure that the prefetching action is accomplished in sufficient time to prepare the resources.

### III. TESTING

#### A. INL DNL

The AWG possesses 16 bit vertical resolution, that is, 65536 codes. The INL/DNL test requires traversing all the codes. We set a digital code and use a high-precision multimeter to measure the output voltage. Then, we continuously increase the digital code until all the codes are traversed. The test takes about 0.1 seconds for one code and about two hours to go through all the codes of a single channel. The high precision multimeter supports an external trigger and possesses 50k sample storage. We considered AWG with 65535 steps with the duration of 1ms for each step, which is synchronized to a trigger signal. The trigger signal is connected to the external trigger input of the multimeter. To collect the measured data, the host computer controls the AWG and the multimeter, and carries out the INL and DNL analysis. By improving the testing scheme, the test time of a single code value is reduced to 1ms, and the whole test time is reduced to 1 minute. The results of the test showing that the AWG DNL and INL are within 2LSB.

#### B. Phase noise

![Phase noise graph](image-url)
Fig. 5 shows the output phase noise of one AWG channel at seven distinct frequencies, i.e., 10, 20, 40, 50, 100, 200 and 250MHz. The noise floor larger than 10MHz frequency offset tends to be consistent. Increasing the signal frequency yields movement of the phase noise curve. In particular, the phase noise curve moves 6dB when the frequency is doubled, which is consistent with the theory.

C. Spurious free dynamic range (SFDR)

In the SFDR measurement, the harmonic noise represents the main spurious noise source. Consider measurement of the harmonic noise, especially when the measurement signal is a monosyllabic sine wave signal. If the RF attenuation setting of the spectrum meter is not reasonable, considerable difference between the tested harmonic noise and the actual harmonic noise will be observed. We consider the lowest output as the gain of the AWG, and set the frequency spectrum instrument input attenuation to 0dB. As shown in Fig. 6, the SFDR curve is achieved at 25 frequency points, i.e., from 10MHz to 250MHz with 10MHz step size. The results are consistent with the chips datasheet.

D. SYNCHRONIZATION

Fig. 7 shows the jitters of 40 arbitrary waveform output channels on 10 AWGs. The minimum and maximum standard deviations are 9.22ps and 10.89ps, respectively, with the mean value of 9.9ps. The skew between the channels is 100ps. The large skew between the channels is due to the fact that different signal line delay amount the clock signals input to the AWGs, and the different signal line delay from the AWG output to the oscilloscope input. The skew is deterministic and may be adjusted by cable length.

E. QUBIT TEST

Fig. 8. T2* measurement results for commercial AWG.

The implemented AWG is tested by a $T_{\frac{1}{2}}$ voltmeter and a 1 GHz bandwidth oscillator. It is demonstrated that the AWG exhibits 14 effective bits, and 10ps jitter among different channels. We test the AWGs performance further by measuring the qubit’s de-coherence time (T2*) which representing an
important parameter for qubits \cite{8}, \cite{9}. Fig.8 and Fig.9 compare the results driven by commercial 1 GSPS, 14 bit AWG. As shown in the figure, T2* of 10us and 15us is achieved separately driven by commercial AWG and our AWG, which is about 33% of the performance promotion.

IV. CONCLUSION

We introduced a scalable and highly integrated AWG array for the superconducting quantum computing control system. The AWG consists of two DACs, one FPGA and a gigabit Ethernet transceiver. An array has been used for the superconducting quantum computing control system. We also investigated the performance of the proposed AWG in detail and compared the qubit T2* test results to that of commercial AWG.

REFERENCES

[1] Y. Chen, D. Sank, P. O’Malley, T. White, R. Barends, B. Chiaro, J. Kelly, E. Lucero, M. Mariantoni, A. Megrant et al., “Multiplexed dispersive readout of superconducting phase qubits,” Applied Physics Letters, vol. 101, no. 18, p. 182601, 2012.
[2] N. Ofek, A. Petrenko, R. Heeres, P. Reinhold, Z. Leghtas, B. Vlastakis, Y. Liu, L. Frunzo, S. Girvin, L. Jiang et al., “Extending the lifetime of a quantum bit with error correction in superconducting circuits,” Nature, vol. 536, no. 7617, p. 441, 2016.
[3] T. Kaufmann, T. J. Keller, J. M. Franck, R. P. Barnes, S. J. Glaser, J. M. Martinis, and S. Han, “Dac-board based x-band epr spectrometer with arbitrary waveform control,” Journal of Magnetic Resonance, vol. 235, pp. 95–108, 2013.
[4] D. Castelvecchi, “Ibm’s quantum cloud computer goes commercial,” Nature, vol. 543, no. 7644, p. 159, 2017.
[5] C. A. Ryan, B. R. Johnson, D. Riste, B. Donovan, and T. A. Ohki, “Hardware for dynamic quantum computing,” Review of Scientific Instruments, vol. 88, no. 10, p. 104703, 2017.
[6] H. Homulle, S. Visser, and E. Charbon, “A cryogenic 1 gsa/s, soft-core fpga adc for quantum computing applications,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 11, pp. 1854–1865, 2016.
[7] H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiano, and E. Charbon, “A reconfigurable cryogenic platform for the classical control of quantum processors,” Review of Scientific Instruments, vol. 88, no. 4, p. 045103, 2017.
[8] R. R. C. Bialczak, Development of The Fundamental Components of A Superconducting Qubit Quantum Computer. University of California, Santa Barbara, 2011.
[9] C. Song, K. Xu, W. Liu, C.-p. Yang, S.-B. Zheng, H. Deng, Q. Xie, K. Huang, Q. Guo, L. Zhang et al., “10-qubit entanglement and parallel logic operations with a superconducting circuit,” Physical review letters, vol. 119, no. 18, p. 180511, 2017.