Circuit Walks in Integral Polyhedra

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Abstract. Circuits play a fundamental role in the theory of linear programming due to their intimate connection to algorithms of combinatorial optimization and the efficiency of the Simplex method. We are interested in better understanding the properties of circuit walks in integral polyhedra. In this paper, we introduce a hierarchy for integral polyhedra based on different types of behavior exhibited by their circuit walks. Many problems in combinatorial optimization fall into the most interesting categories of this hierarchy – steps of circuit walks in the associated polyhedra only stop at integer points, at vertices, or follow actual edges. We classify several classical families of integral polyhedra within the hierarchy, including 0/1-polytopes, polyhedra defined by totally unimodular matrices, and more specifically matroid polytopes, transportation polytopes, and partition polytopes. Finally, we prove several equivalent characterizations of the non-degenerate polytopes that appear in the bottom level of the hierarchy where all circuit walks are edge walks, showing that such polytopes constitute a generalization of the $n$-parallelotope which we call the $(n,d)$-parallelotope.

Keywords: edge walks, circuit walks, diameter, linear programming, integer programming, total unimodularity

MSC: 52B05, 90C05, 90C08, 90C10

1 Introduction

The search for a polynomial pivot rule for the Simplex method is one of the fundamental open questions in linear programming. It motivates the studies of the combinatorial and circuit diameters of polyhedra. The combinatorial diameter of a polyhedron is the maximum number of edges necessary to connect any pair of vertices by a walk. It is a lower bound on the best-case performance of the Simplex method, no matter which pivot rule is applied. In particular, if one can find an $n$-dimensional polyhedron with $f$ facets with a diameter super-polynomial in $f$ and $n$, then the existence of a polynomial pivot rule for the Simplex algorithm would be disproved. While this is a classical field of study, there remain many open questions.

One of the attempts to gain a better understanding of the behavior of edge walks in polyhedra is the study of circuit walks. Circuit walks, and the associated circuit diameter, generalize the concept of walking along the edges of a polyhedron to walking along its circuits, taking steps of maximal length. We introduce some notation [7,8]:

Given a polyhedron $P = \{ x \in \mathbb{R}^n : Ax = b, Bx \leq d \}$, the set of circuits of $P$, denoted $\mathcal{C}(A,B)$, consists of those $g \in \ker(A) \setminus \{ 0 \}$ normalized to coprime integer components for which $Bg$ is support-minimal over the set $\{ Bx : x \in \ker(A) \setminus \{ 0 \} \}$. It can be shown that
this set of circuits consists of all potential edge directions of $P$ as the right-hand side vectors $b$ and $d$ vary [16]. The circuits of a polyhedron also appear as elementary vectors in the literature [24].

As a generalization of the edge directions of the polyhedron, $C(A,B)$ serves as an optimality certificate for the linear program $LP = \min \{ c^T x : x \in P \}$ [16]. That is, if $v$ is a vertex of $P$ that is not an optimal solution of $LP$, there exists a circuit $g \in C(A,B)$ such that $c^T (v + \alpha g) < c^T v$ for some $\alpha > 0$ where $v + \alpha g \in P$. Hence, if $v^*$ is an optimal vertex solution of $LP$, there exists a circuit walk from $v$ to $v^*$ in $P$ as defined below.

**Definition 1.** Let $P = \{ x \in \mathbb{R}^n : Ax = b, Bx \leq d \}$ be a polyhedron. For two vertices $v^{(1)}, v^{(2)}$ of $P$, we call a sequence $v^{(1)} = y^{(0)}, \ldots, y^{(k)} = v^{(2)}$ a circuit walk of length $k$ if for all $i = 0, \ldots, k - 1$ we have:

1. $y^{(i)} \in P$,
2. $y^{(i+1)} = y^{(i)} + \alpha_i g^{(i)}$ for some $g^{(i)} \in C(A,B)$ and $\alpha_i > 0$, and
3. $y^{(i)} + \alpha g^{(i)}$ is infeasible for all $\alpha > \alpha_i$.

If $y^{(i)}$ is a vertex of $P$ for all $i = 0, \ldots, k$, we call the circuit walk a vertex walk. If $y^{(i)}$ has integer components for all $i = 0, \ldots, k$, we call the circuit walk integral (and non-integral otherwise).

Informally, circuit walks follow circuit directions and take steps of maximal length. In particular, these steps may go through the interior of a polyhedron. They are defined to start and terminate at vertices. Note that edge walks are special circuit walks. Hence, by traveling from vertex to vertex along the edges of a polyhedron, the Simplex method finds an optimal solution to a linear program by performing a special circuit walk.

There are many other settings in mathematical programming where algorithms take steps along circuits, construct circuit walks, or use circuits as an optimality certificate [1,2,3,12,14]. For example, the computation of an improving circuit direction is a viable approach to deal with highly degenerate vertices which can cause inefficiencies in the Simplex method [15]. Furthermore, unlike the Simplex method where it is open whether there exists a polynomial pivot rule, an augmentation scheme along so-called greedy circuit directions is guaranteed to take only polynomially many steps [17]. The challenge here lies in finding a greedy circuit direction – it is open whether this can be done in polynomial time for a set of circuits of exponential size. Of course, the circuit diameter gives a lower bound for the number of iterations of any augmentation algorithm along circuit directions.

We are interested in the behavior of circuit walks in integral polyhedra: polyhedra whose vertices have only integer components. For many problems in combinatorial optimization, there is an intimate connection of combinatorial (e.g. graph-theoretic) solution algorithms and circuit walks in the corresponding integral polyhedra. Network flow problems are a prime example which can be solved efficiently [23] (like many problems in combinatorial optimization [27]): circuits of the underlying polyhedron correspond to cycles in the respective directed graph. Classical algorithms like the minimum mean cycle-cancelling algorithm for minimum-cost flow problems construct a so-called steepest-descent circuit walk in the polyhedron. They highlight a class of polyhedra for which the augmentation scheme of [12] is efficient. Our interest in better understanding the circuit walks for combinatorial optimization problems is also motivated by the rich interpretation of circuits in terms of the underlying highly structured problems. There are many examples in clustering, transportation, and networks [5,9,10,18].
In this paper, we introduce and study a hierarchy of integral polyhedra based on the behavior of their circuit walks. The focus of our studies is on the types of endpoints $y^{(i)}$ of circuit steps, in particular whether they are always integral or even vertices. We contrast our approach with the studies in [6], where different relaxations of Definition 1 (such as circuit walks that do not take steps of maximal length or that may even leave the polyhedron) were put in relation to each other. This previous work was used to exhibit a “breaking point” of the Circuit Diameter Conjecture [7]: is there always a circuit walk (subject to different restrictions) of at most $f-n$ steps from any vertex to any other vertex in an $n$-dimensional polyhedron with $f$ facets? The conjecture is false for edges walks – it is well known that the famous Hirsch conjecture is false in general [19,25]. However, it is true for so-called sign-compatible circuit walks and still open for the original notion of circuit walks in which we are interested [7]. See also [11,26].

Our main goal is to understand how circuit walks (with steps of maximal length) behave in integral polyhedra. See Figure 5 for a visualization of our hierarchy. First, it is important to note that the top category is quite general. It contains a representative of all families of polyhedra with rational input that differs only by uniform scaling. This follows from the fact that it is easy to scale any rational polyhedron to be integral by scaling all of its vertices with the least common denominator of all of their components. In doing so, the behavior of circuit walks is not changed and thus can be quite general.

However, the context of integral polyhedra gives us natural restrictions on the general case. The interesting categories describe integral polyhedra in which circuit walks are integral walks (always stop at integer points), are vertex walks (always stop at vertices), and edge walks. Polyhedra in the lower parts of the hierarchy are of significant advantage in that their circuits often allow for an intuitive interpretation in terms of the underlying problem. This helps in the design and understanding of algorithms. After a brief explanation of the different categories through low-dimensional examples, we discuss where classical families of integral polyhedra belong in this hierarchy. These include 0/1-polytopes, polyhedra defined by totally unimodular matrices, matroid polytopes, transportation polytopes, and different types of clustering polytopes.

In particular, we show that the steps of all circuit walks in polyhedra defined by totally unimodular matrices stop only at integral points. We do not find this surprising in light of the well-understood circuits of totally unimodular matrices – see in particular [22]. However, total unimodularity is not a necessary condition for this behavior. Furthermore, we exhibit that 0/1-polytopes can have quite general circuit walk behavior, but in combination with a representation via a totally unimodular matrix, 0/1-polytopes can only have circuit walks that are vertex walks.

Our strongest results are for the bottom category of the hierarchy, where all circuit walks are actual edge walks. This behavior allows us several characterizations of the non-degenerate polytopes belonging to this category. We show that such polytopes constitute a generalization of the highly symmetric $n$-parallelotope which we call the $(n, d)$-parallelotope. In these polyhedra, all faces of dimension two are either parallelograms or simplices. Nevertheless, despite the restrictiveness of this circuit walk behavior, it does appear in some polyhedra of combinatorial optimization.

Summing up, this paper includes:

- The introduction of a hierarchy for integral polyhedra based on the behaviors exhibited by their circuit walks. (Section 2.1.)
- A classification of several classical families of integral polyhedra within the hierarchy. These include 0/1-polytopes, polyhedra defined by totally unimodular matrices, and
more specifically matroid polytopes, transportation polytopes, and partition polytopes.
(Sections 2.2 and 2.3, as well as Section 3 and Section 4.2 for the proofs.)

- Three characterizations of the non-degenerate polytopes in the bottom level of the hierarchy,
  where all circuit walks are edge walks. Our final characterization describes a generalization of the $n$-parallelotope which we call the $(n,d)$-parallelotope. (Section 2.3, and Section 4.1 for the proofs.)

## 2 Main Results

We begin with the introduction and description of a hierarchy of integral polyhedra based on the behavior of their circuit walks in Section 2.1. In Section 2.2, we examine two cases of interest in combinatorial optimization in relation to this hierarchy: $0/1$-polytopes and integral polyhedra defined by totally unimodular matrices. In Section 2.3, we characterize the non-degenerate polytopes belonging to the most restrictive level of the hierarchy in which all circuit walks are walks along actual edges.

### 2.1 A Hierarchy of Integral Polyhedra

A circuit walk in an integral polyhedron $P$ begins and ends at vertices of $P$ by definition. In general, however, each intermediate step of the circuit walk need not be a vertex or even an integral point of $P$, as can be seen in many examples such as the following.

**Example 1.** Consider the polytope $P = \{ x \in \mathbb{R}^2 : Bx \leq d \}$ given by

$$
B = \begin{pmatrix}
-1 & 0 \\
-1 & 1 \\
0 & 1 \\
1 & 1 \\
1 & -1 \\
-1 & -1
\end{pmatrix}
\quad \text{and} \quad
d = \begin{pmatrix}
0 \\
1 \\
2 \\
4 \\
4 \\
0
\end{pmatrix}.
$$

The circuits of $P$ depend only on the constraint matrix $B$ and can be found to be:

$$
C_{\leq}(B) = \left\{ \pm \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \pm \begin{pmatrix} 0 \\ 1 \end{pmatrix}, \pm \begin{pmatrix} 1 \\ 1 \end{pmatrix}, \pm \begin{pmatrix} 1 \\ -1 \end{pmatrix} \right\}.
$$

Although $P$ is an integral polytope, the circuit walk $y^{(0)} = (1, 2), y^{(1)} = (2, -1), y^{(2)} = (2, -2)$ in $P$, depicted in Figure 1, is non-integral.

Non-integral circuit walks do not translate well to combinatorial algorithms, where it would be helpful to have integral solutions at each iteration. Thus, a particularly interesting class of integral polyhedra are those in which all circuit walks are guaranteed to be integral, as in the following example.
Example 2. Consider the polytope $P = \{x \in \mathbb{R}^2 : Bx \leq d\}$ given by

$$B = \begin{pmatrix} -1 & 0 \\ -1 & 1 \\ 0 & 1 \\ 1 & 1 \\ 1 & 0 \\ 1 & -1 \\ 0 & -1 \\ -1 & -1 \end{pmatrix} \quad \text{and} \quad d = \begin{pmatrix} 0 \\ 1 \\ 3 \\ 9 \\ 8 \\ 9 \\ 3 \\ 1 \end{pmatrix}.$$

The circuits of $P$ are the same as those given in Example 1. However, it now holds that all circuit walks in $P$ are integral. In this small example, it is easy to verify this statement via complete enumeration. See Figure 2 for a circuit walk in $P$ with quite representative behavior.

Although the intermediate steps of a circuit walk in such a polyhedron are not necessarily vertices, each step is an integral point. An even more restrictive subclass are those polyhedra whose circuit walks are guaranteed to be vertex walks, such as the polytope in following example. Stopping at a vertex in each iteration of a circuit walk is even more advantageous than only stopping at integral points – for example, vertices in such polyhedra given in standard form have provably sparse support.
Example 3. Consider the polytope $P = \{ \mathbf{x} \in \mathbb{R}^2 : B\mathbf{x} \leq \mathbf{d} \}$ where $B$ is defined as in Example 2 but where $\mathbf{d} = (0, 1, 3, 7, 6, 7, 3, 1)^T$. The set of circuits remains the same, but now all circuit walks in $P$ are vertex walks. This is again easy to prove via complete enumeration. A circuit walk with representative behavior is given in Figure 3.

Fig. 3: A circuit walk in a polytope whose circuit walks are necessarily vertex walks.

Note that Examples 1 to 3 highlight the fundamental importance of the right-hand side for the behavior of circuits walks. We now add an additional, even more restrictive category. Circuit walks in the previous category of polyhedra move from vertex to vertex but are not restricted to only traveling along the edges of a polyhedron. However, in certain such polyhedra, such as those given in Example 4, it indeed holds that all circuit walks are necessarily edge walks. In this case, any circuit-based augmentation scheme is readily interpreted as the Simplex method with a certain pivot rule.

Example 4. In both $n$-simplices and $n$-parallelotopes, such as those pictured in Figure 4, all circuit directions appear as edge directions. Furthermore, at any vertex, the only feasible circuit step directions are those edge directions incident to the vertex. Hence, all circuit walks in these polytopes are edge walks.

Fig. 4: In a tetrahedron (a 3-simplex) and a parallelohedron (a 3-parallelotope), the only circuit walks are edge walks.

Summing up, these different types of circuit walk behaviors define a hierarchy of integral polyhedra consisting of four successively more restrictive levels: general integral polyhedra, integral polyhedra whose circuit walks are integral, integral polyhedra whose circuit walks are vertex walks, and integral polyhedra whose circuit walks are edge walks. A depiction of
This hierarchy is given in Figure 5. As demonstrated in Examples 1 to 4, the levels in the hierarchy are indeed distinct.

![Figure 5: A hierarchy of integral polyhedra based on their circuit walk behavior.](image)

We can connect this hierarchy to one of the biggest challenges in the study of circuit diameters: unlike edge walks, circuit walks are not necessarily reversible [7]. For instance, reversing the circuit walks depicted in Figures 1 and 2 does not yield valid circuit walks. We note that a classification of polyhedra where all circuit walks are reversible aligns well with the hierarchy in Figure 5. More precisely, all circuit walks are reversible in a polyhedron if and only if all circuit walks are vertex walks; see Figure 6.

To prove this, note that all circuit walks that are vertex walks are clearly reversible. On the other hand, if a polyhedron \( P \) contains any circuit walk \( v^{(1)}, \ldots, v^{(2)} \) that is not a vertex walk, then some step of the circuit walks ends at a point \( y^{(i)} \) in the interior of a face \( F \) of \( P \). Since circuits form an optimality certificate, there exists a circuit walk from \( y^{(i)} \) to any vertex \( u \) in \( F \). Hence, we can construct a circuit walk from \( v^{(1)} \) to \( u \) via \( y^{(i)} \) in \( P \) that is not reversible.

Next, we show where some important polyhedra that arise in combinatorial optimization belong in this hierarchy.

### 2.2 0/1-polytopes and Totally Unimodular Matrices

0/1-polytopes are widely studied due to their ability to represent many classical combinatorial optimization problems involving binary decisions. Their combinatorial diameter satisfies the famous Hirsch Conjecture [21], which implies the validity of the Circuit Diameter Conjecture for them. Here, we investigate the behavior of circuit walks in these polytopes in view of our hierarchy.

We note that in general, circuit walks in 0/1-polytopes need not be integral. Consider the example given in Figure 7. The edge direction \((1, 1, 0)\) corresponds to a circuit direction. However, when taking a step in this direction from the vertex \((0, 0, 0)\) we reach the non-integral midpoint \((\frac{1}{2}, \frac{1}{2}, 0)\) of an edge.
Fig. 6: Our hierarchy based on circuit walk behavior aligns with the hierarchy distinguishing polyhedra whose circuit walks are necessarily reversible.

Fig. 7: A 3-dimensional 0/1-polytope with non-integral circuit walks.

While the above is a specific low-dimensional example, there are important classes of 0/1-polytopes for which the same holds. For example, matroid polytopes form a class of 0/1-polytopes in which circuit walks need not be integral. Given a matroid $M$ with ground set $E$ and rank function $f$, the matroid polytope $P(f)$ associated with $M$ is defined to be:

$$P(f) = \left\{ x \in \mathbb{R}^E : x \geq 0, \sum_{e \in S} x_e \leq f(S) \forall S \subseteq E \right\}.$$

The vertices of this polytope consist of all $x \in \{0,1\}^E$ that are incidence vectors of the independent sets of $M$, and its edges are characterized in [28]. In Section 3.1, we describe the circuits of $P(f)$ and show that many of its circuit walks are non-integral.

Another important class of integral polyhedra are those defined by totally unimodular matrices. In particular, these polyhedra are extensively studied due to their arising in transportation, assignment, and network flow problems. The combinatorial (and circuit) diameter of these polyhedra is polynomially bounded [4,13] and linear programming over them is efficient [27].

We show that all circuit walks in integral polyhedra defined by totally unimodular matrices (and with integral right-hand sides) are in fact integral. In a sense, this implies that
any algorithm that traverses such a polyhedron via circuit walks has a combinatorial interpretation.

**Theorem 1.** Let \( P = \{ x \in \mathbb{R}^n : Ax = b, Bx \leq d \} \) be an integral polyhedron whose constraint matrix \( (A_B) \) is totally unimodular. Then all circuit walks in \( P \) are integral.

We formally prove Theorem 1 in Section 3.2. However, we are not surprised by this property due to the well-understood edge directions of polyhedra with totally unimodular matrices. In particular, we see an alternative way to prove the claim from a careful extension of Proposition 3.3 in [22]. The merit of our proof is that it is short, self-contained, and does not require more than basic linear algebra.

Note however that total unimodularity is not a necessary condition for all circuit walks to be integral. This can be seen in Examples 2 and 3. Additionally, total unimodularity is not a sufficient condition for circuit walks to be vertex walks. For instance, the transportation polytope, whose circuits are characterized in [10], can have many non-vertex circuit walks. We discuss the behavior of circuit walks in transportation polytopes in Section 3.3.

However, by combining Theorem 1 with the fact that all integral points in a 0/1-polytope are vertices, we immediately see that all circuit walks in 0/1-polytopes defined by totally unimodular matrices are vertex walks.

**Corollary 1.** Let \( P = \{ x \in \mathbb{R}^n : Ax = b, Bx \leq d \} \) be an integral polyhedron whose constraint matrix \( (A_B) \) is totally unimodular. If \( P \) is a 0/1-polytope, then all circuit walks in \( P \) are vertex walks.

Hence, in a 0/1-polytope defined by a totally unimodular matrix, any algorithm corresponding to a circuit walk necessarily travels from vertex to vertex and is therefore reversible. However, these circuit walks need not be edge walks. We verify this fact by examining a class of polytopes that arise in clustering.

The bounded-size partition polytope \( PP(\kappa^\pm) \) is associated with the partitioning of a set of \( n \) items into \( k \) clusters \( C_1, ..., C_k \), where each cluster \( C_i \) has an upper bound \( \kappa_i^+ \) and a lower bound \( \kappa_i^- \) on the number of items it can hold. In Section 3.4, we characterize both the edges and circuits of this polytope. We use this to show that its circuit walks are vertex walks but that many of them are not edge walks.

A visualization of the classification of the polyhedra mentioned in this section in terms of the hierarchy of Section 2.1 is given in Figure 8. For the sake of completeness, we have included the results of the following section in the figure as well.

### 2.3 Polyhedra whose Circuit Walks are Edge Walks

The most restrictive level of our hierarchy consists of those integral polyhedra whose only circuit walks are edge walks. Any circuit-based augmentation scheme in such a polyhedron must necessarily be some variation of the Simplex method. In this section, we characterize all non-degenerate polytopes whose only circuit walks are edge walks. We find this characterization to be quite restrictive, and it has strong implications on the degenerate polytopes in the category as well. But surprisingly, non-trivial examples of (degenerate) polyhedra from this restrictive category do appear in practice. We exhibit an example at the end of this section.

An \( n \)-dimensional polyhedron is said to be *degenerate* if it contains a vertex belonging to more than \( n \) facets. On the other hand, in a *non-degenerate*, or *simple*, polyhedron, each vertex belongs to exactly \( n \) facets. Non-degenerate polyhedra are of interest in the study of
combinatorial diameters as it suffices to only consider this class of polyhedra when bounding the combinatorial diameter of an \( n \)-dimensional polyhedron with \( f \) facets [19]. While much harder to prove, the same holds for circuit diameters [11].

In Example 4, tetrahedra and parallelohedra are given as two examples of non-degenerate polyhedra whose only circuit walks are edge walks. In this section, we show that the structure of non-degenerate polyhedra offers several useful characterizations of polytopes whose only circuit walks are edge walks. As it turns out, the only non-degenerate polytopes exhibiting this behavior are intimately related to these examples.

Our first important tool is the notion of elementary cones of polyhedra. Consider a full-dimensional polyhedron \( P = \{ x \in \mathbb{R}^n : Bx \leq d \} \) and the hyperplane arrangement in \( \mathbb{R}^n \) consisting of the hyperplanes \( B_i x = 0 \) for each row \( B_i \) of \( B \). These hyperplanes intersect at the origin and partition \( \mathbb{R}^n \) into \( n \)-dimensional polyhedral cones whose interiors do not intersect. We call this arrangement of hyperplanes the elementary arrangement of \( P \), and we call the inclusion-minimal \( n \)-dimensional cones in the arrangement the elementary cones of \( P \).

It is not hard to see that elementary cones are generated by circuits (Lemma 5). We use this fact to give a first characterization of non-degenerate polytopes whose circuit walks are edge walks: the inner cones of all vertices must be elementary cones. Recall that given a vertex \( v \) of a polyhedron \( P \), the inner cone \( I(v) \) of \( v \) is the cone consisting of all feasible directions at \( v \) with respect to \( P \).

**Theorem 2.** Let \( P = \{ x \in \mathbb{R}^n : Bx \leq d \} \) be a full-dimensional, non-degenerate polytope. All circuit walks in \( P \) are edge walks if and only if for each vertex \( v \in P \), the inner cone \( I(v) \) is an elementary cone of \( P \).

Next, we prove that all polytopes satisfying Theorem 2 must be highly symmetric – the inner cones of vertices that do not share a facet are opposites of each other. By imposing that this property transfers to vertices belonging to a common face (and stating it with respect to the affine hull of the face), we obtain a second characterization. Specifically, given a pair of vertices \( u, v \) of a polyhedron \( P \), let \( P^{uv} \) denote the inclusion-minimal face of \( P \) containing \( u \) and \( v \) and let \( I^{uv}(u), I^{uv}(v) \) denote the inner cones of \( u, v \) with respect to \( P^{uv} \).
Then the following theorem gives our second characterization of non-degenerate polytopes whose circuit walks are edge walks.

**Theorem 3.** Let $P$ be a non-degenerate polytope given by a minimal representation. All circuit walks in $P$ are edge walks if and only if $I_{uv}(u) = -I_{uv}(v)$ for all pairs of vertices $u, v$ in $P$.

Naturally, the symmetric inner cone condition stated in Theorem 3 is only satisfied by quite symmetric polyhedra. One such example is the parallelotope of dimension $n$, also called the $n$-parallelotope: a vertex-transitive polytope with $n$ pairs of parallel opposite facets and $2^n$ vertices. Equivalently, an $n$-parallelotope is a zonotope generated by a set of $n$ linearly independent vectors in general position, which correspond to its edge directions. We show that the only other polytopes satisfying the symmetric inner cone condition constitute a generalization of the $n$-parallelotope which we call the $(n, d)$-parallelotope.

**Definition 2.** Given $d \in \{1, ..., n\}$, an $(n, d)$-parallelotope $P$ is an $n$-dimensional polytope that satisfies $I_{uv}(u) = -I_{uv}(v)$ for all pairs of vertices $u, v$ in $P$; furthermore, each pair of vertices shares at least $n - d$ facets and each individual vertex appears in some $d$-parallelotope face.

Thus, an $(n, n)$-parallelotope is simply an $n$-parallelotope. On the other hand, an $(n, 1)$-parallelotope is an $n$-simplex. Other instances of $(n, d)$-parallelotopes, such as the $(3, 2)$-parallelotope shown in Figure 9, must be highly symmetric hybrids of the simplex and the parallelotope. We show that in any $(n, d)$-parallelotope, all circuit walks must be edge walks, which yields our final characterization.

**Theorem 4.** Let $P$ be an $n$-dimensional, non-degenerate polytope given by a minimal representation. All circuit walks in $P$ are edge walks if and only if $P$ is an $(n, d)$-parallelotope.

The proof of Theorems 3 and 4, given in Section 4.1, provides further insight into the structure of $(n, d)$-parallelotopes.

![Fig. 9: The (3, 2)-parallelotope: a 3-dimensional, non-degenerate polytope whose only circuit walks are edge walks. It is neither a simplex nor a parallelotope, but all of its facets are.](image-url)
stopped by some facet of the polyhedron. Thus, if an unbounded polyhedron $P$ has recession cone $R$, no circuit walk in $P$ uses a direction belonging to $R$. In other words, a circuit walk in $P$ is completely contained in the convex hull of the vertices of the polyhedron.

On the other hand, the assumption of non-degeneracy is an actual restriction. Some of our results readily transfer to non-degenerate polytopes – for example, all 2-dimensional faces of (degenerate) polytopes in this category of our hierarchy must be triangles or parallelograms. Others do not readily transfer – for example, since inner cones of an $n$-dimensional (degenerate) polytope need not be generated by exactly $n$ edge directions, it is more difficult to prove whether opposite inner cones need mirror each other. An extension of our characterization for non-degenerate polytopes to all polytopes is a natural next step for the presented line of research.

We conclude the discussion with a practical example of a highly degenerate polytope whose circuit walks are edge walks. The fixed-size partition polytope $PP(k)$ is a polytope associated with the partitioning of a set of $n$ items into $k$ clusters $C_1, \ldots, C_k$, where the size of each cluster $C_i$ is fixed at $\kappa_i$. The edges of this polytope are characterized in [5], and in Section 4, we show that all circuit walks in this polytope are in fact edge walks.

3 Proofs for Section 2.2

3.1 Matroid Polytopes

Recall that for a matroid $M$ with ground set $E$ and rank function $f$, the matroid polytope $P(f)$ associated with $M$ is

$$P(f) = \left\{ x \in \mathbb{R}^E : x \geq 0, \sum_{e \in S} x_e \leq f(S) \forall S \subseteq E \right\}.$$

The extreme points of this polytope consist of all $x \in \{0,1\}^E$ that are incidence vectors of the independent sets of $M$. Two extreme points are adjacent in $P(f)$ if and only if they differ in exactly one component or they differ in exactly two components that satisfy a certain quite technical ordering relation [28].

Let us examine the circuits of $P(f)$. The matrix $B$ in the system of inequalities $Bx \leq d$ defining $P(f)$ consists of the identity matrix and a submatrix corresponding to the constraints of the form $\sum_{e \in S} x_e \leq f(S)$. A vector $g \in \mathbb{R}^E \setminus \{0\}$ with coprime integer components is a circuit of $P(f)$ when $Bg$ is support-minimal over the set $\{Bx : x \in \mathbb{R}^E \setminus \{0\}\}$. Note that each positive and negative unit vector is a circuit of $P(f)$. Any circuit walk that exclusively uses these directions for its circuit steps is an edge walk in $P(f)$ and corresponds to individually adding or removing elements from an independent set of $P$. Additionally, the difference of any two unit vectors is a circuit of $P(f)$. Combinatorially, these circuits correspond to swapping out some element of an independent set of $M$ for another. A circuit walk using only these directions may traverse some edges of $P(f)$ if the adjacency conditions of [28] are satisfied, but it is possible that the walk is only a vertex walk and not an edge walk.

Furthermore, it is possible for a circuit walk in $P(f)$ to be non-integral. Since $P(f)$ is a 0/1-polytope, only circuits from $\{0,1,-1\}^E$ may be used in an integral circuit walk. However, due to the large number of facets defining $P(f)$, the polytope contains many circuits outside this domain. For instance, if $\{1,2,3,4\} \subseteq E$, consider the vector $g \in \mathbb{R}^E$
where:

\[
g_e = \begin{cases} 
2 & \text{if } e = 1 \\
-1 & \text{if } e \in \{2, 3, 4\} \\
0 & \text{otherwise.}
\end{cases}
\]

To see that \( g \) is a circuit, note that for any \( S \subset E \) containing \( \{1\} \) and some 2-set of \( \{2, 3, 4\} \), we have \( \sum_{e \in S} g_e = 0 \). However, for any nonzero \( y \in \mathbb{R}^E \) whose support is strictly contained in the support of \( g \), it can be shown that \( \sum_{e \in S} y_e \neq 0 \) for some such subset \( S \). Therefore, \( g \) is indeed a circuit of \( P(f) \). Many other similar circuits of \( P(f) \) can be constructed, and these can be used to perform non-integral circuit walks in \( P(f) \).

### 3.2 Proof of Theorem 1

The fact that circuit walks are integral in integral polyhedra defined by totally unimodular matrices is not surprising since such a polyhedron has integral vertices for any integral right-hand side. We present a complete proof for a general integral polyhedron of the form \( P = \{x \in \mathbb{R}^n : Ax = b, Bx \leq d\} \). The following arguments require only basic linear algebra, but we note that this result can be obtained in various ways. As another example, we provide a short proof using an equivalent definition of totally unimodular matrices. We also refer the reader to the intimately related and well-presented results surrounding Proposition 3.3 in [22], which will require a bit more background on integer programming.

In the proof of Theorem 1, we assume that the matrix \((A)_{B}^n\) has full rank, else \( P \) would not be pointed. We also assume that the rows of \( A \) are linearly independent and that \( \text{rank}(A) + \text{rank}(B) = n \) by eliminating any redundant rows from \( A \) and \( B \). To begin, we provide a proof for an important bound on the size of the components of a circuit of \( P \).

**Lemma 1 ([22]).** Let \( P = \{x \in \mathbb{R}^n : Ax = b, Bx \leq d\} \) be a polyhedron defined by integral matrices and let \( g \in \mathcal{C}(A, B) \) be a circuit of \( P \). Then \( \max_i |g_i| \leq \Delta(M) \), where \( M = (A)_{B}^n \) and \( \Delta(M) \) is the maximum absolute value of a subdeterminant of \( M \).

**Proof.** Let \( B' \) be a maximal row submatrix of \( B \) such that \( B'g = 0 \). That is, the support of \( Bg \) corresponds to the rows of \( B \) not included in \( B' \). With \( r := \text{rank}(A) \), we have \( \text{rank}(B') \leq n - r - 1 \) since \( g \neq 0 \). Suppose for the purpose of contradiction that \( \text{rank}(B') < n - r - 1 \). Then we can add other rows of \( B \) to \( B' \) to form a matrix \( B'' \) of rank \( n - r - 1 \). The matrix \((A)_{B''}^n\) thus has rank \( n - 1 \) and its one-dimensional kernel is spanned by some \( x \in \mathbb{R}^n \setminus \{0\} \).

However, this implies that the support of \( Bx \) is strictly contained in the support of \( Bg \), contradicting the fact that \( g \) is a circuit.

Therefore, we have \( \text{rank}(B') = n - r - 1 \). Let \( M' \in \mathbb{R}^{(n-1)\times n} \) be a row submatrix of \( M \) consisting of \( A \) and \( n - r - 1 \) linearly independent rows from \( B' \). Note that \( g \in \text{ker}(M') \) and that \( \text{ker}(M') \) is one-dimensional. To complete the proof, it suffices to show that \( \text{ker}(M') \) can be generated by an integral vector whose entries have absolute values at most \( \Delta(M) \).

To find this generating vector, we consider the augmented system

\[
\begin{bmatrix}
M'' & M_n'
\end{bmatrix} = 0,
\]

where \( M'' \) contains the first \( n - 1 \) columns of \( M' \) and \( M_n' \) denotes the \( n \)th column of \( M' \). Assume without loss of generality that the columns of \( M'' \) are linearly independent, so that \( M'' \) is an invertible \((n - 1) \times (n - 1)\) matrix. We can row reduce the augmented system to obtain the form:

\[
\begin{bmatrix}
I_{n-1} & (M'')^{-1}M_n'
\end{bmatrix} = 0,
\]
where \((M'')^{-1}M'_n\) is the unique solution \(x^* \in \mathbb{R}^{n-1}\) to the system \(M''x = M'_n\).

By Cramer’s Rule, it holds for \(i = 1, \ldots, n - 1\) that \(x^*_i = \frac{\det(M_j)}{\det(M''_i)}\), where \(M_j\) denotes the matrix formed by replacing the \(i\)th column of \(M''\) with \(M'_n\). Since \(M\) is integral, it follows that each \(\det(M_j)\) is integral. Hence, scaling \(x^*\) by \(\det(M'')\), we obtain an integral vector whose entries have absolute value at most \(\Delta(M') \leq \Delta(M)\). It follows that \(\det(M'') \cdot (x^{*T}, -1)^T \in \mathbb{R}^n\) is a desired spanning vector of \(\ker(M')\). \(\square\)

As a direct corollary of this lemma, we see that if \((A_B)\) is totally unimodular, any circuit \(g \in C(A, B)\) satisfies \(g \in \{0, 1, -1\}^n\). We use this fact to prove the following lemma, and in turn, Theorem 1.

**Lemma 2.** Let \(P = \{x \in \mathbb{R}^n: Ax = b, Bx \leq d\}\) where \(M = (A_B)\) is totally unimodular, and let \(g \in C(A, B)\) be a circuit of \(P\). Then \(B^Tg \in \{0, 1, -1\}^m\), where \(m\) is the number of rows of \(B\).

**Proof.** Suppose for the purpose of contradiction that there is a row \(B_i\) of \(B\) such that \(B_i^Tg = k\) for some \(k \notin \{0, 1, -1\}\). As in the proof of Lemma 1, let \(M'\) be a row submatrix of \(M\) consisting of \(A\) and \(n - r - 1\) linearly independent rows from \(B\) so that \(M'g = 0\). Next, from the invertible \(n \times n\) matrix \(M''\) by appending the row \(B_i\) to \(M\).

Consider the vector \(y := M''g\), whose only nonzero entry is its last entry \(B_i^Tg = k\). We see that \(y\) is the unique solution to the system \(M''x = y\). Let \(g_j\) be any nonzero entry of \(g\). Then by Cramer’s Rule, we have \(g_j = \frac{\det(M_j)}{\det(M'')}\), where \(M_j\) denotes the matrix formed by replacing the \(j\)th column of \(M''\) with \(y\). Evaluating \(\det(M_j)\) by expanding down this column, we have \(|\det(M_j)| = |k|\det(M''_j)|\), where \(M''_j\) is some \((n - 1) \times (n - 1)\) submatrix of \(M''\). Since \(M\) (and also \(M''\) and \(M'''\)) is totally unimodular, this implies that \(|g_j| = |k|\), contradicting Lemma 1. \(\square\)

Theorem 1 now follows directly from these lemmas.

**Theorem 1** Let \(P = \{x \in \mathbb{R}^n: Ax = b, Bx \leq d\}\) be an integral polyhedron whose constraint matrix \((A_B)\) is totally unimodular. Then all circuit walks in \(P\) are integral.

**Proof 1 of Theorem 1.** Let \(x\) be any integral point in \(P\) and let \(g \in C(A, B)\) be a feasible circuit direction at \(x\). For any strict inequality \((Bx)_i < d_i\) at \(x\), we must have \((Bx)_i \leq d_i - 1\) since \(B\) and \(d\) are integral. Applying a step with step size \(\alpha = 1\) in the circuit direction \(g\), it follows by Lemma 2 that \((B(x + g))_i = (Bx)_i + (Bg)_i \leq (Bx)_i + 1 \leq d_i\). Continuing in this direction until an inequality becomes strict, we see that the stopping point \(x + \alpha g\) must be integral with integral step size \(\alpha\). \(\square\)

Alternatively, Theorem 1 can be proven in a less direct manner using the fact that any polyhedron defined by a totally unimodular matrix is integral for any integral right-hand side.

**Proof 2 of Theorem 1.** We may assume the right-hand side vectors \(b\) and \(d\) are integral, for otherwise either \(P\) would be empty or the entries of \(d\) could be rounded up without changing the polyhedron. Let \(z\) be any integral point in \(P\) and let \(g \in C(A, B)\) be a feasible circuit direction at \(z\). As in the proof of Lemma 1, consider the maximal row submatrix \(B'\) of \(B\) such that \(B'g = 0\). The polyhedron
\[
P' = \{x \in \mathbb{R}^n: Ax = b, B'x \leq d, B'x = B'z\}
\]
has dimension one since \( \text{rank}(\mathbf{A}) = n - 1 \). Furthermore, \( P' \) is integral since duplicating rows preserves total unimodularity and its right-hand side is integral. If \( P' \) is bounded, its two integral vertices must be \( \mathbf{z} \) and the point reached after taking a maximal circuit step from \( \mathbf{z} \) in the direction of \( \mathbf{g} \).

3.3 Transportation Polytopes

Given a set of \( m \) suppliers and \( n \) customers where \( \mathbf{u} \in \mathbb{Z}_+^m \) gives the supply of each supplier and \( \mathbf{v} \in \mathbb{Z}_+^n \) gives the demand of each customer, the corresponding transportation polytope \( P \) consists of all \( \mathbf{y} \in \mathbb{R}^{mn} \) that describe feasible commodity flow assignments from suppliers to customers:

\[
\sum_{j=1}^{n} y_{ij} = u_i, \quad i = 1, ..., m \\
\sum_{i=1}^{m} y_{ij} = v_j, \quad j = 1, ..., n \\
y_{ij} \geq 0, \quad i = 1, ..., m, \quad j = 1, ..., n.
\]

Given a feasible flow assignment \( \mathbf{y} \in P \), the support graph \( B(\mathbf{y}) \) of \( \mathbf{y} \) is the bipartite graph with partite sets corresponding to the suppliers and customers in which there exists an edge with weight \( y_{ij} \) between supplier \( i \) and customer \( j \) if and only if \( y_{ij} > 0 \). It can be shown that any \( \mathbf{y} \in P \) is a vertex of \( P \) if and only if its support graph \( B(\mathbf{y}) \) is acyclic. Furthermore, two vertices are adjacent in \( P \) if and only if the union of the corresponding support graphs contains exactly one cycle [20].

It follows that the circuits of \( P \) consist of all simple cyclical exchanges of flow among the suppliers and customers [10]. Specifically, \( \mathbf{g} \in \mathbb{R}^{mn} \) is a circuit of \( P \) if and only if the support of \( \mathbf{g} \) corresponds to a single cycle in \( K_{m,n} \) whose edges alternately correspond to entries 1 and \(-1\) of \( \mathbf{g} \). Hence, for any \( \mathbf{y} \in P \), applying a step in a feasible circuit direction from \( \mathbf{y} \) corresponds to reducing weight along every other edge of some cycle of \( K_{m,n} \) while simultaneously increasing weight along the remaining edges of the cycle. The step terminates once the weight of an edge in \( B(\mathbf{y}) \) is reduced to 0.

Since the constraint matrix of \( P \) is totally unimodular, we know by Theorem 1 that all circuit walks in \( P \) are integral. However, it need not hold that all circuit walks are vertex walks. Equivalently, if \( \mathbf{x} \) is a vertex of \( P \) and \( \mathbf{y} \) is reached by a maximal circuit step from \( \mathbf{x} \), then although \( B(\mathbf{x}) \) is acyclic, it need not hold that \( B(\mathbf{y}) \) is acyclic.

As an example, consider the transportation problem with suppliers \( s_1, s_2, s_3 \) and customers \( c_1, c_2, c_3 \), where \( \mathbf{u} = \mathbf{v} = (1, 2, 2)^T \). Then

\[
\mathbf{x} = (x_{11}, x_{12}, x_{13}, x_{21}, x_{22}, x_{23}, x_{31}, x_{32}, x_{33})^T = (0, 1, 0, 1, 0, 1, 0, 1, 1)^T
\]

is a vertex of \( P \) and \( \mathbf{g} = (1, -1, 0, -1, 1, 0, 0, 0, 0)^T \) is a circuit. However, after applying a step in the direction of \( \mathbf{g} \) from \( \mathbf{x} \) we reach a solution whose support graph is cyclic, and thus not a vertex. See Figure 10.

3.4 Bounded-size Partition Polytopes

Similar to the partition polytopes for prescribed-size clusterings introduced in [5], the bounded-size partition polytope \( PP(\kappa^{\pm}) \) is associated with the partitioning of a set \( X = \)
\{x_1, \ldots, x_n\} \) of items into clusters \(C_1, \ldots, C_k\), where each cluster \(C_i\) must satisfy \(\kappa^-_i \leq |C_i| \leq \kappa^+_i\) given \(\kappa^-_i, \kappa^+_i \in \mathbb{Z}_+\). For \(i = 1, \ldots, k\) and \(j = 1, \ldots, n\), let \(y_{ij}\) be a binary variable indicating whether or not item \(x_j\) is assigned to cluster \(C_i\). Then \(PP(\kappa^\pm)\) is the 0/1-polytope defined by the following system of constraints:

\[
\begin{align*}
\sum_{i=1}^{k} y_{ij} &= 1 \quad j = 1, \ldots, n \\
\sum_{j=1}^{n} y_{ij} &\geq \kappa^-_i \quad i = 1, \ldots, k \\
\sum_{j=1}^{n} y_{ij} &\leq \kappa^+_i \quad i = 1, \ldots, k \\
y_{ij} &\geq 0 \quad i = 1, \ldots, k, \ j = 1, \ldots, n.
\end{align*}
\]

We note that this polytope is an instance of the bounded-shape partition polytope described in \cite{ref10} if we let \(X\) be the standard basis of \(\mathbb{R}^n\).

As the constraint matrix defining the polytope is totally unimodular and the right-hand sides are integral, the vertices of \(PP(\kappa^\pm)\) indeed consist of those \(y \in \{0,1\}^{kn}\) corresponding to feasible clustering assignments. As in \cite{ref10} and \cite{ref12}, given two such assignments \(y^1, y^2\), define the clustering difference graph \(CDG(y^1, y^2)\) from \(y^1\) to \(y^2\) to be the directed graph with nodes \(c_1, \ldots, c_k\) where an edge \((c_i, c_j)\) with label \(x_i\) is included if and only if \(y^1_{i} = y^2_{j} = 1\) with \(i \neq j\). Thus, the edges of \(CDG(y^1, y^2)\) give all single-item transfers necessary in order to transform the clustering assignment of \(y^1\) into that of \(y^2\).

For two vertices \(y^1, y^2\) of \(PP(\kappa^\pm)\) to share an edge, \(CDG(y^1, y^2)\) must be either a directed path or a directed cycle \cite{ref12}. Here, we use clustering difference graphs to completely characterize both the edges and the circuits of \(PP(\kappa^\pm)\). To do so, given a pair of clustering assignments \(y^1, y^2\), let \(C^1 = (C_1^1, \ldots, C_k^1)\) be the clustering of \(X\) associated with \(y^1\) and let \(C^2 = (C_1^2, \ldots, C_k^2)\) be the clustering associated with \(y^2\). We say that a node \(c_i \in CDG(y^1, y^2)\) is free if \(\kappa^-_i < |C_i^1| < \kappa^+_i\). Hence \(C_i^1\) may receive or give away some item of \(X\) and its size constraints will still be satisfied. Similarly, we say that \(c_i\) is saturated if \(\kappa^-_i < |C_i^1| = \kappa^+_i\), that \(c_i\) is depleted if \(\kappa^-_i = |C_i^1| < \kappa^+_i\), and that \(c_i\) is fixed if \(\kappa^-_i = |C_i^1| = \kappa^+_i\). Finally, we say that a directed graph \(D\) is a valid \(CDG\) at \(y^1\) if there exists a vertex \(y^1 \in PP(\kappa^\pm)\) such that \(D = CDG(y^1, y^1)\). The following lemma characterizes the edges of \(PP(\kappa^\pm)\).
Lemma 3. Let \( y^1, y^2 \) be a pair of vertices in \( PP(\kappa^\pm) \). Then \( y^1 \) and \( y^2 \) share an edge in \( PP(\kappa^\pm) \) if and only if \( CDG(y^1, y^2) \) cannot be non-trivially decomposed into valid \( CDG \)'s at \( y^1 \). Equivalently, \( y^1 \) and \( y^2 \) share an edge if and only if \( CDG(y^1, y^2) \) is a single edge, a single directed path in which no interior vertices are free, or a single directed cycle in which at most one vertex is free.

Proof. For the forward direction, assume that \( y^1 \) and \( y^2 \) are joined by an edge in \( PP(\kappa^\pm) \) and suppose for the purpose of contradiction that \( CDG(y^1, y^2) \) can be decomposed into a collection of valid \( CDG \)'s at \( y^1 \): \( CDG(y^1, y^3), ..., CDG(y^1, y^\ell) \). Since \( y^1 \) and \( y^2 \) share an edge, there exists a vector \( f \in \mathbb{R}^{kn} \) such that \( f^T y^1 = f^T y^2 \) but that \( f^T v > f^T y^1 \) for any other vertex \( v \) of \( PP(\kappa^\pm) \). Specifically, it must hold that \( f^T y^i > f^T y^1 \) for \( i = 3, ..., \ell \).

However, note that the clustering of \( y^2 \) can be derived from that of \( y^1 \) by independent applications of the transfers given by each \( CDG(y^1, y^i) \). In other words, we have \( y^2 - y^1 = (y^3 - y^1) + \cdots + (y^\ell - y^1) \). Thus

\[
f^T (y^2 - y^1) = f^T (y^3 - y^1) + \cdots + f^T (y^\ell - y^1) > 0 + \cdots + 0 = 0,
\]

a contradiction.

Conversely, assume that \( CDG(y^1, y^2) \) cannot be decomposed in such a manner. Note that if \( CDG(y^1, y^2) \) were anything other than a single path or cycle, it could be decomposed into two valid \( CDG \)'s at \( y^1 \) by isolating a directed cycle or a maximal path from the remainder of the graph. Furthermore, if \( CDG(y^1, y^2) \) were a directed path with a free interior vertex \( c_i \), it could be decomposed into two valid \( CDG \)'s at \( y^1 \) by splitting the graph at \( c_i \). Similarly, if \( CDG(y^1, y^2) \) were a directed cycle with at least two free vertices, we could split \( CDG(y^1, y^2) \) into two directed paths at these vertices in order to form two valid \( CDG \)'s at \( y^1 \). Hence, \( CDG(y^1, y^2) \) must meet the specifications of the lemma. See Figure 11 for examples of possible structures for \( CDG(y^1, y^2) \) and their implications.

To show that \( y^1 = (y^1_1, ..., y^1_{kn})^T \) and \( y^2 = (y^2_1, ..., y^2_{kn})^T \) are joined by an edge in \( PP(\kappa^\pm) \), it suffices to find a vector \( f \in \mathbb{R}^{kn} \) such that \( f^T y^1 = f^T y^2 < f^T v \) for any other vertex \( v \in PP(\kappa^\pm) \). Define such a vector \( f = (f_{11}, ..., f_{kn})^T \) by setting

\[
f_{ij} = \begin{cases} 0 & \text{if } x_j \in C^1_i \cap C^2_i \\ 0 & \text{if } c_i \text{ is fixed, free, or an endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(y^1, y^2) \\ -1 & \text{if } c_i \text{ is a saturated non-endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(y^1, y^2) \\ 1 & \text{if } c_i \text{ is a depleted non-endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(y^1, y^2) \\ 2n & \text{otherwise.} \end{cases}
\]

Hence, if \( \alpha \) denotes the number of non-endpoint saturated vertices in the path/cycle of \( CDG(y^1, y^2) \) and \( \beta \) denotes the number of non-endpoint depleted vertices in this component, we have \( f^T y^1 = f^T y^2 = \beta - \alpha \).

Let \( v \) be any other vertex of \( PP(\kappa^\pm) \) and let \( C^v = (C^v_1, ..., C^v_k) \) denote its corresponding clustering. If \( CDG(y^1, v) \) contains any edge \((c_i, c_j)\) not found in \( CDG(y^1, y^2) \), then if \( x_\ell \) is the label of this edge, we have \( f_{j\ell} = 2n \) and \( v_{j\ell} = 1 \). Thus, since \( v \) has exactly \( n \) nonzero components, we obtain \( f^T v > n \geq f^T y^1 \).

Therefore, we may assume that \( CDG(y^1, v) \) is a subgraph of \( CDG(y^1, y^2) \). Given that \( v \) is not equal to \( y^1 \) or \( y^2 \), it follows that \( CDG(y^1, v) \) is a nontrivial proper subgraph of \( CDG(y^1, y^2) \) and hence must be a collection of disjoint directed paths. Assume first that \( CDG(y^1, v) \) is a single directed \( c_i, c_j \)-path for some pair of vertices \( c_i, c_j \). Then either \( c_i \) is
CDG is a saturated non-endpoint of Fig. 11: Possible structures for CDG

In the former case, note that since CDG in the latter case, since CDG clustering difference graphs single directed path. As shown in the previous paragraph, it holds that 

\[ f_i = 3 \]

By Lemma 1, a circuit 

Proof.

The circuits of PP(\(k^\pm\)) have a significantly easier characterization than the edges. Two vertices of PP(\(k^\pm\)) are joined by a circuit step if and only if the corresponding clustering difference graph is a directed path or cycle.

**Lemma 4.** The circuits of PP(\(k^\pm\)) consist of those \(g \in \{0, 1, -1\}^{kn} \) that describe a single cyclical exchange or sequential movement of items among the clusters.

**Proof.** By Lemma 1, a circuit \(g \) of PP(\(k^\pm\)) satisfies \(g \in \{0, 1, -1\}^{kn} \). Furthermore, we must have \(\sum_{i=1}^{k} g_{ij} = 0 \) for \(j = 1, \ldots, n \), implying that \(g \) describes some set of transfers among a clustering of \(X\) – an entry \(g_{ij} = 1 \) implies that \(x_j \) is added to cluster \(C_i \), and \(g_{ij} = -1 \) implies that \(x_j \) is removed from \(C_i \). The inequality constraints \(By \leq d \) for this polytope consist of non-negativity constraints and cluster size constraints. Hence, the support of any
$Bg$ consists of the support of $g$ along with the indices of any clusters whose sizes are changed by the transfers of $g$. It follows that $Bg$ is support-minimal over all such transfers if and only if no subset of the cluster size changes implied by $g$ can be achieved by a nontrivial subset of the transfers of $g$.

Suppose that $g$ describes a single cyclical exchange of items. Then no cluster sizes are changed when applying the transfers of $g$, but applying any nontrivial subset of these transfers results in at least two cluster size changes. Hence, $g$ is a circuit of $PP(\kappa^\pm)$. Similarly, if $g$ describes a single sequential movement of items among the clusters (i.e. the CDG implied by the transfers of $g$ consists of a single directed path), then only two cluster sizes are changed by the transfers of $g$. Any nontrivial subset of these transfers necessarily changes the size of a third cluster. Hence, $g$ is again a circuit of $PP(\kappa^\pm)$.

Conversely, suppose that $g$ does not describe a single cyclical exchange or sequential movement, and let $D$ be a CDG whose transfers are described by $g$. If $D$ contains a directed cycle as a subgraph, the transfers given by this cycle are a proper subset of those given by $g$ that result in no cluster size changes. Hence, $g$ must not be a circuit. If $D$ is acyclic, $D$ must properly contain a maximal path $D'$. The only two clusters whose sizes are changed as a result of the transfers of $D'$ correspond to the two endpoints of $D'$. By the maximality of $D'$, the sizes of these two clusters are also changed by the transfers of $g$. Hence, $g$ again must not be a circuit of $PP(\kappa^\pm)$. □

By Corollary 1, we know that all circuit walks in $PP(\kappa^\pm)$ are vertex walks. However, Lemmas 3 and 4 highlight the difference between edges and circuits in $PP(\kappa^\pm)$ and imply that many of these circuit walks are not edge walks.

Finally, we would like to note that the property stated in Lemma 4 appears as a necessary condition for two vertices to be joined by an edge in some linear projections of bounded-size partition polytopes [9].

4 Proofs for Section 2.3

4.1 Proof of Theorems 2 to 4

Recall the definitions of elementary arrangements, elementary cones, inner cones, and $(n, d)$-parallelopipes provided in Section 2.3. Without loss of generality, assume we have a full-dimensional polyhedron of the form $P = \{x \in \mathbb{R}^n : Bx \leq d\}$ given by a minimal representation. (Note that any polyhedron $P = \{x \in \mathbb{R}^{n'} : Ax = b, Bx \leq d\}$ can be expressed in this form with dimension $n = n' - \text{rank}(A)$ by using the equality constraints to reduce the number of variables.) Although the circuits of a polyhedron $P$ are determined by its constraint system, the use of a minimal representation ensures that each constraint appears as a facet in $P$, allowing us to characterize the set of circuits of $P$ via its geometric properties. Our first observation is that elementary cones are generated by circuits of $P$.

**Lemma 5.** A vector $g \in \mathbb{R}^n \setminus \{0\}$ with coprime integer components is a circuit of the full-dimensional polyhedron $P = \{x \in \mathbb{R}^n : Bx \leq d\}$ if and only if $g$ belongs to the intersection of $n - 1$ hyperplanes $B_i x = 0$ from the elementary arrangement of $P$ whose corresponding rows $B_i$ in $B$ are linearly independent.

**Proof.** Suppose first that $g$ is a circuit of $P$. Let $B'$ be a maximal row submatrix of $B$ such that $B'g = 0$. As in the proof of Lemma 1, we must have $\text{rank}(B') = n - 1$ else $g$ would
not be a circuit of $P$. A set of $n - 1$ linearly independent rows from $B'$ corresponds to $n - 1$
hyperplanes of the form $B_j x = 0$ whose intersection is generated by $g$.

Conversely, let $B'$ be a row submatrix of $B$ consisting of $n - 1$ linearly independent rows $B_i$ where $B_i g = 0$. The one-dimensional kernel of $B'$ must be generated by $g$. Note that any vector $y \in \mathbb{R}^n \setminus \{0\}$ such that $\text{supp}(y) \subseteq \text{supp}(g)$ must satisfy $y \in \ker(B')$, or $y = \lambda g$ for some $\lambda \neq 0$. Hence, we must have $\text{supp}(y) = \text{supp}(g)$, implying that $g$ is a circuit of $P$. □

Note that if $C = \{ x \in \mathbb{R}^n : Dx \leq 0 \}$ is an elementary cone of $P$ generated by circuits $\{g_1, \ldots, g_k\}$, its opposite $-C = \{ x \in \mathbb{R}^n : Dx \geq 0 \}$ is also an elementary cone of $P$ generated by circuits $\{-g_1, \ldots, -g_k\}$. The following theorem relates the inner cones of a non-degenerate polytope whose only circuit walks are edge walks to these elementary cones. Recall that if $v$ is a vertex of $P$, the inner cone $I(v)$ of $v$ consists of all feasible directions from $v$ with respect to $P$ and is generated by the edge directions incident to $v$.

**Theorem 2** Let $P = \{ x \in \mathbb{R}^n : Bx \leq d \}$ be a full-dimensional, non-degenerate polytope. All circuit walks in $P$ are edge walks if and only if for each vertex $v \in P$, the inner cone $I(v)$ is an elementary cone of $P$.

**Proof.** Suppose first that all circuit walks are edge walks in $P$ and let $v$ be a vertex of $P$. The inner cone $I(v)$ is generated by the $n$ circuits of $P$ corresponding to the $n$ edge directions incident to $v$. If $I(v)$ is not an elementary cone of $P$, there exists an elementary cone $C$ of $P$ contained in $I(v)$. As a consequence of Lemma 5, $C$ is generated by at least $n$ circuits of $P$. At least one of these circuits must be different from the $n$ circuits generating $I(v)$. However, this implies that $I(v)$ contains a circuit that is not an edge direction incident to $v$. Since $P$ is bounded, this contradicts the fact that all circuit walks are edge walks in $P$.

Conversely, suppose that all inner cones of vertices in $P$ are elementary cones of $P$, and let $v$ be any vertex of $P$. The inner cone $I(v)$ is again generated by the $n$ circuits $g_1, \ldots, g_n$ corresponding to edge directions incident to $v$. Suppose that some other circuit $g$ is contained in $I(v)$. Then we have $g = \sum_{i=1}^{n} \lambda_i g_i$, where each $\lambda_i \geq 0$. Assume without loss of generality that $\lambda_1 > 0$. Then the circuits $g, g_2, \ldots, g_n$ are linearly independent and generate an $n$-dimensional cone properly contained in $I(v)$. Lemma 5 implies that this cone is formed by hyperplanes from the elementary arrangement of $P$, contradicting the fact that $I(v)$ is an elementary cone of $P$. Hence, it must hold that no other circuit of $P$ is contained in $I(v)$, and since this holds for any vertex $v \in P$, all circuit walks in $P$ are edge walks. □

Theorem 2 is a quite straightforward characterization of non-degenerate polytopes whose only circuit walks are edge walks. We now use it to prove a more descriptive characterization which we call the symmetric inner cone condition. First, we show that this condition is a necessary property of any polytope whose only circuit walks are edge walks. Recall that given a pair of vertices $u, v$ of a polyhedron $P$, we let $P^{uv}$ denote the minimal face of $P$ containing $u$ and $v$ and let $I^{uv}(u), I^{uv}(v)$ denote the inner cones of $u, v$ with respect to $P^{uv}$.

**Lemma 6.** Let $P = \{ x \in \mathbb{R}^n : Bx \leq d \}$ be a full-dimensional, non-degenerate polytope whose only circuit walks are edge walks. Then $I^{uv}(u) = -I^{uv}(v)$ for all pairs of vertices $u, v$ in $P$.

**Proof.** Let $u, v$ be a pair of vertices in $P$, and let $d := \dim(P^{uv})$. If $d = 1$ and $u$ shares an edge with $v$ in $P$, the result is trivial, so assume that $d \geq 2$ and that $u, v$ are not adjacent.
Note that the direction \( v - u \) belongs to the inner cone \( I_u^v(u) \) and that its opposite \( u - v \) belongs to \( I_v^u(v) \). By the definition of \( I_u^v \), both of these directions belong to the strict interiors of their respective cones, implying that the interior of \( I_u^v(u) \) intersects the interior of \(-I_v^u(v)\). By Theorem 2, \( I(u) \) and \( I(v) \) are elementary cones of \( P \). Hence, \( I_u^v(u) \) and \( I_v^u(v) \) must be elementary cones of \( P_{uw} \). Since their interiors intersect, we obtain \( I_u^v(u) = -I_v^u(v) \) by the definition of elementary cones. \( \square \)

To show that this symmetric inner cone condition of Lemma 6 is also a sufficient condition for all circuit walks to be edge walks in a polytope, first suppose that \( P \) satisfies this condition while containing a pair of vertices that shares no facets. It then must hold that \( P \) is a parallelotope, immediately implying that all of its circuit walks are edge walks.

**Lemma 7.** Let \( P \) be an \( n \)-dimensional, non-degenerate polyhedron that satisfies \( I_u^v(u) = -I_v^u(v) \) for all pairs of vertices \( u, v \) in \( P \). If \( P \) contains a pair of vertices that shares no facets, then \( P \) is an \( n \)-parallelotope.

**Proof.** The statement is straightforward for \( n \leq 2 \), so assume \( n \geq 3 \). Let \( u, v \) be a pair of vertices in \( P \) that shares no facets. Hence, \( I(v) = -I(u) \). Note that this immediately implies that \( P \) is a polytope since any extreme ray of \( P \) would have to belong to the two \( n \)-dimensional cones \( I(u) \) and \( -I(u) \). Furthermore, the \( n \) facets containing \( u \) are parallel to the \( n \) facets containing \( v \). Let \( \mathcal{F} \) denote this set of \( 2n \) facets which form an \( n \)-parallelotope \( Q \). Unless \( P \) contains a facet outside of \( \mathcal{F} \), we have \( P = Q \).

So suppose that \( P \) contains facets outside of \( \mathcal{F} \). Some such facet \( F \) contains a vertex \( w \) which is a neighbor of some vertex from \( Q \). Such a vertex \( w \) must not also be a vertex of \( Q \) itself, else it would be a degenerate vertex in \( P \). Hence, \( w \) is formed by the intersection of \( F \) with an edge \( e \) of \( Q \), cutting off some vertex \( y \in Q \) from \( P \). Note that if \( e \) is incident to \( u \), then \( w \) shares no facets with \( v \) and by assumption \( I(w) = -I(v) \). However, this then implies \( I(w) = I(u) \), a contradiction. Hence, \( y \) must not be a neighbor of \( u \). Similarly, \( y \) must not be a neighbor of \( v \).

Now, consider such a facet \( F \notin \mathcal{F} \) in \( P \) that cuts off a vertex \( y \in Q \) sharing the most facets with \( u \) in \( Q \), and let \( k \) denote this number of facets shared by \( y \) and \( u \) in \( Q \). Since \( y \) must not be adjacent to \( u \) in \( Q \), we have \( k \leq n - 2 \). We will show that there then exist three vertices of \( P \) from \( Q \) which share more facets with \( u \) than \( v \) in \( Q \) such that \( y \) completes a 2-parallelotope with these three vertices. In order for \( P \) to satisfy the symmetric inner cone condition, it must follow that \( y \in P \), a contradiction.

In particular, let \( F_1, ..., F_n \) denote the facets of \( Q \) incident to \( u \) and \( G_1, ..., G_n \) denote the facets of \( Q \) incident to \( v \). Assume that \( F_1, ..., F_k, G_{k+1}, ..., G_n \) are the facets incident to \( y \) in \( Q \). As \( Q \) is a parallelotope, the point \( x_1 \) formed by the intersection of facets \( F_1, ..., F_{k+1}, G_{k+2}, ..., G_n \) is a vertex of \( Q \). Since \( x_1 \) shares more than \( k \) facets with \( u \), it is not cut off by any facet outside of \( \mathcal{F} \) and is also a vertex of \( P \). Similarly, the point \( x_2 \) formed by \( F_1, ..., F_{k+2}, G_{k+3}, ..., G_n \) and the point \( x_3 \) formed by \( F_1, ..., F_k, G_{k+1}, F_{k+2}, G_{k+3}, ..., G_n \) are also vertices of \( P \).

However, consider the two-dimensional face \( P' \) of \( P \) formed by the intersection of facets \( F_1, ..., F_k, G_{k+3}, ..., G_n \). It holds that \( x_1, x_2, x_3 \) are vertices of \( P' \). Furthermore, vertices \( x_1 \) and \( x_3 \) of \( P' \) share no facets in \( P' \), so in order for the symmetric inner cone condition to be satisfied, \( P' \) is a 2-parallelotope. The vertex opposite of \( x_2 \) in \( P' \) must then be \( y \), but this contradicts \( y \notin P \). Therefore, no such facet \( F \) exists in \( P \), implying that the only facets of \( P \) belong \( \mathcal{F} \) and thus \( P = Q \). \( \square \)
Next, we show that if a polytope $P$ satisfies the symmetric inner cone condition of Lemma 6 but does not necessarily contain a pair of vertices that shares no facets, then $P$ must still be an $(n,d)$-parallelotope for some $d \leq n$. Namely, if $k$ denotes the minimum number of facets shared by any pair of vertices in $P$, then $P$ is an $(n,n-k)$-parallelotope.

**Lemma 8.** Let $P$ be an $n$-dimensional, non-degenerate polytope that satisfies $I^{uv}(v) = -I^{uv}(v)$ for all pairs of vertices $u,v$ in $P$. Then $P$ is an $(n,n-k)$-parallelotope, where $k$ is the minimum number of facets shared by any pair of vertices in $P$.

**Proof.** If $k = 0$, Lemma 7 implies that $P$ is a parallelotope, so assume $k \geq 1$ and let $u,v$ be a pair of vertices in $P$ that shares exactly $k$ facets. Note that $P^{uv}$ is the intersection of the $k$ facets shared by $u$ and $v$. Hence, $P^{uv}$ is an $(n-k)$-dimensional polytope satisfying the symmetric inner cone condition in which $u$ and $v$ share no facets. By Lemma 7, $P^{uv}$ is an $(n-k)$-parallelotope.

Next, note that $P$ has at least $2n-k$ facets: the $k$ facets shared by $u$ and $v$, the $n-k$ facets containing $u$ but not containing $v$, and the $n-k$ facets containing $v$ but not $u$. Let $F$ denote this set of $2n-k$ facets. By the structure of $P^{uv}$, each vertex of $P^{uv}$ is the intersection of $n$ of these facets. In fact, we show that these are the only facets of $P$.

First, suppose that $P$ contains some facet $F \notin F$ that intersects one of the edges of $P$ that leave $P^{uv}$. This intersection forms a vertex $w$ that shares an edge with some vertex $u' \in P^{uv}$. Since $P^{uv}$ is a parallelotope, there exists a vertex $v' \in P^{uv}$ that shares no facets with $u' \in P^{uv}$. Thus, the only facets shared by $u'$ and $v'$ in $P$ are the $k$ facets forming $P^{uv}$. However, since $v'$ must not be contained in $F$, this implies that $w$ and $v'$ share only $k-1$ facets in $P$, a contradiction with the choice of $k$.

Therefore, no facet outside of $F$ intersects any of the edges leaving $P^{uv}$ in $P$. Hence, since $P$ is bounded, every edge that leaves $P^{uv}$ hits some facet of $F$. Additionally, the vertex $w$ formed by this intersection shares exactly $k$ facets with some vertex of the $(n-k)$-parallelotope $P^{uv}$. Namely, if $u'$ again denotes the neighbor of $w$ in $P^{uv}$ and $v'$ is the vertex of $P^{uv}$ sharing exactly $k$ facets with $u'$ in $P$, then $w$ also shares exactly $k$ facets with $v'$ in $P$: $k-1$ of the facets forming $P^{uv}$ and one facet incident to $v'$ but not $u'$ in $P$. Thus, the face $P^{uv'}$ of $P$ is an $(n-k)$-parallelotope formed by the facets of $F$ which contains the vertex $w$.

Proceeding inductively on combinatorial distance from $P^{uv}$, we see that all vertices of $P$ belong to some $(n-k)$-parallelotope face of $P$ formed by the facets of $F$. Thus, the only facets of $P$ are those of $F$. By definition, it follows that $P$ is an $(n,n-k)$-parallelotope. \(\square\)

An $n$-parallelotope $P$ given by a minimal representation has only $n$ circuit directions: the directions of its $n$ classes of parallel edges. Hence, it is quite clear that all circuit walks in $P$ are edge walks. It is not immediately clear that this result generalizes to $(n,d)$-parallelotopes, but we show in the following lemma that this is indeed the case.

**Lemma 9.** All circuit walks in an $(n,d)$-parallelotope given by a minimal representation are edge walks.

**Proof.** Let $P$ be an $(n,d)$-parallelotope given by a minimal representation. By Theorem 2, it suffices to show that the inner cone of each vertex in $P$ is an elementary cone. Thus, suppose for the purpose of contradiction that the inner cone of some vertex $v \in P$ is not an elementary cone of $P$. Then there exists a facet $F$ of $P$ with corresponding inequality $b^Tx \leq \delta$ such that the parallel hyperplane $H_0 = \{x \in \mathbb{R}^n : b^Tx = 0\}$ divides the inner
cone $I(v)$ into two $n$-dimensional cones. In particular, an edge of $I(v)$ leaves $H_0$ on either side of $H_0$. If this were not the case, the corresponding hyperplanes of all facets of $P$ would intersect $I(v)$ within a proper face of $I(v)$, and it would hold that $I(v)$ is an elementary cone.

Therefore, consider the hyperplane $H = \{ x \in \mathbb{R}^n : b^T x = b^T v \}$ which is parallel to $F$ and incident to $v$. Then there exist edges incident to $v$ in $P$ that leave $H$ on either side of $H$. Namely, since $P$ is non-degenerate, there exist facets $F_1$ and $F_2$ incident to $v$ such that the edge $e_1$ leaving $F_1$ at $v$ leads to a vertex $z_1$ satisfying $b^T z_1 < b^T v$, and the edge $e_2$ leaving $F_2$ at $v$ leads to a vertex $z_2$ satisfying $b^T z_2 > b^T v$.

Since $P$ is an $(n,d)$-parallelotope, there exists some vertex $u \in P$ sharing exactly $n-d$ facets with $v$. Furthermore, since $v \notin F$ but together $u$ and $v$ must be incident to all $n+d$ facets of $P$, we must have $u \in F$.

Now suppose that $u$ belongs to neither $F_1$ nor $F_2$. Then the edges $e_1$ and $e_2$ must be two of the $d$ edges incident to $v$ in $P^{uv}$ since $F_1$ and $F_2$ are not among the $n-d$ facets shared between $u$ and $v$. We will say that an edge with direction $e$ is parallel to a facet with normal $b$ if and only if $b^T e = 0$. Hence, neither of the edges $e_1$ and $e_2$ are parallel to $F$. However, in order to satisfy the symmetric inner cone condition $I^{uv}(v) = -I^{uv}(u)$, there must exist a pair of edges incident to $u$ in $P^{uv}$ which are parallel to $e_1$ and $e_2$. This contradicts the fact that since $P$ is non-degenerate, only one of the $n$ edges incident to $u$ is not parallel to $F$.

Therefore, $u$ must belong to at least one of $F_1$ and $F_2$. If $u$ belongs to both $F_1$ and $F_2$, we may take a step along the edge incident to $u$ that leaves $F_2$ to reach a new vertex in $F_1$ sharing exactly $n-d$ facets with $v$. Hence, there always exists a vertex sharing $n-d$ facets with $v$ that is incident to precisely one of $F_1$ and $F_2$. Without loss of generality we will assume $u \in F_1$ and $u \notin F_2$.

There exists an edge incident to $u$ that leaves $F_1$ and intersects some facet $G$ of $P$ at a vertex $w$. Recall that $u \in F$, so since the edge between $u$ and $w$ does not leave $F$, we also have $w \in F$. As seen in the proof of Lemma 8, $w$ shares exactly $n-d$ facets with $v$ in $P$. Hence, if $G$ is not $F_2$, it holds that $w$ is a vertex in $F$ belonging to neither $F_1$ nor $F_2$, and we again obtain the above contradiction. Thus, we may assume $G = F_2$ and therefore $w \in F_2$.

Since $v$ shares exactly $n-d$ facets with $w$ in the $(n,d)$-parallelotope $P$, the face $P^{uw}$ must be a $d$-parallelotope. Because $w \notin F_1$, the edge $e_1$ incident to $v$ is contained in $P^{uw}$.

Furthermore, since $w \in F$ while $v \notin F$, it holds that $P^{uw} \cap F$ is a facet of $P^{uw}$. Note that in a parallelotope, the only edges that are not parallel to a given facet must intersect that facet. The edge $e_1$ is not parallel to $F$, so it must not be parallel to any of its lower dimensional faces. Thus, $e_1$ is not parallel to the facet $P^{uw} \cap F$ of $P^{uw}$, implying that $e_1$ intersects $P^{uw} \cap F$. This yields $z_1 \in F$.

Similarly, if we consider the edge $e_2$ in the $d$-parallelotope $P^{uw}$, we see also that $z_2 \in F$. However, this would imply that $b^T v > b^T z_1 = \delta = b^T z_2 > b^T v$, a contradiction. \hfill \Box

Theorems 3 and 4 now follow directly from Lemmas 6, 8 and 9. If all edge walks are circuit walks in a non-degenerate polytope, then the opposite inner cone condition must be satisfied, implying that the polytope is an $(n,d)$-parallelotope. Conversely, any non-degenerate polytope that satisfies the symmetric inner cone must be an $(n,d)$-parallelotope, which then implies that all circuit walks are edge walks if the polytope is given by a minimal representation.
4.2 Fixed-size Partition Polytopes

Recall that the characterization in Theorem 4 is restricted to non-degenerate polytopes. Thus, polytopes in which all circuit walks are edge walks are not limited to the described structure, if we allow for degeneracy. We close the discussion with a class of (highly) degenerate polytopes that are relevant in practice, and for which all circuits walks are edge walks.

As a special class of transportation polytopes introduced in [5], the fixed-size partition polytope $PP(\kappa)$ is associated with the partitioning of a set $X = \{x_1, ..., x_n\}$ of items into clusters $C_1, ..., C_k$ where each cluster $C_i$ has prescribed size $\kappa_i \in \mathbb{Z}_+$. Note that the well-known Birkhoff polytope is an instance of this polytope for $k = n$ and $\kappa_i = 1$ for $i = 1, ..., n$. Furthermore, it is equivalent to the bounded-size partition polytope $PP(\kappa^\pm)$ of Section 3.4 if we let $\kappa^- = \kappa^+$ for $i = 1, ..., k$. However, we show here that $PP(\kappa)$ is more restrictive than $PP(\kappa^\pm)$ in regard to its circuit walk behavior.

For $i = 1, ..., k$ and $j = 1, ..., n$, let $y_{ij}$ be a binary variable indicating whether or not item $x_j$ is assigned to cluster $C_i$. Then $PP(\kappa)$ is the 0/1-polytope defined by the following system of constraints:

$$
\sum_{j=1}^{n} y_{ij} = \kappa_i \quad i = 1, ..., k
$$

$$
\sum_{i=1}^{k} y_{ij} = 1 \quad j = 1, ..., n
$$

$$
y_{ij} \geq 0 \quad i = 1, ..., k, \ j = 1, ... n.
$$

Since the constraint matrix defining the polytope is totally unimodular and the right-hand sides are integral, the vertices of $PP(\kappa)$ indeed consist of all feasible clustering assignments $y \in \{0, 1\}^{kn}$. As in Section 3.4, given two such assignments $y^1, y^2$, the clustering difference graph $CDG(y^1, y^2)$ from $y^1$ to $y^2$ is the directed graph with nodes $c_1, ..., c_k$ where the edge $(c_i, c_j)$ with label $x_l$ is included if and only if $y^1_{il} = y^2_{jl} = 1$ with $i \neq j$. Hence, $CDG(y^1, y^2)$ gives all single-item transfers necessary to transform the clustering assignment of $y^1$ into that of $y^2$. Since the sizes of all clusters are fixed, it holds that $CDG(y^1, y^2)$ decomposes into directed cycles. It is shown in [5] that $y^1$ and $y^2$ are adjacent in $PP(\kappa)$ if and only if $CDG(y^1, y^2)$ consists of a single directed cycle. This characterization of edges allows for useful bounds on the combinatorial diameter of $PP(\kappa)$.

Let us examine the circuits of $PP(\kappa)$. Since the polytope is defined by a totally unimodular matrix, a circuit $g$ of $PP(\kappa)$ satisfies $g \in \{0, 1, -1\}^{kn}$ by Lemma 1. Also, since $g$ satisfies $\sum_{j=1}^{n} g_{ij} = 0$ for $j = 1, ..., n$, we see that $g$ describes a set of transfers of items among the clusters. Furthermore, we have $\sum_{j=1}^{n} g_{ij} = 0$ for $i = 1, ..., k$, so the transfers described by $g$ do not change the size of any cluster. Thus, $g$ describes some set of cyclical exchanges among the clusters. However, $g$ must also be support-minimal over all such sets of exchanges, which holds if and only if $g$ describes a single cyclical exchange of items.

We now see that all circuit walks in $PP(\kappa)$ are edge walks. If $y^1$ is a vertex of $PP(\kappa)$ and $g$ is a feasible circuit direction at $y$, taking a maximal step in the direction of $g$ corresponds to applying a single cyclical exchange of items among the clusters. Hence, the resulting clustering assignment $y^2$ yields a clustering difference graph $CDG(y^1, y^2)$ consisting of a single cycle, implying that $y^1$ and $y^2$ indeed share an edge in $PP(\kappa)$. Note, however, that $PP(\kappa)$ is a highly degenerate polytope. Hence, its structure is not limited to $(n, d)$-parallelotopes.
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