Abstract—This article presents design techniques proposed for efficient hardware implementation of feedforward artificial neural networks (ANNs) under parallel and time-multiplexed architectures. To reduce their design complexity, after the weights of ANN are determined in a training phase, we introduce a technique to find the minimum quantization value used to convert the floating-point weight values to integers. For each design architecture, we also propose an algorithm that tunes the integer weights to reduce the hardware complexity avoiding a loss in the hardware accuracy. Furthermore, the multiplications of constant weights by input variables are implemented under the shift-adds architecture using the fewest number of addition/subtraction operations found by prominent previously proposed algorithms. Finally, we introduce a computer-aided design (CAD) tool, called SIMURG, that can describe an ANN design in hardware automatically based on the ANN structure and the solutions of proposed design techniques and algorithms. Experimental results indicate that the tuning techniques can significantly reduce the ANN hardware complexity under a design architecture and the multiplierless design of ANN can lead to a significant reduction in area and energy consumption, increasing the latency slightly.

Index Terms—artificial neural networks, parallel and time-multiplexed architectures, hardware-aware post-training, multiplierless design.

I. INTRODUCTION

Recent years have seen a tremendous interest in artificial neural networks (ANNs), their successful applications in a wide range of problems, including image recognition [1] and face detection [2], their promising development on graphical processing units (GPUs) [3], and their efficient hardware implementations on different design platforms, such as analog, digital, hybrid very large scale integrated circuits (VLSI), and field programmable gate-arrays (FPGAs) [4]. An ANN is a computing system built up by a number of simple and highly interconnected processing elements [5]. As shown in Fig. 1(a), its fundamental unit, called neuron, sums the multiplication of weights by input variables, adds the bias value to this summation, and propagates this result to the activation function. While the bias value has the effect of increasing or decreasing the input of the activation function, the activation function limits the amplitude of the neuron output [6]. Mathematically, the neuron behavior can be defined as $y = \sum_{i=1}^{n} w_{i}x_{i}$ and $z = \phi(y + b)$ where $n$ denotes the number of input variables and weights. On the other hand, Fig. 1(b) presents an ANN design including hidden and output layers where each circle denotes a neuron.

Observe from Fig. 1 that the hardware complexity of an ANN depends heavily on weight and bias values and is dominated by a large number of multiplications of constant weights by input variables. Over the years, many algorithms and design architectures have been introduced to reduce the hardware complexity of ANNs [7]–[14]. In this article, we explore the hardware complexity of ANNs under the parallel and time-multiplexed architectures. Note that a time-multiplexed design, where computations are realized at a time, re-using the computing resources, is preferred to a parallel design in applications with a strict area requirement. However, since the time-multiplexed design needs multiple clock cycles to obtain the final result, it has a higher latency and energy consumption with respect to the parallel design [15]. To further explore the area versus latency and energy consumption trade-off, in this article, we consider two time-multiplexed architectures. Moreover, since the floating-point multiplication and addition operations occupy larger area and consume more energy than their integer counterparts [16], the floating-point weight and bias values found during training are converted to integers. Since the sizes of integer weight and bias values have a direct impact on the hardware complexity, we introduce a technique that can find the minimum quantization value, sacrificing a little loss in the hardware accuracy. Also, for each design architecture, we propose an algorithm that can tune the weight and bias values such that the hardware complexity is reduced avoiding a loss in the hardware accuracy. Furthermore, since the ANN design includes a large number of multiplications of constant weights by input variables and these weights are determined beforehand, these constant multiplications are realized under the shift-adds architecture using the fewest number of addition/subtraction operations found by previously proposed optimization algorithms [17]–[19]. Experimental results clearly indicate that the hardware-aware post-training and the multiplierless design lead to a significant reduction in the ANN hardware complexity with a little loss in the hardware accuracy. Moreover, different design architectures present alternative ANN realizations with different hardware
CAVM

MCM

SCM

y = cx

y = c_1 x_1 + c_2 x_2 + \ldots + c_n x_n

Fig. 2. Constant multiplications: (a) single constant multiplication (SCM); (b) multiple constant multiplication (MCM); (c) constant array vector multiplication (CAVM); (d) constant matrix vector multiplication (CMVM).

complexity so that a designer can choose the one that fits best in an application.

The rest of this article is organized as follows. Section II presents the background concepts and related work. The parallel and time-multiplexed design architectures are described in Section III. The hardware-aware post-training techniques are introduced in Section IV. Section V describes the multiplierless design of ANN. The CAD tool is introduced in Section VI and the experimental results are presented in Section VII. Finally, Section VIII concludes the article.

II. BACKGROUND

A. ANN Basics

Although the design techniques presented in this article can be applied to different ANN architectures, such as convolutional and recurrent, we consider the feedforward ANNs which do not include any feedback loop. Given the ANN structure including the number of inputs, outputs, layers, and neurons in each layer and the activation functions in each layer, the weight and bias values of ANN are determined in a training phase where the error between the desired and actual values is reduced using an iterative optimization algorithm. State-of-art training algorithms [13, 20, 21] consist of efficient techniques on initialization, optimization, and stopping criteria and include a number of activation functions. The training process is generally carried out offline on processors and/or GPUs. In the testing process, the ANN response on the applied inputs is computed using the weight and bias values determined in the training phase. The ANN computation is generally carried out online on a hardware design platform, such as application specific integrated circuits (ASIC) and FPGAs.

B. Multiplierless Constant Multiplications

Multiplication of constants by variable(s) is a ubiquitous and crucial operation in many applications, such as digital signal processing, cryptography, and compilers [22]. As illustrated in Fig. 2, constant multiplications can be categorized in four main classes:

1) The single constant multiplication (SCM) operation realizes the multiplication of a single constant $c$ by a single variable $x$, i.e., $y = cx$.

2) The multiple constant multiplication (MCM) operation computes the multiplication of a set of $m$ constants $C$ by a single variable $x$, i.e., $y_j = c_j x$ with $1 \leq j \leq m$.

3) The constant array-vector multiplication (CAVM) operation implements the multiplication of a $1 \times n$ constant array $C$ by an $n \times 1$ input vector $X$, i.e., $y = \sum_k c_k x_k$ with $1 \leq k \leq n$.

4) The constant matrix-vector multiplication (CMVM) operation realizes the multiplication of an $m \times n$ constant matrix $C$ by an $n \times 1$ input vector $X$, i.e., $y_j = \sum k c_{jk} x_k$ with $1 \leq j \leq m$ and $1 \leq k \leq n$.

Observe that the CMVM operation is the most general case and corresponds to an SCM operation when both $m$ and $n$ are 1, to an MCM operation when $m > 1$ and $n$ is 1, and to a CAVM operation when $m$ is 1 and $n > 1$.

Since the constants are determined beforehand, these constant multiplications can be realized using addition, subtraction, and shift operations under the shift-adds architecture. Note that parallel shifts can be implemented using only wires in hardware without representing any area cost. A straightforward shift-adds design technique, called the digit-based re-coding (DBR) [23], can realize constant multiplications in two steps given as follows: i) define the constants under a particular number representation, such as binary or canonical signed digit (CSD) [24]; ii) for the nonzero digits in the representation of constants, shift the input variables according to digit positions and add/subtract the shifted variables with respect to digit values. As a simple example, consider the CMVM operation in Fig. 3(a). Its direct realization needs 4 multiplication and 2 addition operations. The DBR method finds a solution with a total number of 8 adders and subtractors when constants are defined under the CSD representation as shown in Fig. 3(b).

The number of adders/subtractors can be further reduced by maximizing the sharing of common partial products among constant multiplications [17–19, 24–26]. Returning to our example, the algorithm of [18] finds a solution with 4 operations sharing the subexpression $x_1 + x_2$ as shown in Fig. 3(c). Moreover, prominent algorithms, that can find multiplierless designs of constant multiplications taking into account the gate-level area, delay, power dissipation, and throughput of the design, are introduced in [27–30]. Furthermore, efficient algorithms are proposed for the multiplierless realization of time-multiplexed constant multiplications in [31–33].

C. Related Work

For the multiplierless realization of neural networks, binary neural networks (BNNs), where weights values and activation functions are constrained to be either 1 or -1, were introduced in [8]. It is shown that BNNs drastically reduce the memory size and the number of accesses to the memory during training, and replace multipliers with XOR operators in hardware. However, they lead to a worse accuracy when compared to conventional neural networks [9]. In [9, 12], weights of ANNs are determined to include a small number of nonzero digits in training and hence, their multiplications by input variables can be realized using a small number of adders and subtractors. In [10], floating-point weights in each layer

1 An integer can be written in CSD using $n$ digits as $\sum_{i=0}^{n-1} d_i 2^i$, where $d_i \in \{-1, 0, 1\}$. The nonzero digits are not adjacent and a constant is represented with a minimum number of nonzero digits under CSD.
are quantized dynamically, fixed-point weights are expressed in binary representation, and the ANN is implemented in a hardware accelerator. The multiplierless hardware realization of ANNs is considered in [13] where the multiplication of weights by input variables is realized in a bit-serial fashion, defining weights under the CSD representation. In [14], for the time-multiplexed realization of ANN design, a post-training algorithm, that tunes weights to reduce the hardware complexity, is introduced and the multiplication of constant weights by input variables in each neuron at each layer is realized under the shift-adds architecture.

Under the time-multiplexed design architecture, the multiply-accumulate (MAC) block is a central operation. To reduce its high latency, a delay-efficient MAC structure, which uses accumulators and carry-save adders, was introduced in [15]. Efficient implementation of ANN designs using MAC blocks on FPGAs was introduced in [16]. Recently, MAC blocks have been used in the realization of neuromorphic cores using two models, namely axonal-based and dendritic-based [11].

III. DESIGN ARCHITECTURES

In this section, we present parallel and time-multiplexed design architectures used to realize ANNs in hardware.

A. Parallel Design

Fig. 4 presents the realization of neuron computations at the $k^{th}$ layer of ANN.

B. Time-Multiplexed Design

The MAC block is a fundamental operation in an ANN design under the time-multiplexed architecture. As shown in Fig. 5, it can be used to realize the neuron computation given in Fig. 1(a), re-using the multiplication and addition operations. Observe that the multiplication of a weight by an input variable is realized at a time synchronized by the control block, which is actually a counter, and is added to the accumulated value stored in the register $R$. In this figure, clock and reset signals are omitted for the sake of clarity. Under this architecture, the neuron computation is obtained after $n + 1$ clock cycles. The design complexity of the MAC block depends on the size of the counter and multiplexers, determined by the number of weights and input variables, on the size of the multiplier, determined by the maximum bitwidths of the input variables and weights, and on the size of adder and register, determined by the bitwidth of the inner product of inputs and weights, i.e., $y = \sum_{i=1}^{n} w_i x_i$.

In this subsection, we present two time-multiplexed architectures to design the whole ANN using MAC blocks. Under the first architecture, called SMAC_NEURON, each neuron at each layer is realized using a single MAC block and under the second architecture, called SMAC_ANS, the whole ANN is realized using a single MAC block. In following, these architectures are described in detail.

1) SMAC_NEURON Architecture: Fig. 6 presents the neuron computations at the $k^{th}$ layer of an ANN using $m$ MAC blocks and a common control block. The control block synchronizes the multiplication of associated weights by input variables.
Assuming that an ANN includes $\eta_i$ neurons at each layer, where $1 \leq i \leq \lambda$ and $\lambda$ denotes the number of layers, the required number of MAC blocks is $\sum_i \eta_i$, i.e., the total number of neurons. Note that the complexity of operations and registers in the MAC blocks is determined by the number of inputs and outputs at each layer and the weight values related to each neuron of each layer. The complexity of the control block is determined by the number of inputs at each layer. Since the neuron computations are obtained layer by layer, the neuron computations in a latter layer are started after the neuron computations in a former layer are finished. This is simply done by generating an output signal at each layer indicating that all neuron computations are obtained, which also disables the hardware to do unnecessary computations and enables us to reduce the power dissipation. The computation of the whole ANN with $\lambda$ layers and $\iota_i$ inputs at each layer, where $1 \leq i \leq \lambda$, is obtained after $\sum_i (\iota_i + 2)\eta_i$ clock cycles.

2) SMAC_Ann Architecture: Fig. 6 shows the ANN design using a single MAC block where clock and reset signals are omitted for the sake of clarity. In this figure, the control block includes three counters to synchronize the multiplication of a weight by an input variable, the addition of a bias value to each inner product, and the application of the activation function. These counters are associated with the number of layers, number of inputs at each layer, and number of outputs (or neurons) at each layer. Note that the variables $X_1, X_2, \ldots X_n$ denote the primary inputs of ANN and these variables are multiplied by the related weights during the computations at the first layer. While the size of multiplexers for the input variables is determined by the maximum number of inputs at all layers, the size of multiplexers for the weight and bias values are defined by the total number of weight and bias values, respectively. In the MAC block, the size of multiplier is determined by the maximum bitwidth of all input variables and weights and the sizes of adder and register are defined by the maximum bitwidth of the multiplication of weights by input variables in the whole ANN. Moreover, the number of registers used to store the outputs at each layer is determined by the maximum bitwidth of all input variables.

**IV. HARDWARE-AWARE POST-TRAINING**

In this section, we present a technique proposed for finding the minimum quantization value to convert the floating-point weight and bias values to integers and methods introduced for tuning weight and bias values to reduce the ANN design complexity under the parallel and time-multiplexed architectures.

A. Finding the Minimum Quantization Value

While converting floating-point weight and bias values found during training to integers, we aim to reduce bitwidths of weight and bias values. To do so, initially, we generate a validation data set, which is used to compute the hardware accuracy, by moving 30% of the training data set to this set randomly. We note that this validation data set is also used while computing the hardware accuracy during the post-training phase described in following subsections. The proposed technique is described as follows:

1) Set the quantization value, $q$, and the related ANN accuracy in hardware, $ha(q)$, to 0.
2) Increase $q$ value by 1.
3) Convert each floating-point weight and bias value to an integer by multiplying it by $2^q$ and finding the least integer greater than or equal to this multiplication result.
4) Compute $ha(q)$ value on the validation data set using the integer weight and bias values.
5) If $ha(q) > 0$ and $ha(q) − ha(q − 1)$ is greater than 0.1%, go to Step 2.
6) Otherwise, return $q$ as the minimum quantization value.

Observe that we sacrifice maximum 0.1% loss in the ANN accuracy in hardware computed on the validation data set in order to use small size weight and bias values.

B. Post-Training under the Parallel Architecture

The main idea for the post-training under the parallel architecture comes from the fact that weight values, which have CSD representations with a small number of nonzero digits, lead to constant multiplications with a small hardware complexity as shown in Fig. 3. After weight values are converted to integers using the minimum quantization value $q$, we check if the least significant nonzero digit in the CSD representation of a weight can be removed avoiding a loss in accuracy. The tuning procedure is described as follows:
1) Set $ha(q)$ computed in finding the minimum quantization value to the best ANN accuracy in hardware, $bha$.
2) For each weight $w$ other than 0, find its CSD representation.
   a) Find an alternative weight $w'$ for $w$ by removing the least significant nonzero digit in the CSD representation of $w$ and compute the ANN accuracy in hardware, $ha'$, when $w$ is replaced by $w'$.
   b) If $ha' \geq bha$, replace $w$ by $w'$ and update $bha$.
3) If at least one weight is replaced by an alternative one, go to Step 2.
4) Otherwise, return weight values.

Note that in Step 2 of the tuning procedure, the number of nonzero digits in the CSD representation of an alternative weight, which replaces the original weight, is always less than that of the original weight.

C. Post-Training under the Time-Multiplexed Architectures

The main idea for the post-training under the time-multiplexed architectures comes from the fact that in the MAC block shown in Fig. 5 if all weights are multiples of $2^k$, where $k > 0$, the inner product can be realized as $y = (\sum_{i=1}^n c_i x_i) \ll k$, where $c_i = w_i/2^k$ and $\ll$ stands for the left shift operation. Thus, bitwidths of constant weights to be multiplied by input variables in the MAC block, and consequently, sizes of the multiplier, adder, and register can be reduced. After weight values are converted to integers using the minimum quantization value $q$, under the SMAC_NEURON architecture, for each neuron, we aim to maximize the smallest left shift value among all its weights, denoted as $sls$, while avoiding a decrease in the ANN accuracy. As a simple example, the $sls$ value for the integer values 20 = 5 $\ll$ 2, 24 = 3 $\ll$ 3, and 26 = 13 $\ll$ 1, is computed as 1. The tuning procedure presented for the SMAC_NEURON architecture [14] is described as follows:

1) Set $ha(q)$ computed in finding the minimum quantization value to the best ANN accuracy in hardware, $bha$.
2) For each neuron in the ANN design, compute the $sls$ value for its weights.
   a) For each weight associated the $m^{th}$ neuron and $n^{th}$ input at the $k^{th}$ level, $w_{kmn}$, find its largest left shift value, $lls$.
   b) If $lls$ is equal to $sls$, determine the first possible weight as $pw_1 = w_{kmn} - (w_{kmn} \mod 2^{lls+1})$. If the bitwidth of $pw_1$ is less than or equal to the maximum bitwidth of weights associated with $N_i$, compute the ANN accuracy in hardware, $ha_1$, when $w_{kmn}$ is replaced by $pw_1$. Similarly, determine the second possible weight as $pw_2 = pw_1 + 2^{lls+1}$ and compute the related ANN hardware accuracy, $ha_2$.
   c) If $max(ha_1, ha_2) \geq bha$, replace $w_{kmn}$ by the possible weight that leads to the maximum ANN accuracy in hardware and update $bha$ accordingly.
   d) Otherwise, assuming that $w_{kmn}$ is replaced by the possible weight that leads to the maximum ANN accuracy in hardware, change the bias value of the neuron, $b_{km}$, in between $[b_{km} - \delta, b_{km} + \delta]$ and compute the ANN accuracy in hardware. If the ANN accuracy in hardware in one of these cases is greater than or equal to $bha$, update the values of $w_{kmn}$, $b_{km}$, and $bha$ accordingly.
3) If $sls$ value of any neuron is improved, go to Step 2.
4) Otherwise, return weight and bias values.

Note that in Step 2 of the tuning procedure, a possible weight, which replaces the original weight, has always the largest left shift value greater than that of the original weight.

For the SMAC-ANN architecture, we apply a similar procedure where the increment of the smallest left shift of all ANN weights is aimed in the MAC block as shown in Fig. 7.

V. ANNs UNDER THE SHIFT-ADDS ARCHITECTURE

This section presents the multiplierless realizations of ANN designs under the parallel and time-multiplexed architectures.

A. Multiplierless ANN Design under the Parallel Architecture

A straightforward way for the multiplierless realization of ANN under the parallel architecture is to describe each inner product at each layer, i.e., $y_{k1}, y_{k2}, \ldots, y_{kn}$ shown in Fig. 6 as a CAVM operation and to implement each CAVM block independently under the shift-adds architecture. We use the algorithm of [19] to optimize the number of adders/subtractors in the multiplierless designs of these CAVM blocks.

As shown in Fig. 8, all inner products at the $k^{th}$ layer can be described as a CMVM operation and the number of adders/subtractors in the multiplierless realization of the CMVM block can be reduced using the algorithm of [18]. Thus, the possible sharing of subexpressions can be increased, reducing the number of adders and subtractors in the multiplierless ANN design.

B. Multiplierless ANN Design under the Time-Multiplexed Architectures

Under the SMAC_NEURON architecture, the multiplications of associated weights by input variables at the $k^{th}$ layer shown in Fig. 6 can be computed in an MCM block and can be diverted to the corresponding adders using multiplexers as shown in Fig. 9. Rather than using an MCM block for each neuron, a single MCM block, which realizes the multiplication of all weights in a layer by an input variable, is used to increase the sharing of partial products, and thus, to reduce the required number of adders/subtractors. The exact algorithm of [17] is
used to find the shift-adds realization of the MCM block using a minimum number of adders/subtractors.

Similarly, the multiplierless realization of ANN under the SMAC_Neuron architecture presented in Fig. 7 can be obtained when the multiplication of all weight values by the selected input variable is implemented using an MCM block. However, since one multiplier is replaced by a large number of adders/subtractors, such a multiplierless realization increases the hardware complexity significantly.

VI. SIMURG: THE CAD TOOL

In this section, we present our CAD tool called SIMURG developed to generate automatically the hardware description of an ANN under the design architectures given in Section III using the post-training methods mentioned in Section IV and the multiplierless design techniques described in Section V.

Given the ANN structure, including the number of inputs, outputs, hidden layers, and neurons in the hidden layers and the type of activation function of neurons in each layer, initially, the ANN is trained using a state-of-art technique and different activation functions used in training and hardware design. The activation functions used in training (hardware) were respectively hsig, htnah, lin, ReLU, and satlin due to their simplicity in hardware. The tool can define the multiplication of constant weights by input variables in a behavioral fashion. Also, it can find the multiplierless realizations of these constant multiplications as described in Section V. The tool also generates a test-bench and necessary files to verify the ANN design and the synthesis scripts automatically. The SIMURG tool with its limited number of functions is available at https://github.com/leventaksoy/ANNs.

VII. EXPERIMENTAL RESULTS

In this work, we used the pen-based handwritten digit recognition problem [40] as an application. In the convolutional neural network design of this application, we implemented 5 feed-forward ANN structures with different number of layers and number of neurons in layers, denoted as $p_{in} \eta_1 \eta_2 \ldots \eta_\lambda$, where $p_{in}$ stands for the number of ANN primary inputs, which is equal to 16, and $\eta_k$, where $1 \leq k \leq \lambda$, indicates the number of neurons in the $k^{th}$ layer. Note that the activation function of each neuron in the hidden and output layers in training (hardware) was respectively htnah (htnah) and sigmoid (hsig) in our training algorithm ZAAL and PYTORCH. In MATLAB, it was respectively as htnah (htnah) and satlin (satlin). The activation functions were determined based on the software test accuracy found in training. The ANNs were trained using 7494 data and tested using 3498 data. We note that each training algorithm was run 30 times and weight and bias values, that yielded the best accuracy value, were chosen. Table I presents the training and hardware design details on different ANN design structures. In this table, sta, hta, and tmzd denote the software test accuracy, hardware test accuracy, and the total number of nonzero digits in the CSD representations of integer weights and bias values, respectively. Floating-point weight and bias values were converted to integers using the minimum quantization value determined as described in Section IV. In the ANN hardware design, bitwidths of ANN inputs and outputs at each layer were determined as 8.

Observe from Table I that different training algorithms lead to ANN designs with different hardware accuracy and integer weights and bias values. However, they yield software test accuracy values close to hardware test accuracy values. Note that the difference between the software and hardware test accuracy is due to the quantization value, bitwidths of ANN inputs and outputs at each layer, and different activation functions used in training and hardware design.
In this work, we present gate-level results of ANN designs implemented in three different architectures, namely parallel, SMAC_NEURON, and SMAC_ann, as described in Section III. In parallel designs, to make a fair comparison with time-multiplexed designs, flip-flops were added to outputs of the ANN design. ANN designs were described in Verilog and were synthesized using the Cadence RTL Compiler with the TSMC 40nm design library.

In order to explore the impact of a design architecture on the ANN hardware complexity, Figs. 10-12 present respectively area (in $\mu m^2$), latency (in $ns$), and energy consumption (in $pJ$) results of ANN designs under the parallel, SMAC_NEURON, and SMAC_ann architectures where no post-training technique is applied and constant multiplications are described in a behavioral fashion. Note that the latency is computed as the multiplication of the clock period by the number of clock cycles to obtain the ANN output. The clock period was reduced using the retiming technique in the synthesis tool iteratively. The switching activity data required for the computation of power dissipation was generated using the test data in simulation. This test data set was also used to verify the ANN design. Energy consumption is computed as the multiplication of latency and power dissipation.

Observe that weight and bias values found by different training algorithms lead to ANN designs with different hardware complexity where their impact is clearly observed on ANN designs under the parallel architecture since there exist a large number of constant multiplications. On the other hand, while ANN designs under the SMAC_ann architecture have the smallest area, the ones under the parallel architecture occupy the largest area. However, the latency of ANN designs under the parallel architecture is significantly smaller than those of ANN designs under the time-multiplexed architectures. Moreover, ANN designs under the SMAC_ann architecture consume the most energy. Note that area, latency, and energy consumption values of ANN designs under the SMAC_NEURON architecture are in between those of ANN designs under the parallel and SMAC_ann architectures.

| Structure | ZAAL | PYTORCH | MATLAB |
|-----------|------|---------|--------|
| 16-10     | 86.2 | 224     | 111    |
| 16-16-10  | 95.1 | 425     | 851    |
| 16-10-10-10 | 93.4 | 456     | 912    |
| 16-16-10-10 | 95.2 | 544     | 1127   |
| **Average** | 92.6 | 415     | 668    |

Fig. 10. ANN designs under the parallel architecture when constant multiplications are described in a behavioral fashion and no post-training is applied.

Fig. 11. ANN designs under the SMAC_NEURON architecture when constant multiplications are described in a behavioral fashion and no post-training is applied.

Fig. 12. ANN designs under the SMAC_ann architecture when constant multiplications are described in a behavioral fashion and no post-training is applied.

TABLE II
DETAILS OF ANNS DESIGNS UNDER THE PARALLEL ARCHITECTURE AFTER THE POST-TRAINING PHASE.
where the hardware test accuracy is increased after the post-training phase, such as all 16-10 ANN designs trained using ZAAL and 16-10-10 ANN designs under SMAC_NEURON and SMAC荜N architectures trained using PYTORCH.

In order to explore the impact of tuning algorithms on the ANN hardware complexity, Figs. 13–15 present respectively gate-level results of ANN designs obtained after weight and bias values are tuned to reduce the hardware complexity of ANN designs under the parallel, SMAC_neuron, and SMAC荜N architectures where constant multiplications are described in a behavioral fashion.

Observe from Figs. 10 and 12 that the use of a tuning algorithm can significantly reduce the hardware complexity of ANN designs under the parallel architecture. When compared to ANN designs realized without the post-training phase, we note that the maximum reduction on area, latency, and energy consumption is found as 65%, 44%, and 84% on the 16-16-10 ANN design trained using ZAAL, 16-10-10-10 and 16-16-10 ANN designs trained using PYTORCH, respectively. Similar results are observed on time-multiplexed designs. On the ANN designs under the SMAC荜N architecture, the maximum reduction on area, latency, and energy consumption is found as 35%, 15%, and 34% on the 16-16-10 ANN design trained using ZAAL, 16-10-10-10 ANN design trained using MATLAB, and 16-10-10-10 ANN designs trained using ZAAL, respectively. Finally, on the ANN designs under the SMAC࠳N architecture, the maximum reduction on area, latency, and energy consumption is found as 12%, 19%, and 37% on the 16-10-10-10 ANN design trained using ZAAL, 16-10-10-10 and 16-16-10 ANN designs trained using PYTORCH, respectively. Observe that the reduction on the hardware complexity of ANN designs under the parallel architecture is greater than that of the ANN designs under the time-multiplexed architectures due to a large number of multipliers and adders under the parallel architecture.

In order to compare the impact of the multiplierless design on the ANN hardware complexity, Figs. 16–18 present respectively gate-level results of multiplierless ANN designs under the parallel architecture using CAVM and CMVM blocks.
and of multiplierless ANN designs under the SMAC_NEURON architecture using MCM blocks after the post-training phase.

Observe from Figs. 14 and 16 that the multiplierless realization of CAVM and CMVM blocks reduces the area of ANN designs under the parallel architecture significantly. When compared to ANN designs where constant multiplications are described in a behavioral fashion after the post-training phase, the multiplierless design of ANNs using CAVM blocks leads to a maximum 11% area reduction obtained on the 16-10-10 ANN design trained using PyTorch. Note that the multiplierless realization of ANNs using CMVM blocks leads to a larger area reduction than those using CAVM blocks. This is due to the fact that the sharing of subexpressions is increased in the CMVM block, reducing the total number of adders and subtractors. When compared to ANN designs where constant multiplications are described in a behavioral fashion after the post-training phase, the multiplierless design of ANNs under the SMAC_NEURON architecture achieves a maximum 20% area reduction obtained on the 16-10-10 ANN design trained using MATLAB.

We note that proposed post-training and multiplierless design techniques can reduce the ANN hardware complexity independently of the training algorithm, although different training methods lead to ANN designs with different hardware complexity and accuracy.

VIII. CONCLUSIONS

This article presented alternative implementations of feedforward ANNs under the parallel and time-multiplexed architectures. For each architecture, it also introduced a hardware-aware post-training phase where weight and bias values of ANNs are tuned in order to reduce the hardware complexity taking into account the hardware accuracy. Moreover, it proposed design techniques to implement ANNs under the shift-adds architecture without using multipliers. Furthermore, it introduced a CAD tool that can automatically generate the hardware description of the ANN design under the given ANN specifications. Experimental results indicate that proposed post-training methods can reduce the ANN hardware complexity significantly and the multiplierless design of ANNs can reduce the area and energy consumption further, increasing the latency slightly.
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