An Adaptive Performance-oriented Scheduler for Static and Dynamic Heterogeneity

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Abstract
With the emergence of heterogeneous hardware paving the way for the post-Moore era, it is of high importance to adapt the runtime scheduling to the platform’s heterogeneity. To enhance adaptive and responsive scheduling, we introduce a Performance Trace Table (PTT) into XiTAO, a framework for elastic scheduling of mixed-mode parallelism. The PTT is an extensible and dynamic lightweight manifest of the per-core latency that can be used to guide the scheduling of both critical and non-critical tasks. By understanding the per-task latency, the PTT can infer task performance, intra-application interference as well as inter-application interference. We run random Direct Acyclic Graphs (DAGs) of different workload categories as a benchmark on NVIDIA Jetson TX2 chip, achieving up to 3.25× speedup over a standard work stealing scheduler. To exemplify scheduling adaption to interference, we run DAGs with high parallelism and analyze the scheduler’s response to interference from a background process on a Intel Haswell (2650v3) multicore workstation. We also showcase the XiTAO’s scheduling performance by porting the VGG-16 image classification framework based on Convolutional Neural Networks (CNN).

CCS Concepts • Software and its engineering → Runtime environments;

Keywords Heterogeneous architectures, Interference, Performance, Dynamic scheduling

1 Introduction
In order to deal with the stringent energy constraints of current IT systems, modern HPC systems are increasingly being architected as heterogeneous platforms. Systems may include both static and dynamic sources of heterogeneity. Static heterogeneity sources are those that are fixed at design time, for example, single-ISA cores with different power-efficiency (e.g. big.LITTLE), or asymmetric ISA systems consisting of processor cores and accelerators (e.g. CPU/GPU/FPGA platforms). Dynamic sources of heterogeneity are those that arise from runtime reconfiguration. For example, usage of Dynamic Voltage-Frequency Scaling (DVFS) [11] to tune the performance and efficiency of individual cores or clusters of cores is an example of dynamic heterogeneity. Another example is the usage of cache partitioning to tune cores to the working sets of applications [9]. The landscape of heterogeneous configurations creates a challenging scheduling problem.

To make matters worse, there are many sources of uncontrolled heterogeneity generally called interference. Interference refers to performance degradation resulting from shared resources. Interference can occur within a process, e.g. resulting from oversubscription of caches and memory bandwidth, or it can occur across processes, e.g. resulting from time-sharing of a single processing unit in order to run multiple concurrent applications. Obviously, designing scheduling strategies that address all these sources of heterogeneity under a optimization target (performance, energy, etc.) is a complex task. A solution necessarily requires online monitoring that can identify and adapt both to static and dynamic heterogeneity.

A scheduling solution for multithreaded computations requires an overlying execution model that is flexible and effective for performance portability. Prior research suggests that mixed-mode parallel computations, in which the nodes of a computational task-DAG are themselves parallel computations that can be assigned different amounts of processing resources [3, 12, 19], are a promising execution model for modern hierarchical and heterogeneous platforms. An important result from our research [12] is that greedy scheduling [2] is often an undesirable goal as it easily leads to resource over-subscription, particularly with the bandwidth-constrained and cache-constrained nature of modern compute systems1. This occurs because greedy schedulers will always try to schedule a ready task as long as there are idle processing units, even if the resulting interference results in a global deterioration of performance. One way to avoid the problem of resource oversubscription is to aggregate enough resources into a single execution place such that potentially interfering processes are forced to wait. In the context of mixed-mode parallelism this translates into providing the internally parallel tasks with enough resources to avoid interference.

The XiTAO library2 is an embodiment of this concept. In XiTAO, parallel tasks are scheduled into resource partitions called Elastic Places [12]. The method has been shown to perform efficiently on homogeneous manycore and NUMA systems. To achieve higher power efficiency, however, it is important to make XiTAO aware of heterogeneous platforms. Furthermore, XiTAO traditionally requires the programmer to statically determine the size of the N-core-places. This property limits productivity and performance portability.

In this paper, we explore and propose schemes to automatically determine resource partitions at runtime. Furthermore, we research how this knowledge can be used to leverage modern single-ISA platforms with both static and dynamic sources of heterogeneity. To this end, we present a scheduler inspired by Criticality-Aware Task Scheduling (CATS) [6] and extend it with a performance trace table

1https://www.karlrupp.net/2013/06/cpu-gpu-and-mic-hardware-characteristics-over-time/
2https://sites.google.com/site/mpericas/xitao
(PTT) that monitors the system’s performance characteristics at runtime. Despite its simplicity, the PTT provides enough information to implement both heterogeneity-aware and interference-free schedules at runtime at minimum cost. Most notably, these features are achieved with no static knowledge about the features of the application and no platform knowledge beyond what can be easily obtained with a tool such as hwloc [8].

To validate our proposal, we evaluate the scheme using irregular DAGs and the VGG-16 neural network on both an Nvidia Jetson TX2 development board featuring an heterogeneous multicore architecture, and on an Intel Xeon Haswell platform composed of two NUMA nodes and a total of 20 cores. Our experiments focus on the benefits of criticality-aware and interference-free scheduling on both static and dynamic heterogeneity. Sources of heterogeneity include static platform characteristics and dynamic interference episodes, such as co-scheduling of conflicting processes. We conclude by analyzing the scalability of a VGG-16 implementation on the PTT-enabled XiTAO framework.

In summary, this paper contributes:

- A heterogeneous scheduler on top of XiTAO and a study of the impact of its main tuning parameters.
- A tracing scheme called Performance Trace Table (PTT) that allows to infer the dynamic system heterogeneity.
- An in-depth evaluation of adaptability of the PTT in the context of interference and architectural heterogeneity.
- A showcase implementation of VGG-16 on XiTAO and a scalability analysis.

The remainder of this paper is organized as follows. Section 2 describes the background of graph theory which is used to describe computations. We present our approach in Section 3. Section 4 describes the experimental setup which is used to evaluate our approach (Section 5). Section 6 describes related work, while Section 7 concludes the work.

## 2 Task-DAG Scheduling

This work focuses on computations that can be described as DAGs (Directed Acyclic Graphs). An example of a task-DAG is shown in Figure 1. We define the critical path of a task-DAG as its longest path. In Figure 1, the critical path is marked with dotted lines whose length is 5. This can be obtained by traversing the nodes A → C → G → D → F. Tasks in the critical path are from now on called critical tasks, while the others are non-critical tasks. Nodes B and E are non-critical tasks in Figure 1. The task-DAG in Figure 1 also shows the criticality values of each node. Setting the criticality value in the DAG is achieved by traversing the DAG bottom-up until it reaches the start node(s). Hence, this requires the full DAG to be available before execution. The criticality value is set to be the maximum criticality of children plus 1. Effectively, this results in the first node of the longest path having the highest criticality value. As we can see, task A has the highest criticality. This strategy also shows how criticality can be determined at runtime: the task’s current criticality value is compared with the parent’s criticality value. If the difference is 1, then the task is on the critical path. Another important concept in this paper is the average DAG parallelism, which we define as $\text{Parallelism} = \frac{\text{Number of total tasks}}{\text{Number of critical tasks}}$. For example, the parallelism in Figure 1 is $7/5 = 1.4$.

![Figure 1](image.png)

**Figure 1.** An illustration of a DAG with a critical path in dotted lines. Different color represents different kernels. The number of tasks is seven and the critical path has length five.

## 3 Scheduling for Heterogeneous Systems

We begin this section by introducing the main concepts of the XiTAO runtime. We then present the performance trace table (PTT), a data structure that implements an online model of the execution time of each task type. Based on the PTT data structure, we then describe our implementation of the performance-based scheduler.

### 3.1 The XiTAO library

XiTAO is a novel runtime for executing mixed-mode computations in which the individual tasks of a task-DAG are themselves parallel computations. These parallel computations are usually data-parallel computations, but any sort of parallel structure is possible. In XiTAO, the individual task is a Task Assembly Object (TAO) and the task-DAG is called the TAO-DAG. For generality, we use the terms task and TAO interchangeably in this paper. A TAO type contains a concurrent computation, an internal scheduler, and a resource width. At runtime, the TAO type is instantiated by providing input arguments to its functionality. The resource width denotes how many cores are used to execute a task. The resource width must be a natural divisor of the number of available logical cores in a particular core-cluster, e.g., such as a NUMA domain. The leader core is the logical core with the smallest id. Resource partitions assigned to TAOs are composed of consecutive core ids. At execution time, the runtime pins the logical threads to physical cores so that consecutive thread ID’s map to cores sharing the same last level cache.

The XiTAO scheduler implements two queues for each core: a work stealing queue (WSQ) and a FIFO assembly queue (AQ). The WSQs store the ready tasks and use random work stealing as a policy for load balancing. When a ready TAO is fetched from the WSQ and its resource width is determined, pointers to the TAO are then inserted into all AQs representing the resource partition of the TAO. Subsequently, each core synchronously fetches these pointers and executes the TAO. Note that the resource partitions are irrevocable once assigned. Once the TAO pointers have been inserted into the AQs, the TAO must necessarily execute in the selected set of resources. In other words, all scheduling decisions must happen before the TAO is inserted in the AQs. More details about the theory and implementation of XiTAO can be found in [12].

### 3.2 Performance Trace Table

Typical scheduling implementations surveyed in Section 6 assume prior knowledge of task loads. However, that is not applicable in our case where the runtime has no prior knowledge of the core type.
In a heterogeneous platform, this work considers the case in which no assumption is made on which type of cores are faster and which kinds of tasks are more suitable for the different core types. Therefore, to be able to intelligently distribute tasks to the corresponding core type and to dynamically affect the scheduling decisions based on the available resources, we introduce a performance tracer of tasks at runtime and a table (PTT) to model task execution times. The table provides an online model of the execution time for each valid combination of leader core and resource width, (core id, resource width). The left part of Figure 2 shows all the scenarios of resource width when the total number of cores seen by the runtime is four. Therefore, the resource width in this case can be 1, 2 and 4.

The PTT is implemented in the XiTAO runtime. It is organized as shown in the right of Figure 2. The size of the table is core_number × resource_width_number. The fields of the table are initialized to 0 that models a zero execution time. This ensures that all configuration pairs will eventually be visited and trained at runtime. Due to the decentralized implementation of the scheduler, the table is organized to fit into cache lines where each core only accesses one cache line indexed with core number, hence avoiding false sharing. For each entry, the execution time of the pair is temporarily stored. Then each entry is updated with a weighted time of 1:4, thus, the old execution time of the entry occupies 80% and the new time occupies 20%. That is, $\text{updated\_value} = \frac{4 \times \text{old\_value} + \text{new\_value}}{5}$.

The performance trace table is updated always by the leader core of a task. This simplifies the implementation and reduces cache migrations. This also means that every core can have a model value of the task with width = 1 but only every fourth core will have a model value of the task with width = 4. As shown in Figure 2, in the case of width=1 (purple field), each core is the leader for its own partition. For the case width=2 (orange), the leading core 0 (2) handles the resource partition containing cores 0 (2) and 1 (3). By restricting the leader core to update the PTT, a potential skew of the model may result, since the leader may not provide the most accurate record of that execution time of the TAO, i.e., it could have had the least or the most amount of work. This is because these workers enter and exit the execution of the TAO asynchronously [12]. However, the weighted average that is used to updated PTT values ensures that the impact of imbalance will be limited. Although averaging results in an additional read of the table, the table size is small and it is very important to be resilient to divergent measurements as this table is the key point of scheduling decisions. While the impact of this feature requires a detailed study, our experiments so far do not provide evidence that the potential imbalance is problematic.

This implementation of tracing execution history requires as little information as the number of cores and their distribution into core-clusters with shared caches. The cores simply update the corresponding index, independent of its resource type, and thus create a model of performance. In the other words, no matter what core-types a platform has, be them big or little, the performance of these cores will be reflected by PTT values. This is beneficial not only for portability and potentially functional heterogeneity, but also for temporally added heterogeneity such as DVFS caused by heat variations, or interference caused by other tasks and/or uncontrollable system activities such as background processes or interrupts.

### 3.3 Performance-based Scheduler

Based on the implementation of the performance trace table, we develop a heterogeneity-unaware scheduler with the goal of optimizing performance. To achieve this, we follow the basic strategy of CATS [6] and extend it with our heterogeneity-unaware methodology. This scheduler is named performance-based scheduler. The main feature of the performance-based scheduler is the ability to
find the optimal cores and resource width using the optimal values depicted by globally searching the PTT.

The operation of the performance-based scheduler follows four steps. Figure 3 is an example of the scheduler implementation based on the task-DAG shown in Figure 1. Firstly, we fetch the ready tasks from our application task-DAG. These tasks are then inserted into a particular work stealing queue according to the default policy or to programmer annotations. When the task reaches the head of the WSQ, it is permitted to be executed locally or randomly stolen. The work stealing queues. For instance, core 1 and 3 steal task 

width 1, respectively, according to the best PTT resource width. For example, we can see that from the work stealing queues of core 0 respectively. As a critical task, task 1 is distributed into the assembly queues from 0 to 3. Task E is a non-critical task, it searches only the entry for core 3 in the performance trace table for a optimal width. As resource width=1 is the best choice for core 3, the task E is distributed into the assembly queue of core 3, as Figure 3(c) shows. Since its parent tasks B and C have completed, task G is woken up by core 1. By searching the performance trace table, it finds out that the pair (0,4) is the best one, then core 1 distributes the task into assembly queues from 0 to 3 (see Figure 3(d)). Then, as shown in Figure 3(e), the critical task D is woken up by core 1 but stolen by core 2 and the optimal pair for it is determined to be (2,2). Core 2 complete the task D and then wake up its final children and the critical task F with the best configuration (0,4) in performance trace table, as shown in Figure 3(f).

4 Experimental Setup
4.1 Evaluation Platforms
The benchmarks herein are evaluated on two platforms. From the static heterogeneous family, we use a NVIDIA Jetson TX2 development board, featuring a dual-core NVIDIA Denver 2 64-bit CPU, a quad-core ARM A57 Complex (each with 2 MB L2 cache) and an NVIDIA Pascal Architecture GPU with 256 CUDA cores. Both the Denver 2 and the A57 cores implement the ARMv8 64-bit instruction set and are cache coherent. For the purpose of this work, we consider only the two ARMv8 cores, and leave GPU scheduling as future work. On the homogeneous side, an Intel 2650v3 (codenamed "Haswell") based platform is used to evaluate the effect of interference while scheduling Random DAGs, and to evaluate the behavior of XiTAO when executing the Image Classification network (VGG-16) [16].

4.2 Random Directed Acyclic Graph
4.2.1 Kernels
We generate random DAGs to evaluate the properties of the PTT-enhanced scheduler. The random DAGs are based on a mix of different kernel types. When selecting the kernels, the priority is to achieve different characteristics in terms of memory-intensiveness (streaming), cache-intensiveness (i.e. data reuse) and compute-intensiveness. The following three kernels are selected for this purpose.

Matrix Multiplication. A matrix multiplication kernel is created for the compute-intensive property. We implement a matrix multiplication that achieves parallelism by ensuring that the writing of output data is done to separate cache lines for each thread while still sharing the input data.

Sort. For the data reuse property, a quick sort and merge sort kernel combination is selected. This kernel first splits the input array into chunks and performs in-place sorting with quick sort before carrying out two levels of merge sort, effectively reusing the data within the kernel. This kernel has a maximum parallelism of four.

Copy. Finally, a copy kernel handling large inputs is implemented for the streaming property. This kernel reads and writes large portions of data to memory, effectively creating a streaming behavior where the kernel has to access the main memory continuously. Each core copies a subset of the data.
For each kernel, we select the appropriate working set size corresponding to the desired behavior. For the matrix multiplication kernel, we choose a 64 × 64 matrix. For the sort kernel, we choose a 262KB input array, taking up a total space of 524KB due to double buffering, effectively fitting it on the L2 caches. Finally, the copy kernel uses a 16.8MB array, taking up a total space of 33.6MB, which is much larger than the space of the L2 caches.

4.2.2 DAG construction

To properly evaluate the performance of our scheduler, randomized DAGs composed of random selections of these three kernels are implemented. By tuning the parameters, it is possible to achieve different degrees of average parallelism and thus generate different scheduling scenarios.

To generate a suitable randomized DAG, a set of configuration parameters are used, similar to the generation of DAGs by Topcuoglu et al. [17]. The first parameter is the number of tasks of each kernel. This is useful to choose which kernel should be most prominent in the DAG. The second parameter is the average width of the DAG. This is used to obtain the desired level of parallelism. The last configuration parameter, the edge rate parameter, determines the average amount of connected edges a task has, which also affects the parallelism of the DAG. A seed value is used to manipulate the randomization to recreate a different DAG several times for comparison.

The DAG generation algorithm produces a DAG in three steps. The first step generates the shape (nodes and edges) of the DAG. This step is separated from the TAO creation step in order to get proper memory utilization and data reuse (see below). The second step consists of allocating memory and deciding which tasks are reusing data. To achieve data reuse between nodes, we maintain a vector for every kernel where each index in the vector represents a memory location. Initially, the size of the vector is zero. For every node, we search its predecessors for a node number matching any of the numbers in the vector. If a matching number is found, it is replaced by our current node number and the index to the location is saved in the node. If we cannot find a match, a new entry is created in the vector with the unique node number and that index is saved in the node instead. The size of the vectors is then used for allocation of memory and each node will have a designated data location. The memory is allocated this way to maximize data reuse between tasks of the same kernel while guaranteeing isolated data execution when tasks are run in parallel. The final step is to traverse the nodes and spawn the corresponding tasks and edges between them, thus effectively creating the DAG in the XiTAO format.

4.3 Image Classification

To demonstrate the behavior of the performance-based scheduler in XiTAO, we port the VGG-16 [16] image classification model from the Darknet framework [14]. The application uses a 16 layered deep convolutional neural networks (CNNs) to classify an image using a pre-trained model. Each convolutional (CONV) and fully-connected (FC) layer implements GEneral Matrix Multiply (GEMM) that takes most of the computation time. Figure 4 shows the XiTAO implementation of VGG-16. In VGG-16, input size varies as the network progresses. For example, the convolutional layer iterates over a minimum 64 channels to a maximum of 512 channels. Therefore, in the XiTAO implementation we partition the work among TAOs. The number of TAOs in each layer depends on the number of channels and block_length. The parameter block_length refers to the number of channels assigned to each TAO, which is tuned at runtime. Each TAO performs parallel GEMM with the number of threads equal to the width of TAO. Note that the width is dynamically determined by the XiTAO scheduler. Since there are no loop carried dependencies inside the layer we benefit from two levels of parallelism in the XiTAO implementation. However, each layer is dependent on the previous layer, we therefore synchronize all TAOs at the end of each layer.

5 Performance Evaluation

The outline of the evaluation is as follows: we first analyze the impact of using the performance-based scheduler versus the homogeneous scheduler (i.e. the base random work stealing algorithm as implemented in XiTAO [2]) that is both unaware of the hardware and of the ongoing performance state modeled by the PTT. We study Random DAGs consisting of a mixture of kernels (MatMul, Sort, Copy) to cover the spectrum of real DAGs as much as possible. We also port the Darknet VGG-16 code to XiTAO and compare it to the base CPU implementation to assess the enhancements on Convolutional Neural Networks that are of high relevance to contemporary applications.

5.1 Comparison with Homogeneous Scheduler

Figure 5 denotes a heatmap per each described scheduler executing between 250–4000 tasks (X-Axis) on random DAGs with a parallelism between 1-16 (Y-Axis). The underlying random DAG is a combination of the aforementioned kernels with equal proportions. In the most challenging case with low task count and parallelism (tasks=250, par=1), we observe that the temperature of the performance-based scheduler (depicted by Figure 5(a)) is at least twice higher. The additional ingredient of scheduling critical tasks on the high performing cores (mainly Denver cores in this case) and the ability to dynamically tune the resource width renders this scheduler superior even with no external task-DAG parallelism. The throughput is higher across the table except for a few cases of very high parallelism that pose almost no challenge on scheduling decisions. Another interesting yet expected observation is that the number of tasks plays a negligible role on the performance of the homogeneous scheduler, whereas the throughput of the counterpart is a factor of both axes. A twofold increase in the number of tasks provides twice the amount of PTT training data. This directly reflects on the performance by improving the quality of the dynamic, PTT-based choices. In addition, a higher degree
5.2 Performance Impact of Kernels

As highlighted before, we select three different kernels *matrix multiplication*, *sort*, and *copy* with different characteristics. It is therefore important to evaluate the performance impact of such kernels and their mixture while varying parallelism. Figure 6 compares the throughputs of the performance-based scheduler and homogeneous scheduler on the Jetson TX2 platform for various degrees of parallelism. Besides the higher throughput achieved by the performance-based scheduler especially for lower parallelism, it exhibits a greater stability across the X-axis, which is an essential attribute that suggests that the hardware is being efficiently utilized and that the scheduler is less sensitive to parallelism constraints. For a concrete quantification of performance gains, Figure 7 shows the speedup achieved using the performance-based scheduler over the homogeneous scheduler. In this case, we use 4000 tasks for each kernel (i.e., *matrix multiplication*, *sort* and *copy*), and a Random DAG that contains a mixture of even number of tasks/kernel that sum up to 4000. We can see that our performance-based scheduler generally runs faster than homogeneous scheduler. Specifically, it has significant speedup when the parallelism is low. For a parallelism of 1, it achieves $3.3 \times$ of the throughput when compared with the homogeneous scheduler in *matrix multiplication*. The speedup for *sort*, *copy* and the mixture of three kernels are $2.5 \times$, $2.2 \times$ and $2.7 \times$ for the same parallelism, respectively. When the parallelism increases, the speedup of performance-base scheduler compared with homogeneous scheduler decreases, but we still have better performance than homogeneous scheduler. For scenarios of high parallelism, criticality-aware scheduling has little impact on performance. Instead, in such scenarios it is important to try to avoid interference due to resource oversubscription. This results highlight how the PTT can be used to select appropriate resource width to avoid oversubscription. This is particularly visible for the case of the *sort* kernel, which relies on good usage of cache capacity. Scheduling too many *sort* kernels in parallel leads to oversubscription and performance degradation. Classical heterogeneity aware schedulers such as HEFT [17] or CATS [6] are not able to address such scenarios.

5.3 Process Interference

One of the remarkable advantages of using PTT is maximizing performance via minimizing the side effects of interference. This feature is especially important since it is highly anticipated that user or kernel level resources are shared. Figure 8(a) depicts the response of the XiTAO performance-based scheduler running a background parallel process, in this case a chain of MatMul DAGs, alongside a highly parallel random DAG. The black dots represent the time-stamp at which the threads start executing TAOs. A vertical green line shows the resource partition used to execute the TAO. While bootstrapping the PTT, a few width choices are attempted. At the point of interference (i.e. in Figure 8(a)), we show the PTT value at (width=1,core=1). Other relevant values are dropped for brevity. Due to the jitters in PTT values, the scheduler automatically selects cores from (2-9) for executing the critical tasks. Cores (0-1) are still selected under typical circumstances according to Figure 8(b). Shortly after the interference event, the scheduler recovers to normal operation yielding a marginal wall time difference across the two experiments. Note that non-critical task continue to be executed on cores with interference, as long as these cores succeed in stealing tasks. This is important so that the PTT is continuously updated to reflect the status of the system.

5.4 ImageNET Classification

Figure 9 depicts a strong scalability study of the performance of the XiTAO version of the VGG-16 code for predicting a predefined image class by multiple convolutions of a crop layer (1024 x 1024) converted to matrix (512 x 512 x 3). The study is to assess the scheduling performance of the conventional fork-join application class with minimal effort. It is carried out on a dual-socket Intel Haswell platform. It is worthwhile noting that XiTAO reorders threads to ensure data locality, since the core ids are not always laid out continuously, as is the case in both this platform and the Jetson TX2 platform. The scheduler still exhibits 0.69 parallel efficiency compared to the serial performance, even though there is no criticality notion to this experiment, i.e., all tasks are marked

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**Figure 5.** The performance impact over parallelism and number of TAOs and the performance comparison between performance-based scheduler and homogeneous scheduler.

**Figure 6.** The performance impact over parallelism and number of TAOs and the performance comparison between performance-based scheduler and homogeneous scheduler.

**Figure 7.** Comparison of throughput for different degrees of parallelism.
non-critical. Figure 10 shows the number of TAOs scheduled with corresponding widths. During execution, PTT chooses the best width to schedule a TAO. For example, in the case of running VGG-16 with 8 threads, 67% of TAOs are scheduled with width = 1 and 30% TAOs are scheduled with width = 8, indicating that these widths lead to the best speed-up. The approximately linear speedup shown in Figure 9 combined with the PTT-assisted choices of widths as in Figure 10 demonstrate how negligible the resource tuning overhead is especially if compared to the potential performance gains prescribed by this paper.

6 Related Work

6.1 Scheduling in Heterogeneous Environments

Task scheduling on a heterogeneous platform, contrary to a homogeneous platform, includes the problem of assigning the appropriate tasks to the most suitable cores. Most multicore scheduling approaches today assume equal performance. For example, dynamic scheduling techniques such as work-stealing or work-sharing do not consider the individual performance of cores.

Scheduling DAGs on heterogeneous multicores is a well studied problem in the context of single-threaded task-DAGs [5–7, 10, 17, 18]. These schemes either assign a ranking to each tasks based on the critical path and then assign more critical tasks to faster cores [5–7, 17], or they compute a best fit between tasks and cores and then schedule appropriately [10, 18]. In this study we extend upon ideas introduced in CATS [6]. In the following paragraph we describe CATS along with HEFT [17], a classical heterogeneous scheduler, and Bias Scheduling [10].

HEFT is a static scheduling method for heterogeneous task scheduling proposed by Topcuoglu et al. [17]. The HEFT algorithm consists of ranking the tasks of a DAG in order of longest path to finish and then assigning the highest-ranking tasks to the core that will minimize the overall finish time. An analysis of the DAG is done to calculate the execution time and communication cost of each node and edge before the tasks can be ranked. The tasks are then placed in a queue where the scheduler picks the top task and calculates which core will be able to finish this task earliest using insertion-based scheduling.

CATS is a dynamic scheduling approach where no prior knowledge about the execution time of the tasks is assumed [6, 7]. Instead, CATS solely uses the number of successors to find the critical path. The critical path is then put in a critical queue. Tasks from the critical queue are scheduled on high-performance cores and tasks from the non-critical queue are scheduled on lower-performance cores. In [6], Chronaki et al. introduce the dynamic Heterogeneous Earliest Finish Time (dHEFT) algorithm as a reference to evaluate CATS. dHEFT uses the same principles as HEFT but instead of knowing the load of tasks prior to scheduling, discovers them at runtime.

Finally, Bias Scheduling [10] is a proposed method for single-ISA heterogeneous multicore processors that tracks how different kinds of tasks perform on each core. The main idea is to categorize tasks into two groups: Tasks gaining large speedup by running on a big core compared to a LITTLE core and tasks gaining modest speedup by running on a big core. The speedup is approximated by accessing hardware counters for stall cycles. Tasks are then scheduled on big cores if they provide large speedup and on LITTLE cores if the speedup would be modest.
(a) Dynamic migration of processes in response to PTT spikes during interference.

(b) The scheduler’s behavior when there is no interference

Figure 8. The effect of interference on PTT scheduling of critical tasks.

Figure 9. Performance of CPU GEMM on XiTAO VGG-16 with variable number of threads

Figure 10. Percentage of TAOs scheduled with corresponding TAO width by PTT

While all these schedulers can improve the execution time of task-DAGs in which tasks have diverse behaviors, they have a few limitations. First, none of them is able to avoid resource over-subscription and provide interference-free execution. And second, all of them are based on the notion of only two static performance classes, i.e. big and LITTLE. In practice, sources of heterogeneity are diverse, hence performance needs to be tracked and modeled on a per-core basis. Our proposal can model the performance of all cores and, furthermore, thanks to its reliance on XiTAO it can exploit this information to provide interference-free scheduling.

6.2 Management of shared resources

One of the main goals of XiTAO is to provide a good solution for shared resource contention. The focus of XiTAO is on multithreaded computations. Prior work on resource contention has mostly focused on multiprogrammed workloads, i.e. multiple single-threaded workloads running in parallel. Both software-based scheduling [20] and hardware-based partitioning [9, 13] approaches have been proposed to address issues related to cache and memory sharing. Multiprogrammed workloads are less challenging in the sense that the different tasks do not have any dependencies. Hence, XiTAO addresses a more problematic case in which scheduling and resource partitioning decisions can negatively impact the application execution time, particularly if bad decisions are taken concerning the critical path of the application. In the context of structured parallelism, such as divide-and-conquer, one scheduler that targets constructive sharing is the parallel depth first (PDF) scheduler [1, 4]. Other runtime systems that support mixed-mode parallelism have been proposed by Wimmer et al. [19] and by Sbirlea et al. [15]. However, they focus only on restricted forms of parallelism, such as divide-and-conquer [19] or worksharig constructs [15].

7 Conclusion

We have introduced a performance-based scheduler for heterogeneous architecture that leverages online monitoring on top of the XiTAO runtime. The presented scheduler improves task execution throughput and latency, and it provides interference-free execution and task migration in the event of process interference. All these features allow our proposed scheduler to adapt to next generation heterogeneous systems with shared resources. We evaluated the performance-based scheduler on random DAGs and compared it to the homogeneous counterpart.

A future direction of this work is to include GPU kernels as part of the scheduling strategy, fully utilizing the Jetson TX2 chip by offloading GEMM kernels of the VGG-16/Random DAGs benchmark to the underlying Pascal GPU. We also intend to study the
interaction between non-critical tasks and the PTT in terms of updating resources and locality.

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